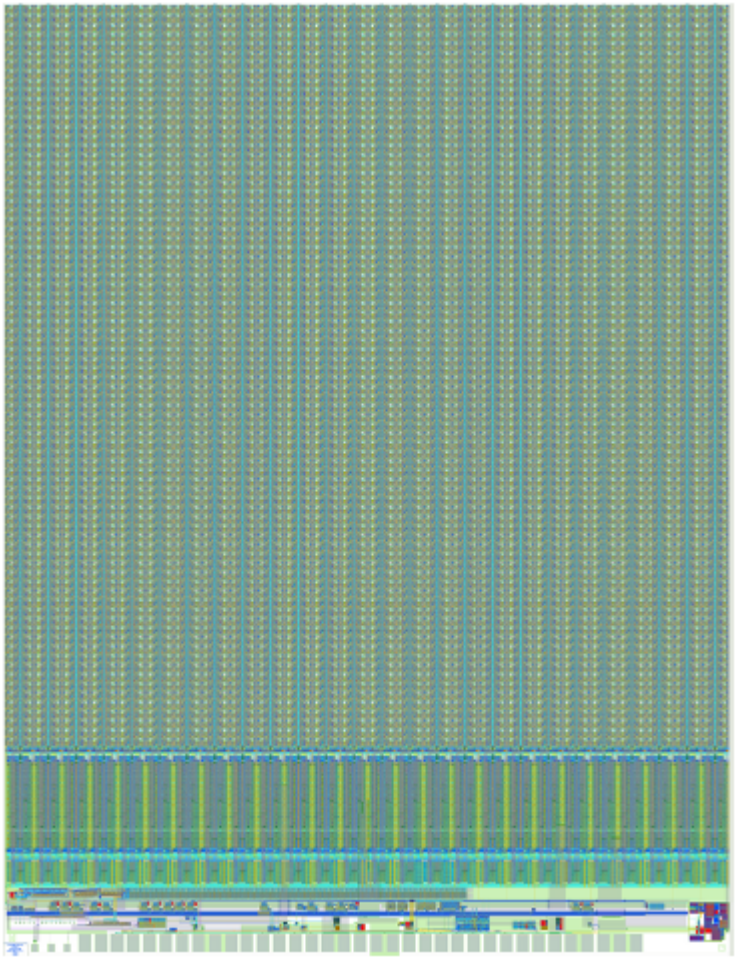
Plans for testing the PSI46xdb pixel chip

Daniel Pitzl

DESY CMS Phase I pixel upgrade, 1.6.2012

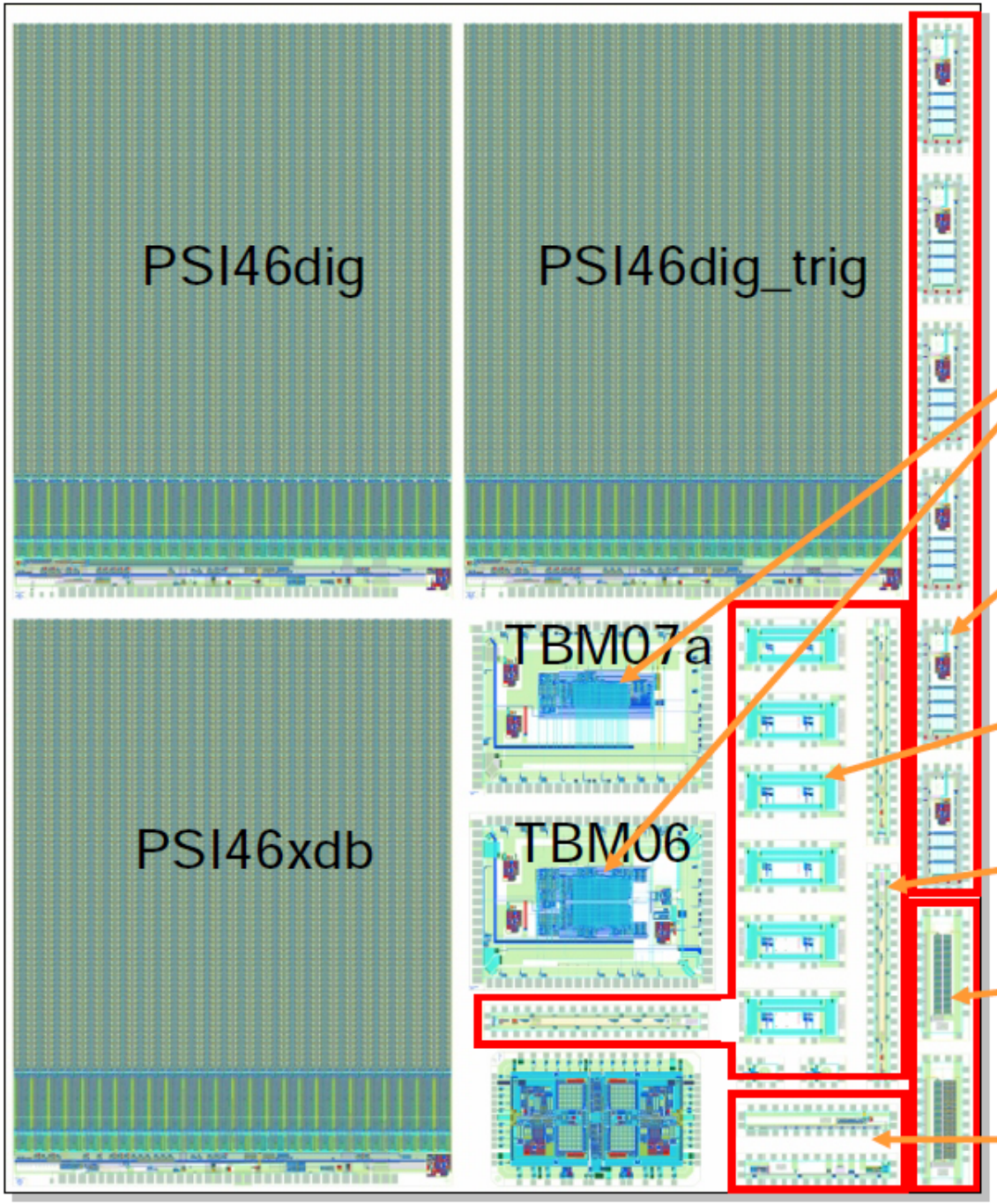


4160
pixels

extended
data buffer

- PSI46xdb
- Test plans

PSI ROC submission 2012a



Size: 17.4 mm x 21.2 mm

60 recticles/wafer, 6 wafers

3 new ROC versions (PSI)

2 new TBM versions
Ed Bartz, Rudgers

LCDS cable drivers with bug fixed in read back (PSI)

Digital Level Translator DTL to replace the ALT chip (PSI)
Christoph Nägeli

LCDS/LVDS converter for test setups (PSI)

SEU resistent register test structures (PSI)

ADC, PLL and oscillator test structures (PSI)

Beat Meier (PSI): Pixel Upgrade plenary at CERN, 1.2.2012

ROC submission 2012a

- **PSI46xdb**: Enlarged data buffers, reduced crosstalk and better level distribution; - 3 DACs
- **PSI46dig_trig**: Digital readout added; - 4 DACs
- **PSI46dig**: Trigger mechanism removed; read back; - 7 DACs
- 2 **TBM** versions
- **DLT** Digital Level Translator for POH, replacing the ALT
- LCDS/LVDS level translator for test boards (LCDS not a standard)
- Other test structures (ADC, PLL)
- Tape out: January 2012 to IBM
- 6 wafers on 28 March 2012 (6 weeks earlier than expected)

Beat Meier (PSI): Pixel Upgrade plenary at CERN, 1.2.2012

`https://indico.cern.ch/conferenceDisplay.py?confId=172930`

PSI46xdb

Data Rate, Efficiency:

- Extended data buffer 32 → 80 cells
- Extended time stamp buffer 16 → 24

Crosstalk, threshold uniformity:

- 6 metal layer (process option)
- Thick top metal (LM instead of MZ process option, +37%)
  → better power and ground distribution (lower resistance)
  → better threshold uniformity
- New routing for calibrate signal → less crosstalk of calibrate signal
- Better decoupling of comparator and digital voltage → less crosstalk
- Different other minor layout changes to reduce crosstalk

PSI46xdb

DAC:

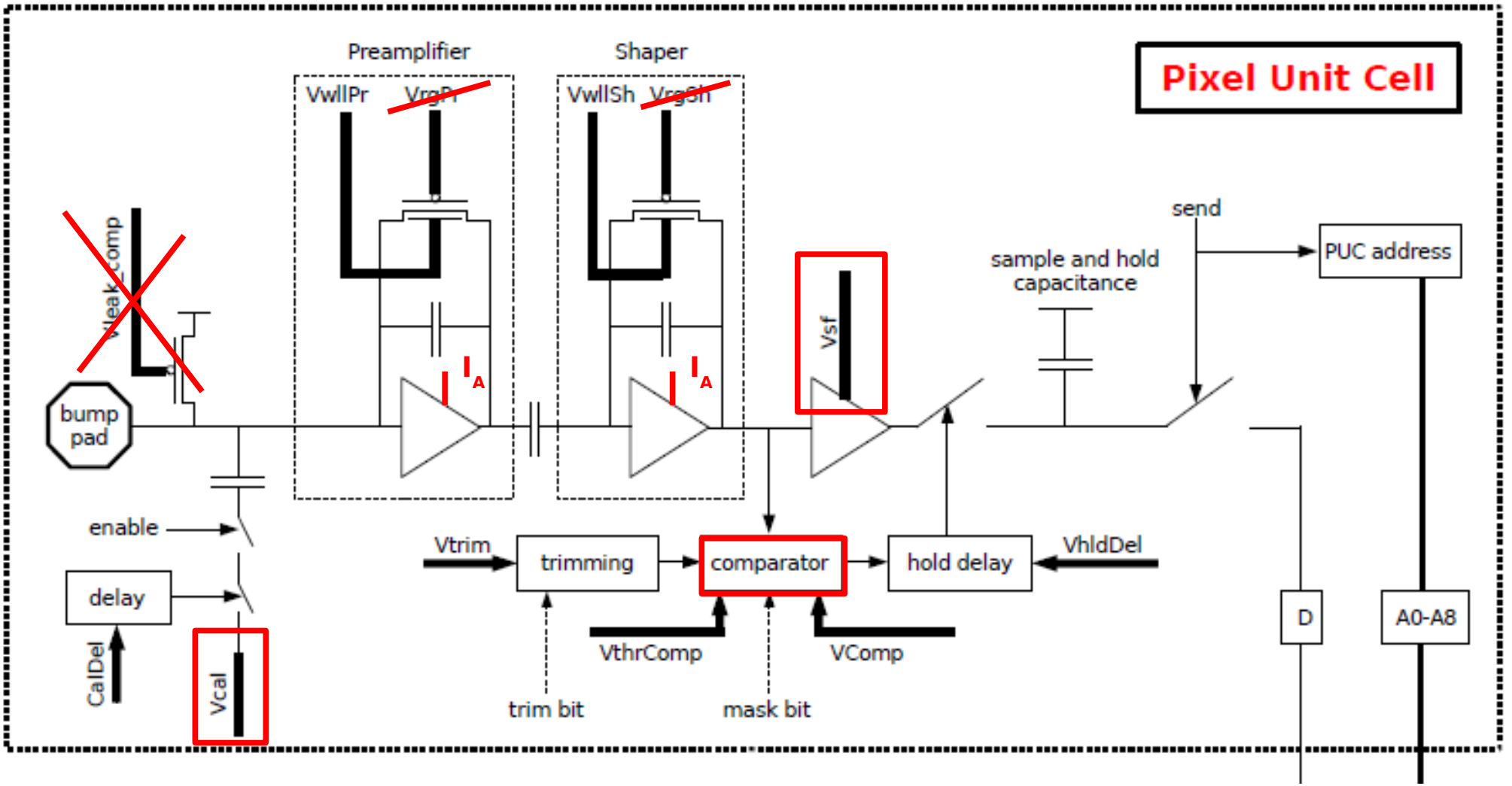
- 3 DACs removed: VRGPR, VRGSH and Vleakage
- All DAC's with power on reset for low power ROC configuration
- Current control instead of voltage control for S&H and analog power supply → easier and independent setup

Timing:

- Small performance optimization in column drain mechanism (timing)
- Modified comparator with reduced timewalk

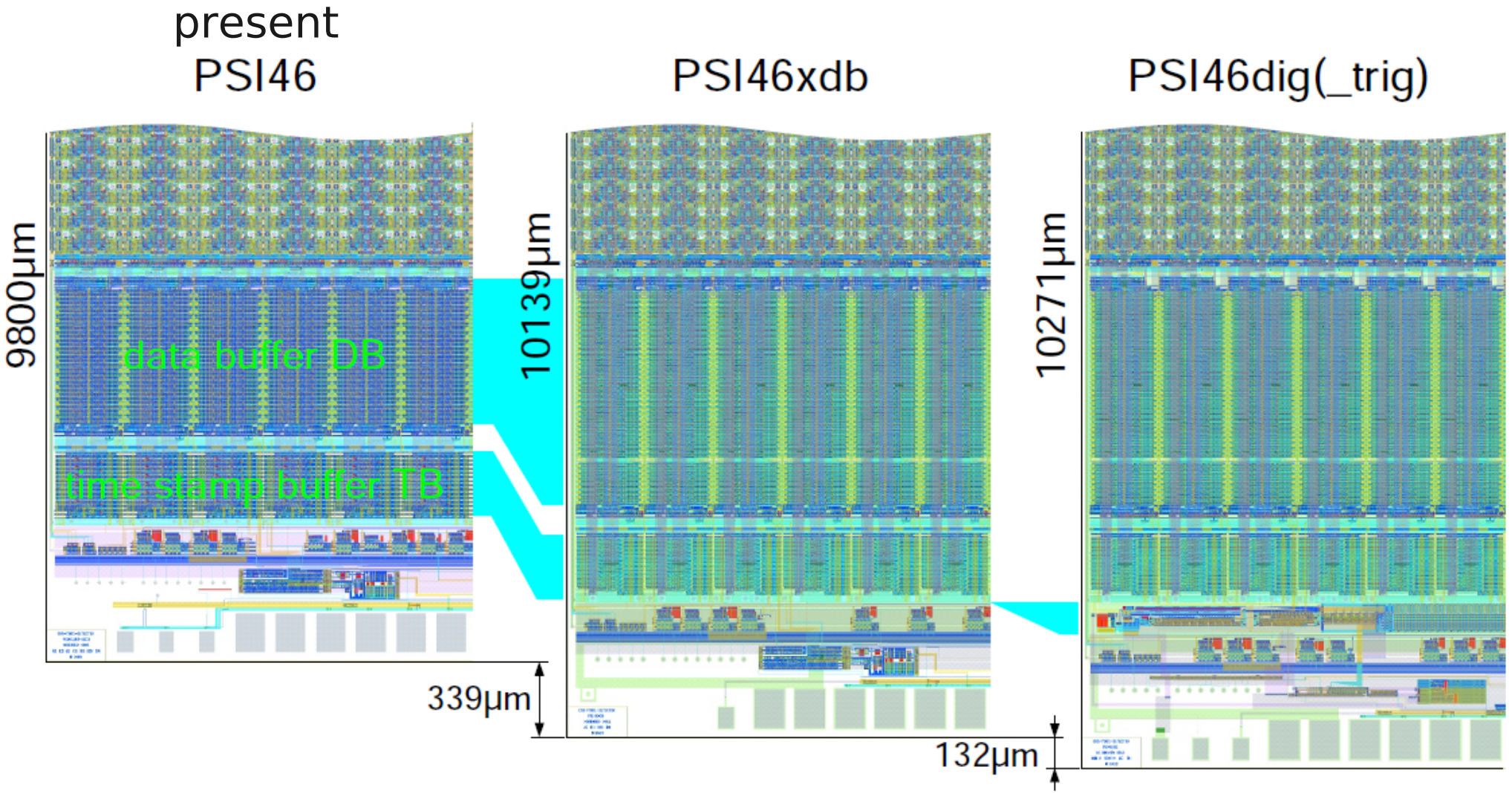
- Same analog read out as PSI46 → same test board
- Comparison possible between PSI46 and PSI46xdb

PSI46xdb pixel unit cell



modified in PSI46xdb

PSI46 versions

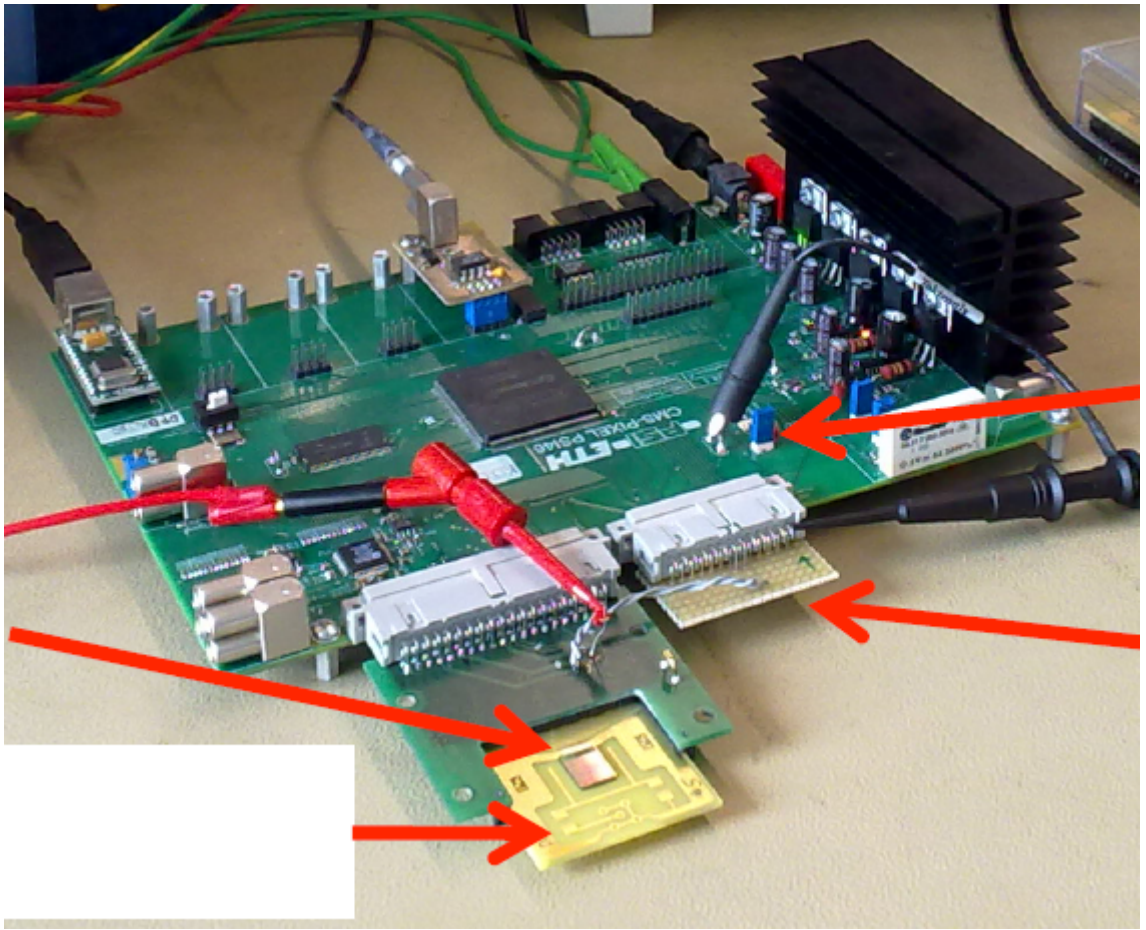


- DB 32
- TB 16

- DB 80
- TB 24

- DB 80
- TB 24
- RB 64
- 8-bit ADC

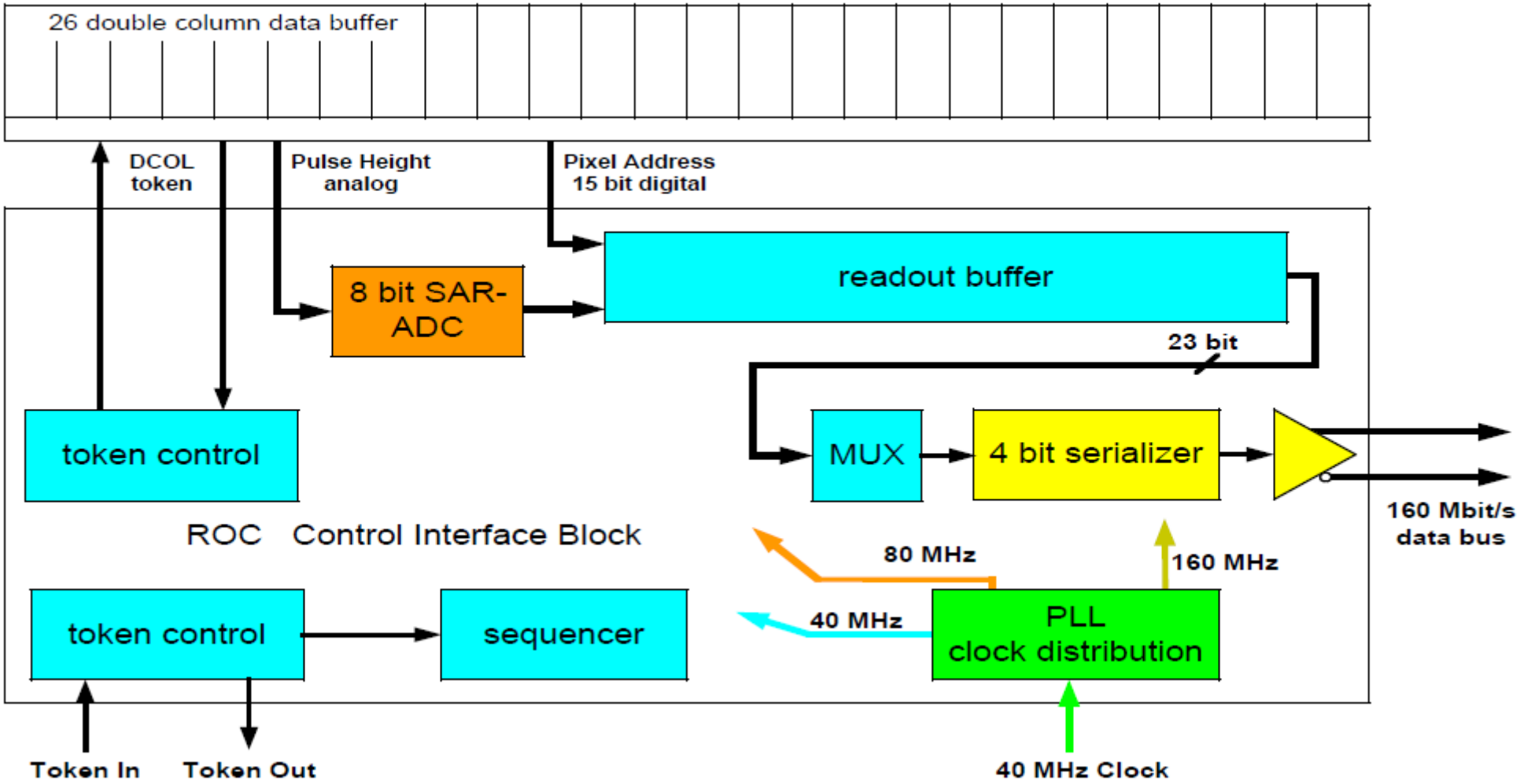
test setup at PSI



- single chip module:
  - Indium bump bonded at PSI
  - Glued and wired bonded to carrier printed circuit board
  - Interface card to PSI46 test board with edge connector
- PSI46xdb uses the same analog signal path as before.
- PSI46dig needs special adapter for 160 MHz data:
  - directly into FPGA (bypassing the board ADC)

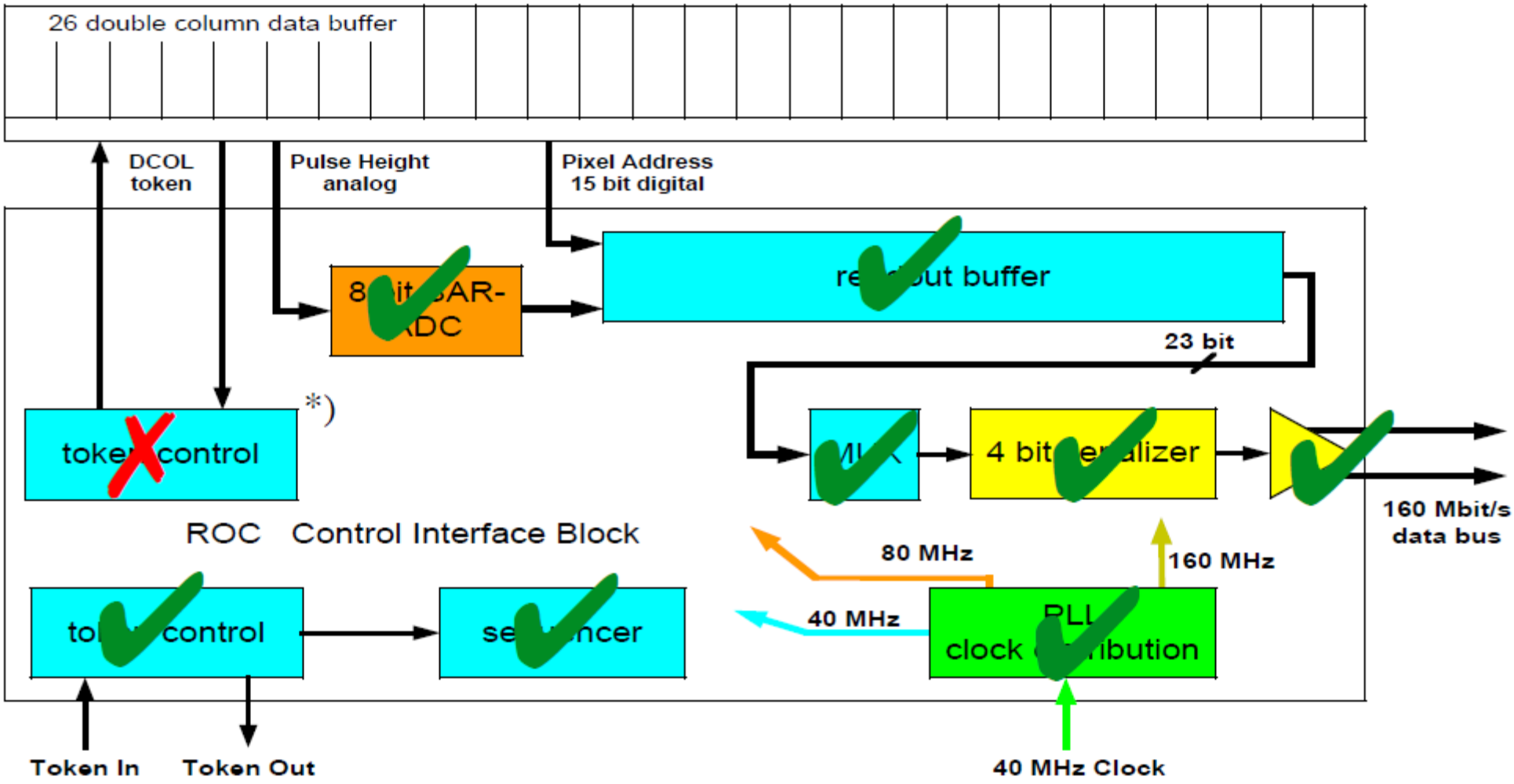
Hans-Christian Kästli, CMS upgrade plenary 22.5.2012

PSI46dig new periphery



Hans-Christian Kästli, CMS upgrade review 25.4.2012

PSI46dig testing



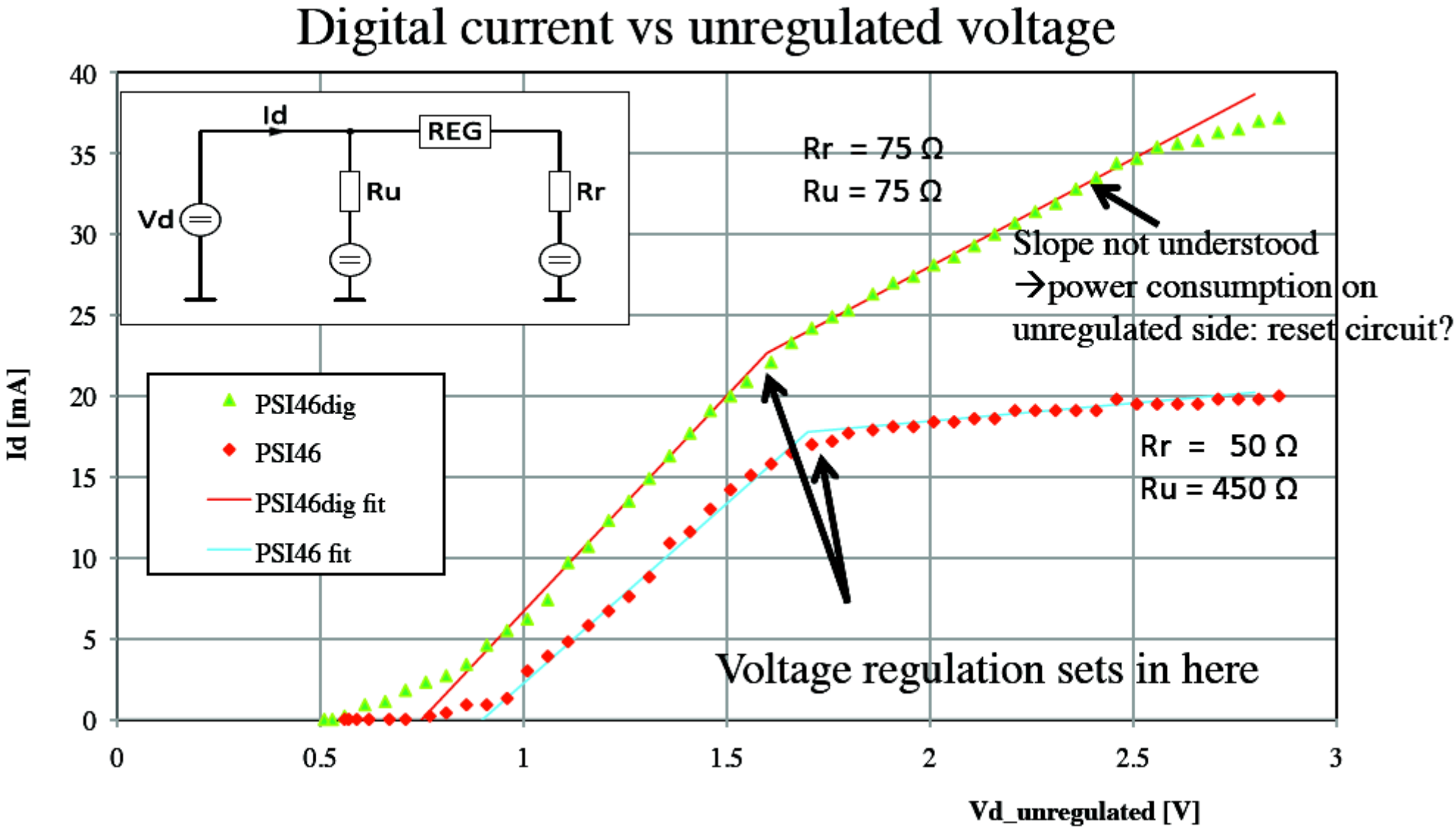
Hans-Christian Kästli, CMS upgrade review 25.4.2012

PSI46 Problems

1. Power up reset circuit loads low power settings into ROC when switching power on
   - •Required in order not to overload DC/DC converters at startup
   - •Testing has shown immediately: Reset signal does not release!
     → Cannot program ROC
   - •Workarounds for ROC testing exist : scratch a metal-6 line
   - •Related to this there is an anomalous power consumption on the unregulated voltage side
2. Flaw in readout logic found
   - Need to wait for ongoing readout to finish before sending next trigger
   - No important cosequences for testing. High rate tests (X-ray, beamtest) still possible

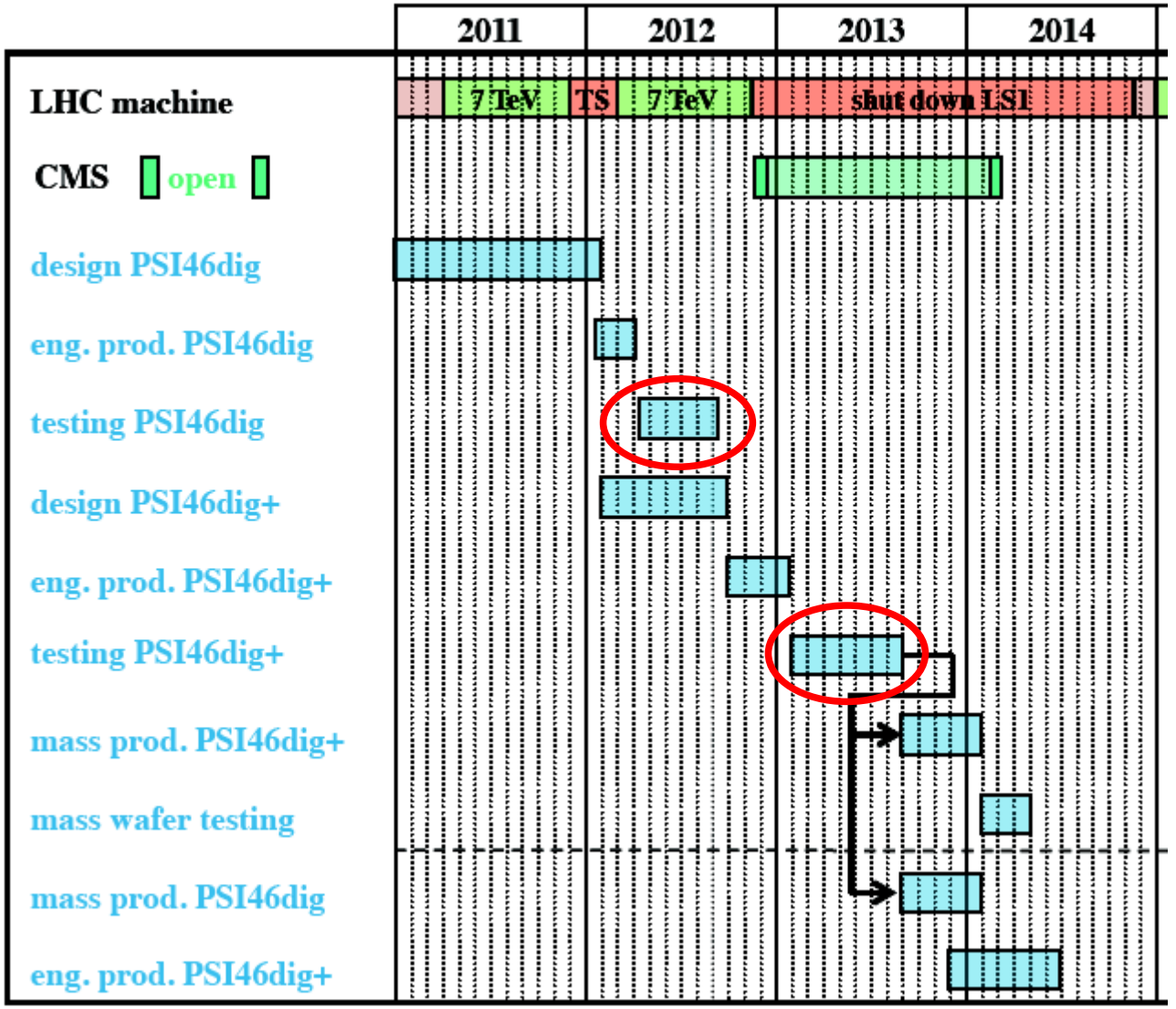
Hans-Christian Kästli, CMS upgrade plenary 22.5.2012

PSI46 anomalous power consumption



Hans-Christian Kästli, upgrade plenary 22.5.2012

PSI46 testing schedule

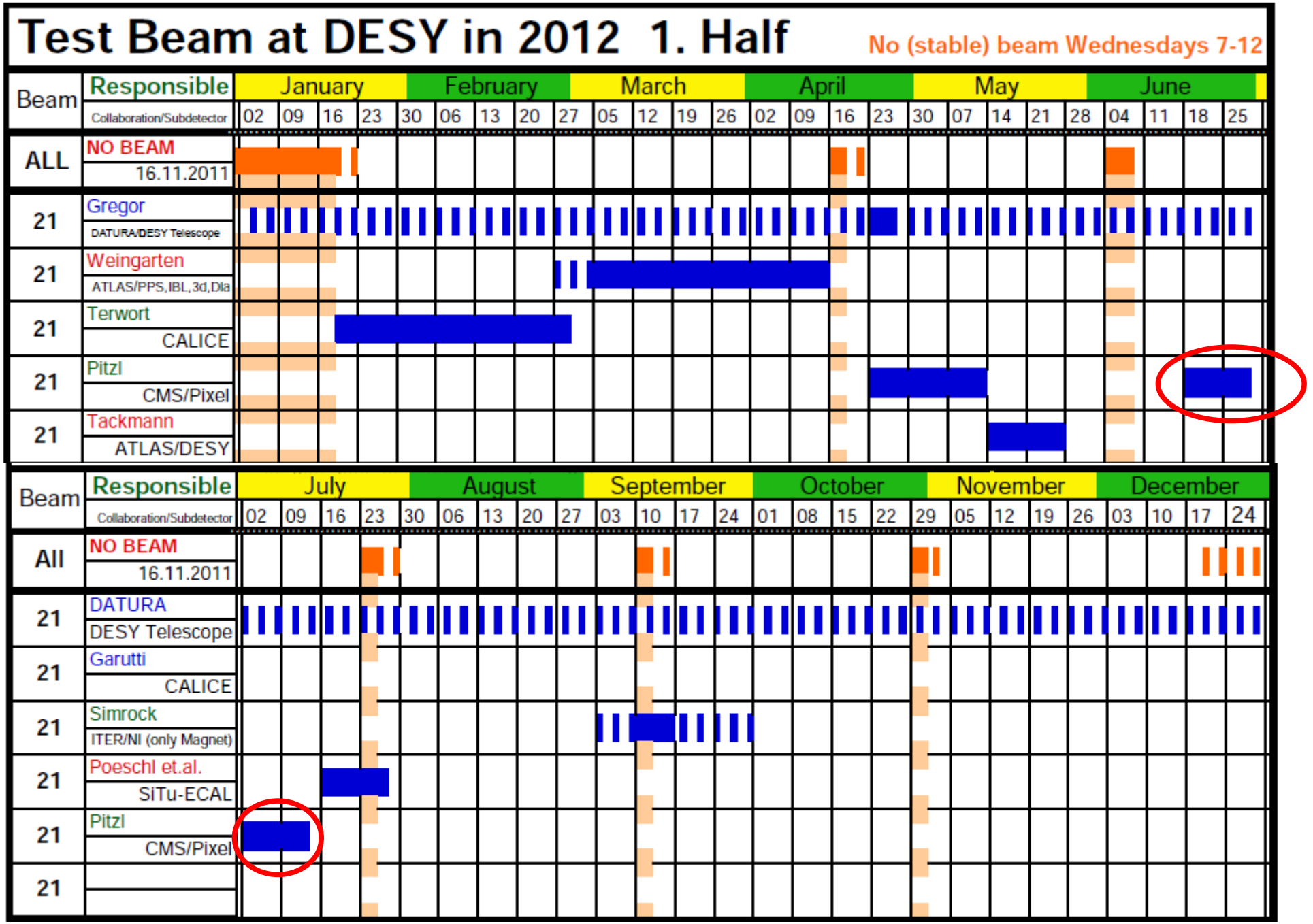


Hans-Christian Kästli, upgrade plenary 22.5.2012

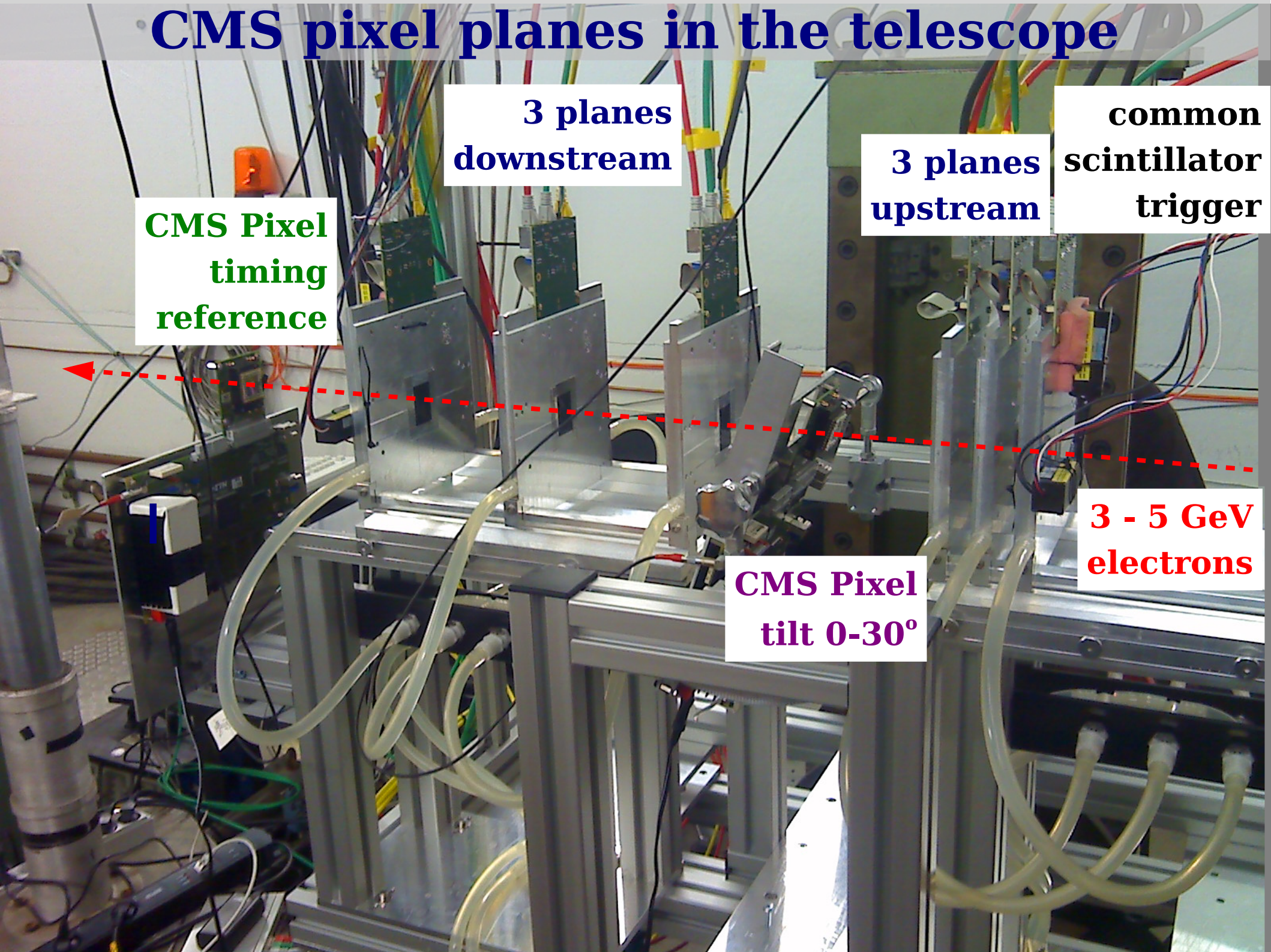
CMS Pixel in the DESY test beam

http://adweb.desy.de/~testbeam/

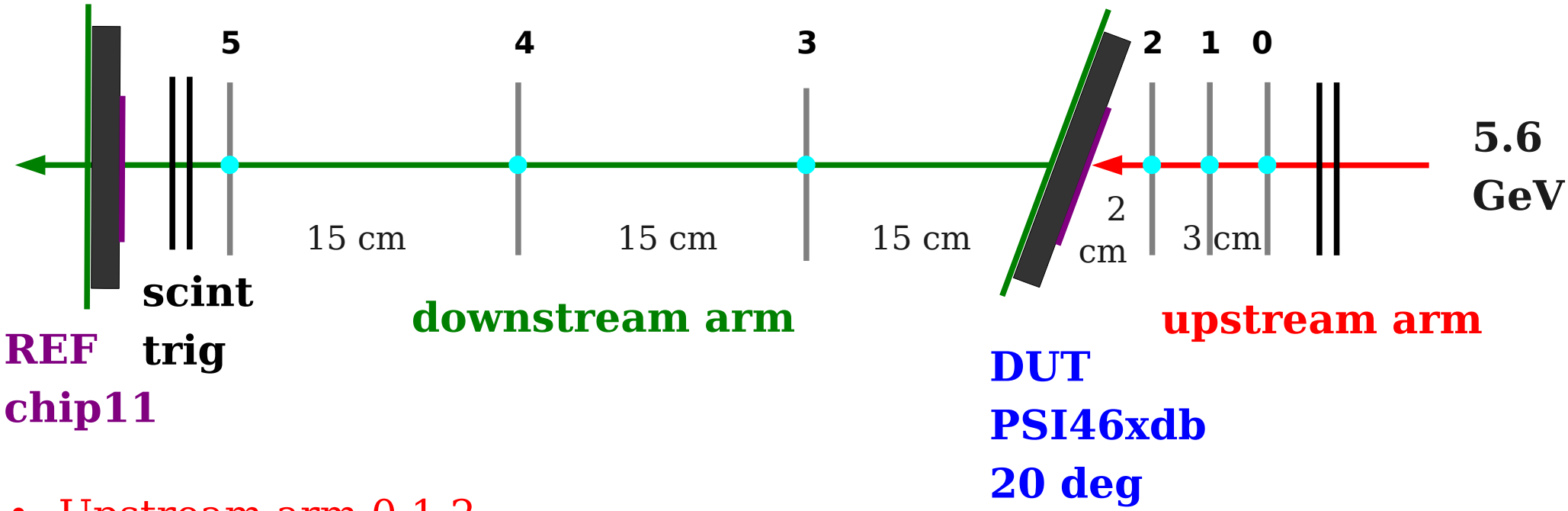
29.05.2012



CMS pixel planes in the telescope



Default set up

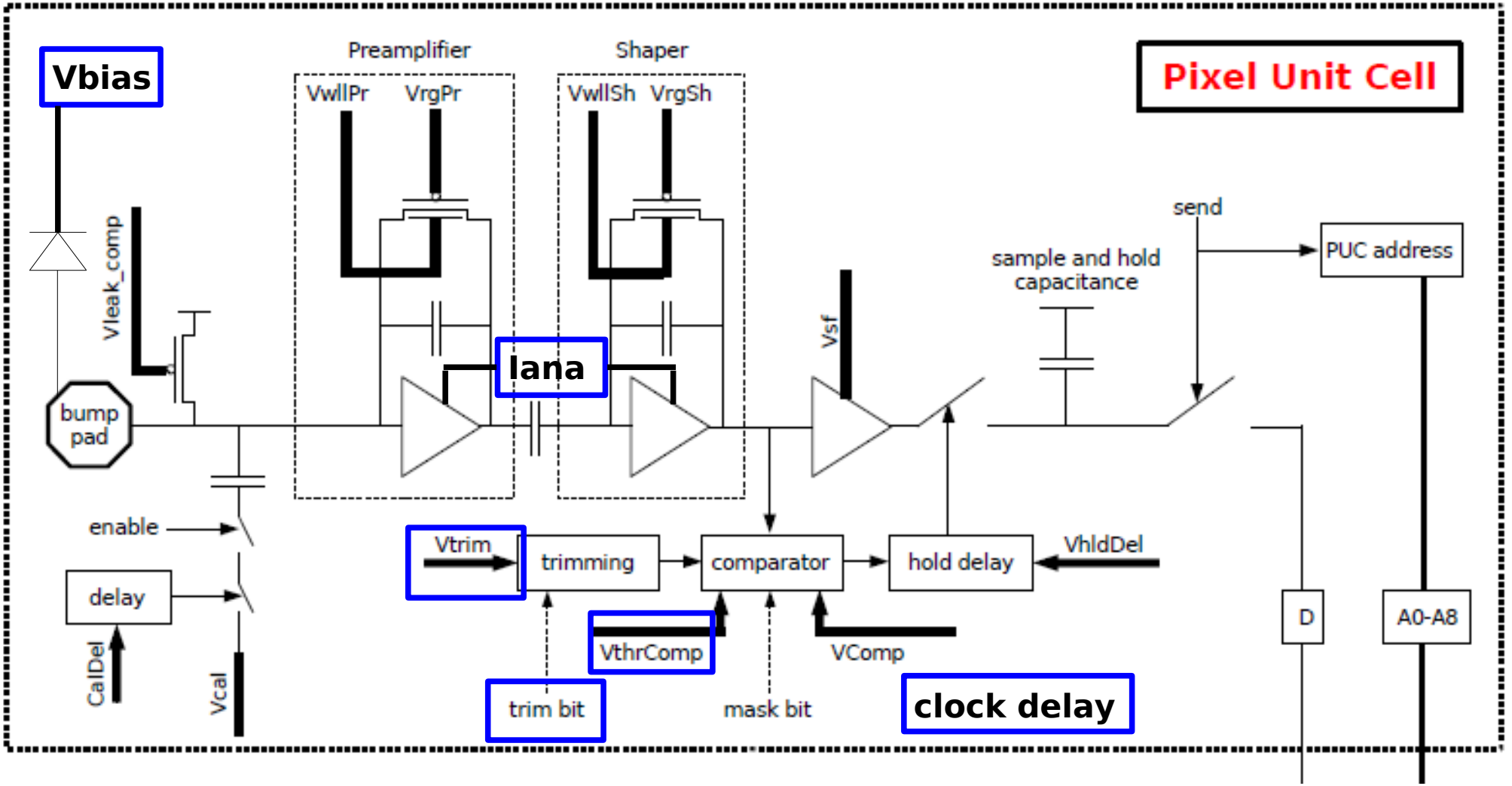


- Upstream arm 0-1-2:
  - as close as possible to DUT, but allow for tilting (open for insertion)
- DUT = single chip module, tilted by up to 30°,
- Downstream arm 3-4-5:
  - equally spaced between DUT and REF, allow for DUT tilting
- REF = single chip module for timing, as close as possible behind scint
- trigger: 2-fold coincidence (config: TLU AndMask 12)

PSI46xdb test beam goals

- Measure efficiency
  - present ROC reached 99.9%
- Measure resolution
  - present ROC reached 7 µm at 20^{o} tilt
  - new ROC might be better with lower thresholds
- Measure gain:
  - calibration from Landau peak vs tilt angle
- Study any problems
- Give feedback to chip designers at PSI
- Present results in CMS meetings and at conferences
- Publish

PSI46 pixel ROC

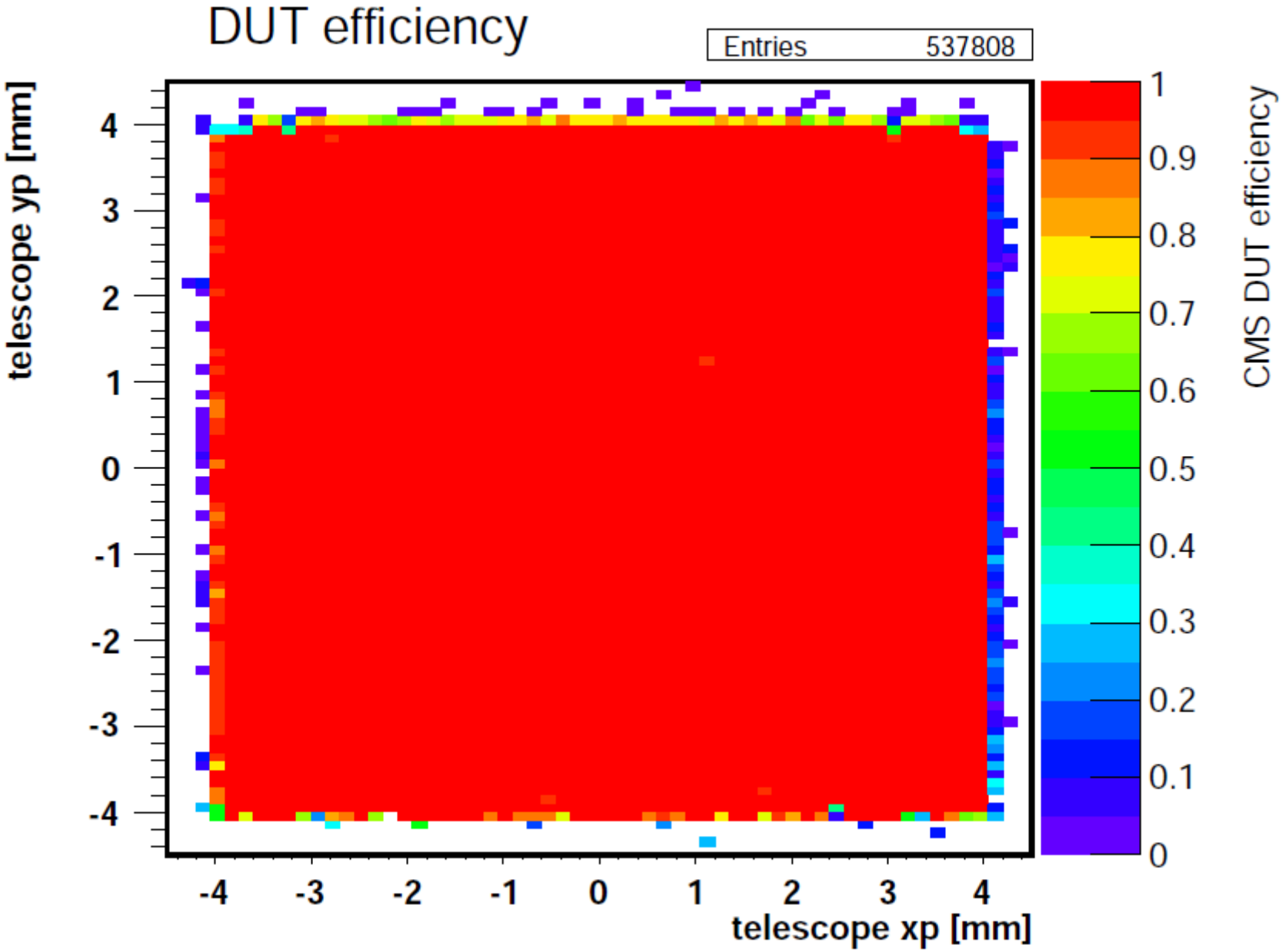


vary in beam test

previous programme

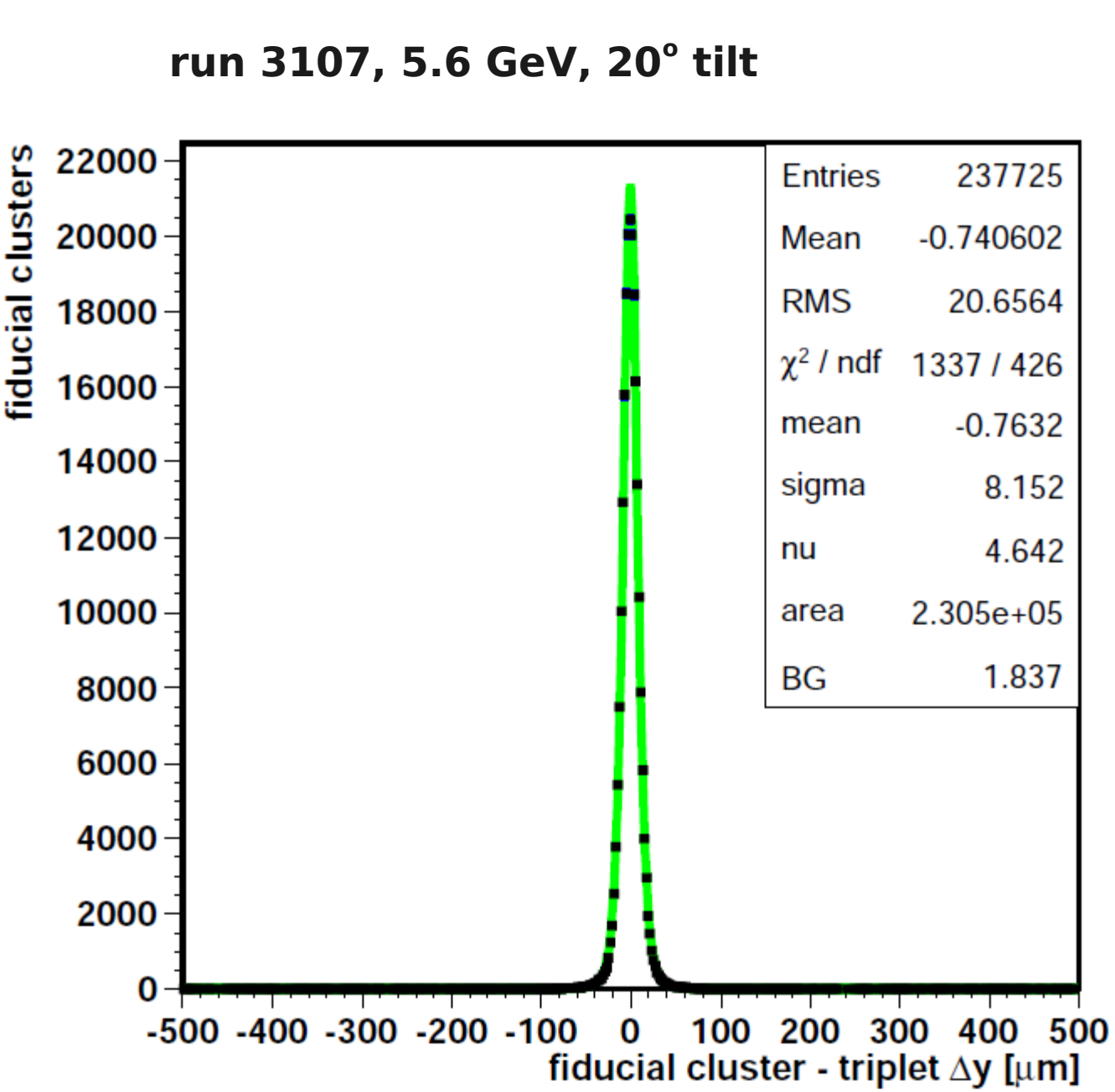
- Defaults: DUT at 20°, bias -150 V, softest threshold, optimal delays
- Optimize rate in test beam by adjusting position ½ day
- Clock delay scan: 0..24 ns, 4 ns steps, finer at edges (~10 runs) ½ day
- Bias voltage scan: -150 to -10 V, 20 V steps (8 runs) ½ day
- DUT tilt scan: 0°, 5°, 10°, 15°, 18°, 20°, 22°, 25°, 30° (9 long runs) 1.5 day
- Threshold scan: `VthrComp` 97 to 7 step 10 (10 long runs) 1.5 day
- gain calibrations each day
- scan Vana (less power), always re-optimize other DACs 2 days
  - possibly repeat delay and threshold scans
- another chip as DUT 1 day
- repeat problematic runs 1 day
- reserve 1 day + weekends + extension week

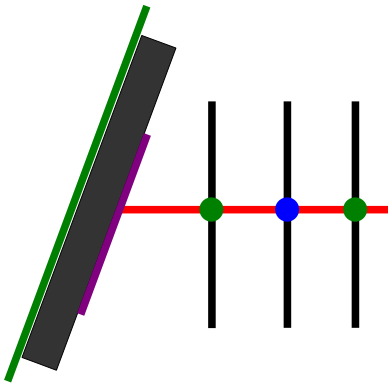
Efficiency map



- run 3096
  - 2800 s
- 5.6 GeV
- chip 10
- tilt 20°
- 99.88% in fiducial volume

CMS pixel row resolution





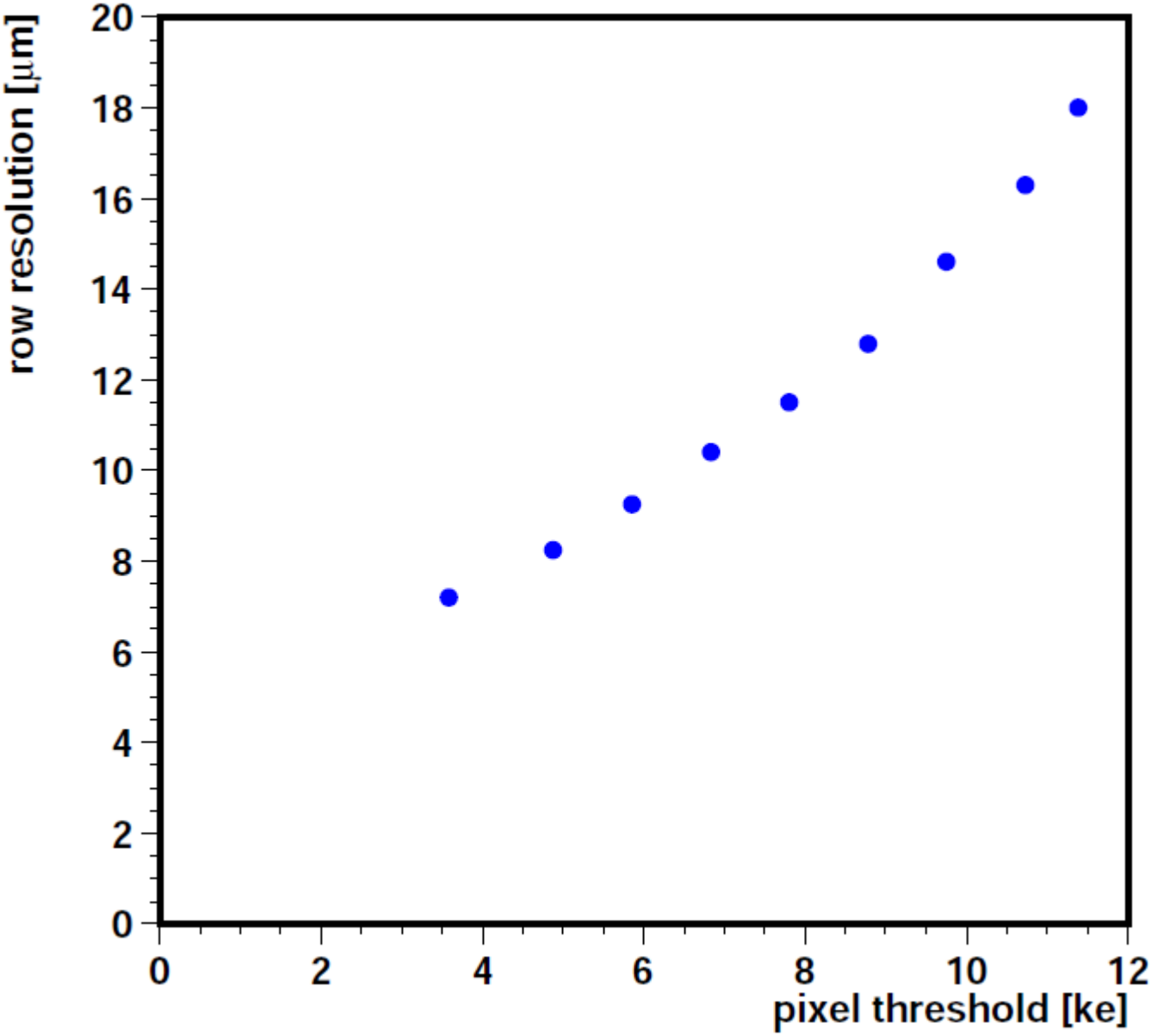
Vertical = rows

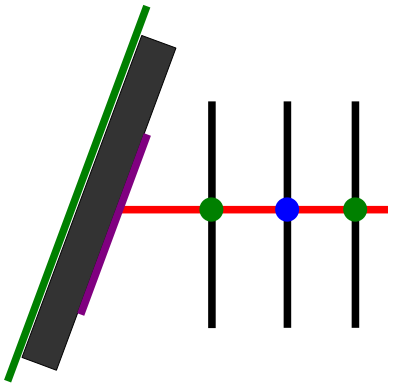
- CMS pixel = 100 µm.

Residual:

- σ = 8.2 µm,
- telescope extrapolation: 4.5 µm,
- **CMS resolution: 7 µm.**

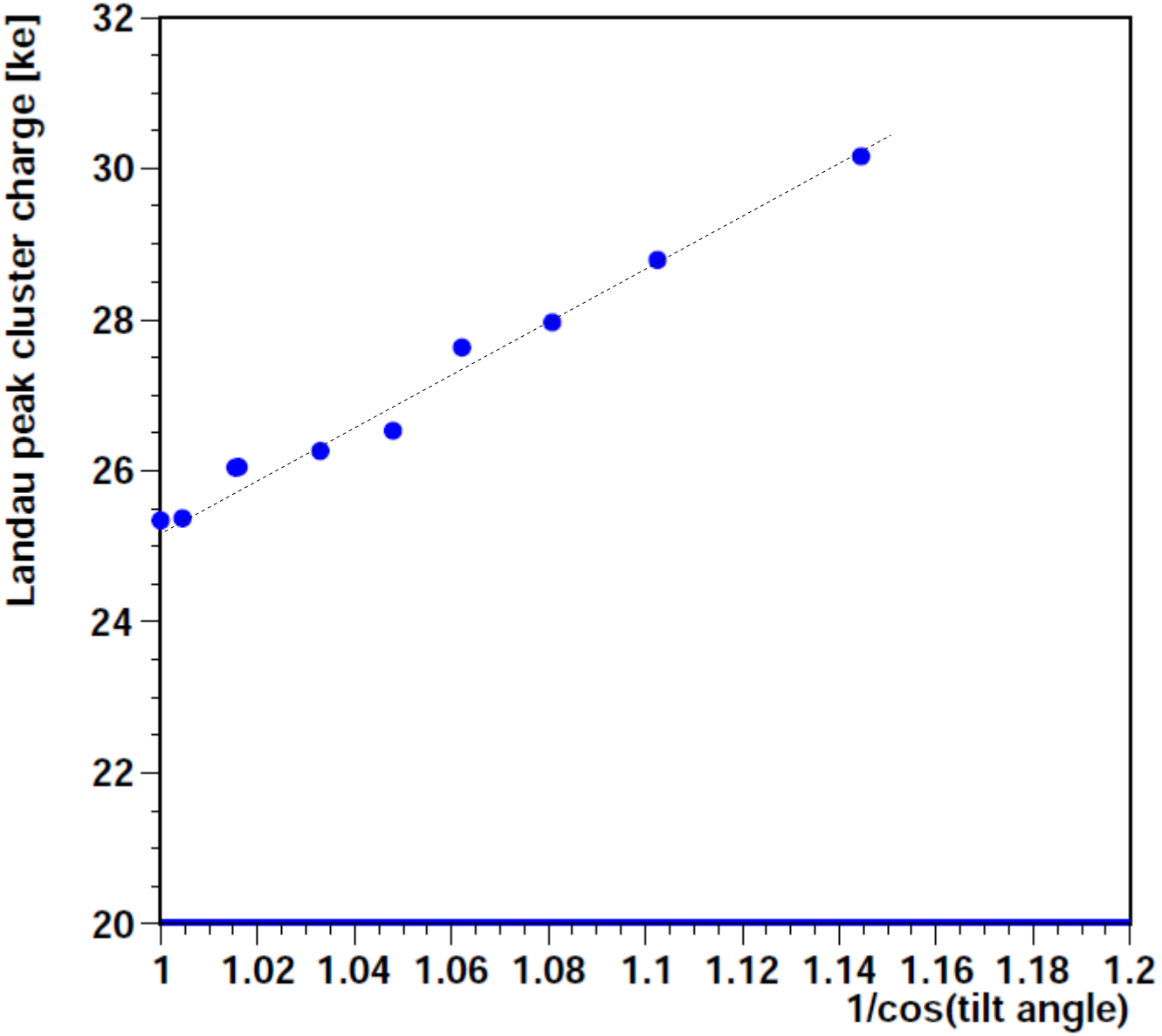
CMS pixel row resolution vs threshold

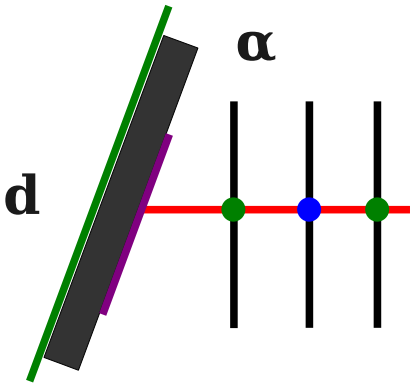




- Chip 10, 20° tilt
- 5.6 GeV, telescope extrapolation uncertainty subtracted.
- lower threshold:
  - charge sharing better exploited
  - better resolution

CMS pixel cluster charge vs tilt angle





- Chip 10, 120V
- effective sensor thickness:
  - d = 285 µm / cos α
- position of the Landau peak should be linear in d
  - timing problems?
  - threshold effects?

Outlook

- One analog PSI46xdb bump bonded to a single chip sensor at PSI is underway to DESY:
  - lab tests may start on Monday!
  - verify functionality, adapt software (DAC2 is Iana instead Vana)
  - optimize DAC parameters: gain linearity, lowest thresholds
- Test beam measurements:
  - Efficiency
  - Resolution
  - Threshold
  - Landau peak gain calibration in tilt scan
- Summer:
  - X-ray test (need adapter and cable for single-chip module)
  - get and learn to operate psi46dig (without and with sensor)