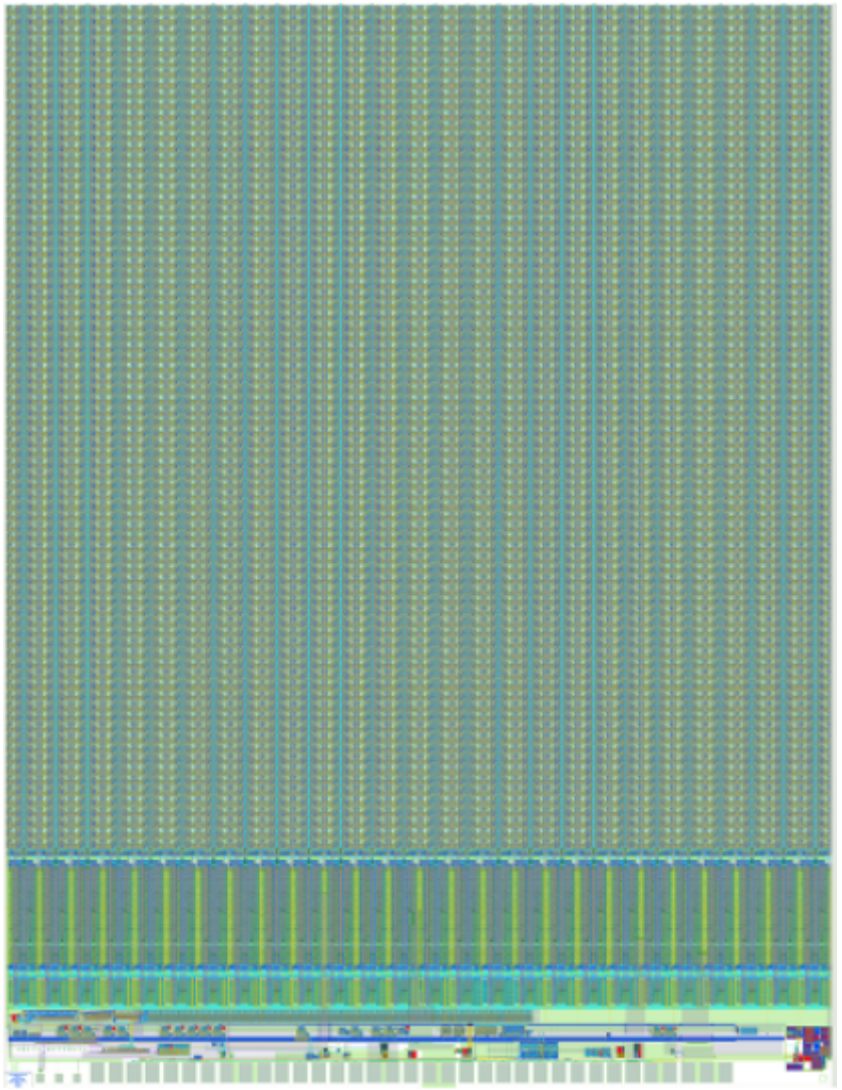
XDB ROC Tests

A. Petrukhin, D. Pitzl, S. Matthiesen

Pixel upgrade, 15.6.2012



- DESY setup
- Various tests
- Summary

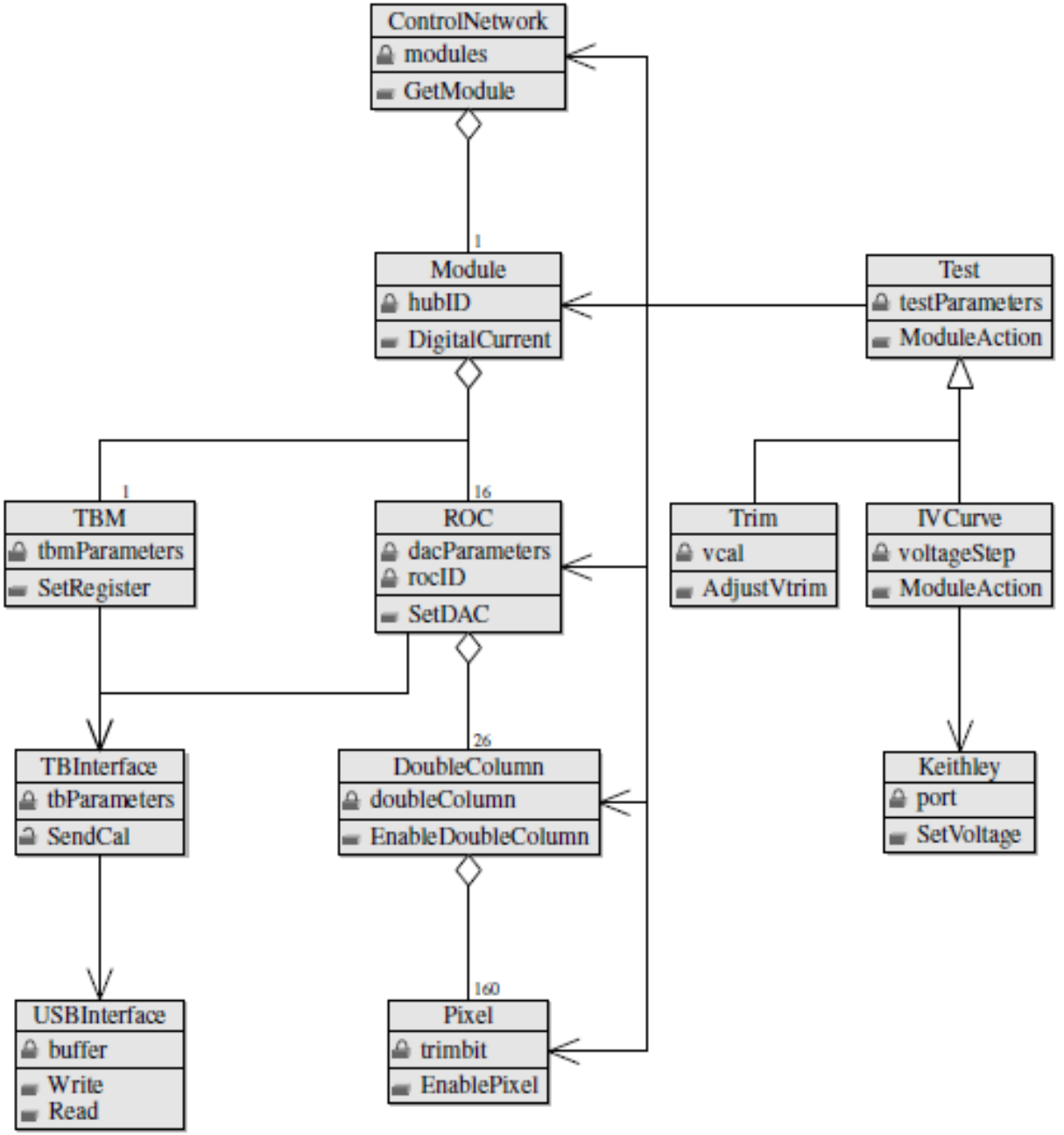
Configuration at DESY

- New xdb ROC with sensor and new adapter
- PSI test board, with Aug 2010 FPGA firmware (binary file from Beat Meier downloaded using ALTERA USB Blaster via JTAG connector)
- run in 40 MHz mode
- Dell laptop running Ubuntu 10.10 Linux.
- psi46expert software compiled using gcc-4-5-2 in AMD 64 bit.
- libftd2xx1.0.2 for USB interface from FTDI: http://www.ftdichip.com/Drivers/D2XX.htm

PSI46expert software at DESY

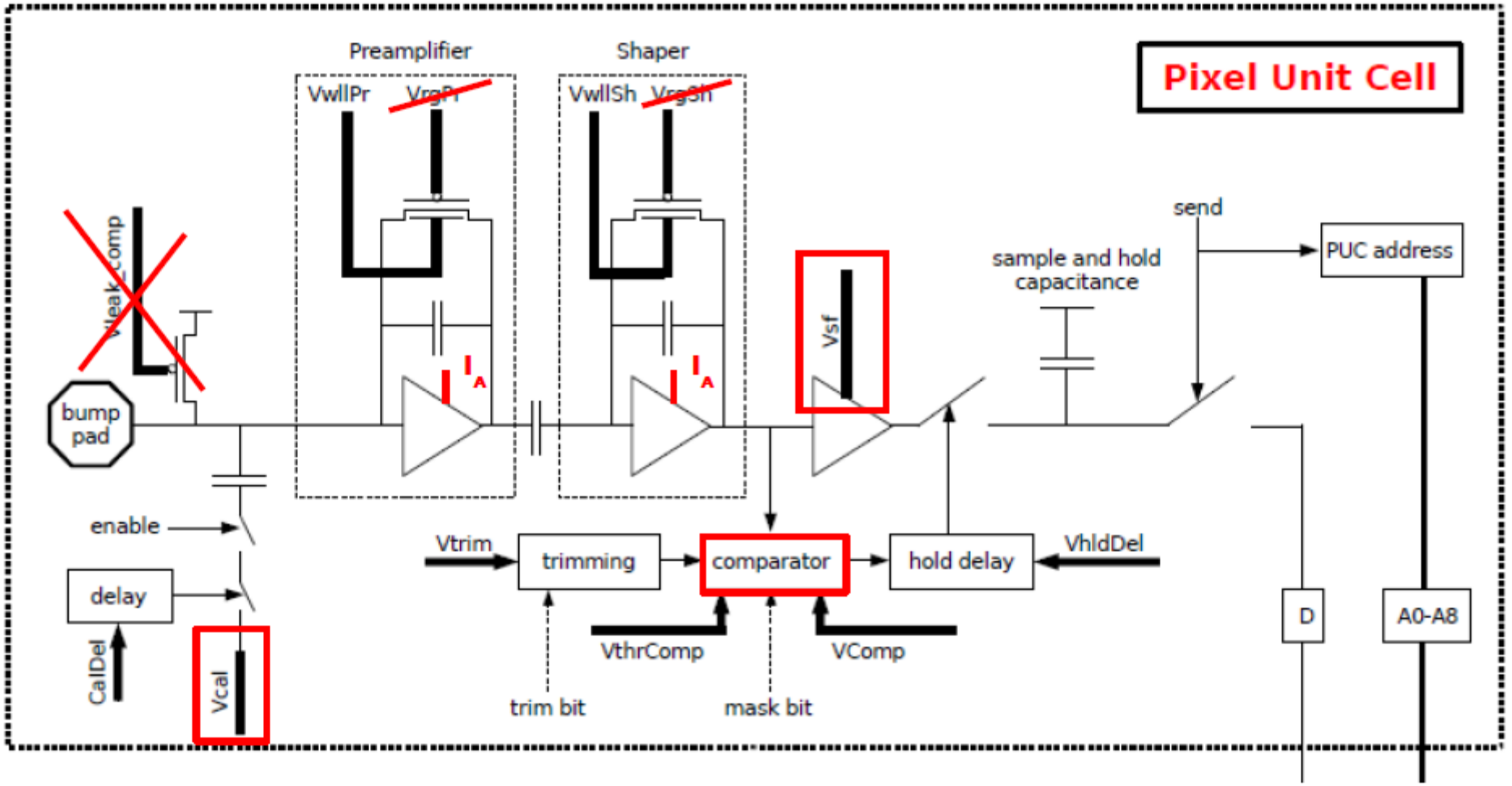
- Several new routines written:
  - DAC scans, noise maps, address decoding…
- DAC and TB settings for new chip are determined from Pretest.
- Threshold trimming is applied
- New slope of 0.15 A/DAC is measured
- FullTest confirms the determined parameters except BumpBonding test and AddressDecoding test (for part of the ROC)
- More individual tests are ongoing

psi46expert software



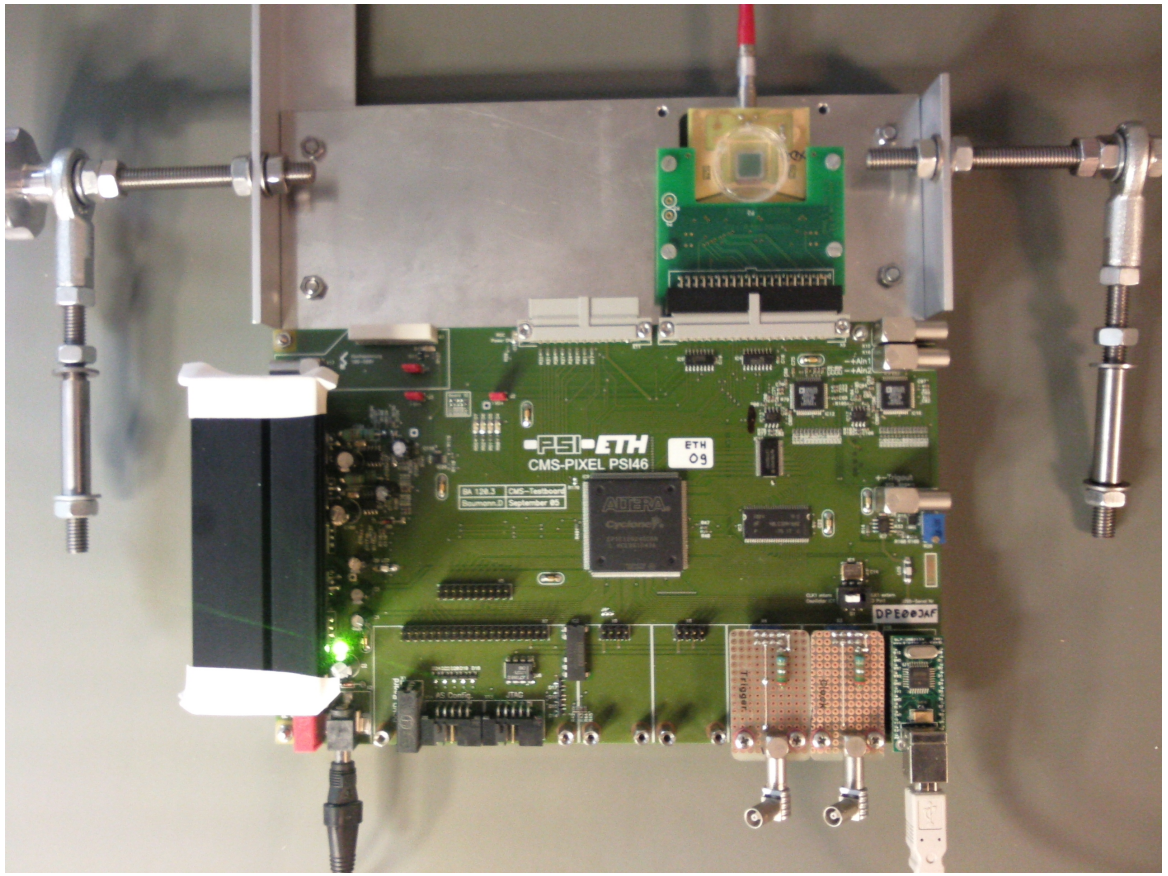
- C++ class library.
- Written by Peter Trüb (ETH, 2005-2007) for Scientific Linux (32 bit).
- Now compiled with g++ 4.4.5 under Ubuntu 10.10 (64 bit).
- USB interface required some changes (long → int).
- All tests were working properly with old ROC

PSI46xdb pixel unit cell



modified in PSI46xdb

Test setup at DESY



- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
- Use the same analog signal path as before

First step xdb

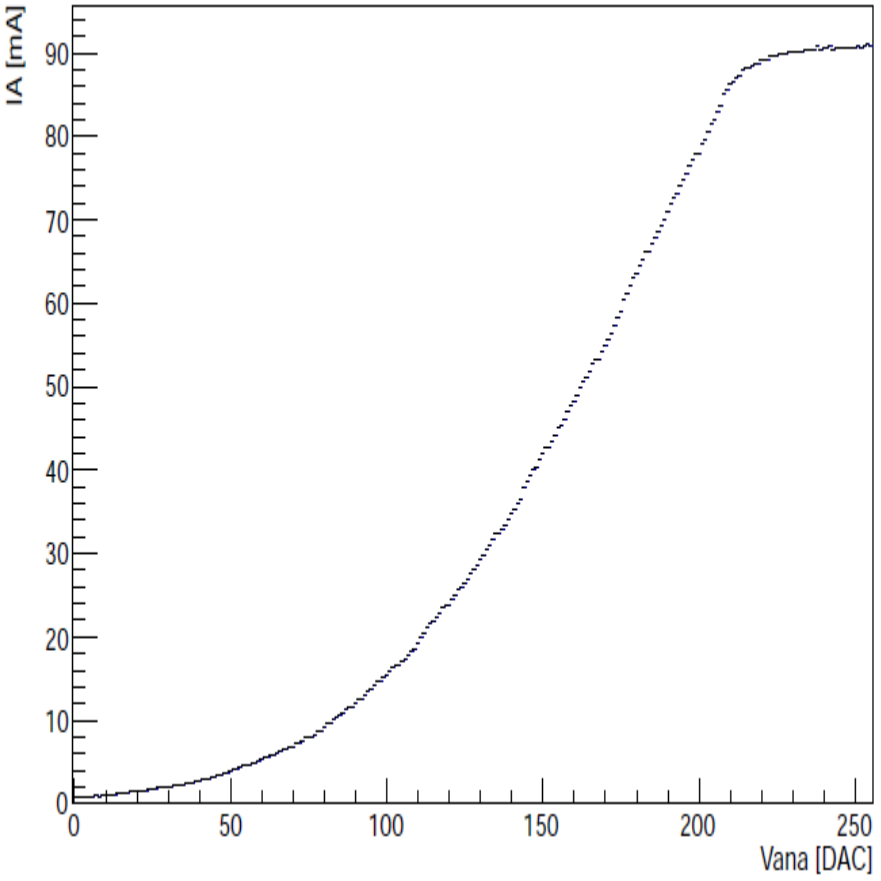
```
psi46expert> tb ia
[TBAnalogInterface] Analog current 0.0298
psi46expert> tb id
[TBAnalogInterface] Digital current 0.0472
psi46expert> tb va
[TBAnalogInterface] Unknown testboard command: va
psi46expert> tb getva
[TBAnalogInterface] Analog voltage 1.733
psi46expert> tb getvd
[TBAnalogInterface] Digital voltage 2.54
psi46expert> adc
ADC with TBM enabled
Count 19
Data: -750 -750 -750    0    0    0    0    0 : -900   36  536 : -750 -750    0    0  374 -188  186 -188
```

Second step xdb

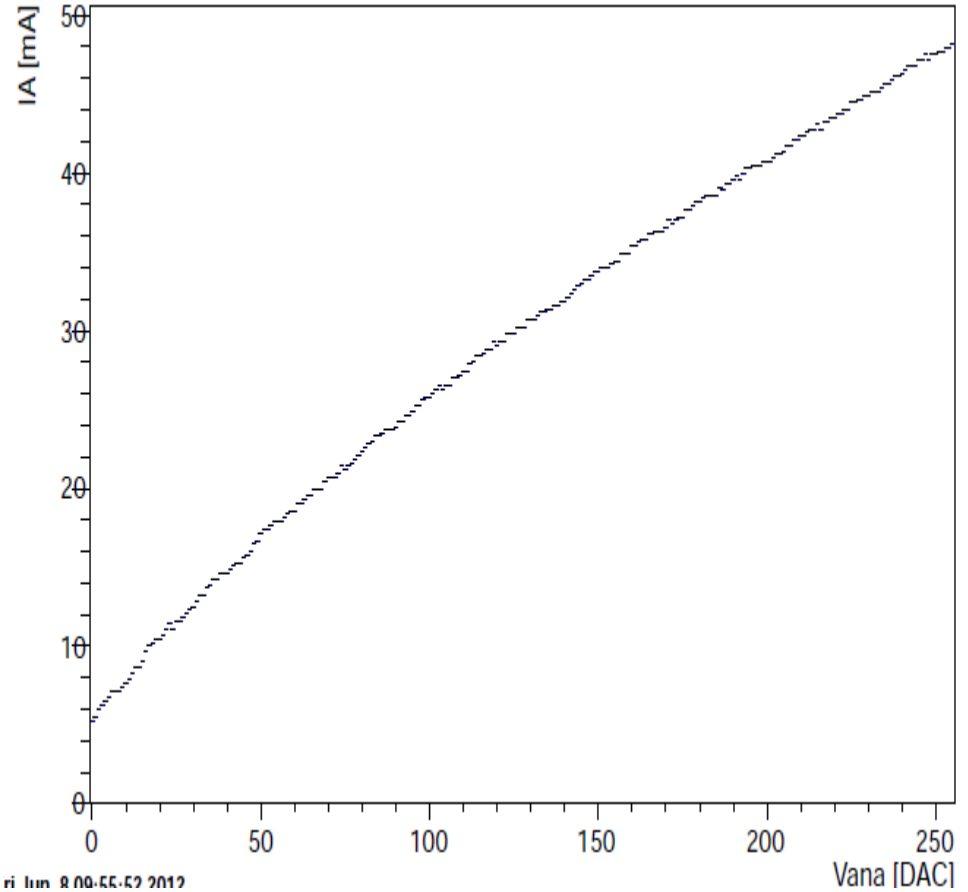
```
psi46expert> arm 2 2
psi46expert> Vcal 99
psi46expert> adc
ADC with TBM enabled
Count 25
Data: -750 -750 -750    0    0    0    0  186 : -900   44  616 : -208   36  744  260 -208 -536 : -750 -750
 0    0  374 -188  186 -188
psi46expert> Vcal 255
psi46expert> adc
ADC with TBM enabled
Count 25
Data: -750 -750 -750    0    0    0    0  374 : -896   40   64 : -200   36  748  264 -208 -492 : -750 -750
0    0  374 -188  186 -188
psi46expert> Vcal 0
psi46expert> adc
ADC with TBM enabled
Count 19
Data: -750 -750 -750    0    0    0  186 -188 : -900   40  932 : -750 -750    0    0  374 -188  186 -188
```

Power

Chip 5



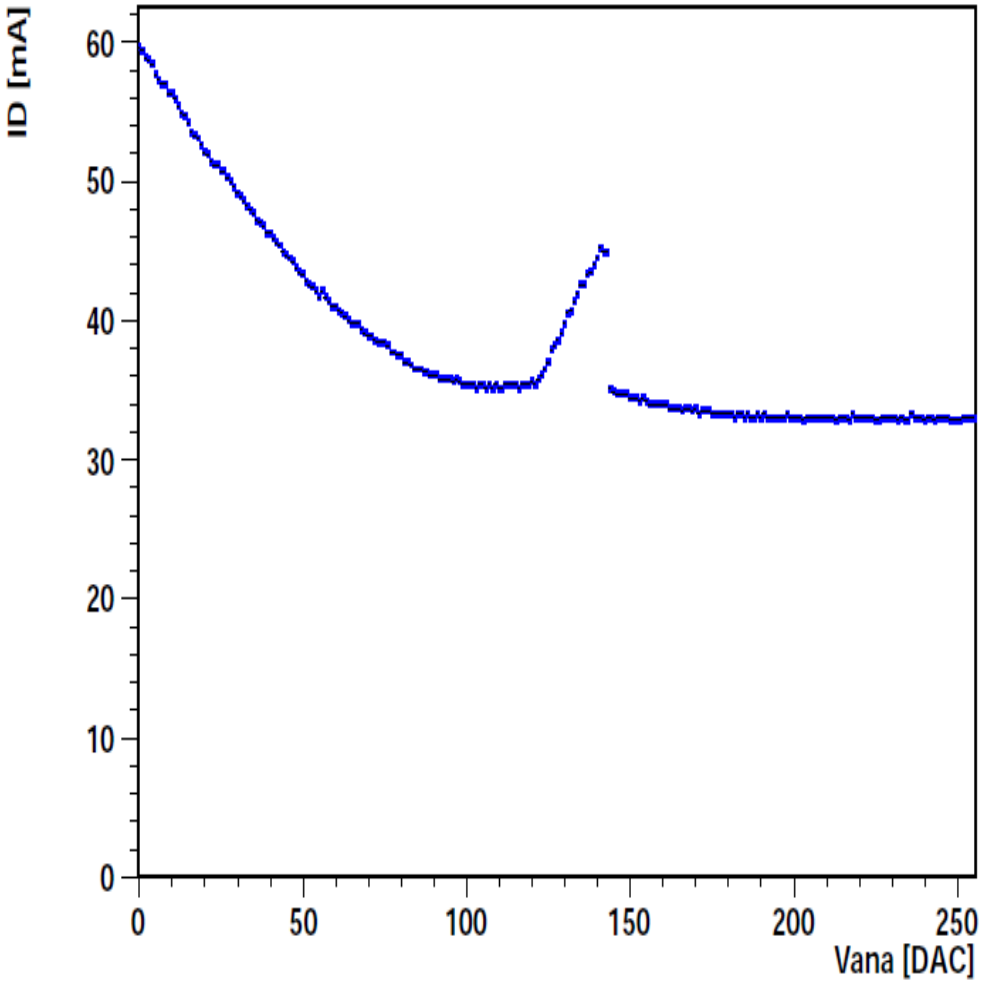
Chipx



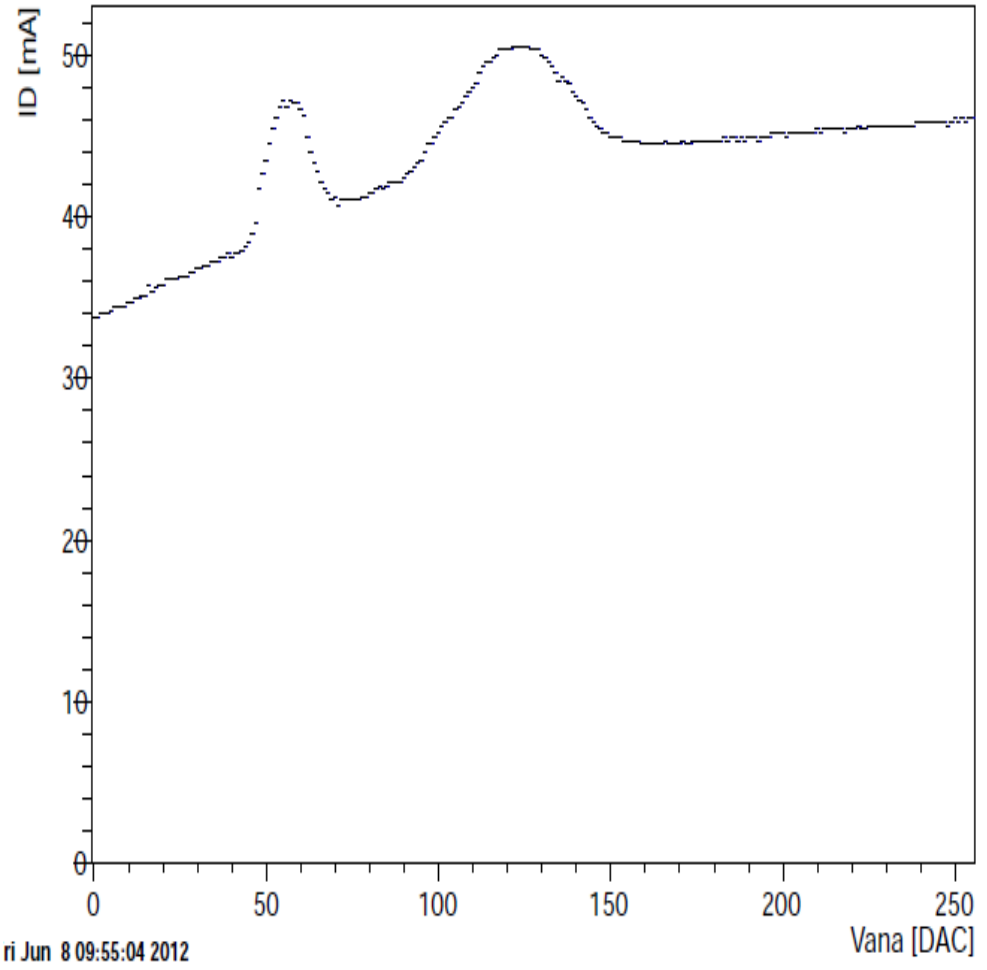
IA is a linear now (and smaller ?)

ID vs Vana

Chip 5



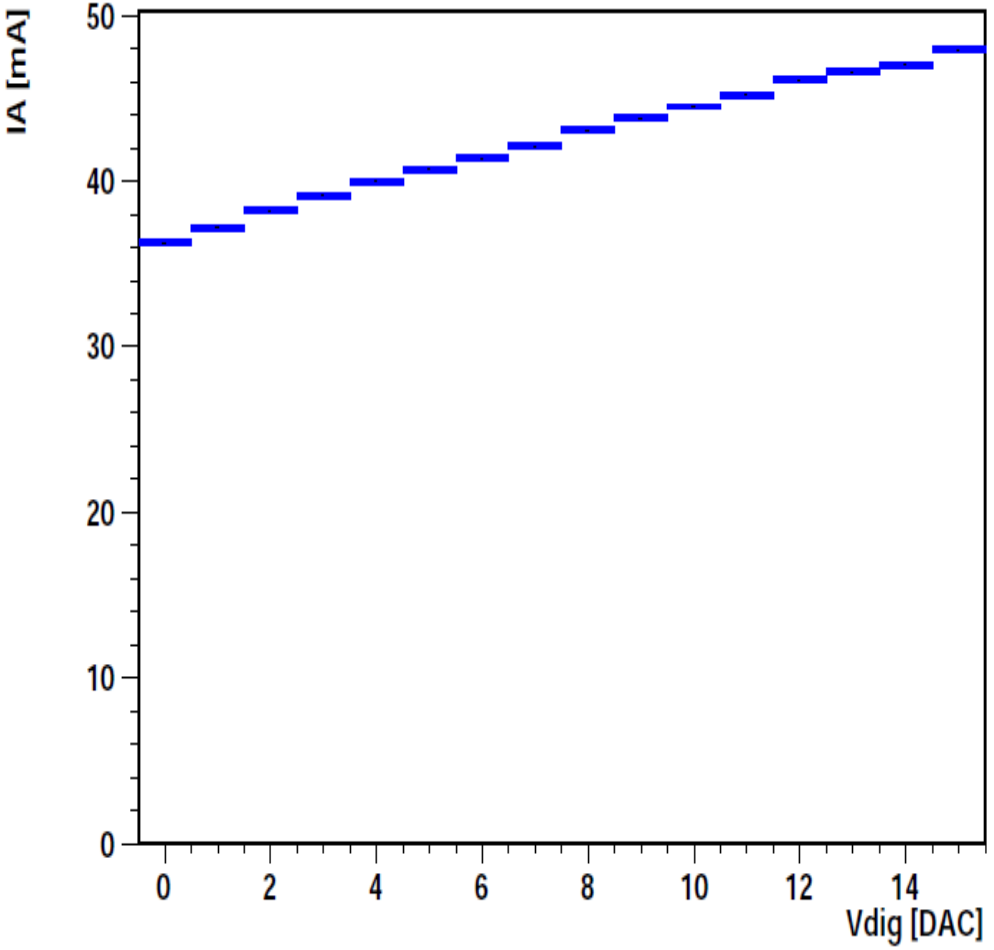
Chipx



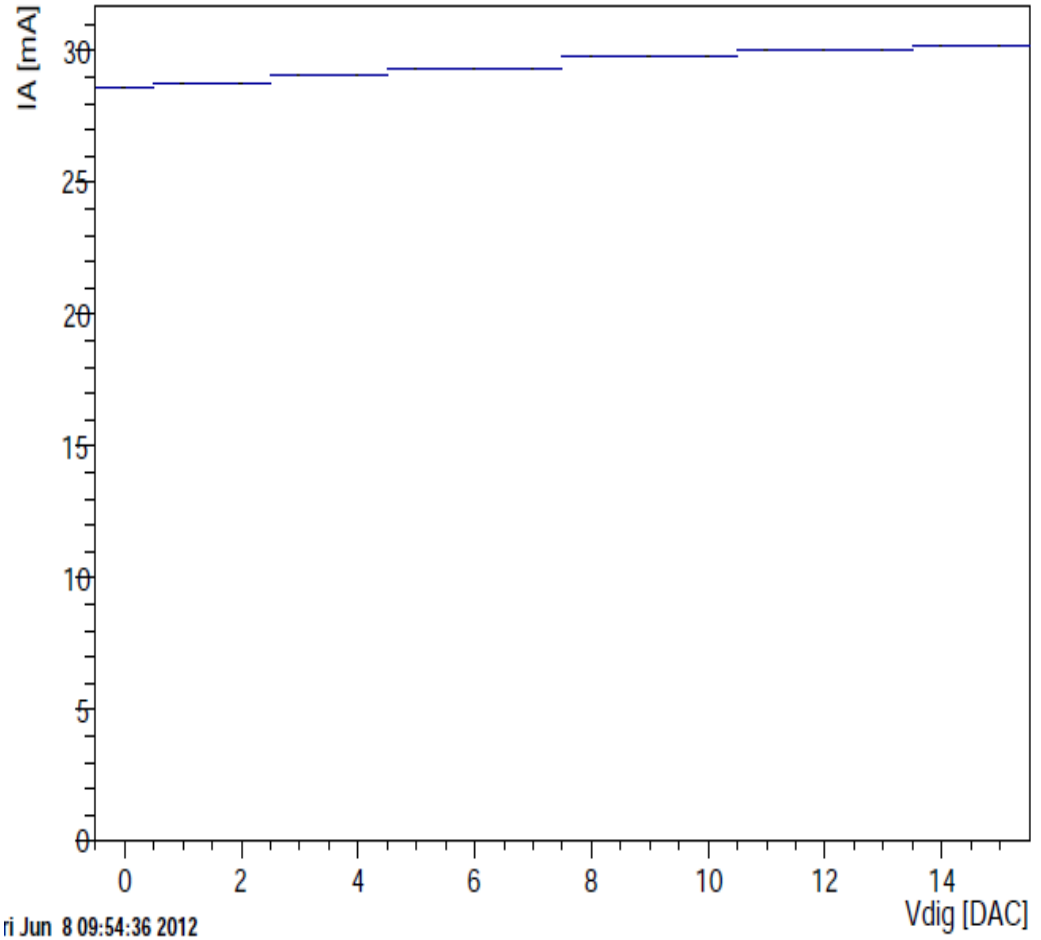
Different ID behavior

IA vs Vdig

Chip 5



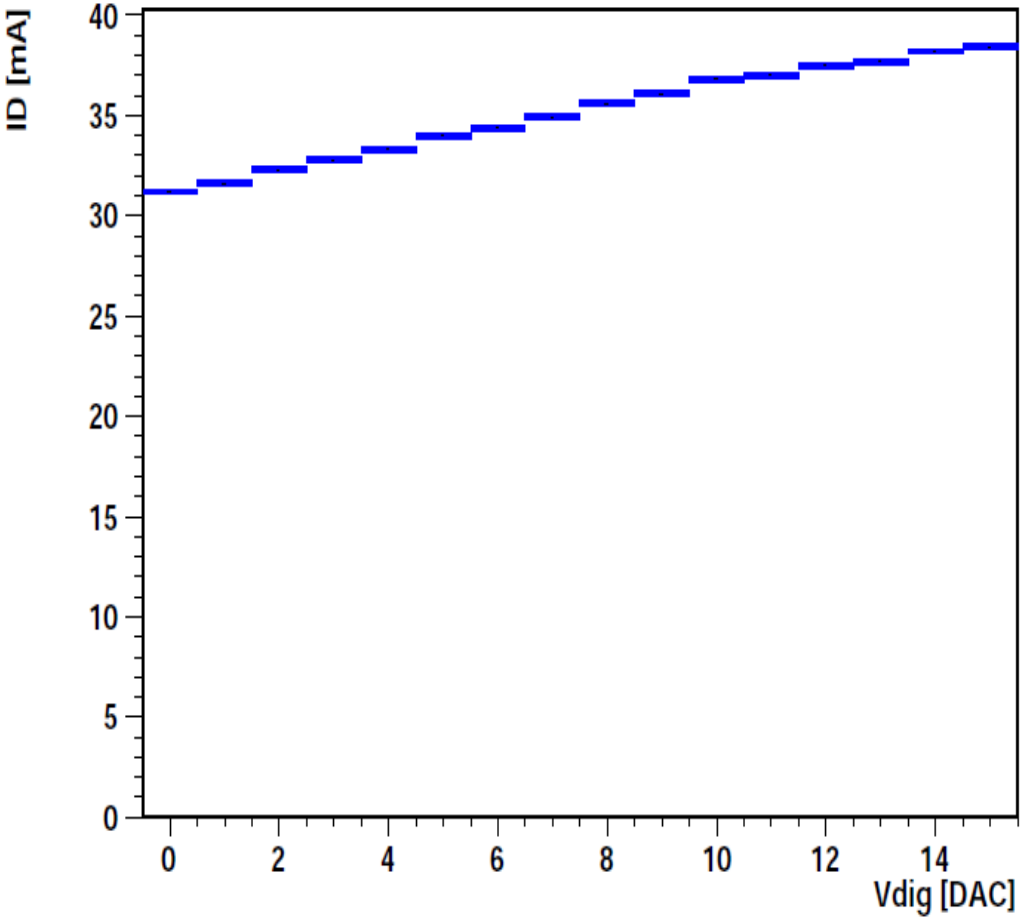
Chipx



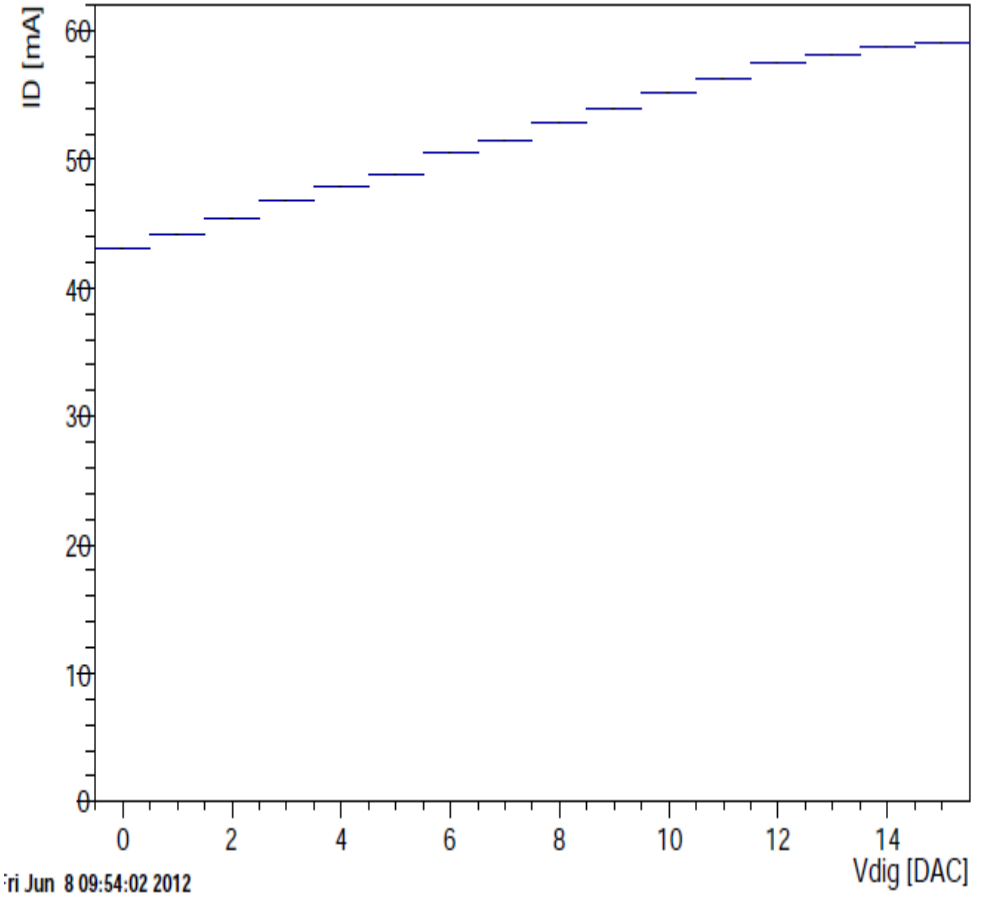
More flat dependence on Vdig

ID vs Vdig

Chip 5

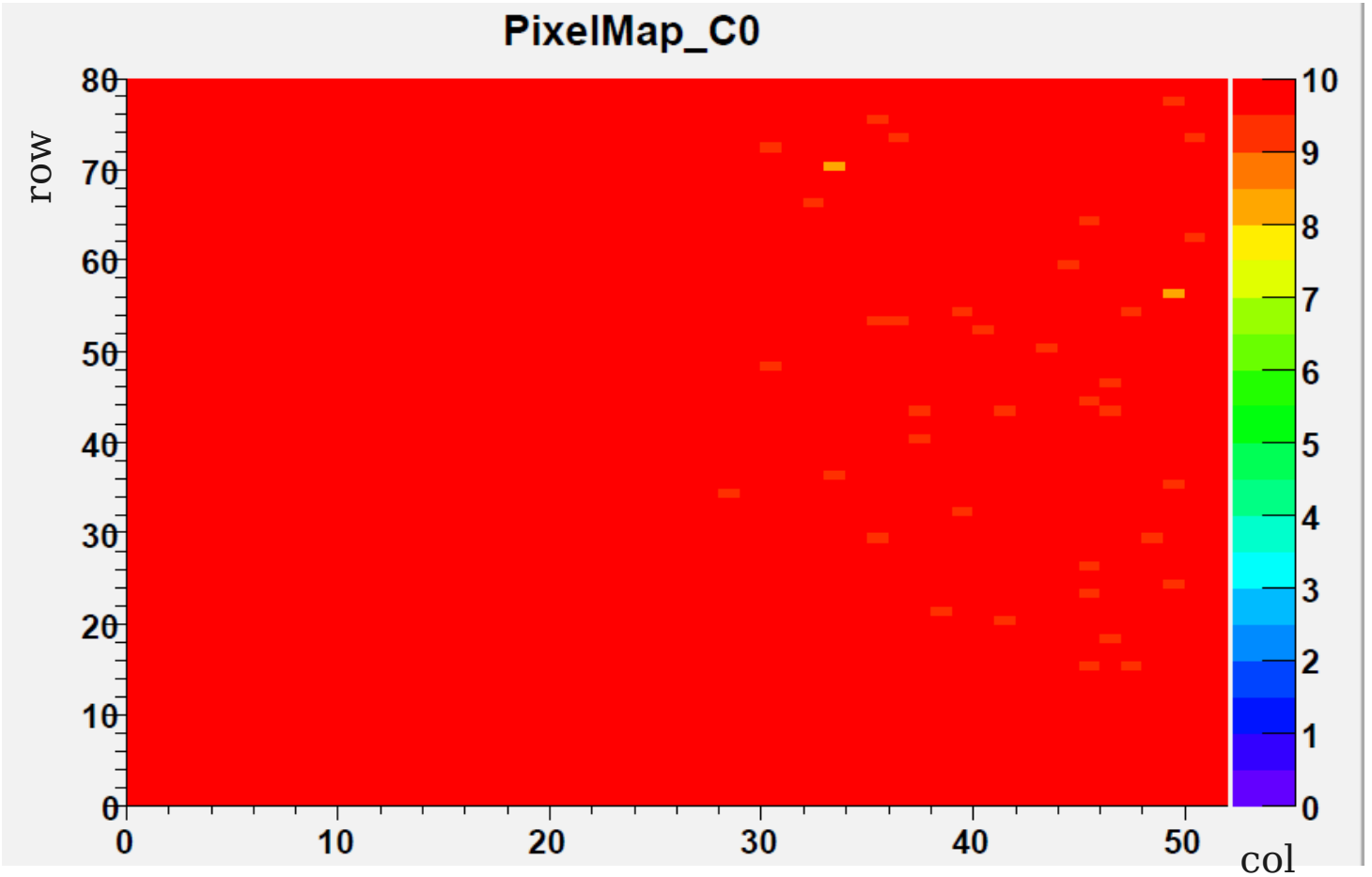


Chipx



Higher ID ?

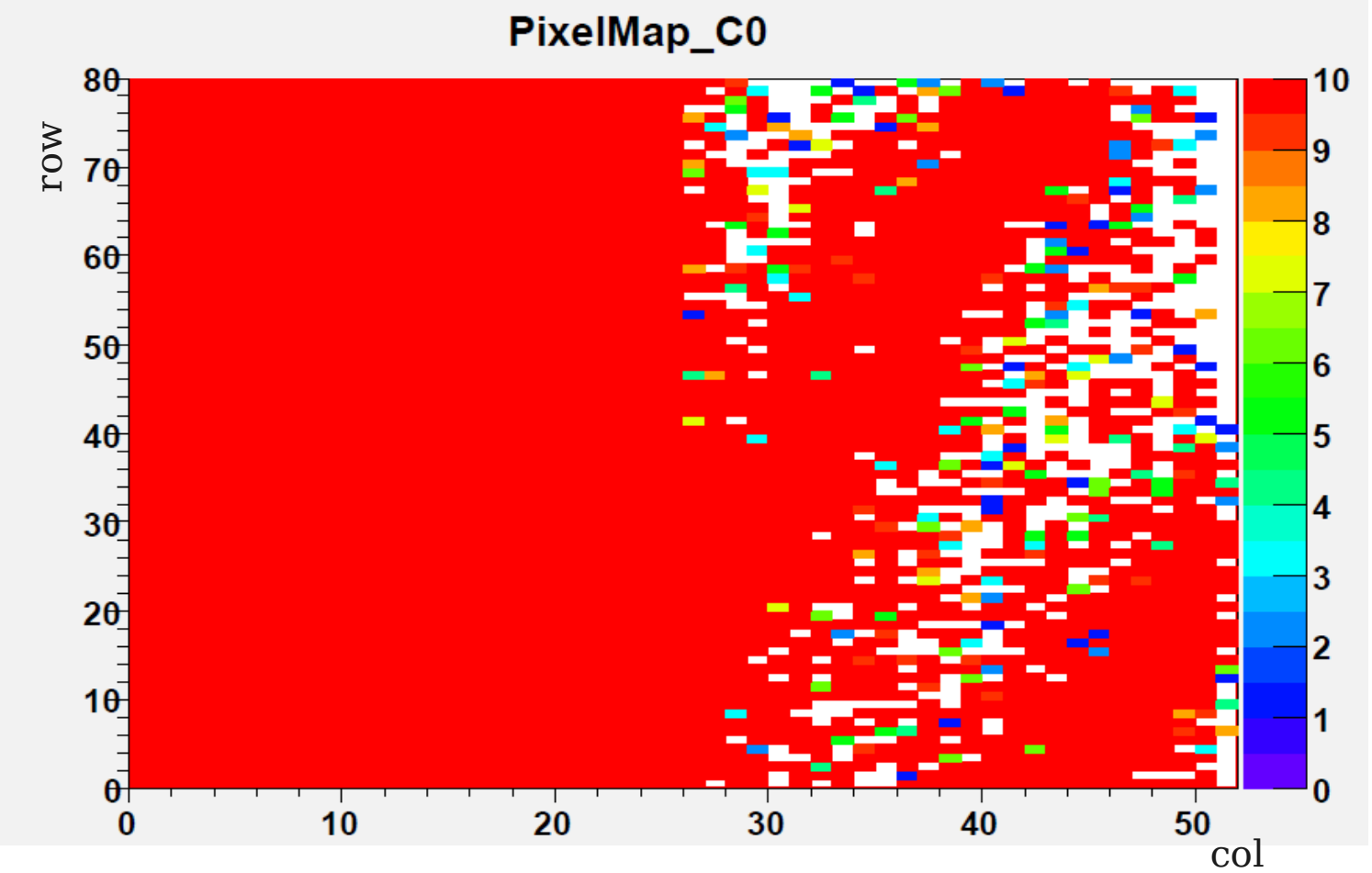
Pixel Alive test xdb



Charges above threshold are injected into all pixels in a ROC and the correct response of each pixel is verified

Chip is protected from the light

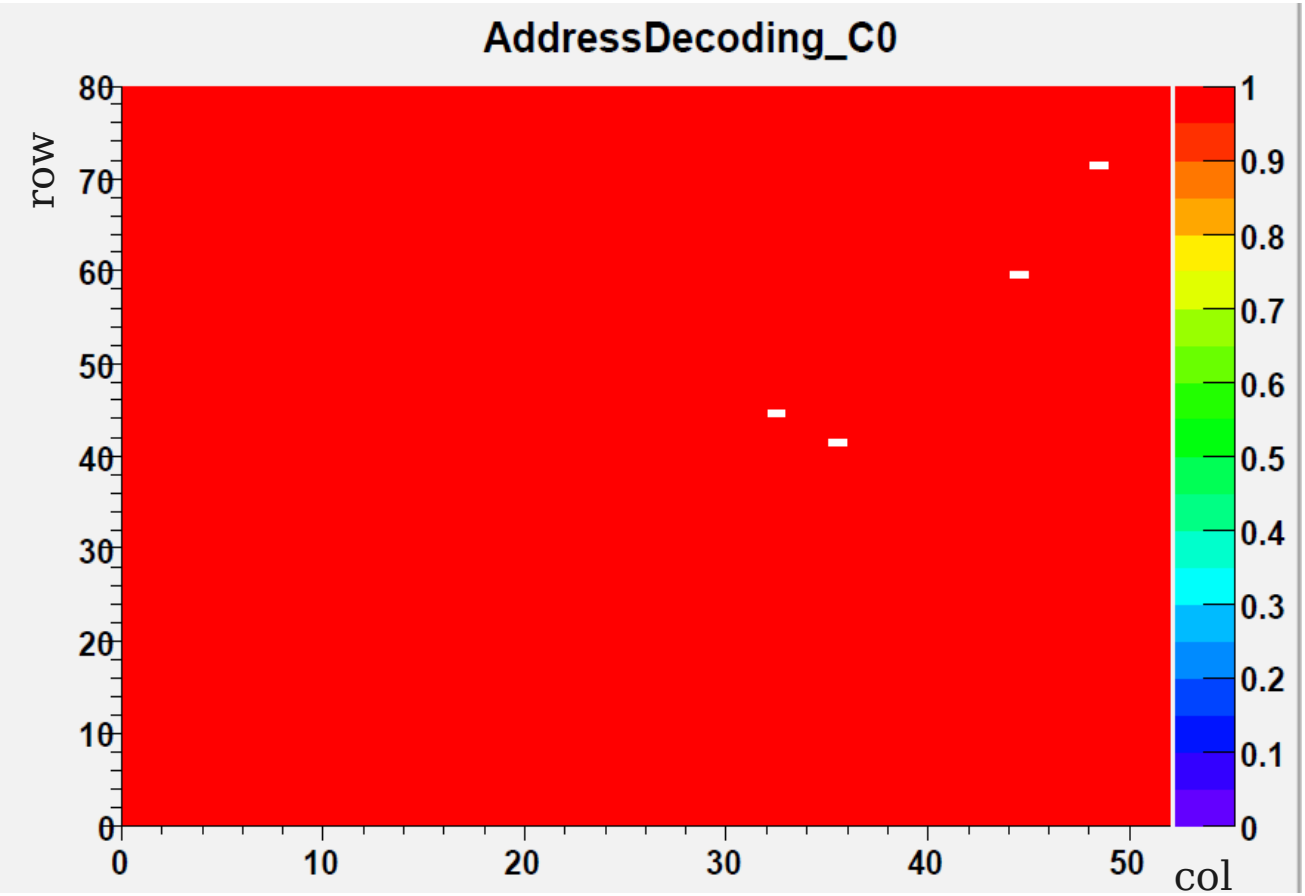
Pixel Alive test xdb



Chip is not protected from the table lamp: strong reaction of the right half

Overcurrent has happened after few test repetitions. Bias V=-90 V, current limit is set to 2mA

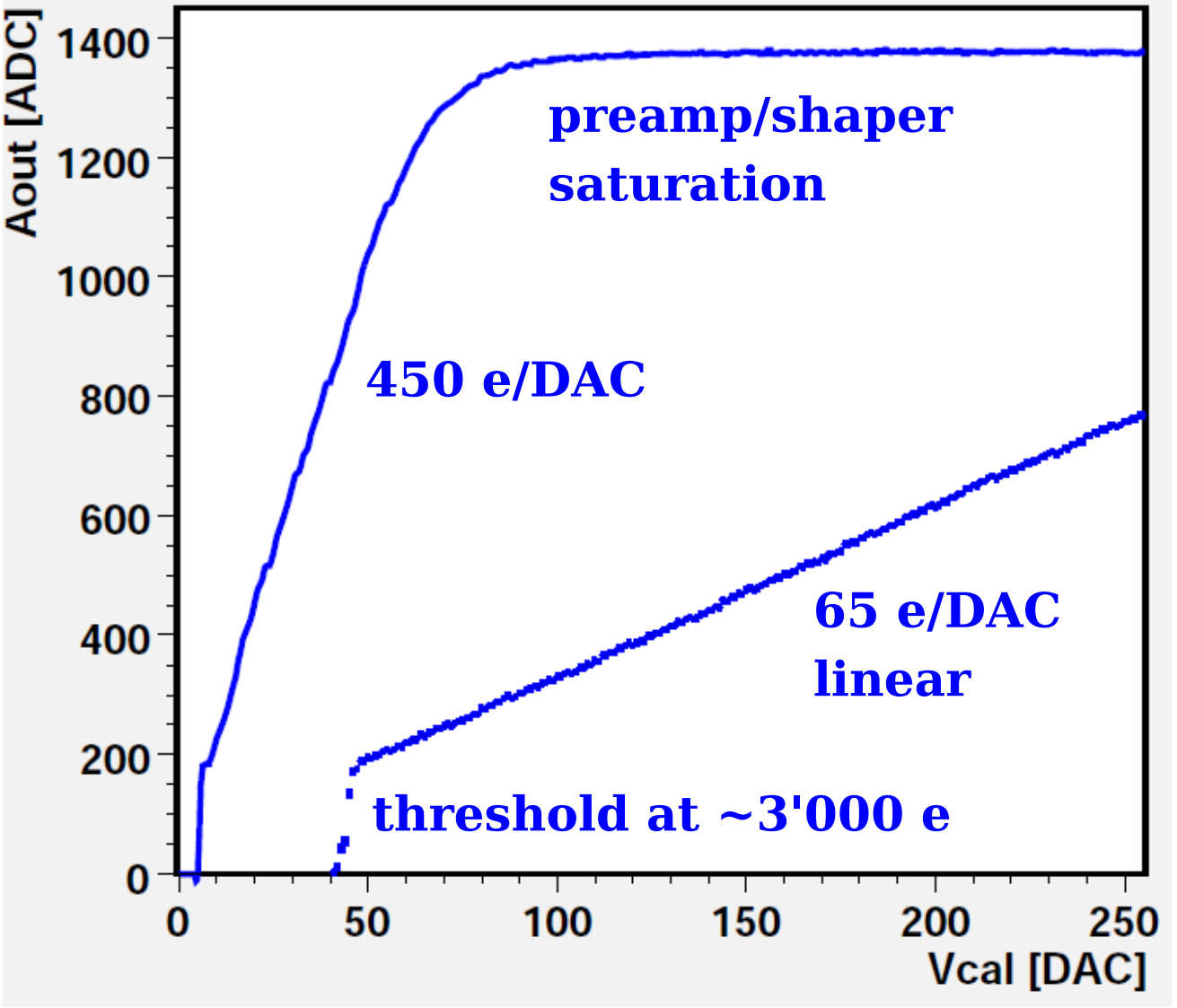
xdb functionality



Pulse each pixel and count number of data words. Fill a pixel word map if nwords = 25 (chip Header + pixel Address + analog Pulse Height).
Normalize it to 1.
4 pixels are not responding correctly.

Gain and linear range Chip5

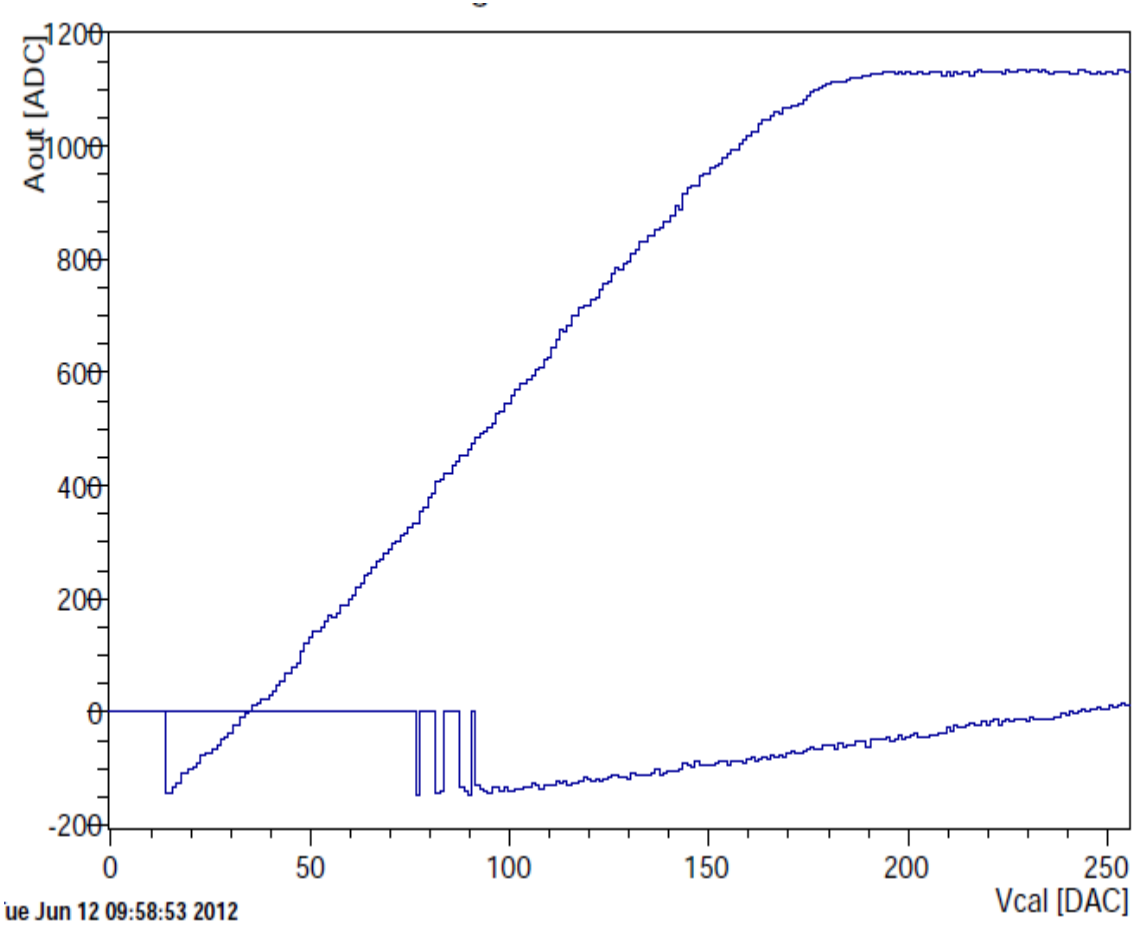
Chip 5



- One pixel.
- 2 Vcal ranges (PSI X-ray calibration):
  - CtrlReg 0 or 4,
  - 65±5 e/DAC,
  - 450 e/DAC.
- Linearity for small pulses important for spatial resolution using charge sharing.
- Saturation around 36'000 e (~2 MIP).

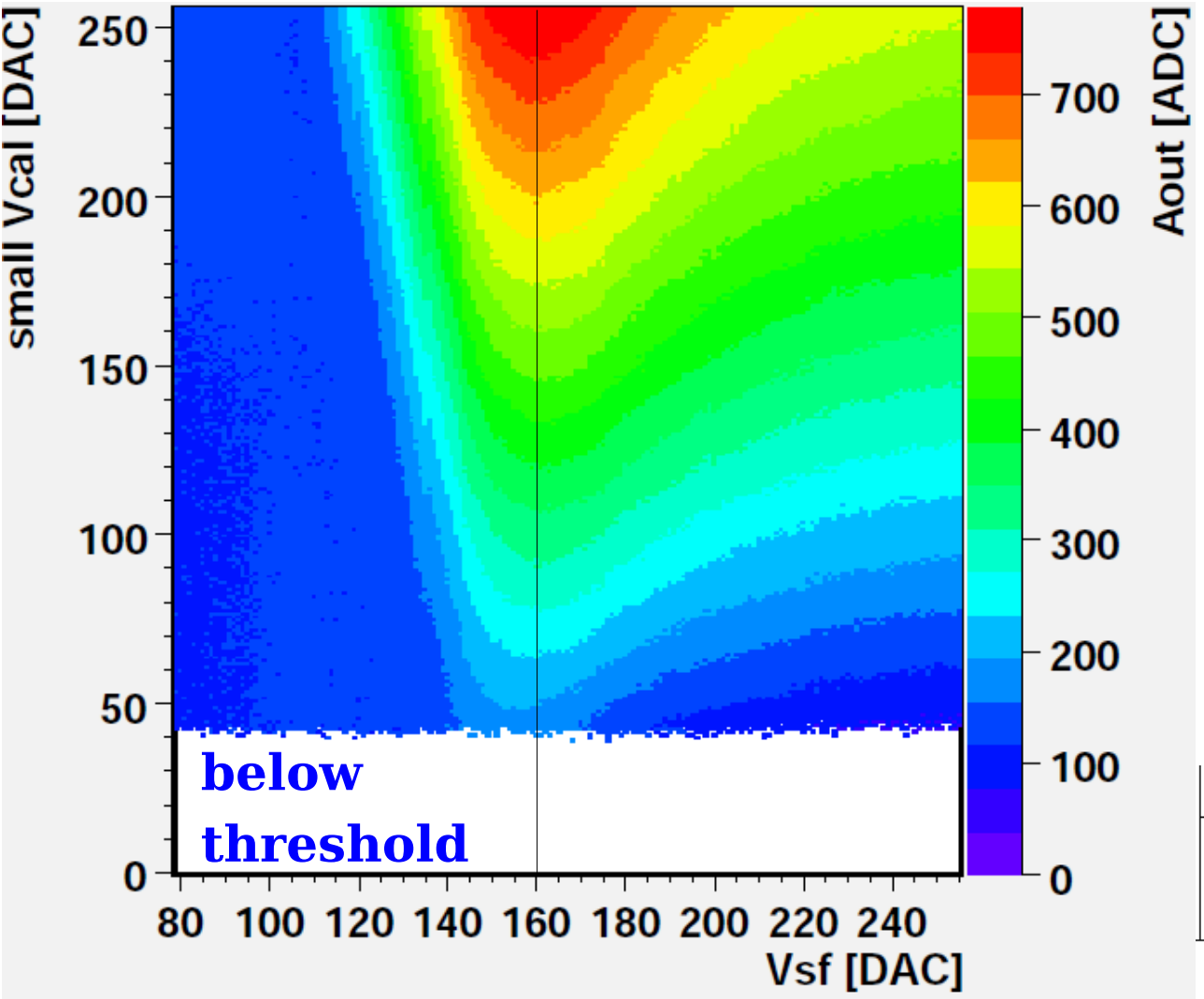
Gain and linear range xdb

Chipx

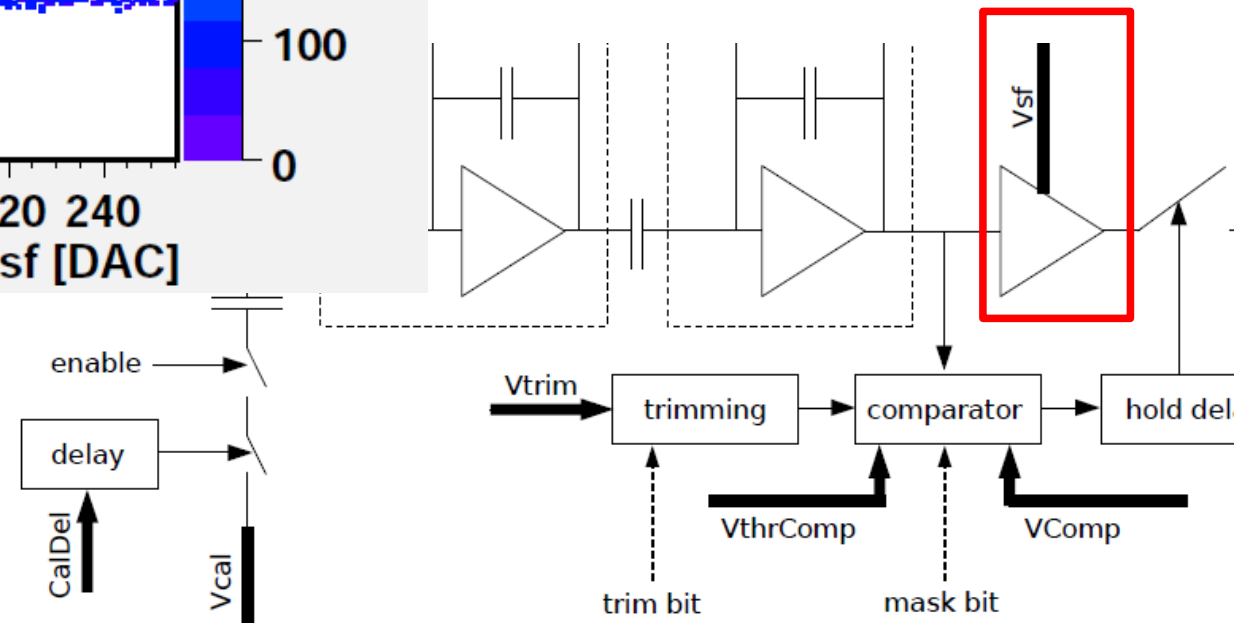


- One pixel.
- 2 Vcal ranges:
  - CtrlReg 0 or 4,
  - ?? e/DAC,
  - ?? e/DAC.
  - Needs xray calib.
- Saturation at higher Vcal, different slope
- Trimming was done for CtrlReg 4 (first time)

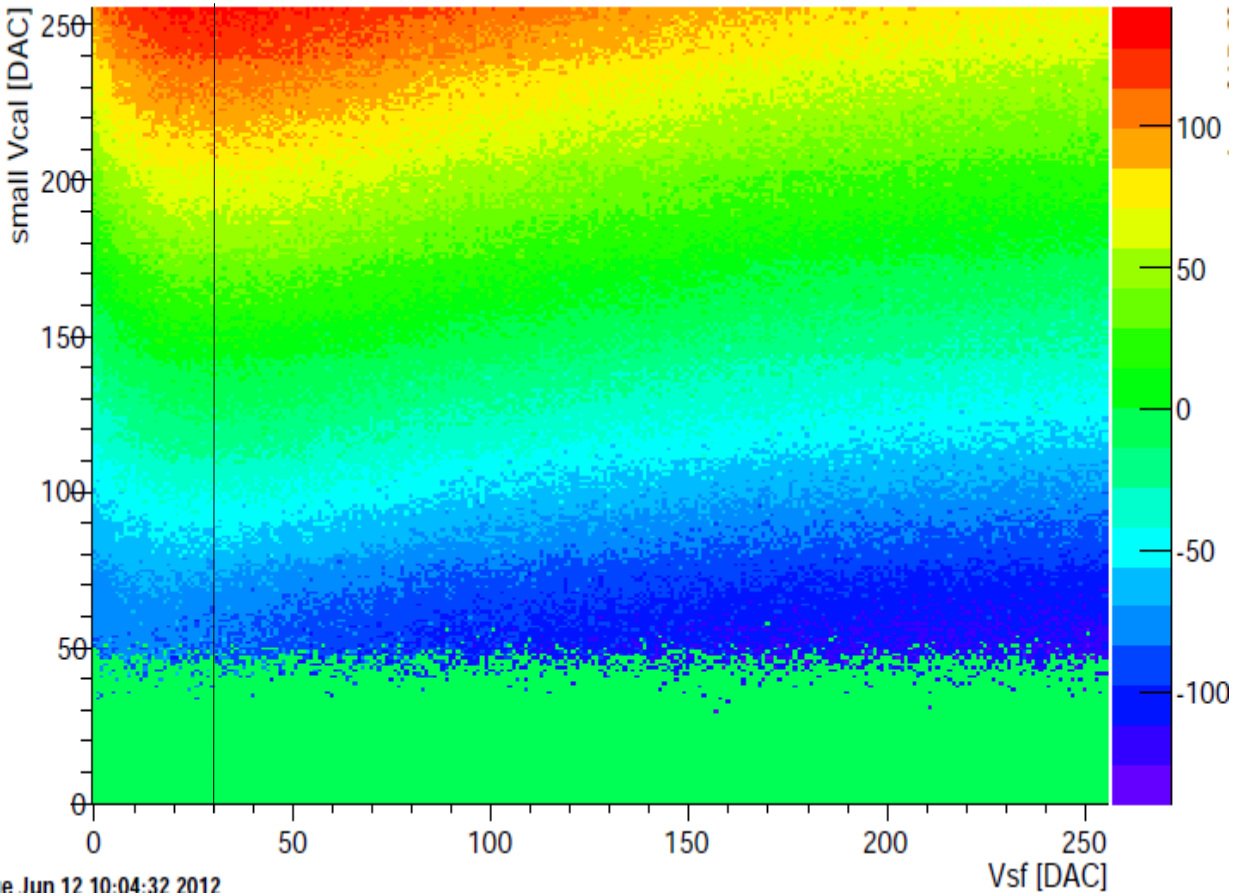
Linear range vs Vsf Chip5



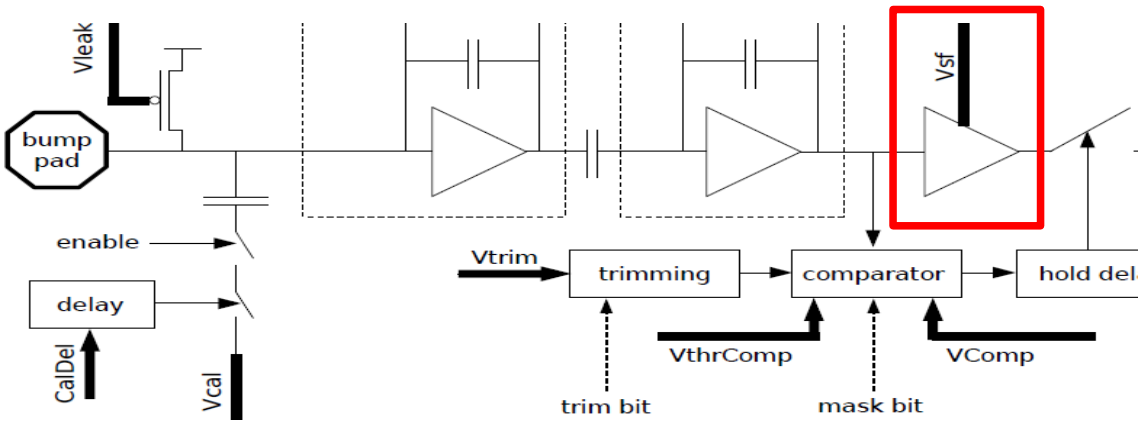
- One pixel
- Analog pulse height vs calibrate amplitude and source follower voltage.
- Best linearity in valley.



Linear range vs Vsf xdb

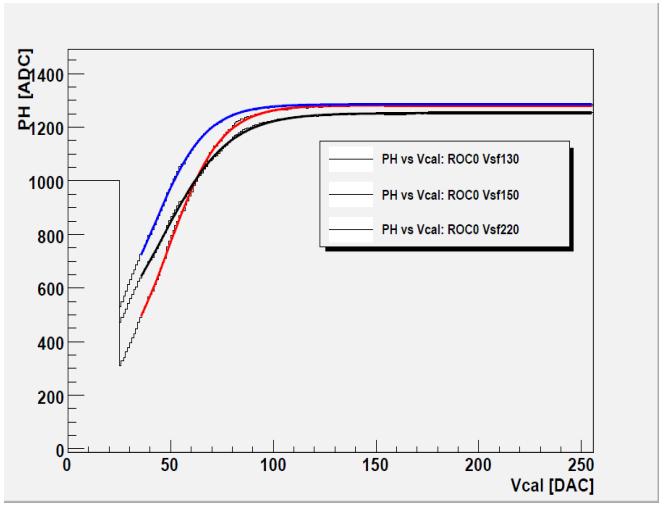


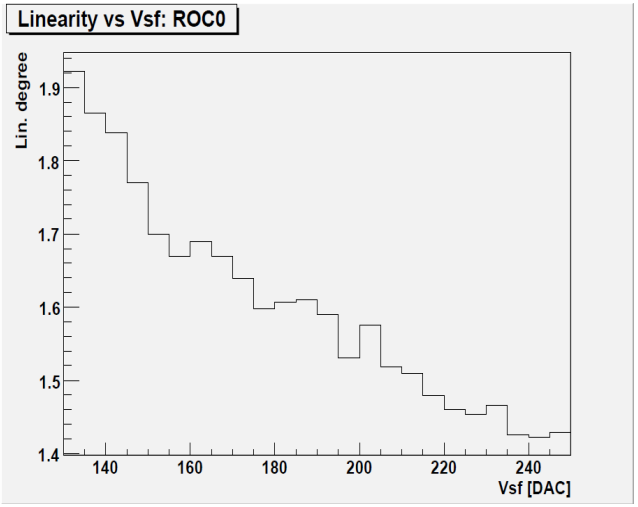
- One pixel
- Analog pulse height vs calibrate amplitude and source follower voltage.
- Vsf is lower

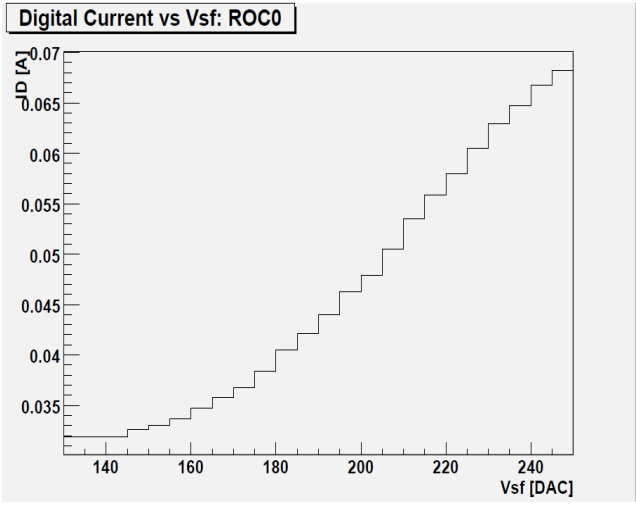


Vsf scan Chip2

- Arm one pixel. Scan Vsf
- Measure PH for vs Vcal for each Vsf value
- Fit the curves with hyperbolic tangent function $y = P3 + P2 * \tanh(P0 * x - P1)$
- Plot linearity degree (P1) and ID

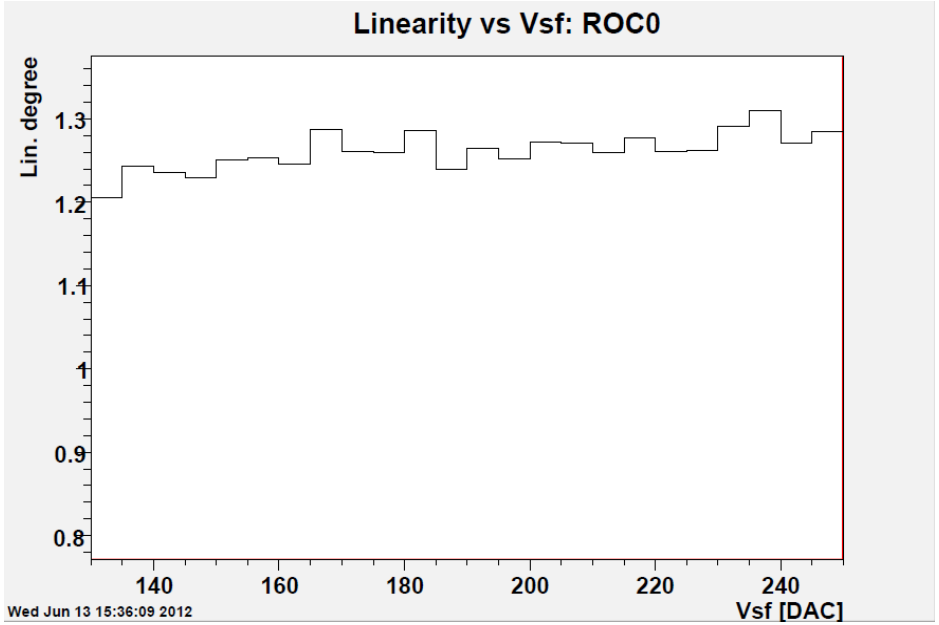


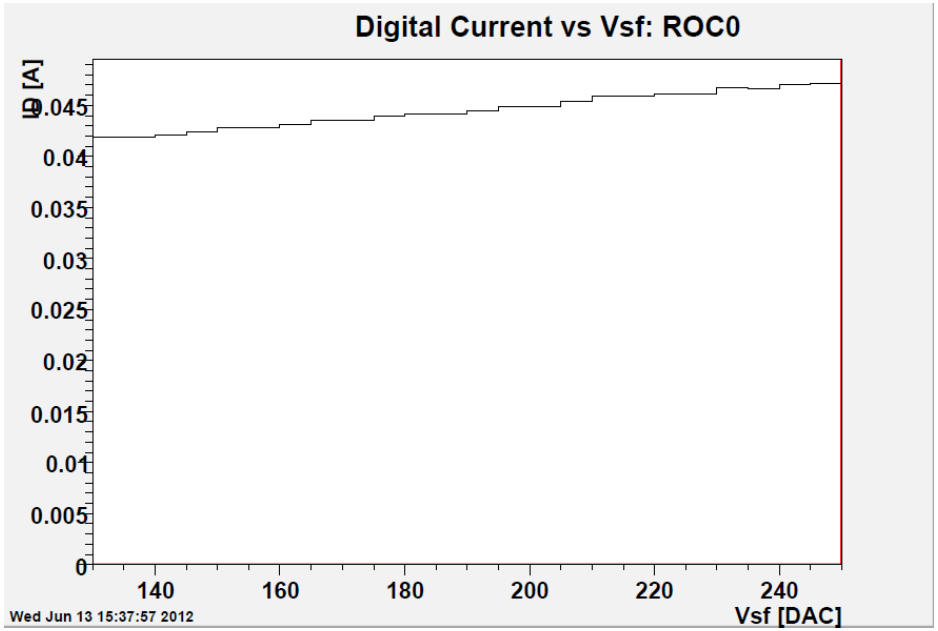




Vsf scan Chip x

- Arm one pixel. Scan Vsf
- Measure PH for vs Vcal for each Vsf value
- Fit the curves with hyperbolic tangent function $y = P3 + P2 * \tanh(P0 * x - P1)$
- Plot linearity degree (P1) and ID

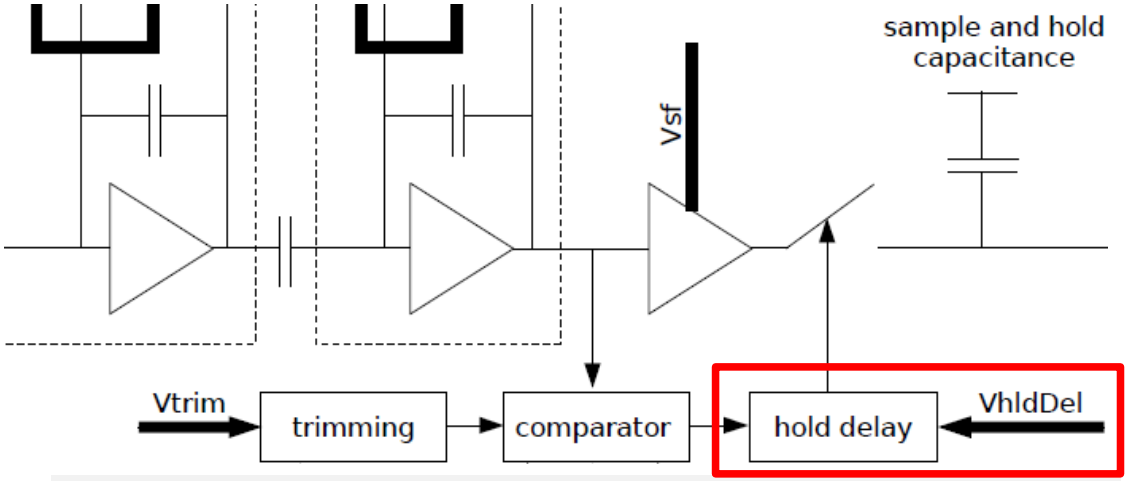


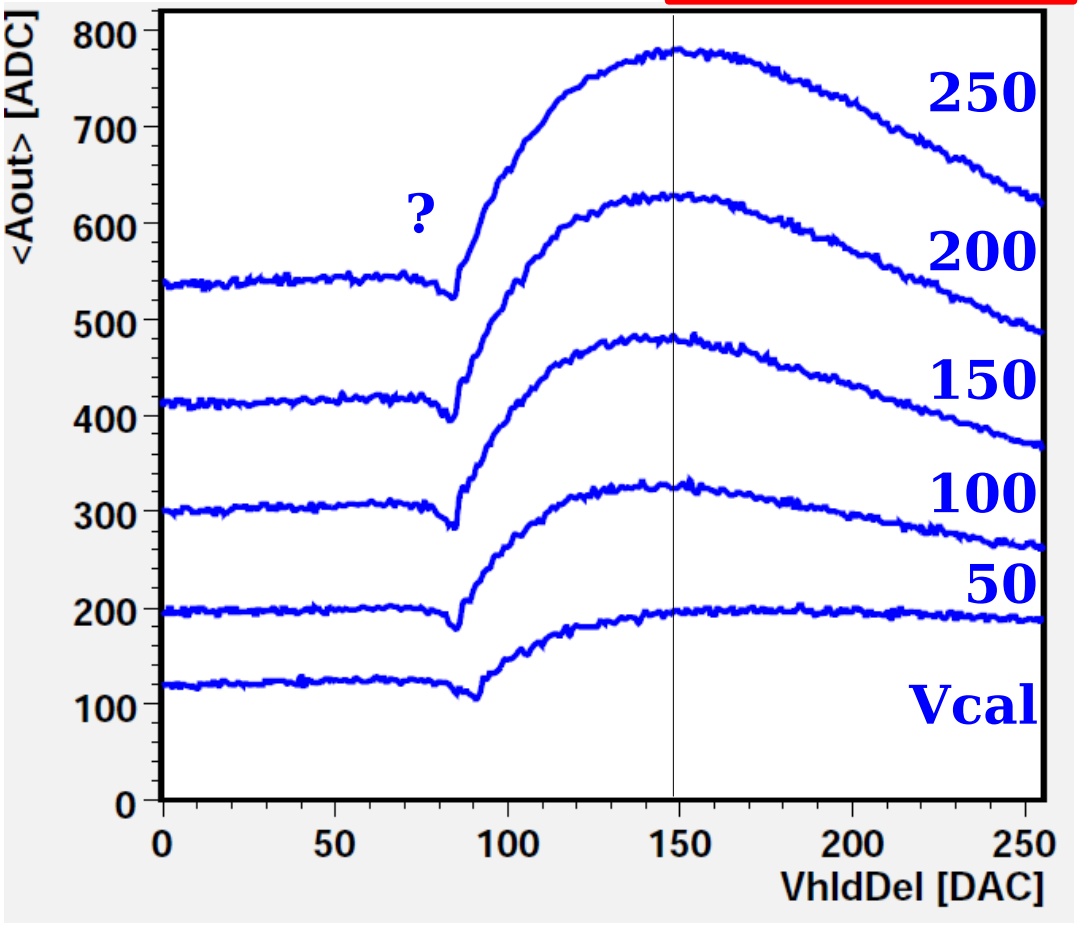


Better linearity degree

Flat ID

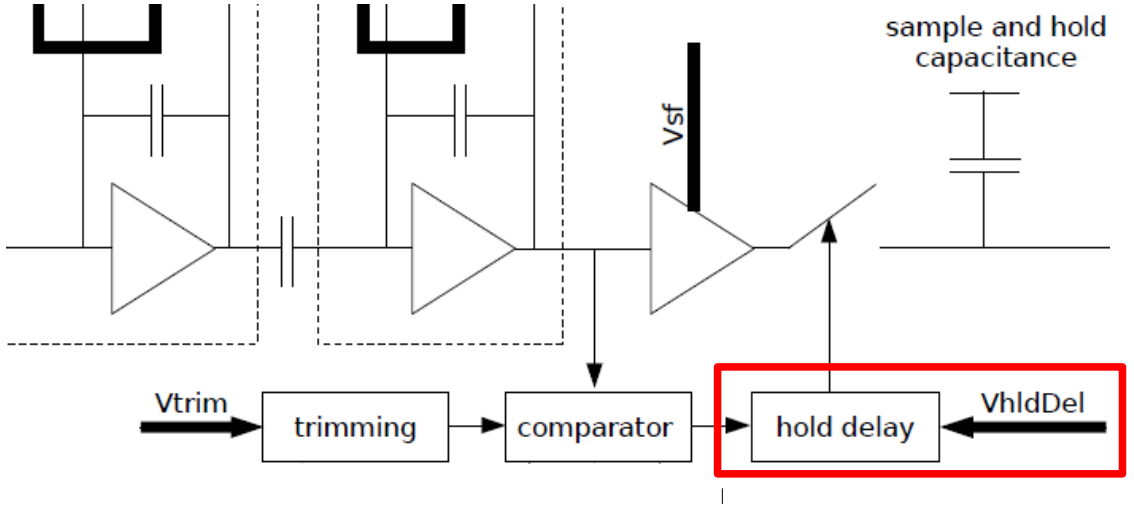
Sample and hold timing Chip 5

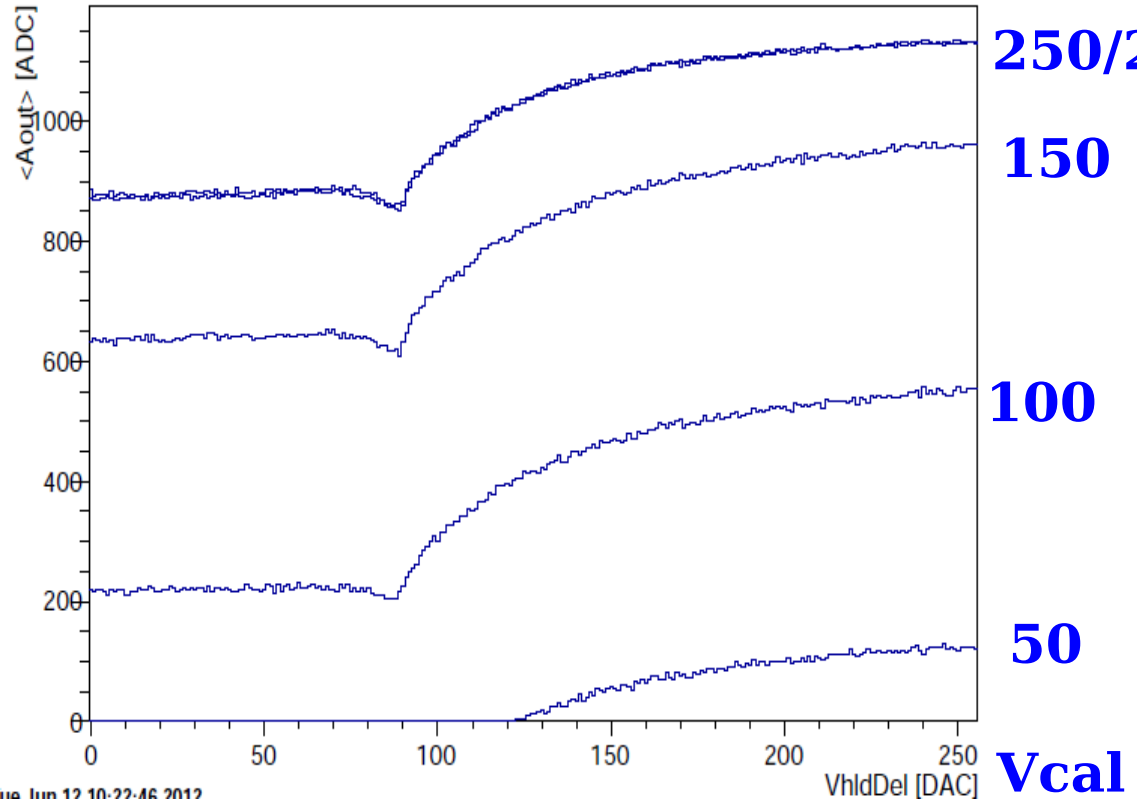




- One pixel.
- Position of maximum depends on pulse height:
  - time walk.
- DAC 150 is compromise

Sample and hold timing xdb





250/200

150

100

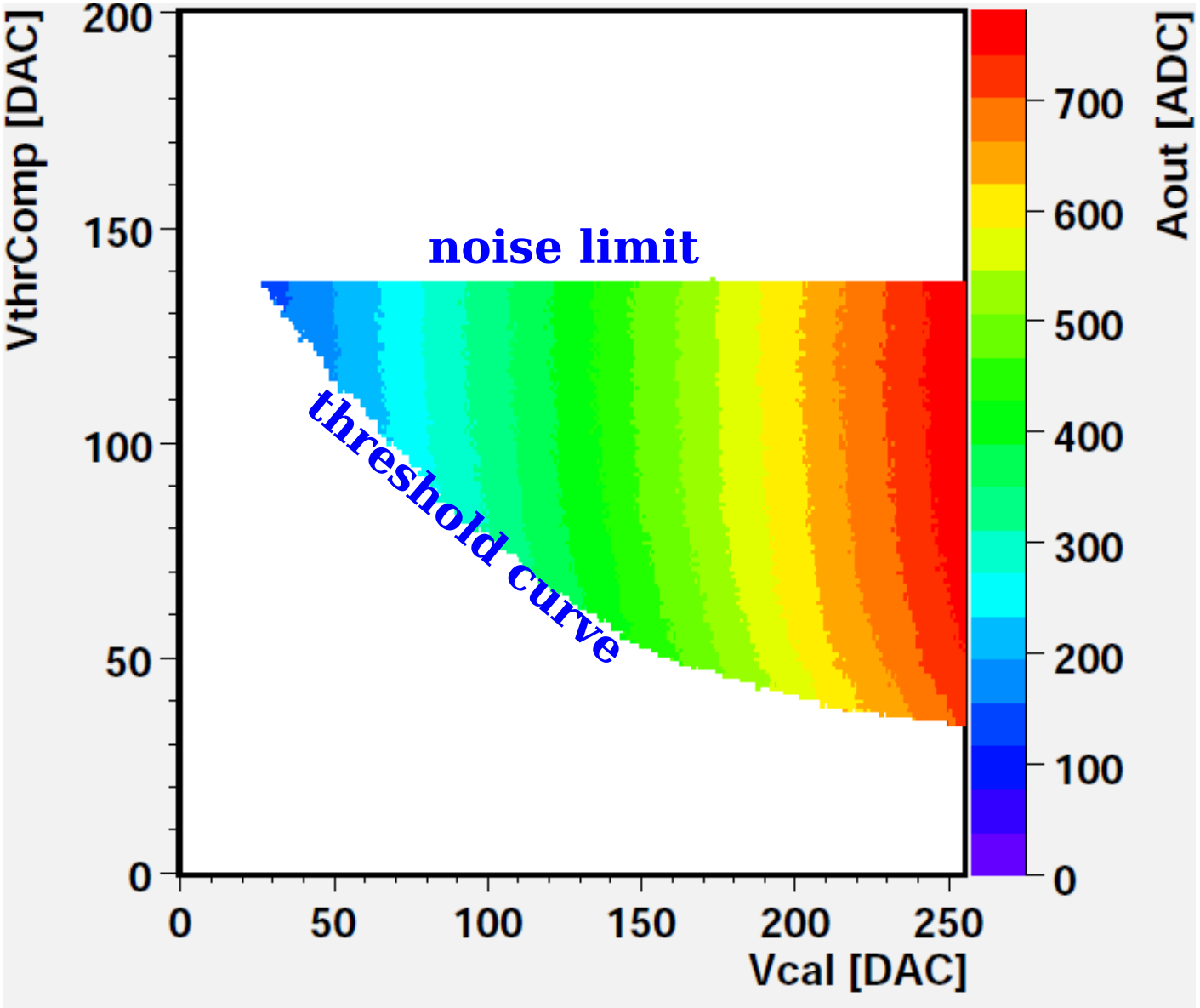
50

Vcal

- One pixel.
- Position of maximum depends on pulse height:
  - time walk.
- DAC 250 is compromise ?

Comparator threshold Chip 5

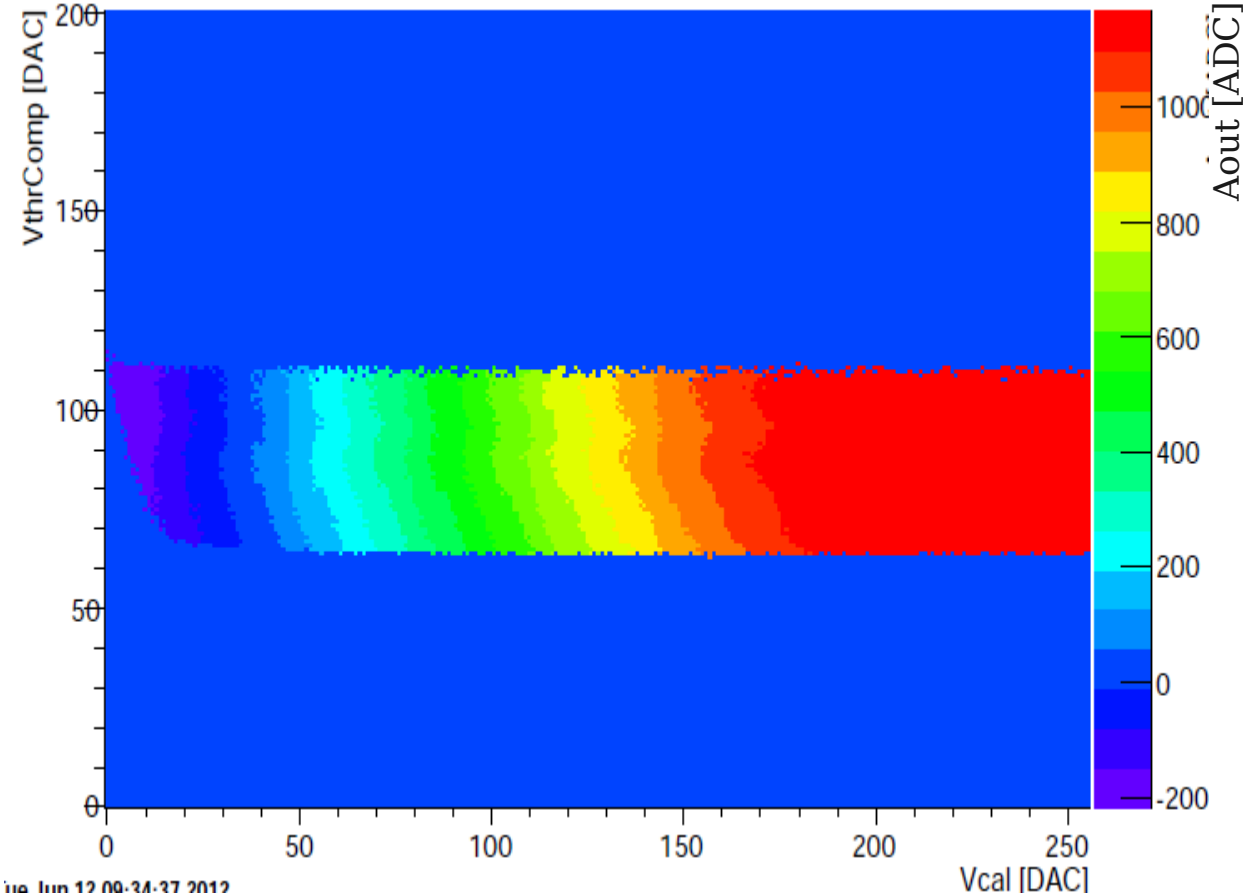
low threshold



high threshold

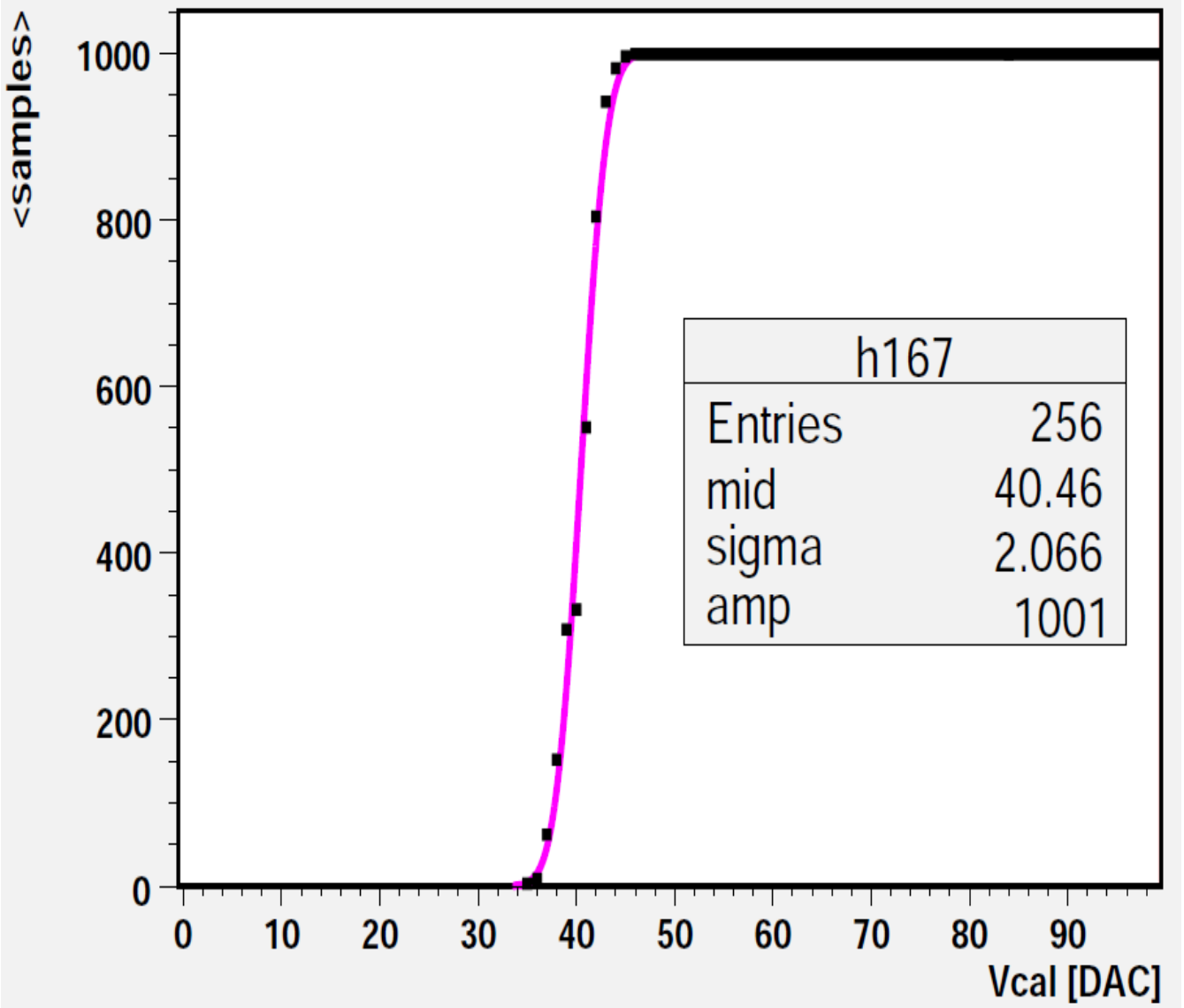
- One pixel
- Analog pulse height vs threshold and calibrate amplitude.
- White region:
  - no signal.
- Colored bands are not vertical:
  - time walk.

Comparator threshold xdb



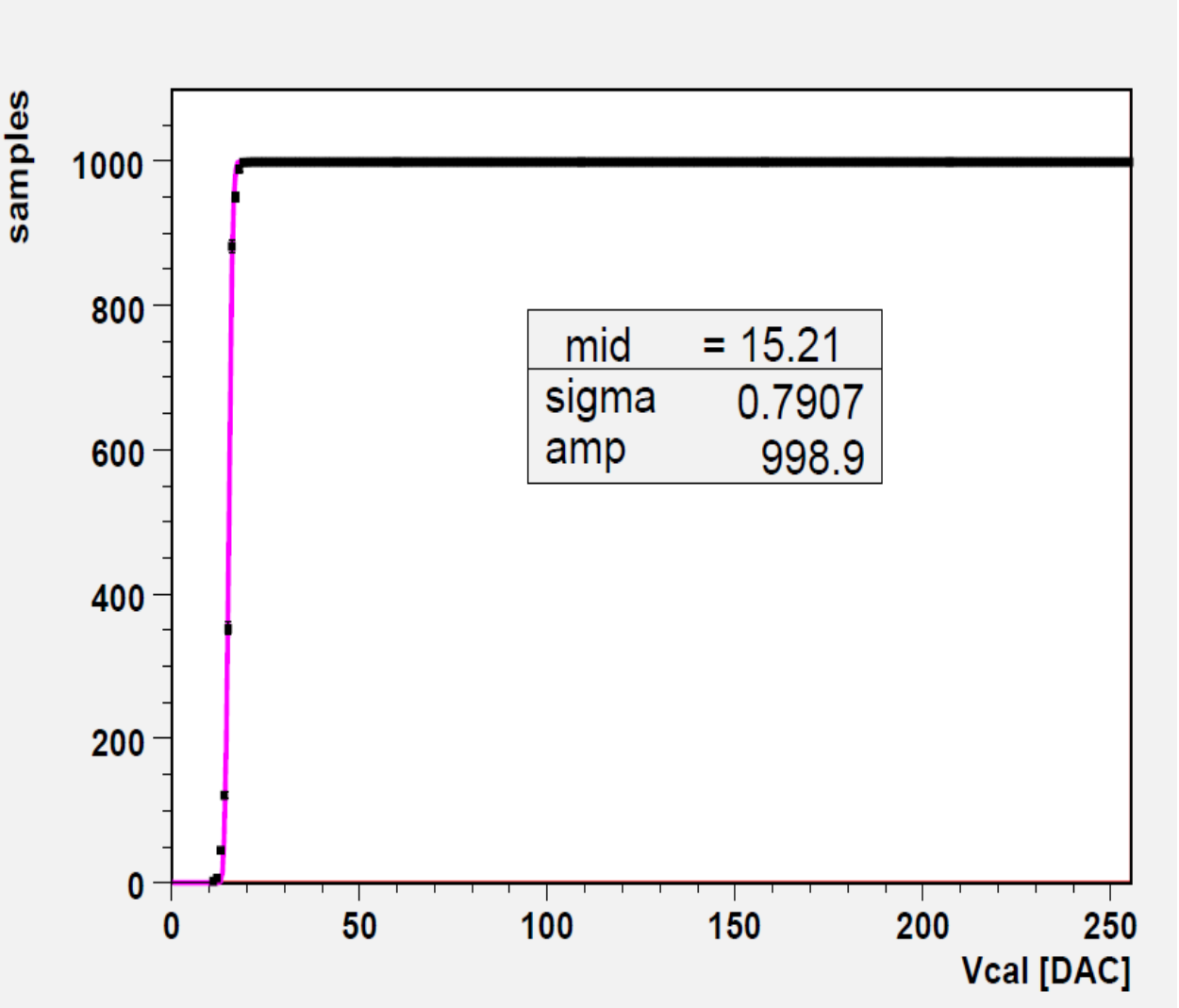
- One pixel
- Analog pulse height vs threshold and calibrate amplitude.
- Colored bands are not vertical:
  - time walk
- Narrow threshold window

Threshold curve Chip 5



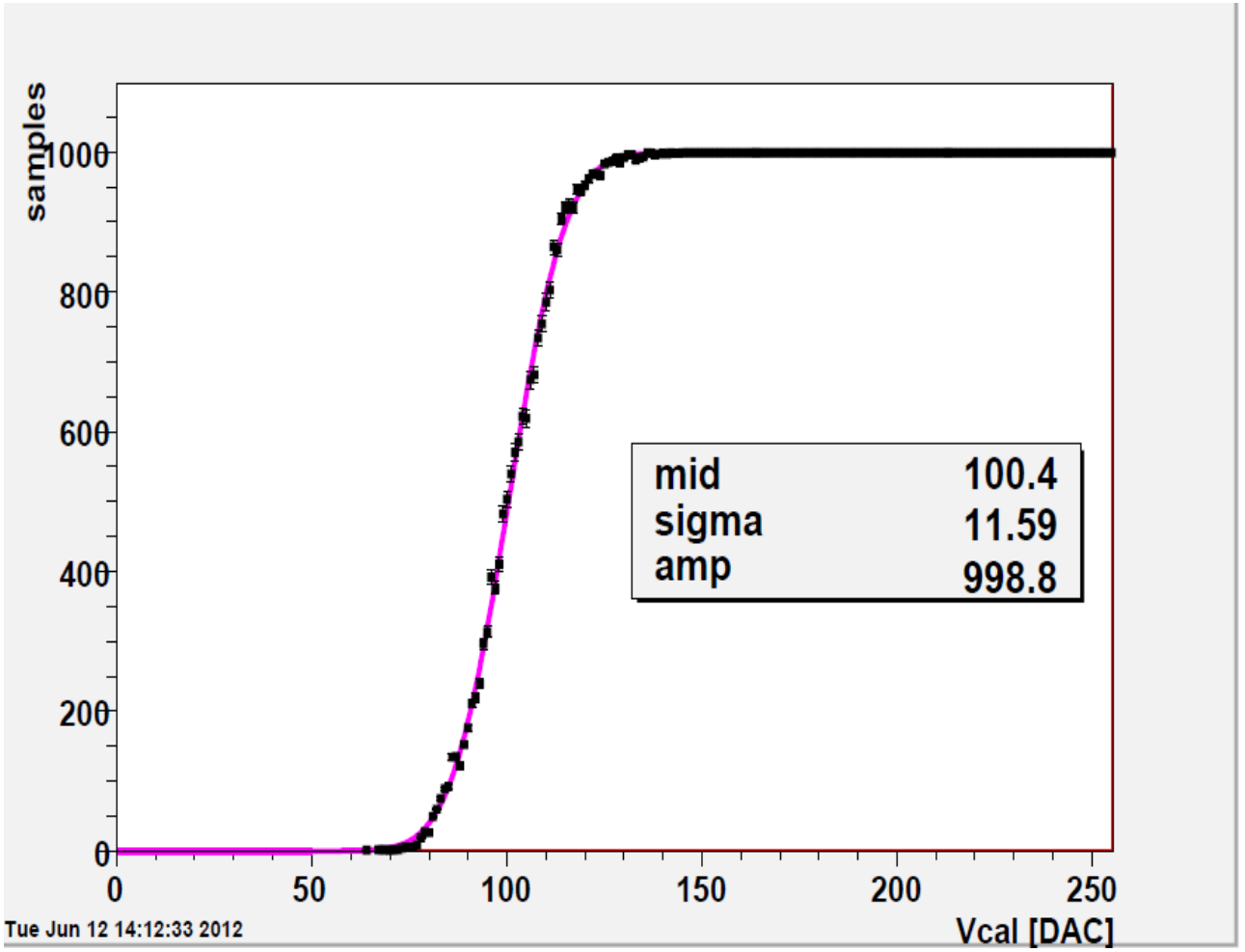
- One pixel.
- Fixed threshold
- Scan Vcal
  - 999 times
- count valid readouts
- threshold curve:
  - error function
  - width = noise
  - noise = 2.1 DAC
  - = 130 electrons.
  - (bare chip without sensor).

Threshold curve xdb



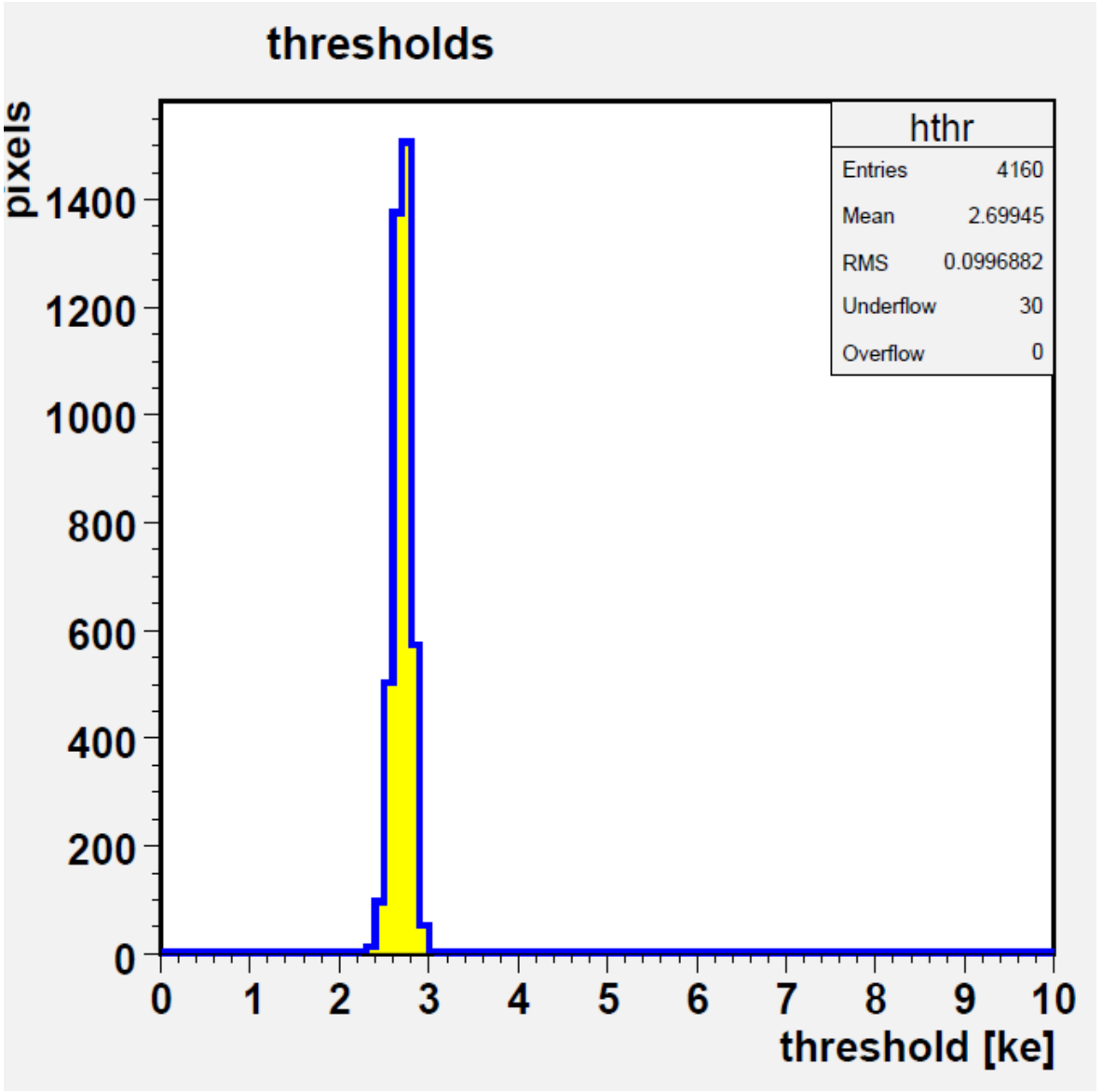
- One pixel (left half)
- Fixed threshold
- Scan Vcal
  - 999 times
- count valid readouts
- threshold curve:
  - error function
  - width = noise
  - noise = 0.8 DAC
  - Smaller Vcal ?
  - Done with CtrlReg 4

Threshold curve xdb



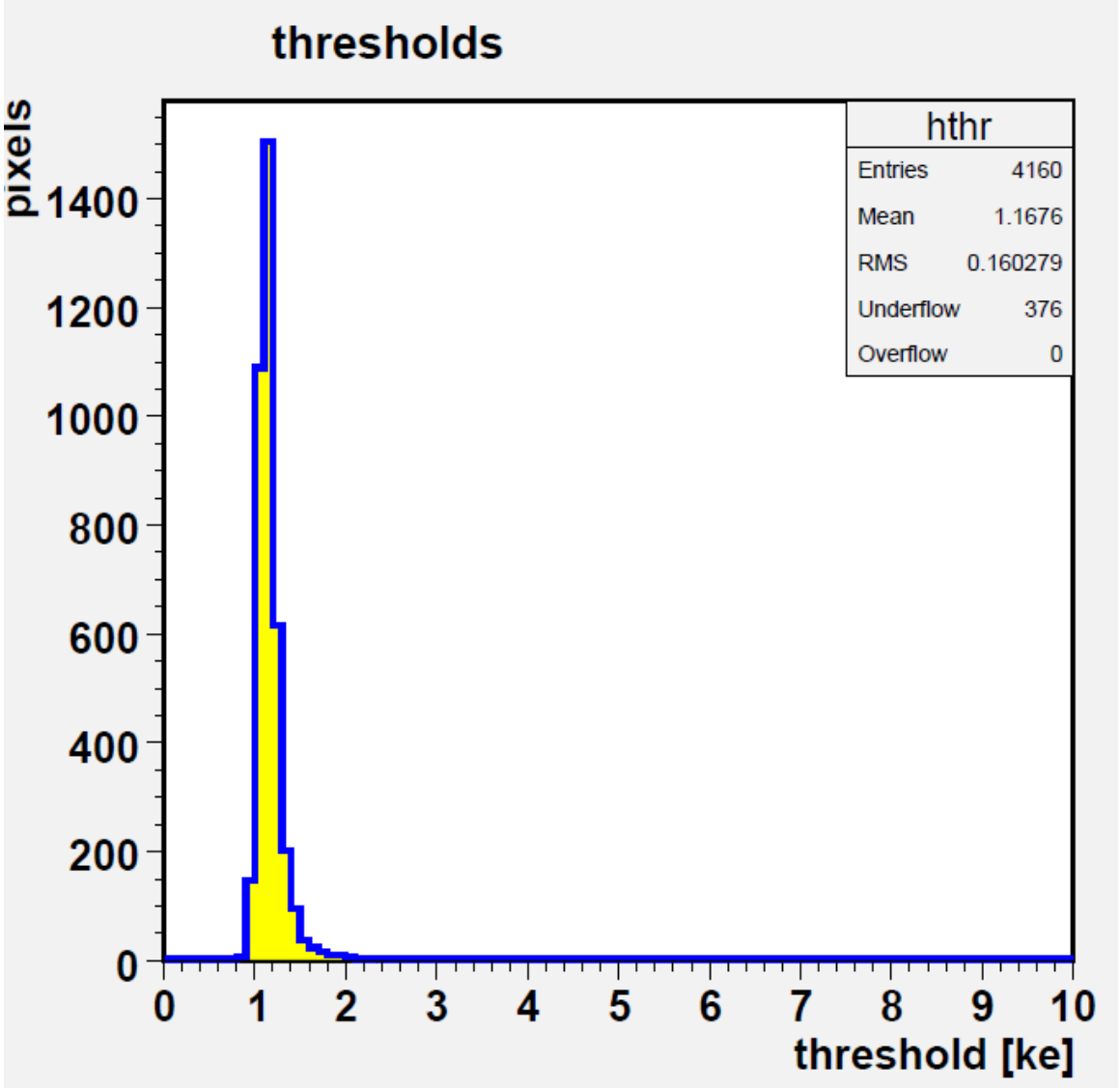
- One pixel (left half)
- Fixed threshold
- Scan Vcal
  - 999 times
- count valid readouts
- threshold curve:
  - error function
  - width = noise
  - noise = 11 DAC
  - Higher Vcal ?
  - Done with CtrlReg 0

Threshold variation trimmed Chip 10



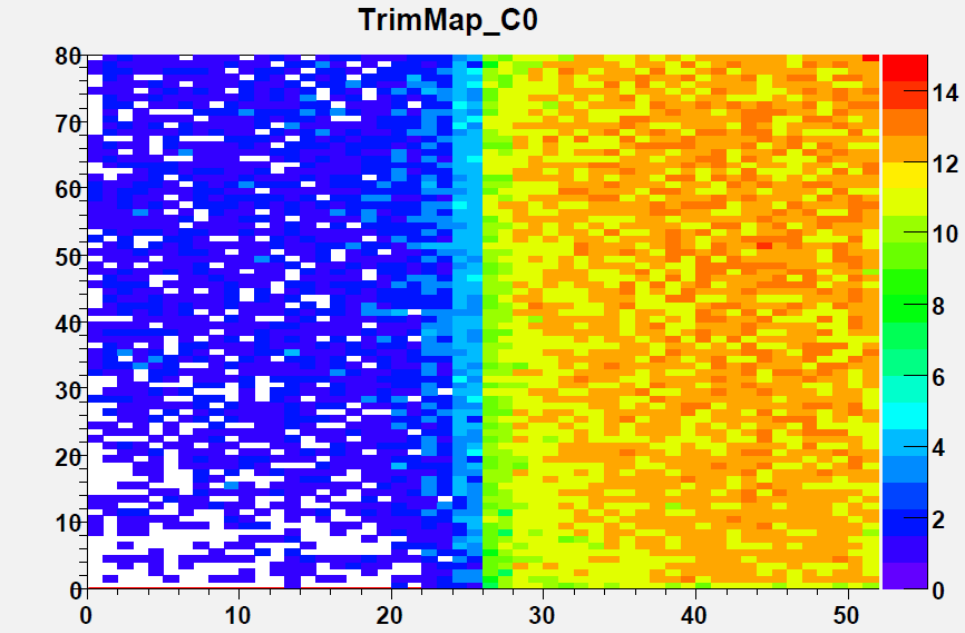
- Chip10 (sensor)
- Target Vcal=40
- VthrComp 101
- Vtrim 122
- 4160 TrimBits set
- Mean at 2.7 ke
- 99 e threshold variation

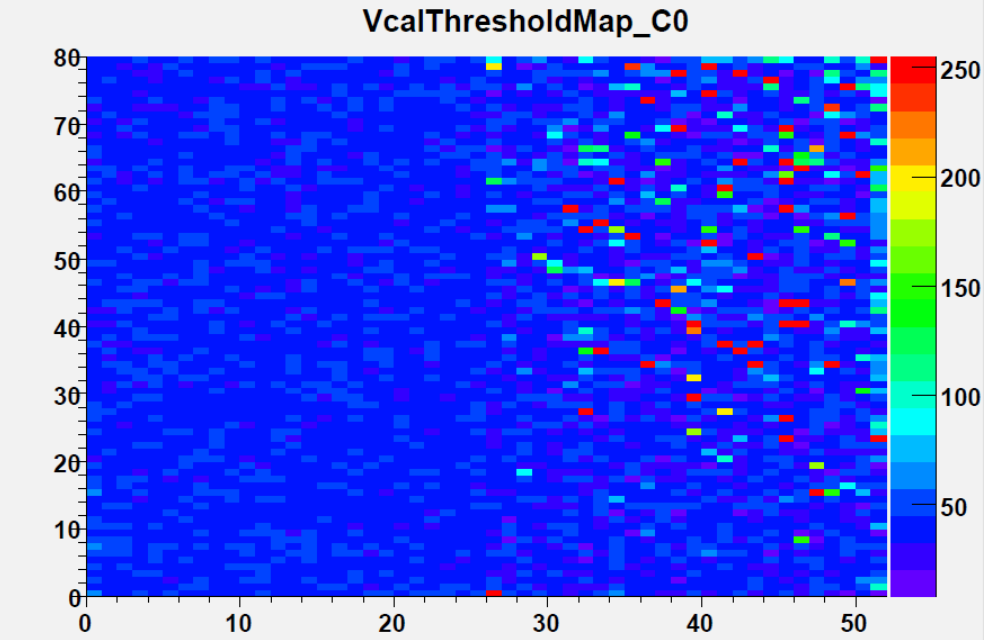
Threshold variation trimmed xdb



- Chipx (sensor)
- Target Vcal=40
- VthrComp 72
- Vtrim 160
- 4160 TrimBits set
- Mean at 1.2 ke
- 160 e threshold variation
  - Old conversion factor is used

Maps after trimming xdb





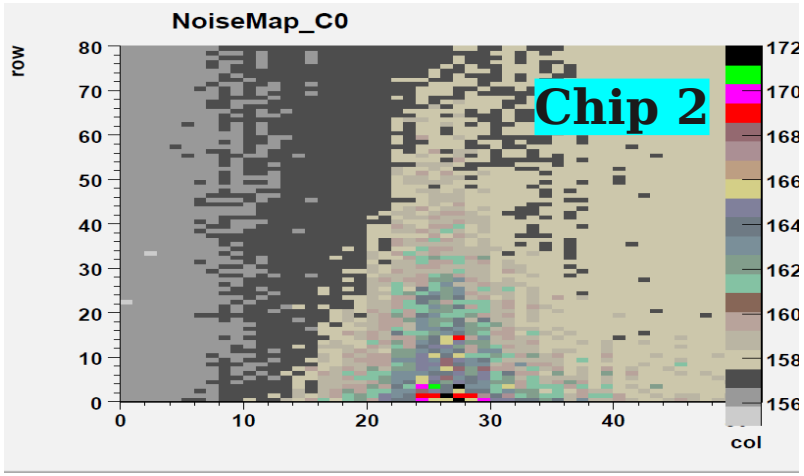
Trim bits map

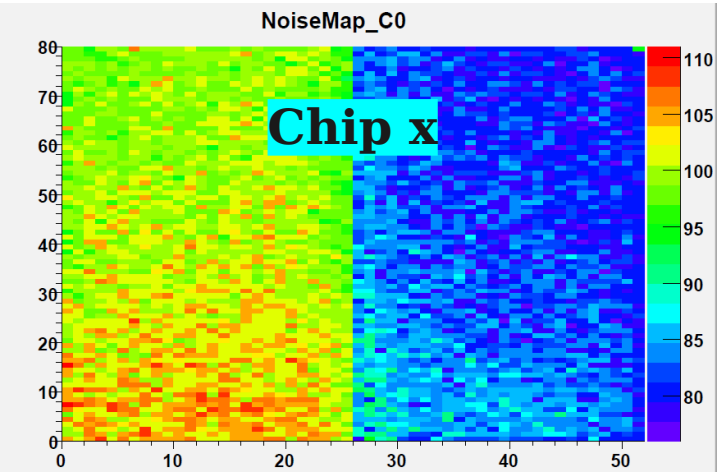
Vcal thresholds map

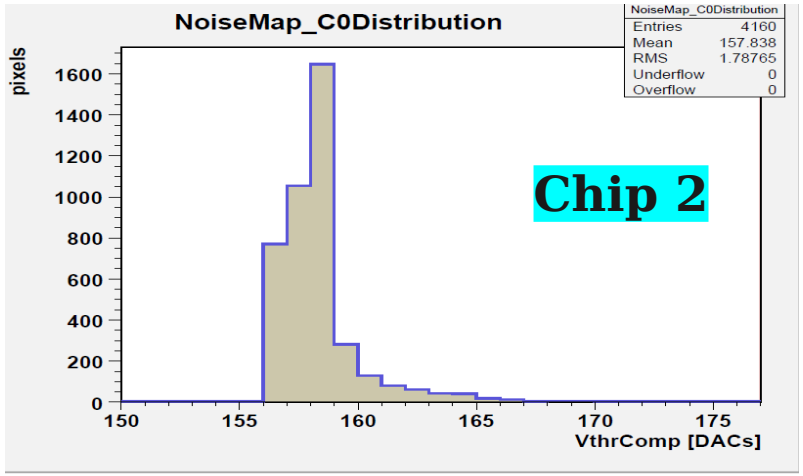
Big difference in trim bits and thresholds for 2 halves. Some thresholds are set to maximum – underflow bins ?

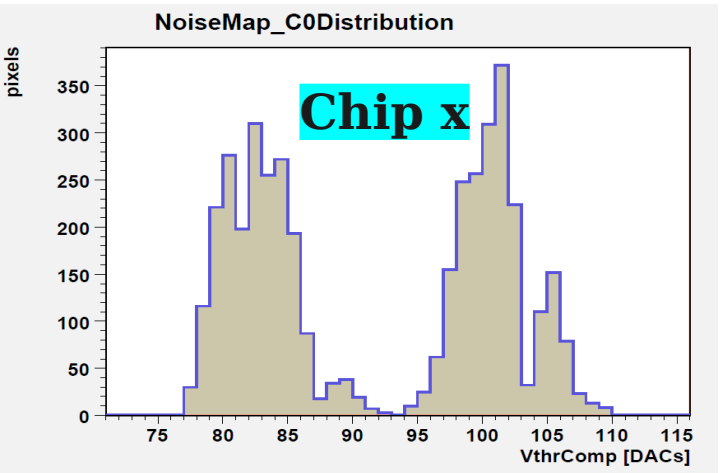
Noise map (GUI Thr)

- **Set Vcal = 200. Read Trim parameters**
- **Pulse pixels and scan VthrComp DAC close to noise (High VthrComp = low threshold ⇒ noise area)**
- **Plot thresholds**



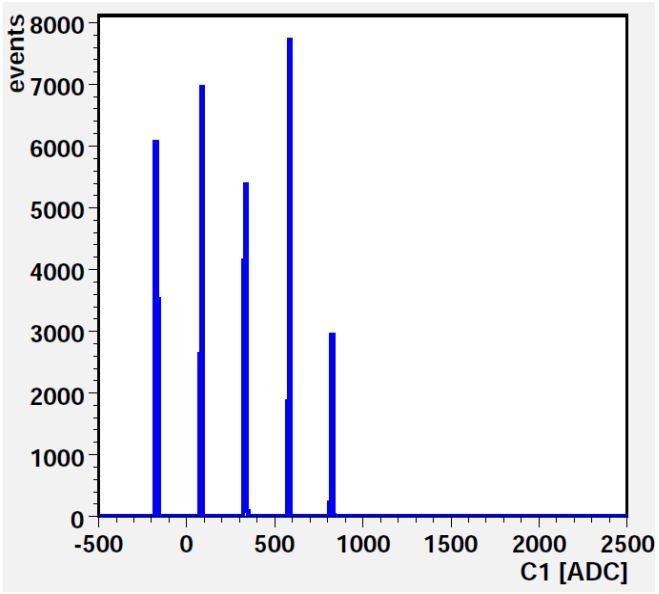


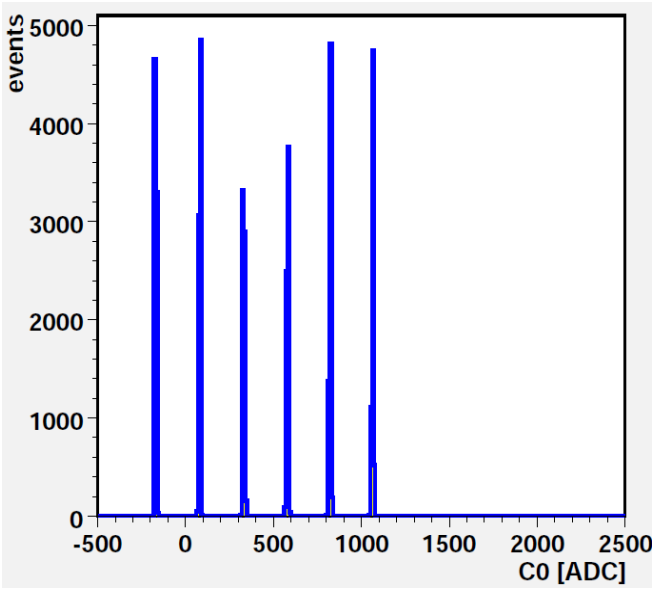




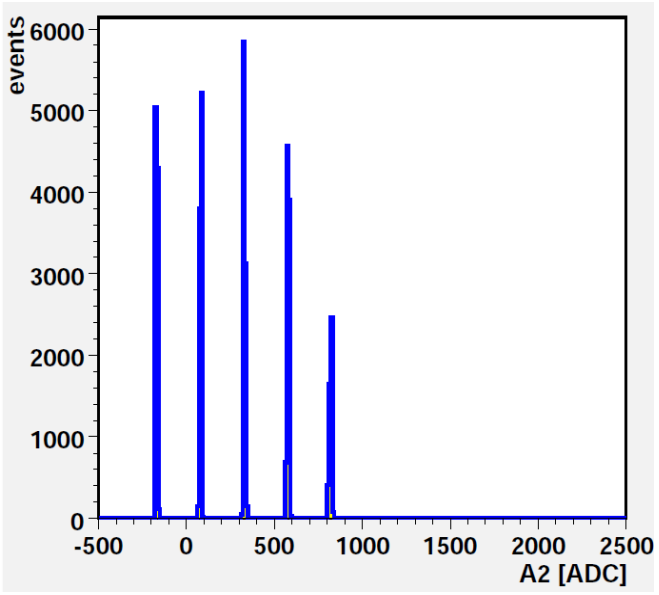
Smaller VthrComp, 2 peaks for Chip x ?

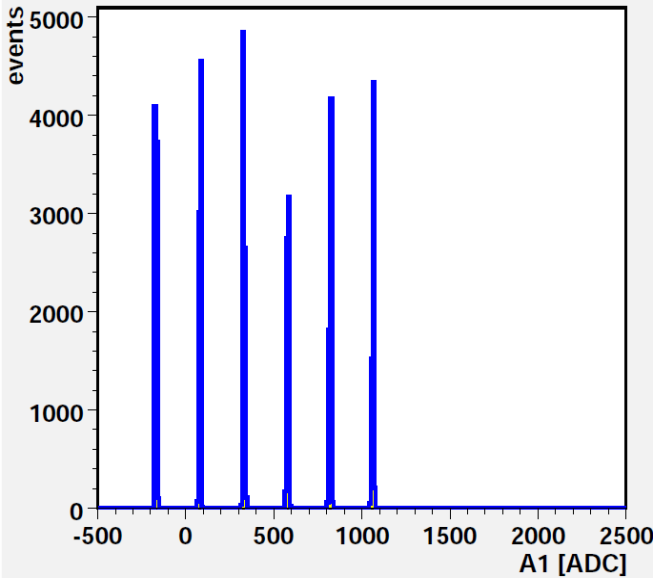
Pixel address Chip 5

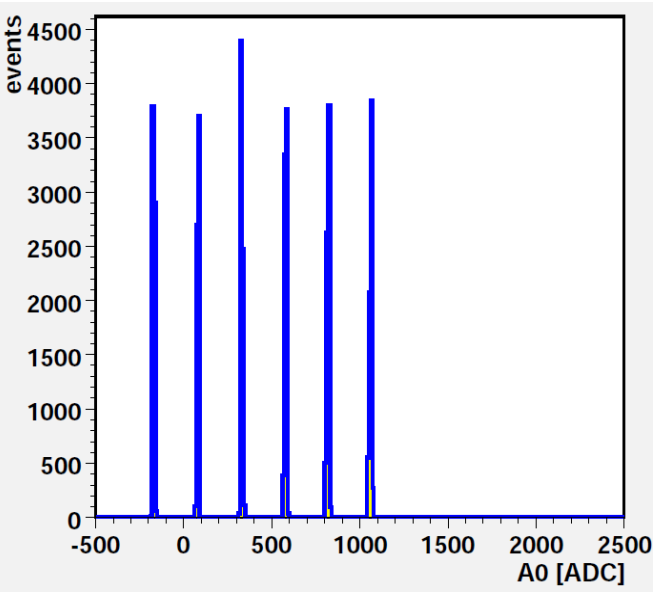




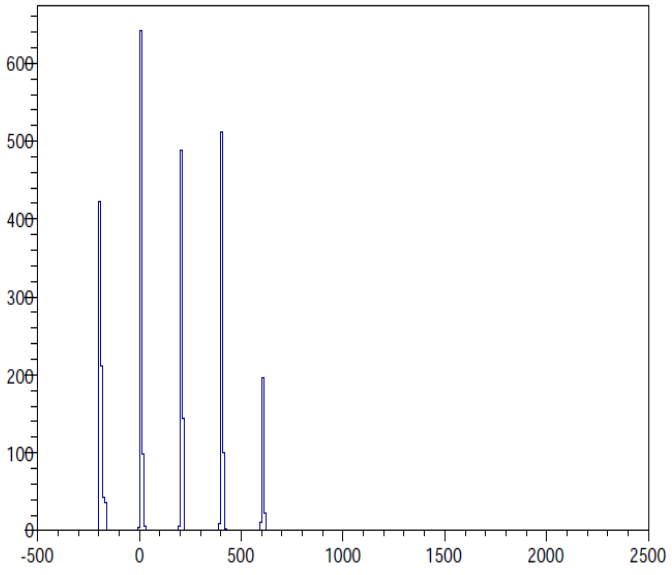
Pixel address in 5 data:
C1,C0 d-columns 0..25
A2, A1, A0 rows
each with 6 analog levels.
All well separated.
Decode → col, row.

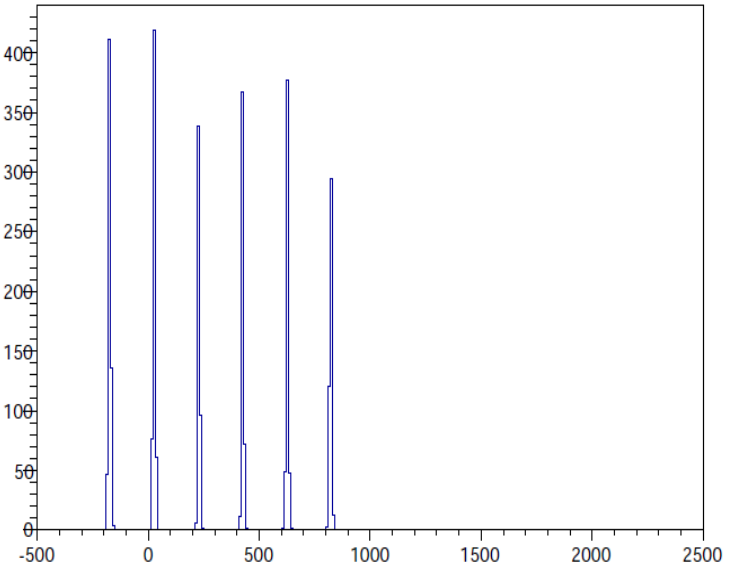




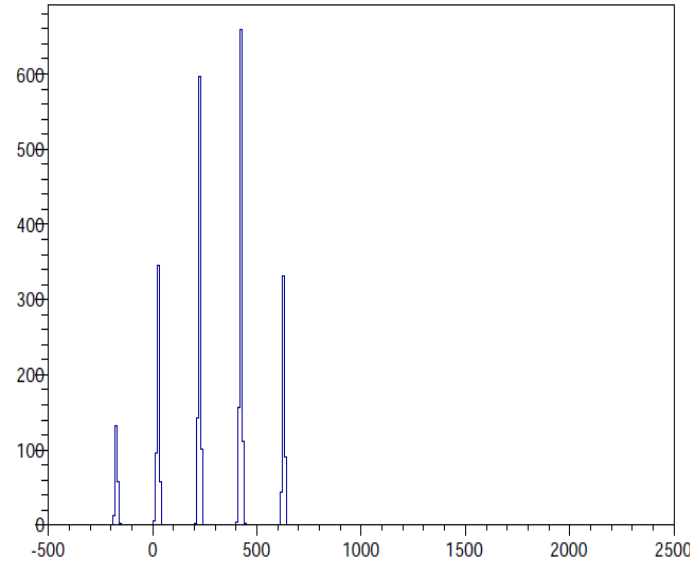


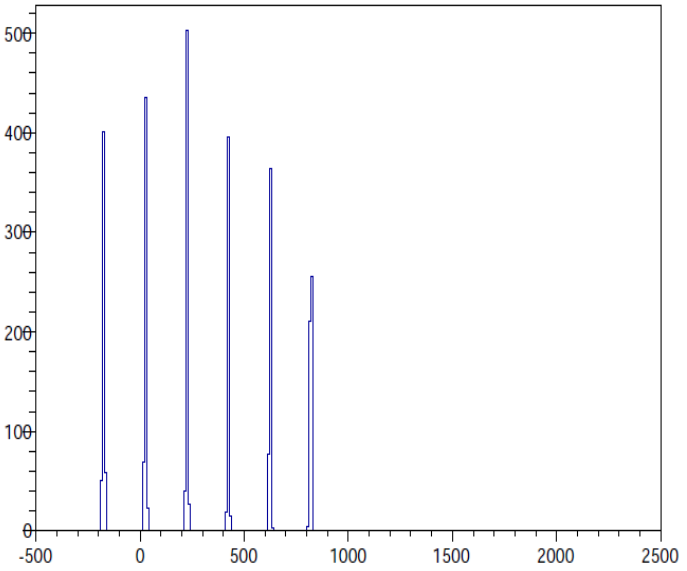
Pixel address xdb

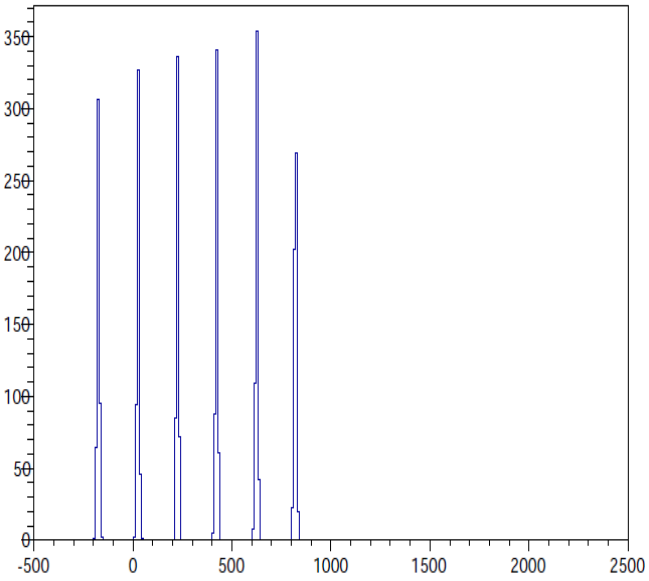




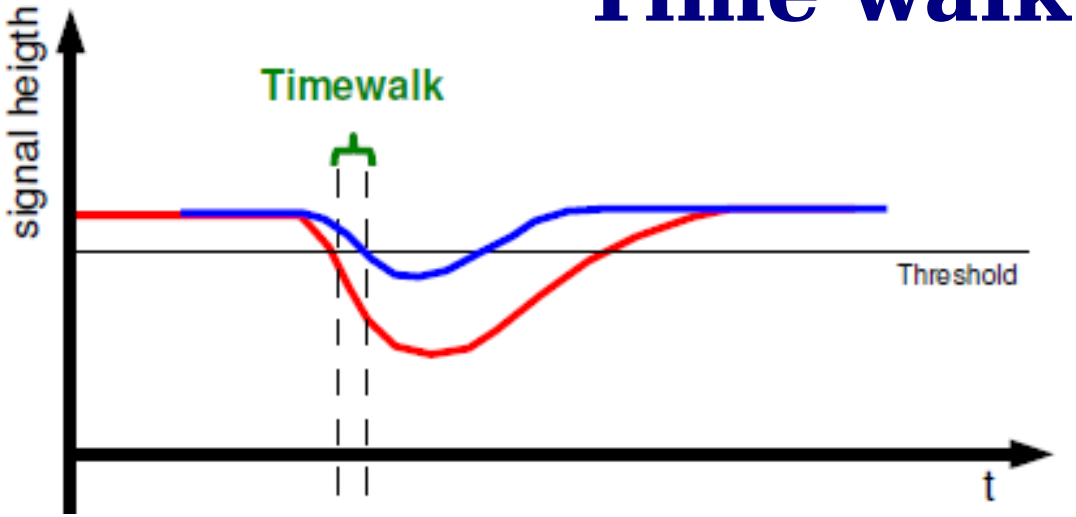
Pixel address in 5 data:
C1,C0 d-columns 0..25
A2, A1, A0 rows
each with 6 analog levels.
All well separated.
Decode → col, row.

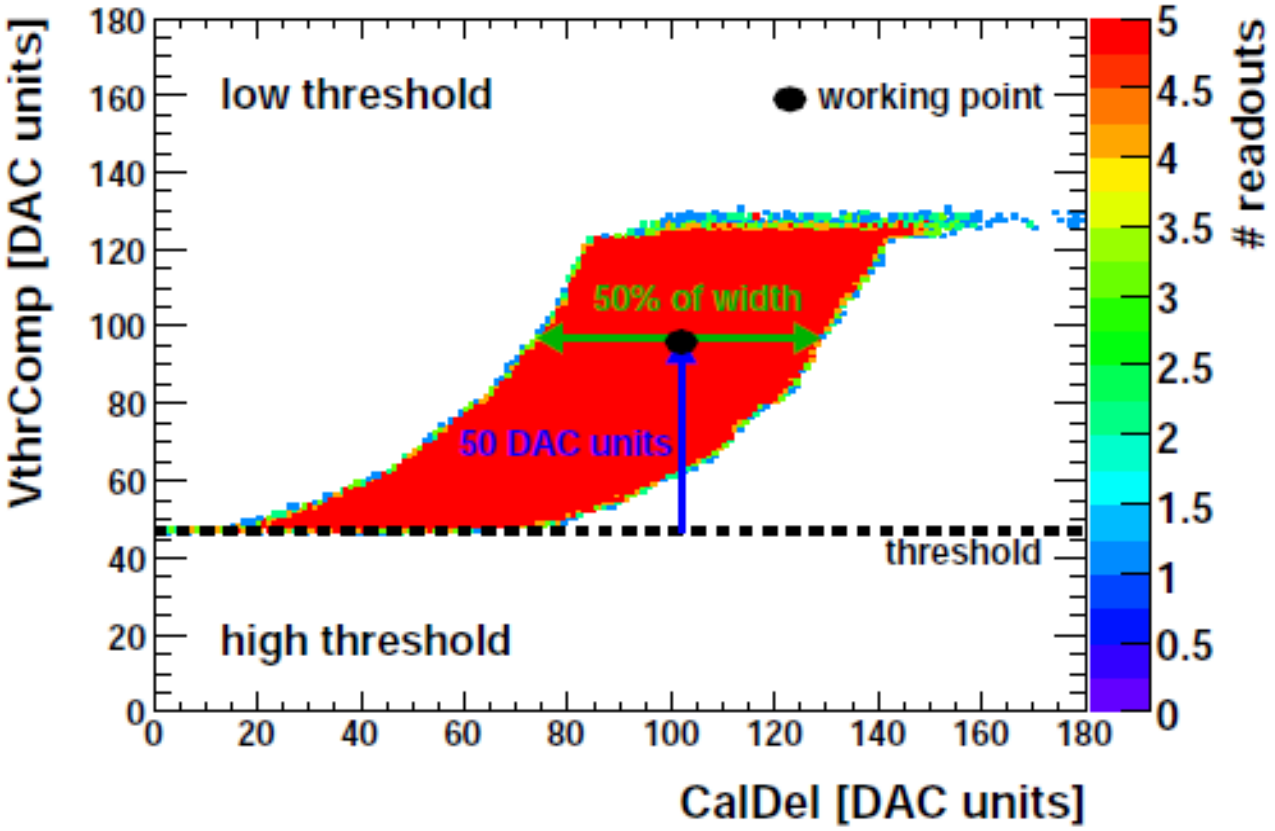






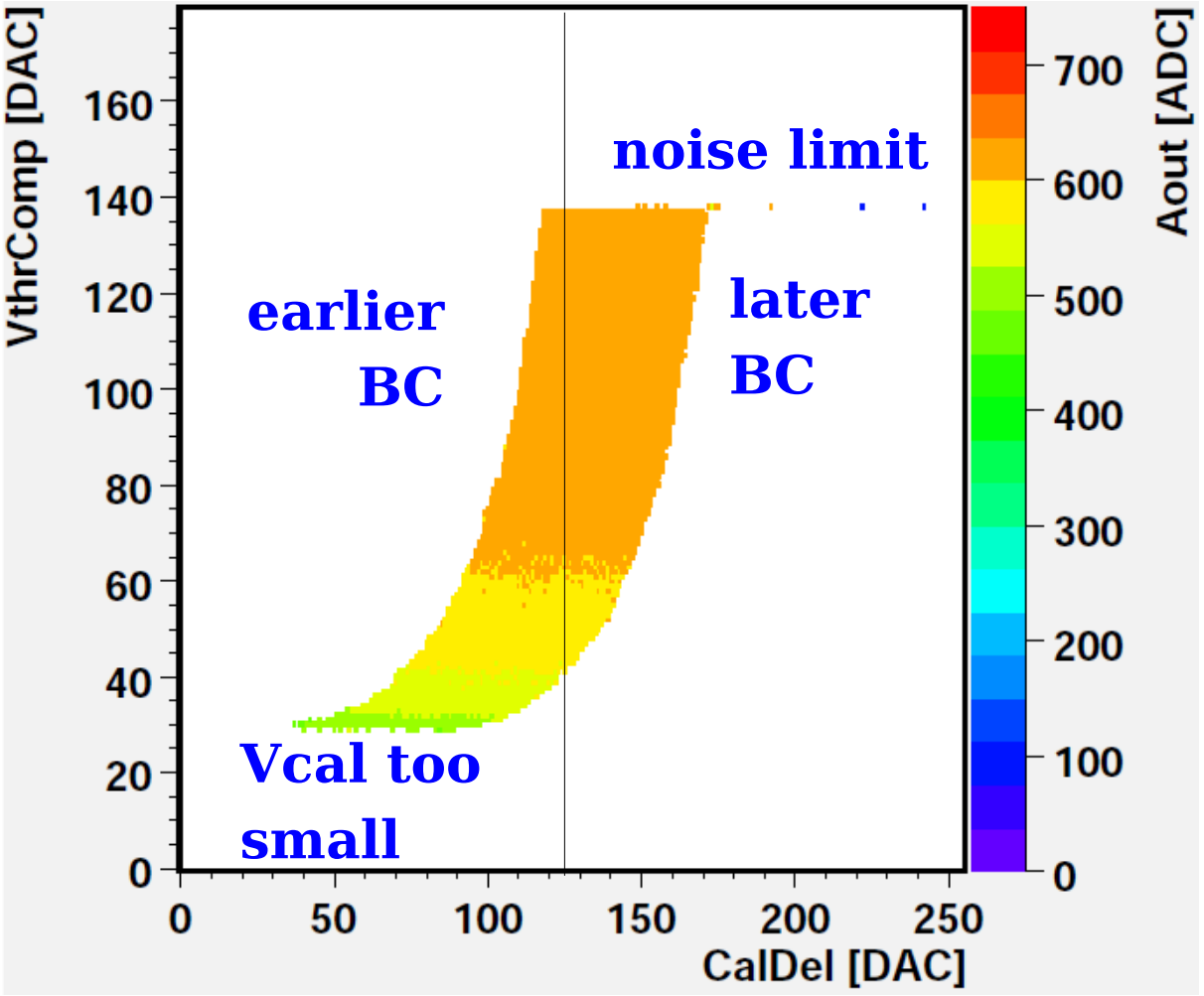
Time walk at PSI





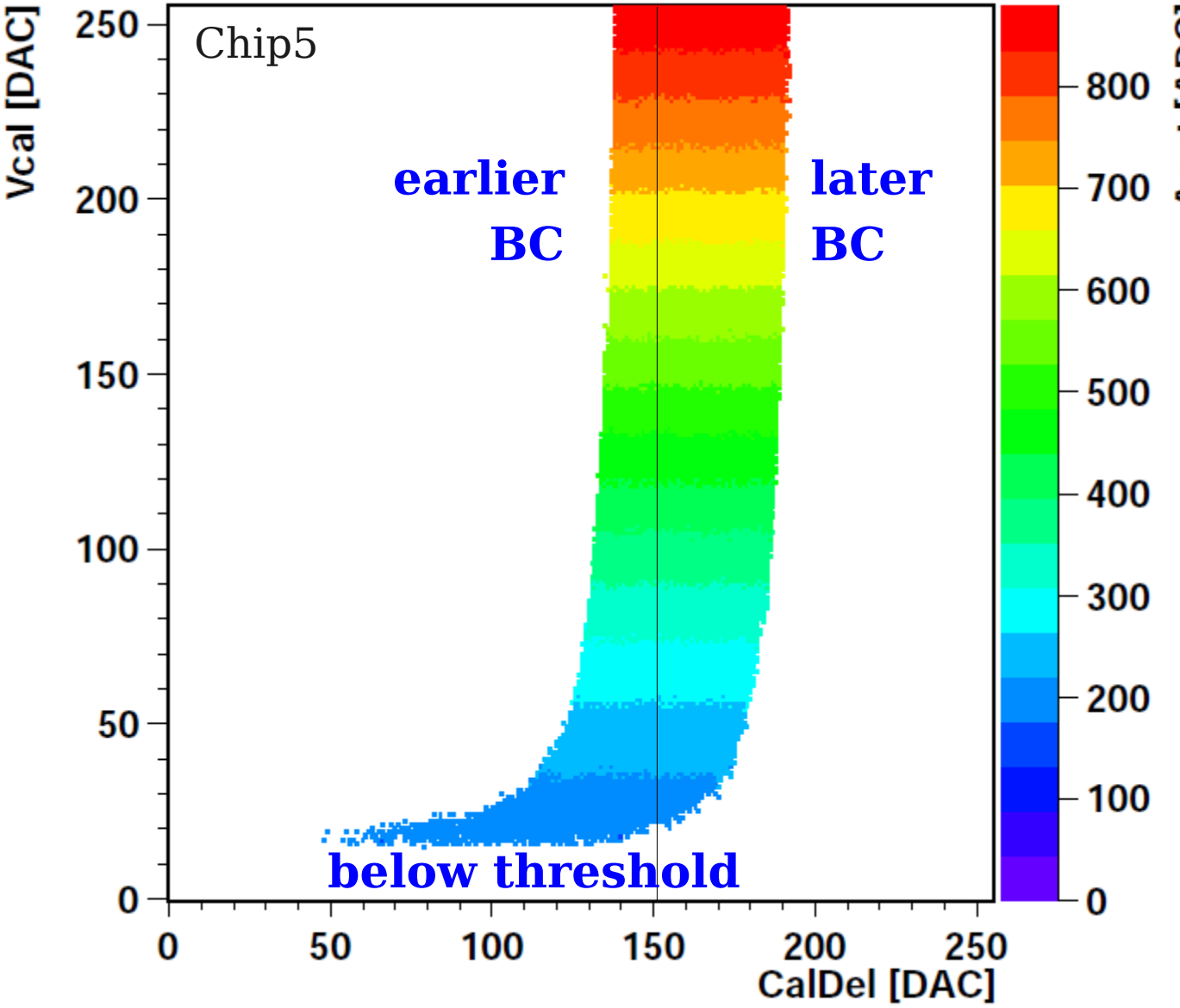
S. Dambach, ETH phd 2009

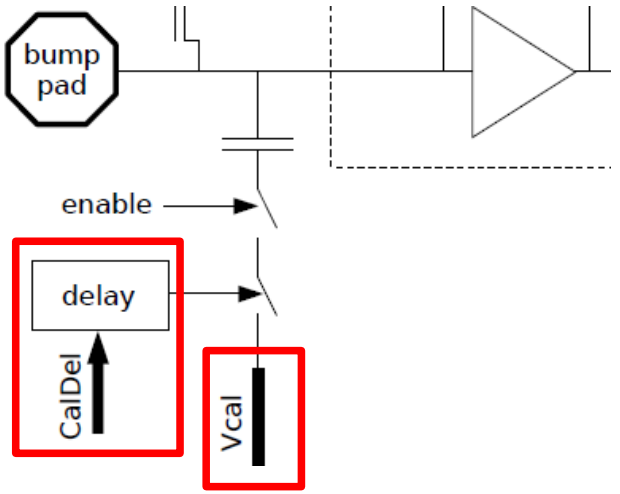
Time walk Chip5



- One pixel.
- Vcal 200 small DAC.
- Moving the threshold shifts the timing:
  - time walk.

Calibrate timing Chip5

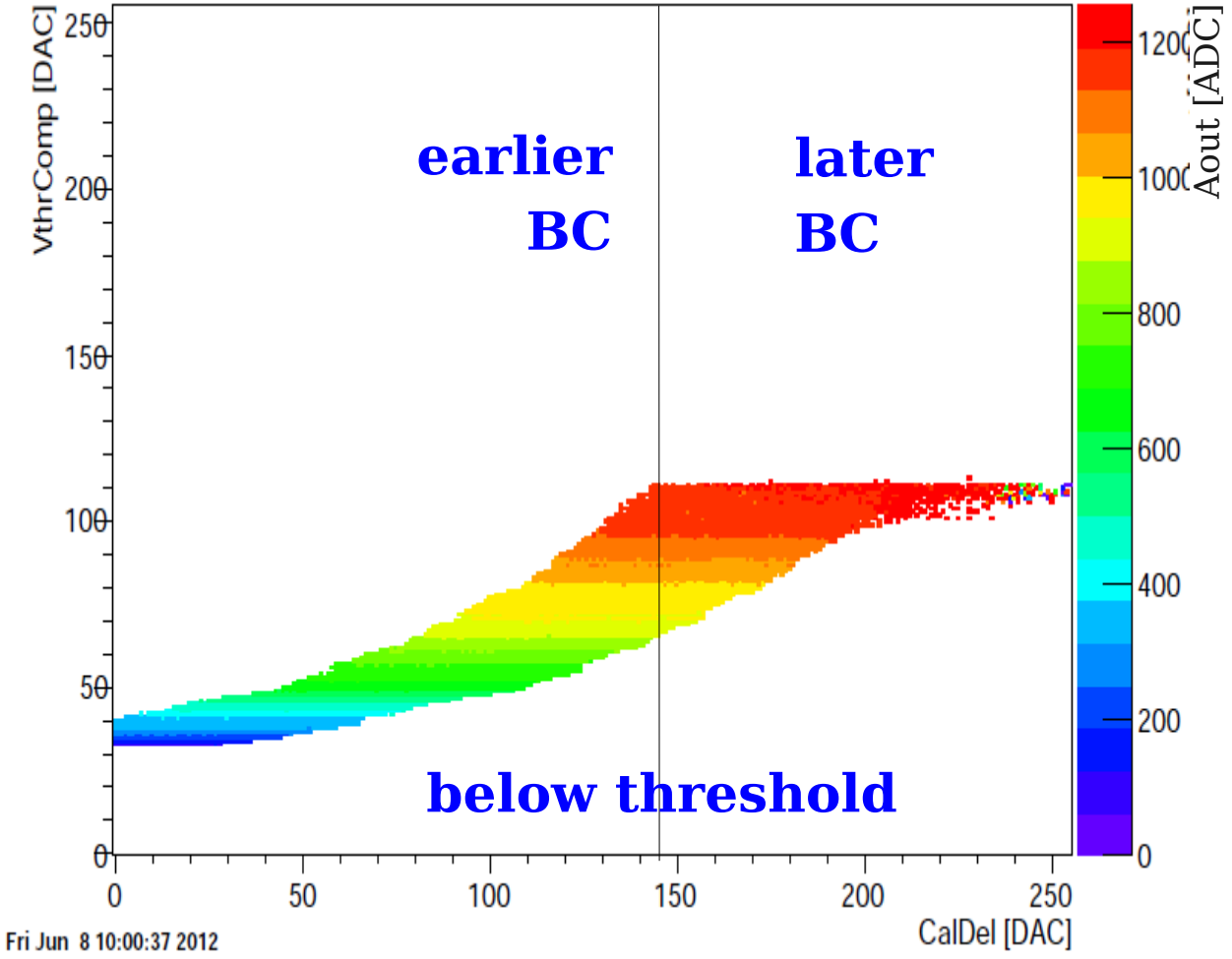




- One pixel.
- Threshold set close to noise limit.
- Window is 1 BC wide.
- We choose 150.
- Small pulses:
  - time walk.

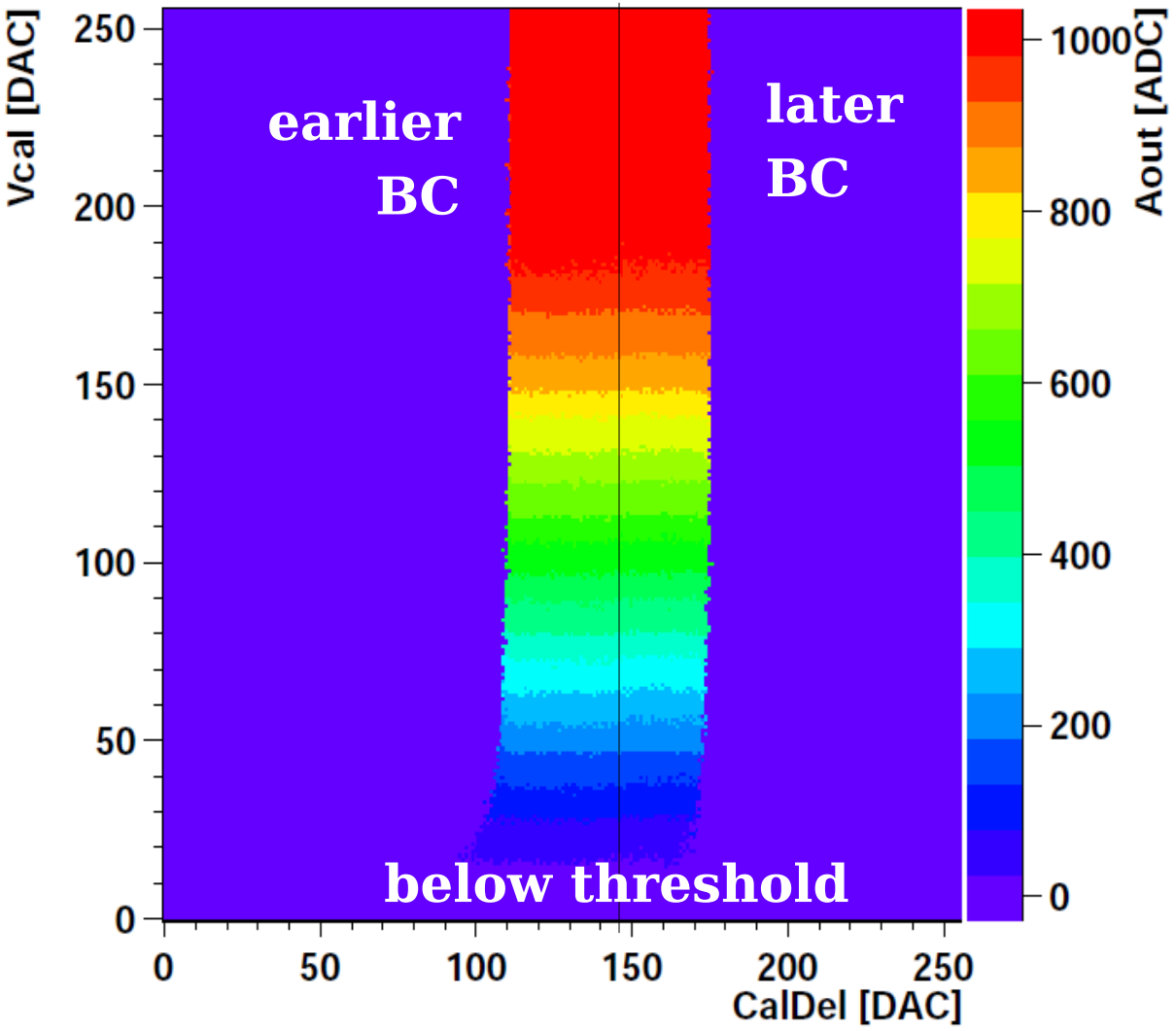
Time walk xdb

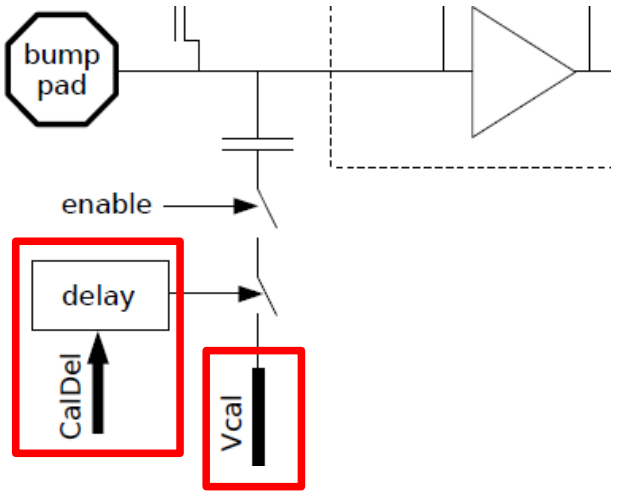
Chipx



- One pixel.
- Threshold set close to noise limit.
- Window is 1 BC wide.
- We choose 146.
- Small pulses:
  - time walk.

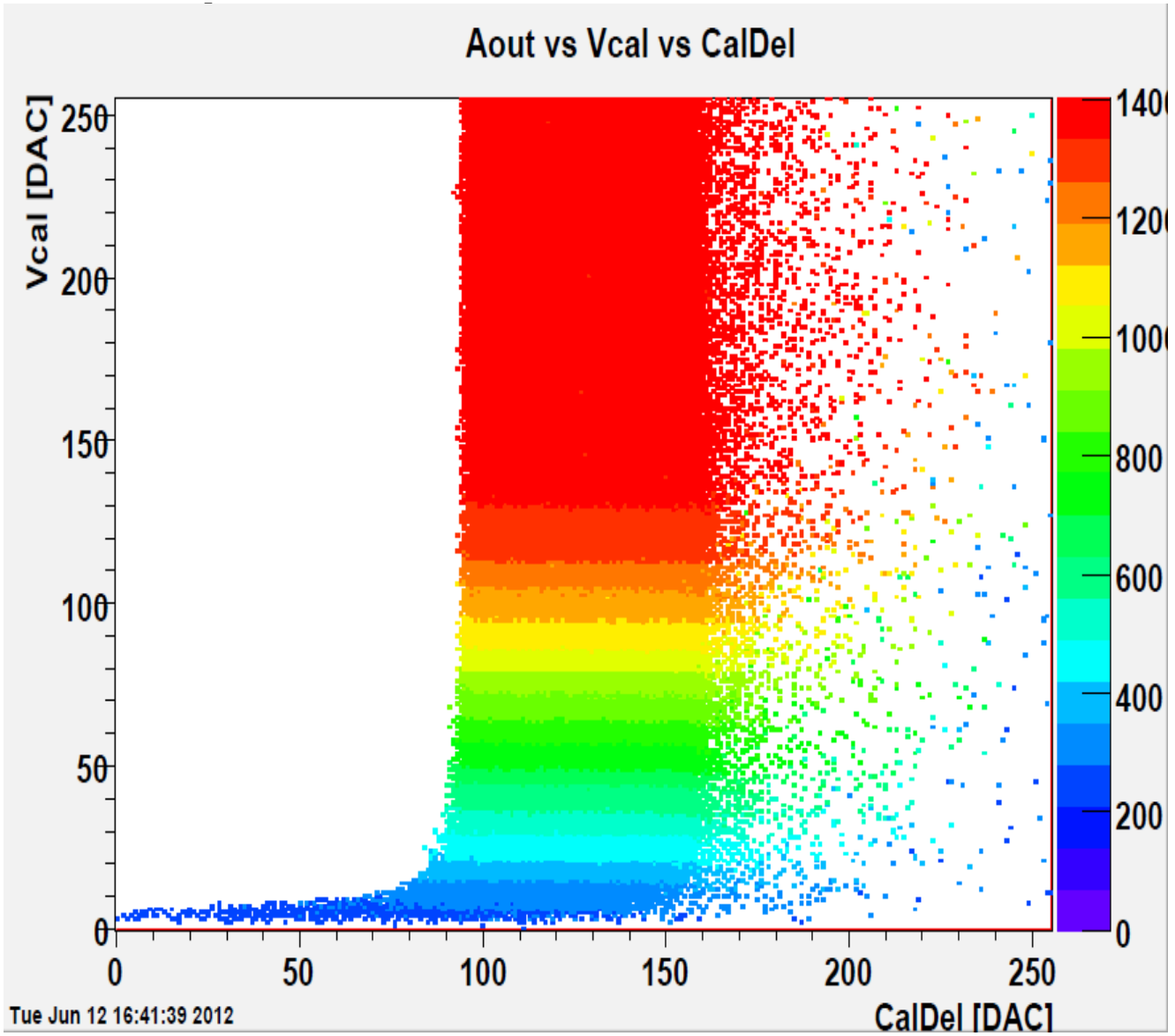
Calibrate timing xdb

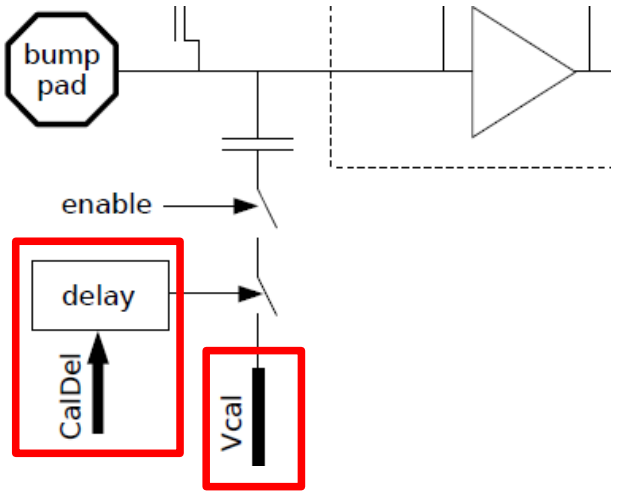




- One pixel.
- Threshold set close to noise limit.
- Window is 1 BC wide.
- We choose 146.
- Small pulses:
  - almost NO time walk ?
- Pixel from left half

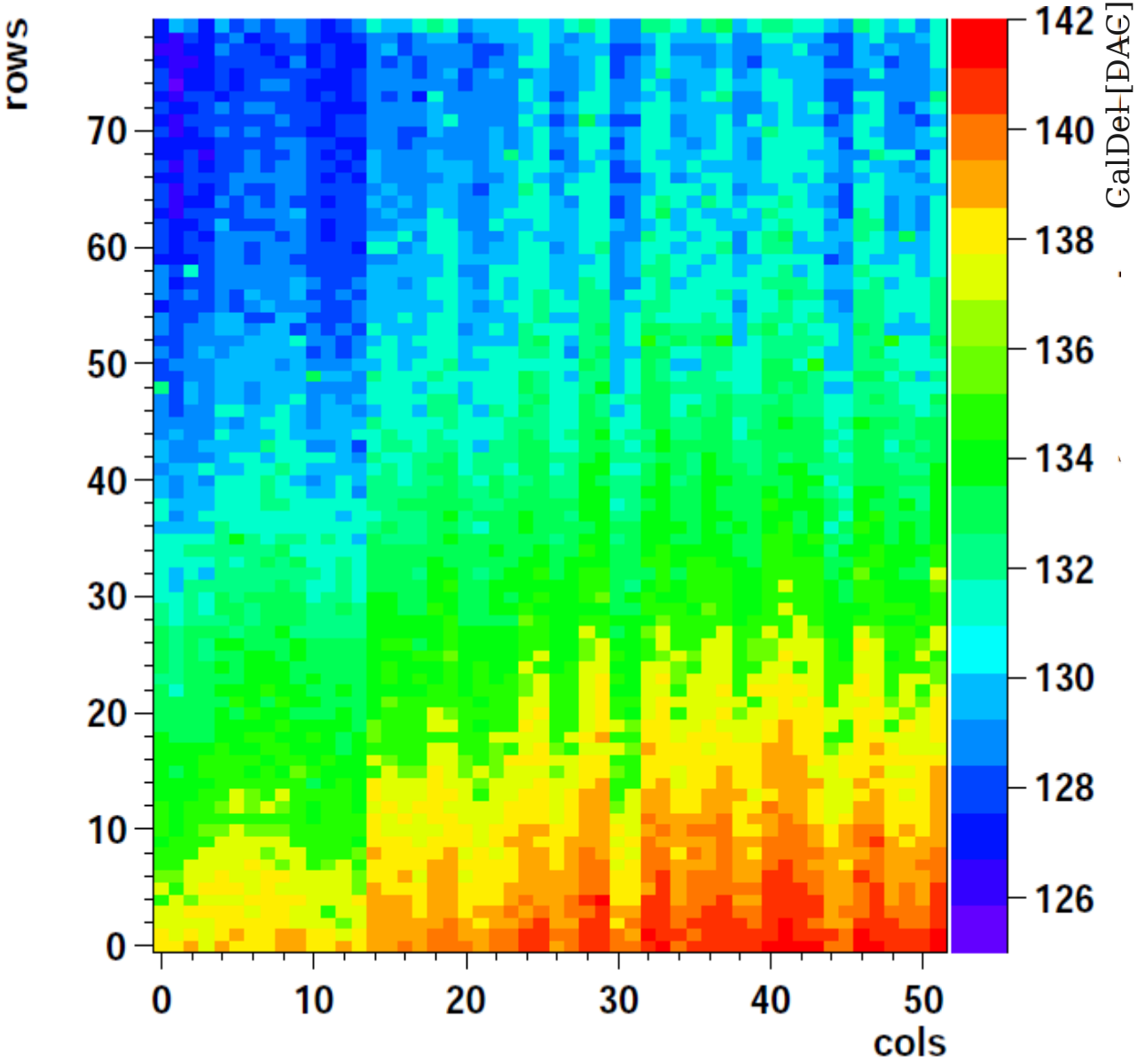
Calibrate timing xdb

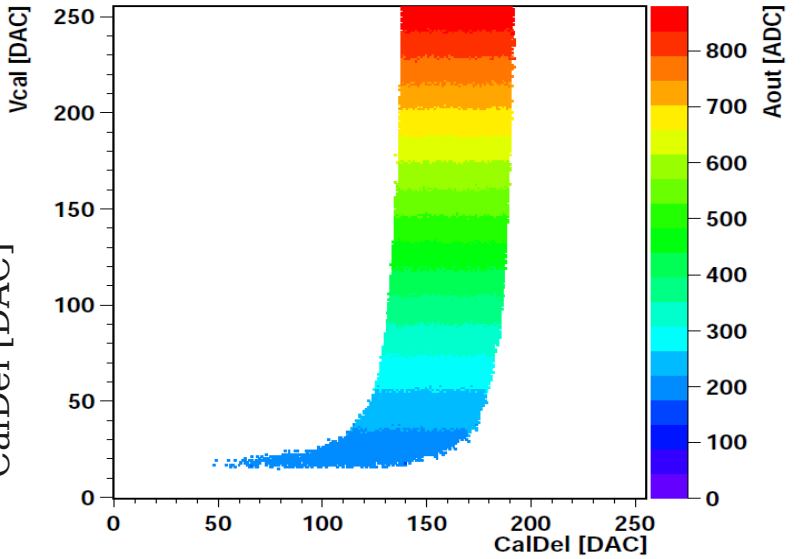




- Pixel from right half of the chip xdb

Timing map Chip 5

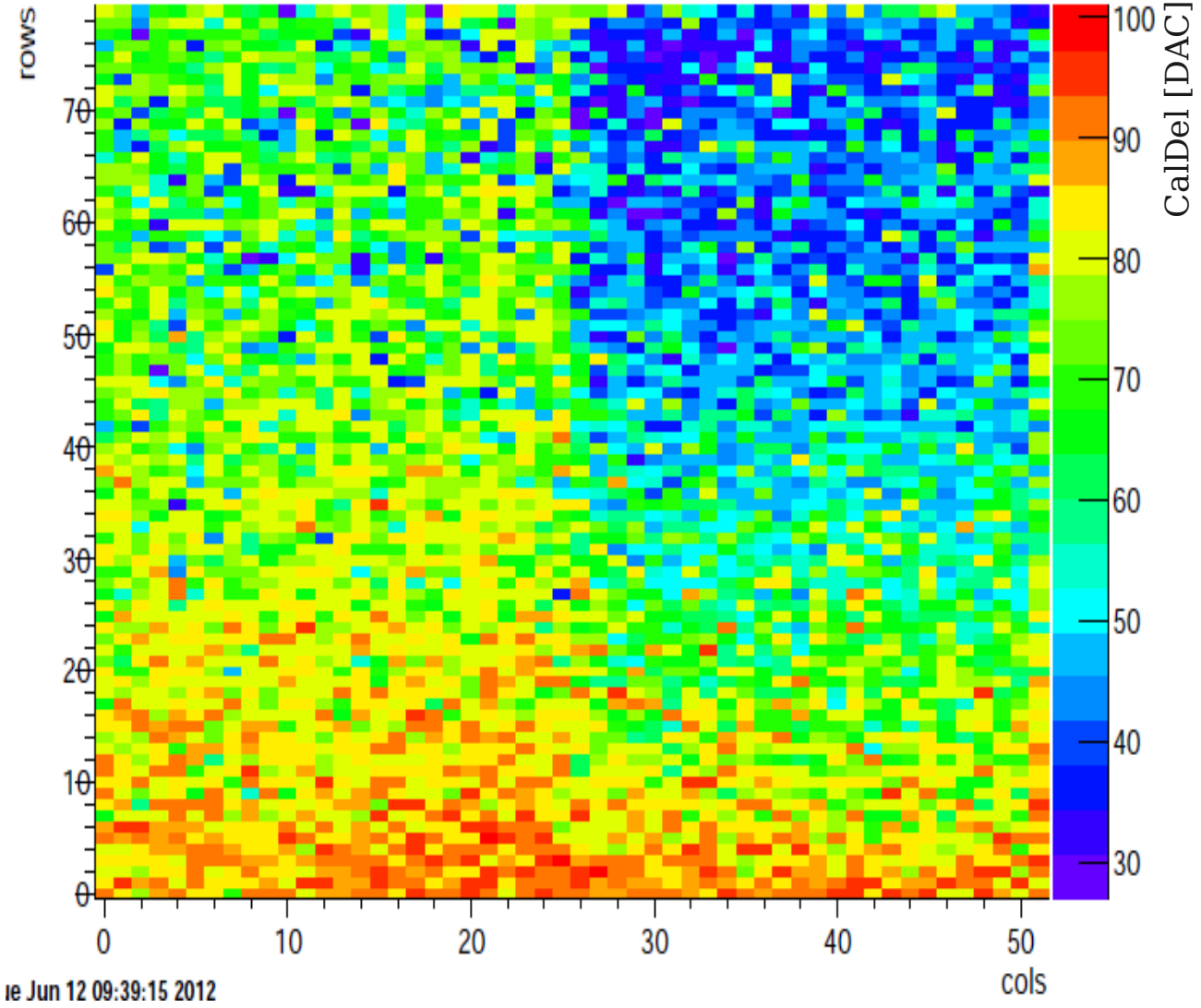




- All pixels.
- Left edge of time window for Vcal=255.
- trend along rows
- sharp variation from column to column

Timing map for xdb

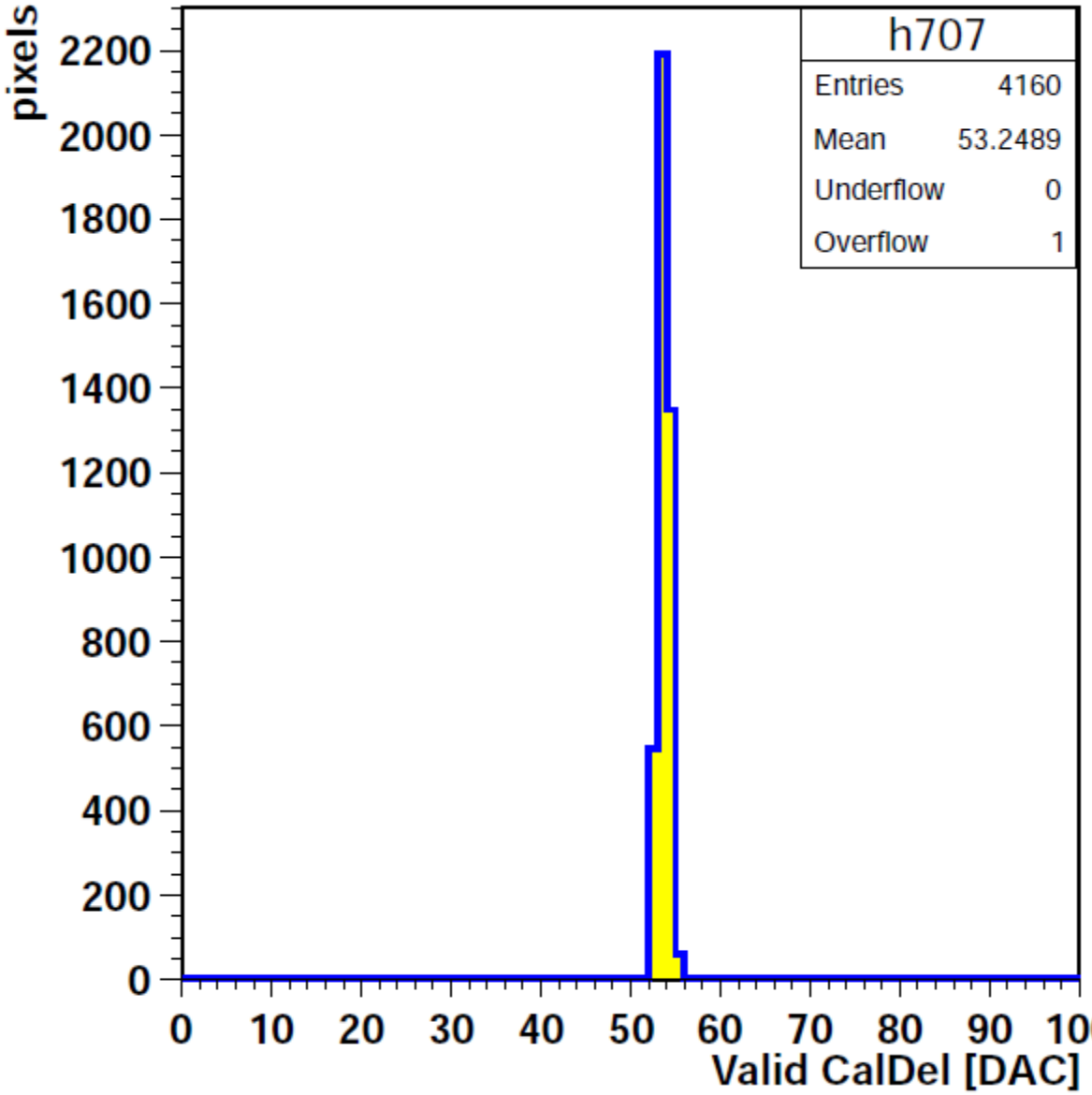
1st CalDel for Vcal=255

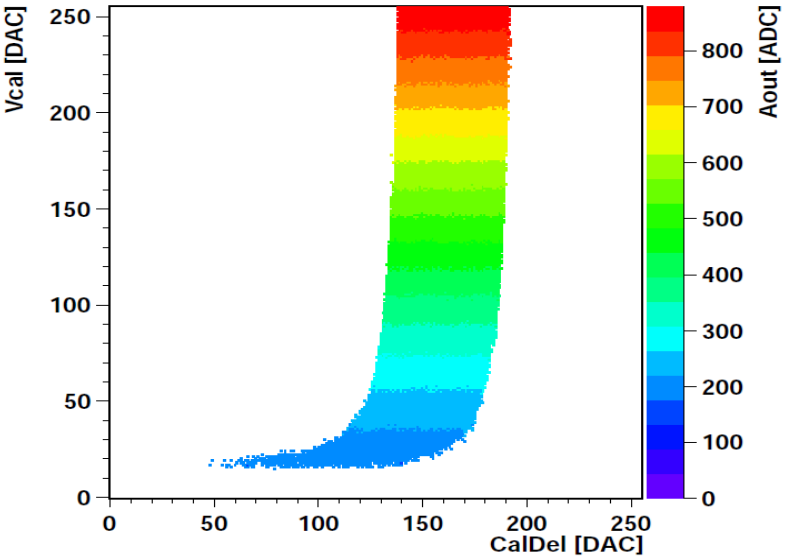


- All pixels.
- Left edge of time window for Vcal=255.
- all quarters are different
- smaller CalDel

Width of timing window

Chip5

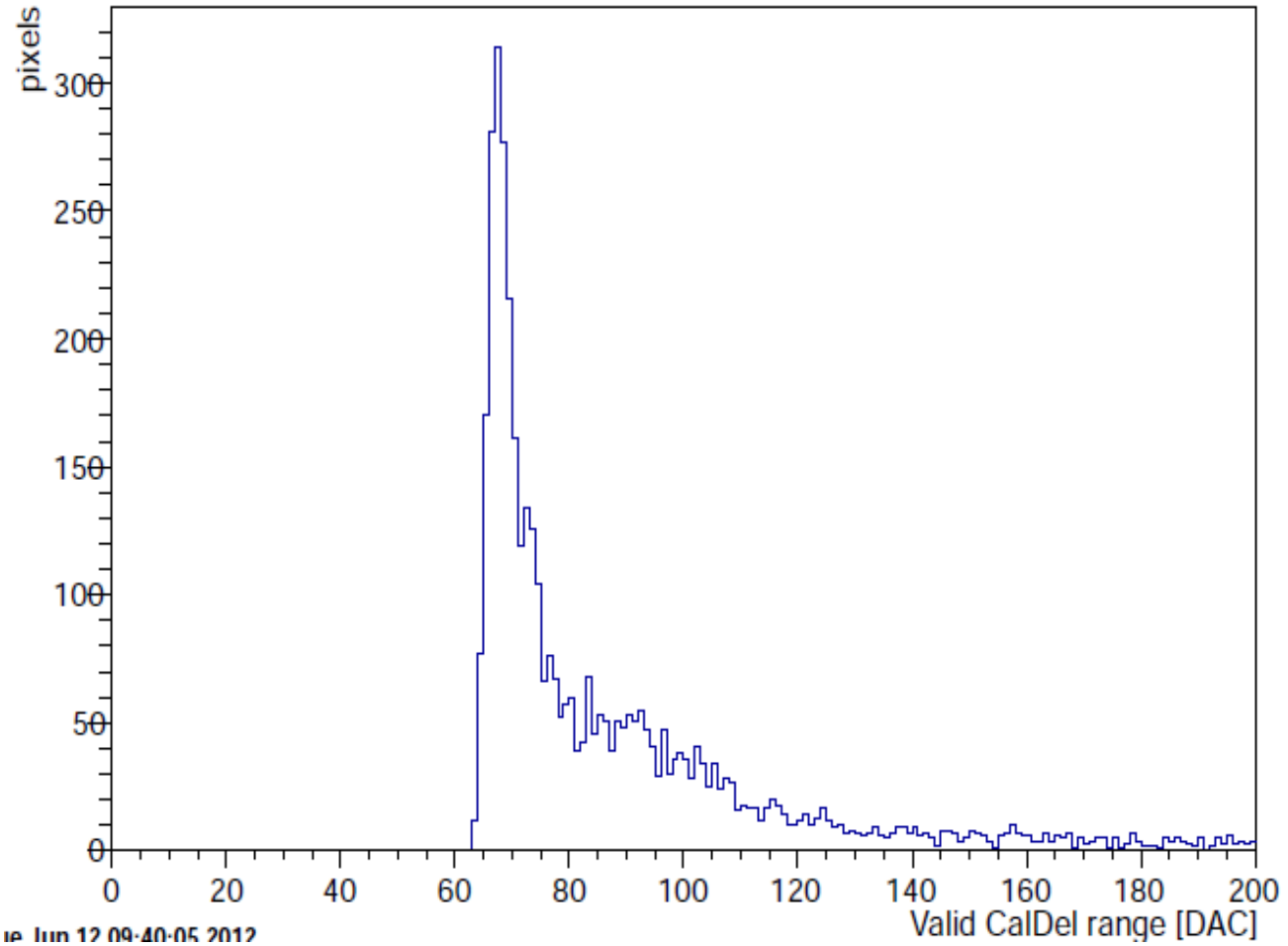




- All pixels.
- width of time window for Vcal=255.
- sharp distribution
- Mean 53,2 corresponds to one BC (25 ns)

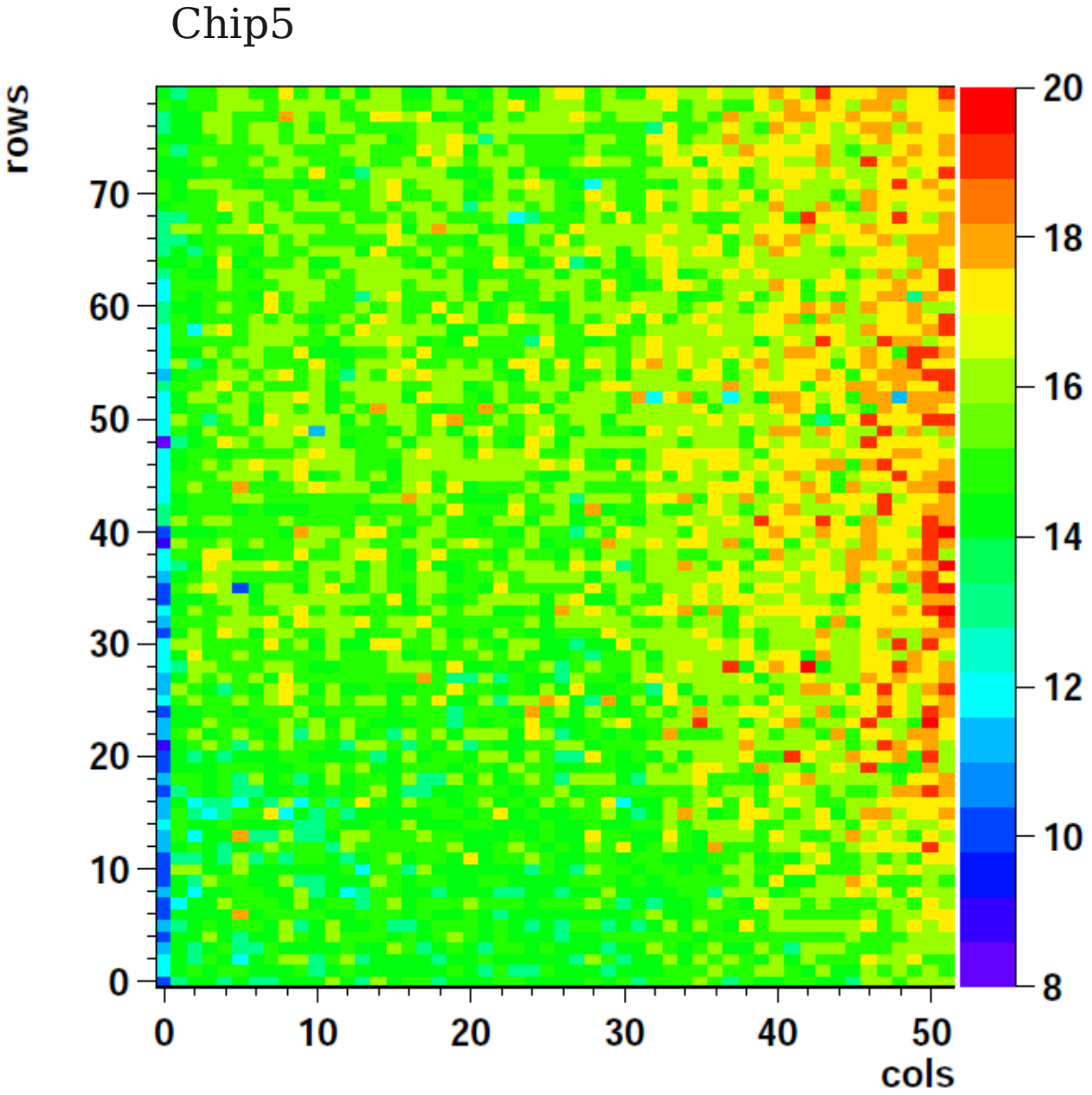
Width of timing window xdb

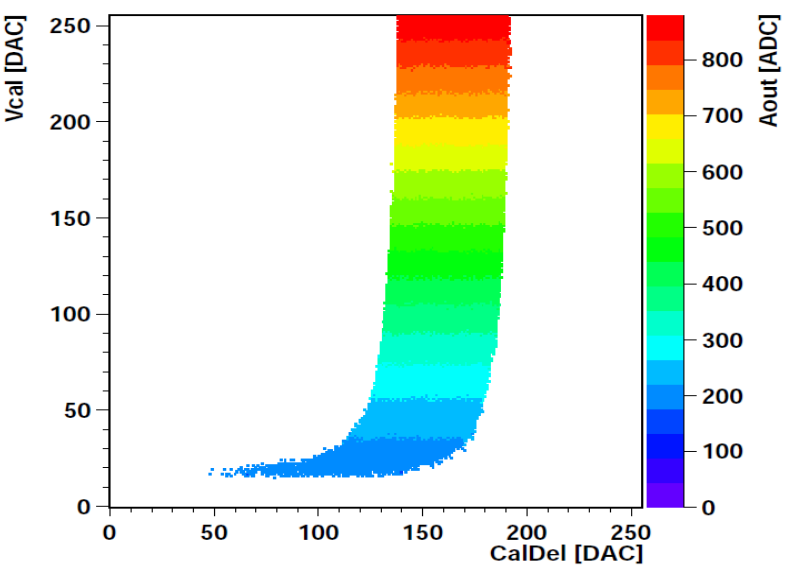
Chipx



- All pixels.
- width of time window for Vcal=255.
- Peak for the left half
- Tail for the right half

Time walk Chip 5



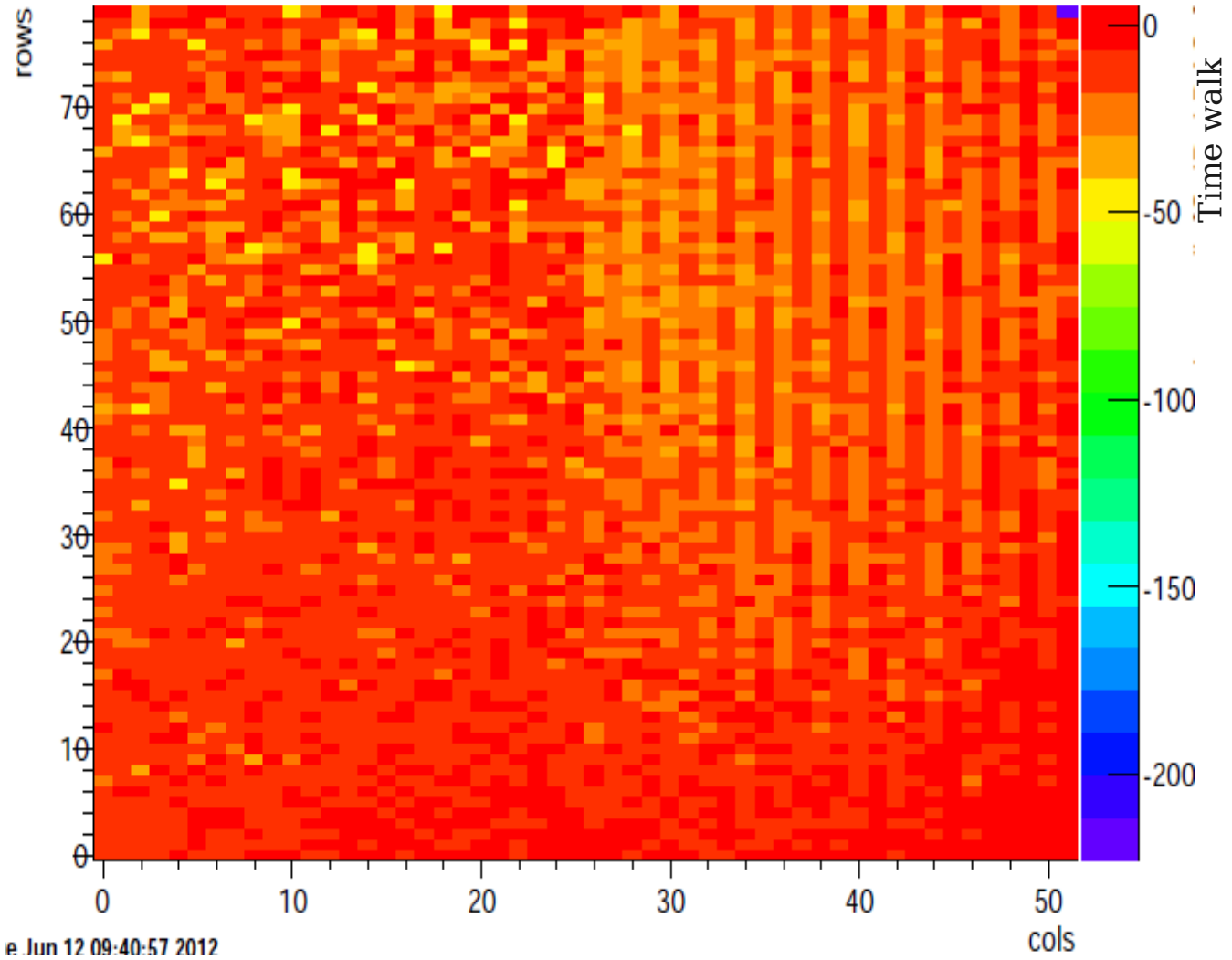


time walk

- All pixels.
- Time walk=left edge at Vcal=255 – left edge at Vcal=55
- trend across columns
- Mean value=15 corresponds to 7 ns

Time walk xdb

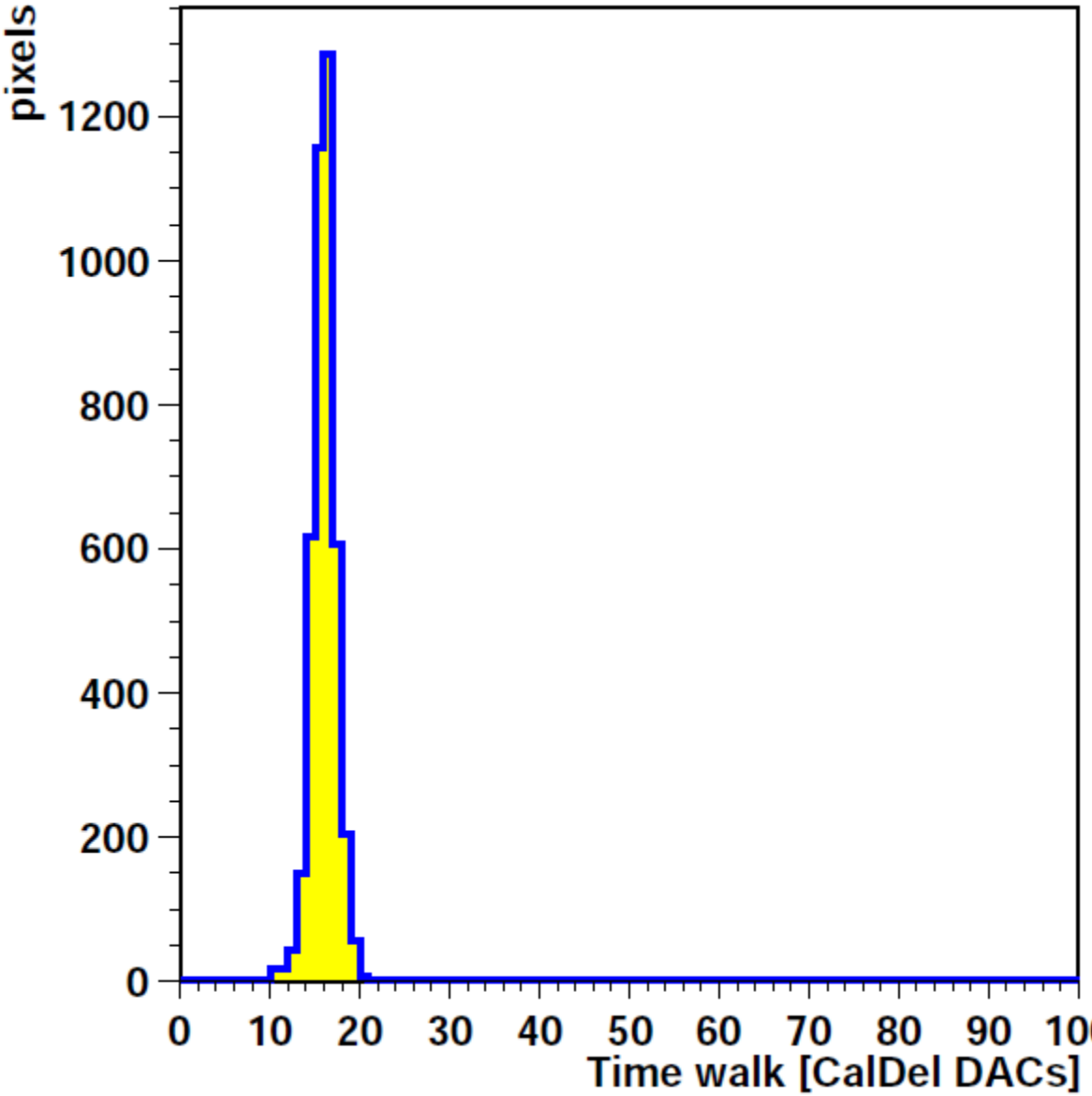
Chipx

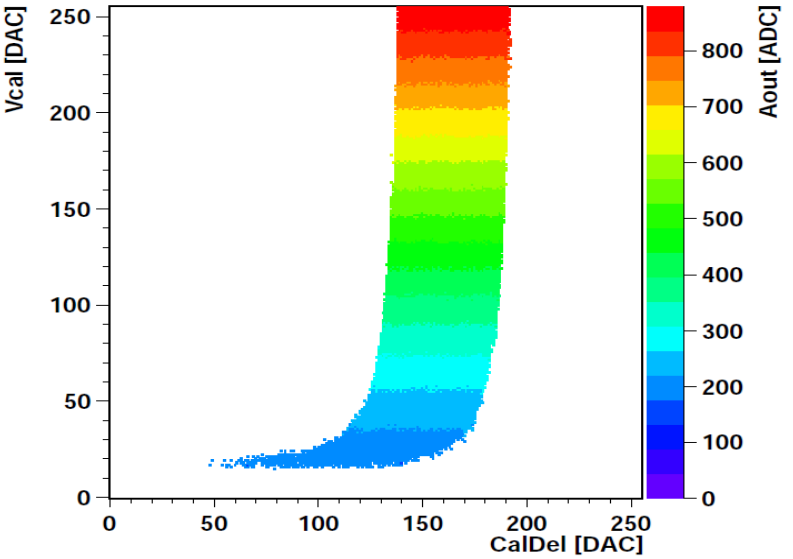


- All pixels
- Time walk=left edge at Vcal=255 – left edge at Vcal=55
- Trend across columns
- Mean value is negative

Time walk distribution

Chip5

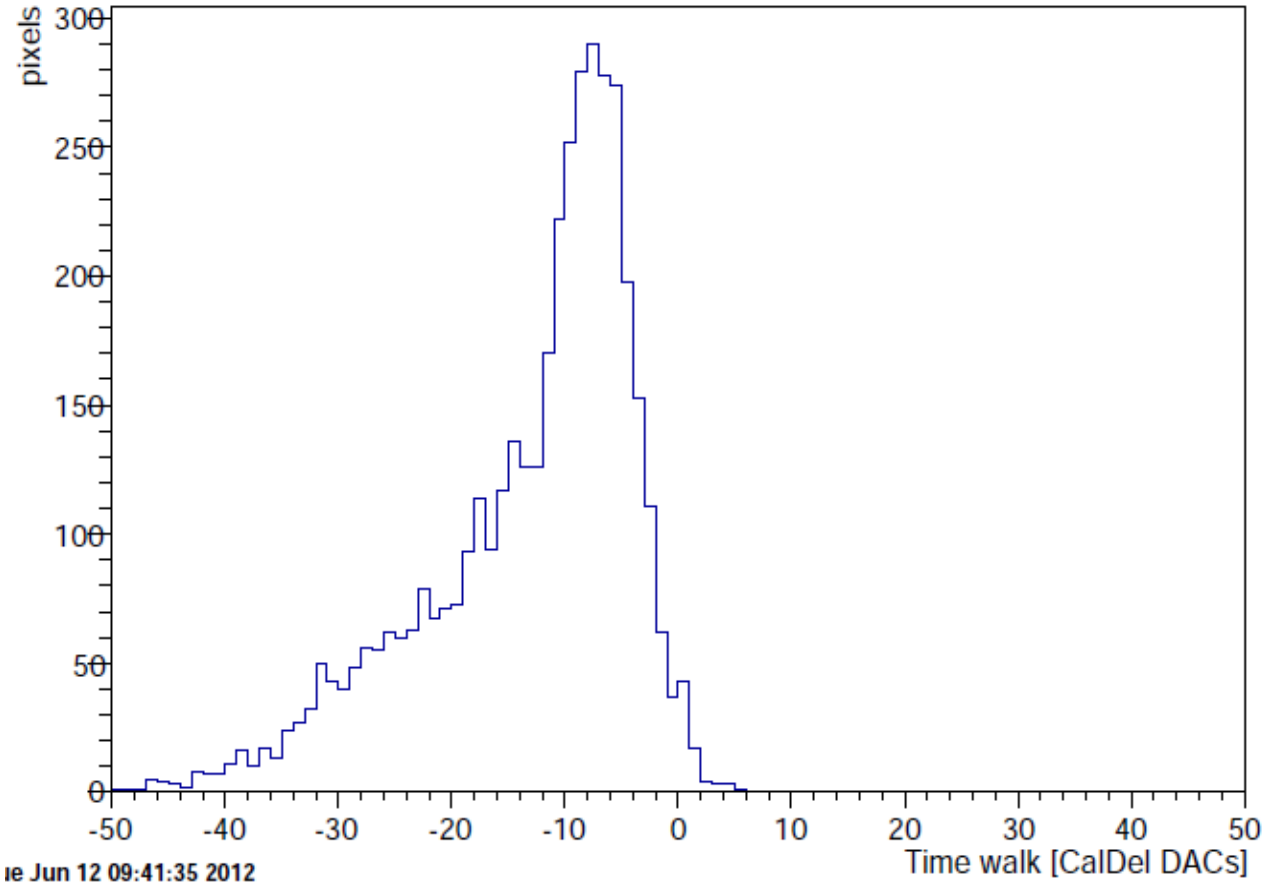




- All pixels.
- Time walk=left edge at Vcal=255 – left edge at Vcal=55
- Mean value=15 corresponds to 7 ns

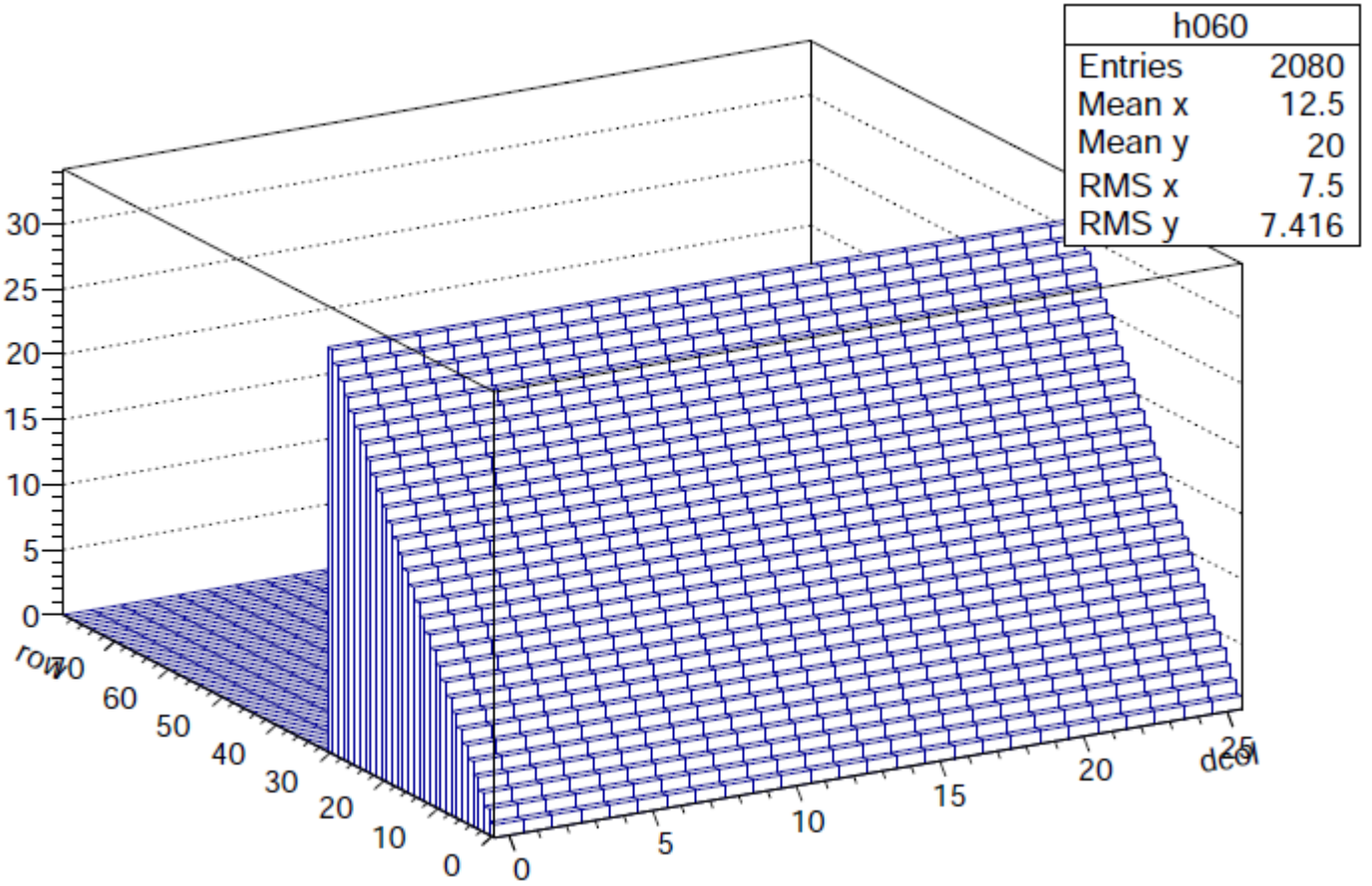
Time walk distribution xdb

Chipx



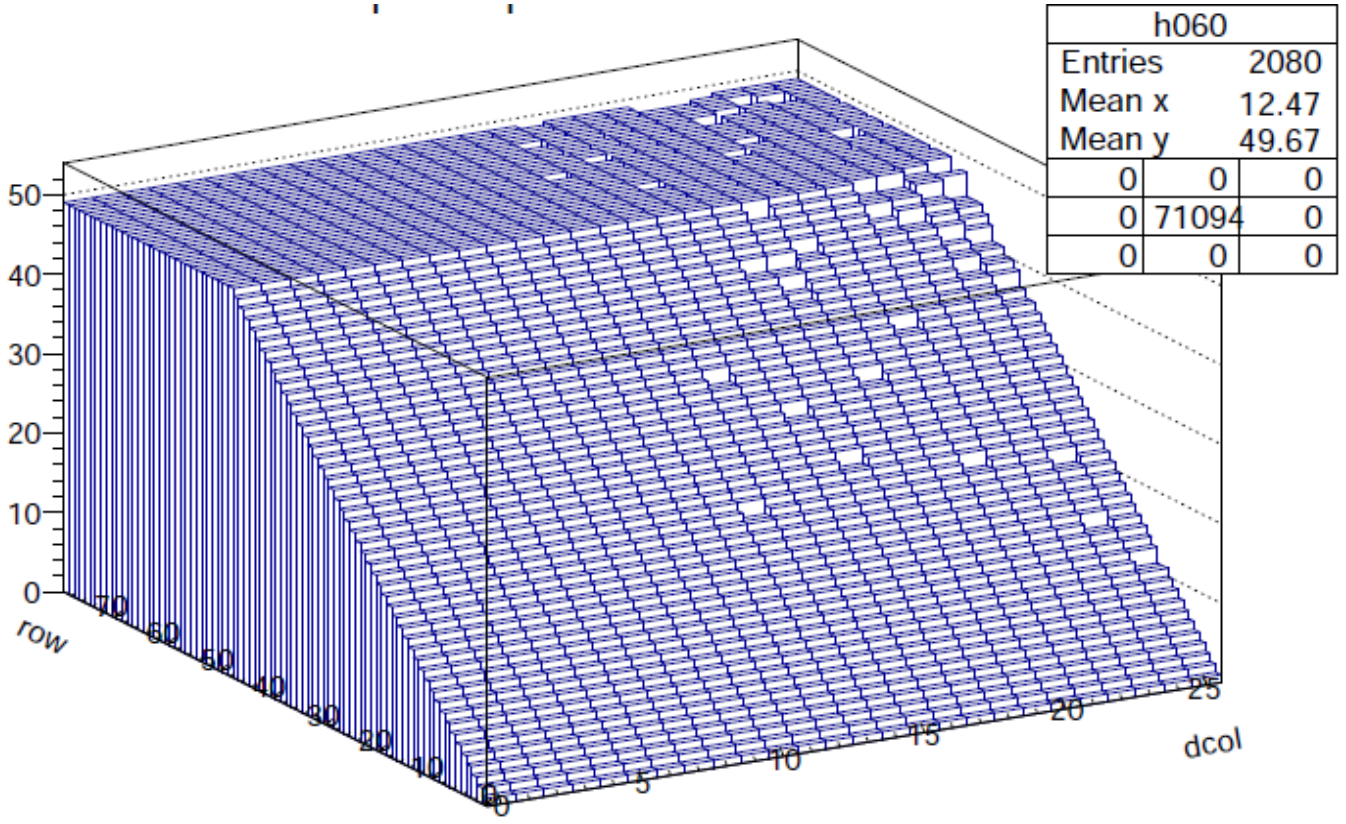
- All pixels.
- Time walk=left edge at Vcal=255 – left edge at Vcal=55
- Mean value is negative:
  - small time walk for the left half
  - long tail for the right half

Data buffer test Chip 5



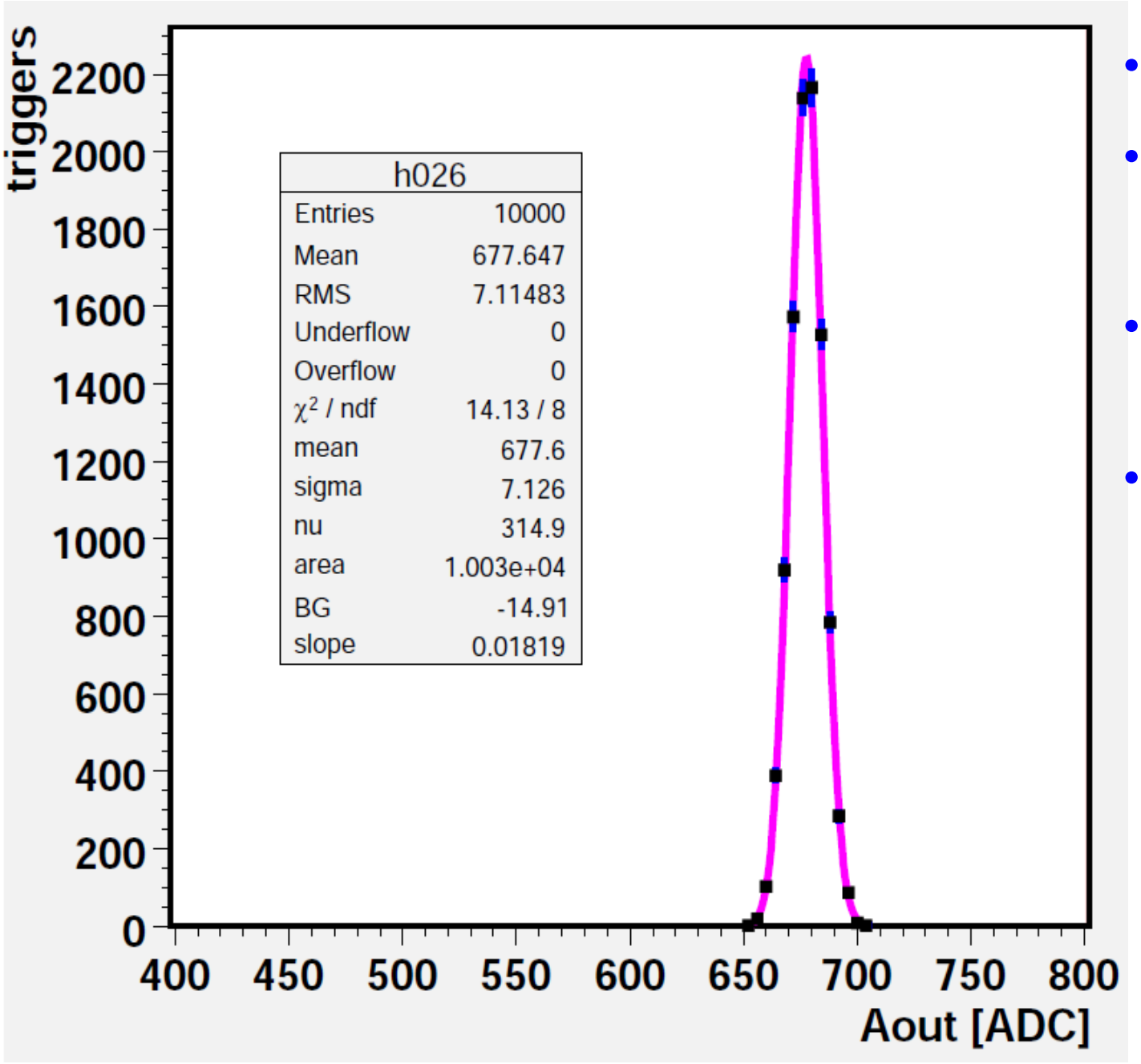
- Enable rows for each double column and count pixels
- Expect one pixel per activated row – until the data buffer is filled
- Up to 31 data bufferes for each double column are filled – OK

Data buffer test xdb



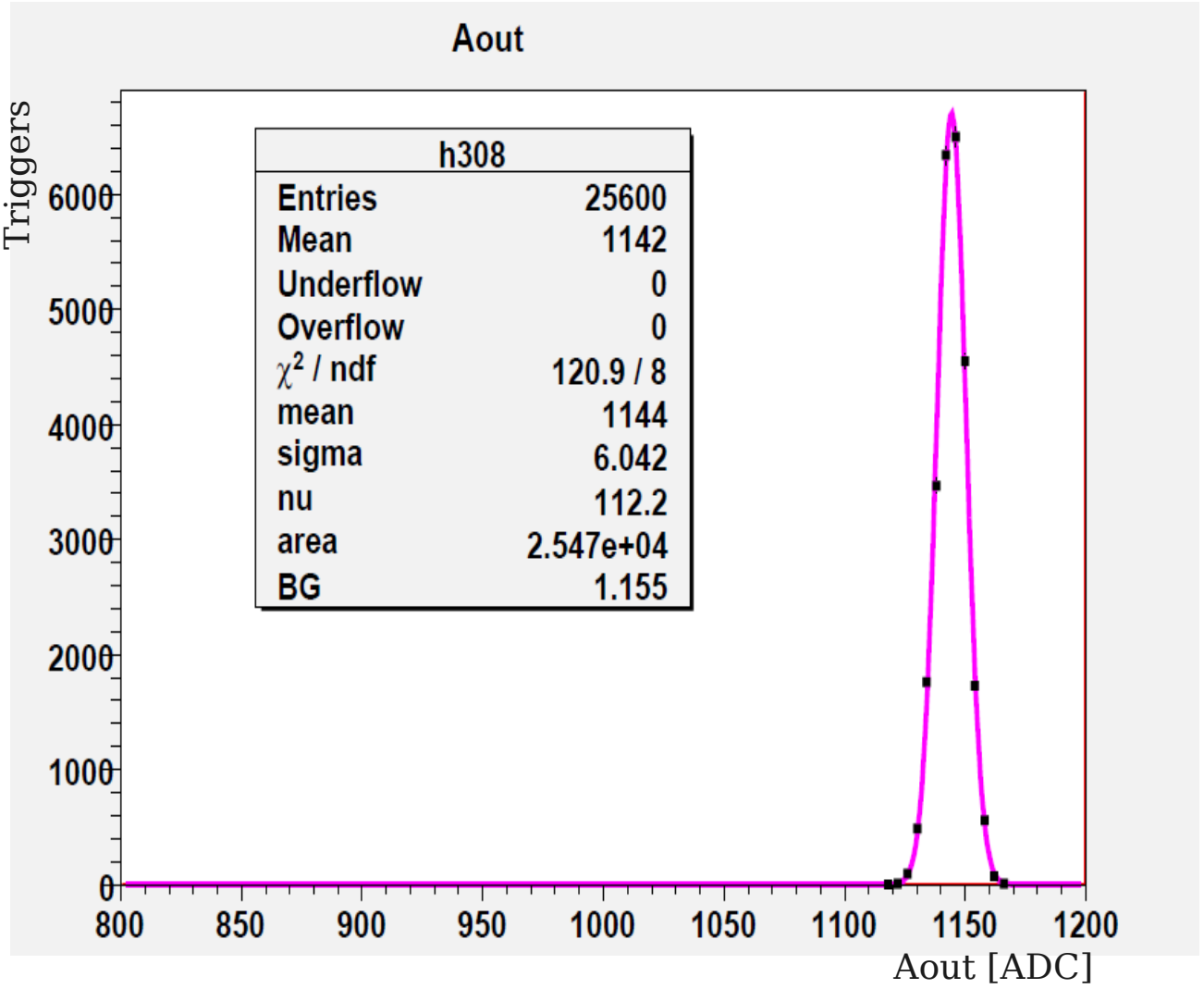
- All double columns.
- Up to 48 data buffers filled per double column
- No reset at the end ?

One pixel with test pulse Chip 5



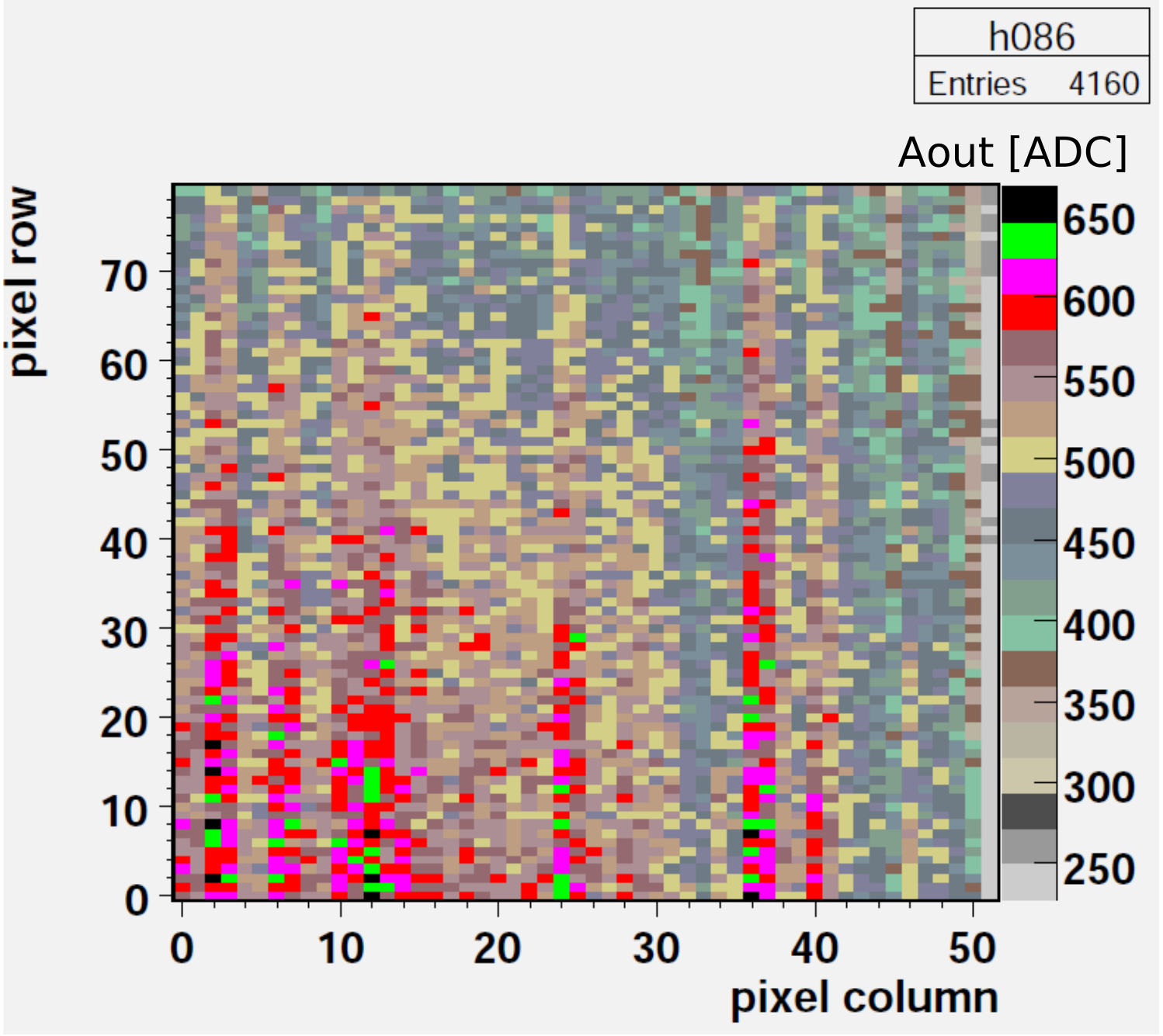
- one pixel.
- 10k triggers:
  - at 100 Hz = 100 s.
- Calibrate 200 small DAC = 13'000 e (PSI).
- Width = 7 ADC counts:
  - thermal noise,
  - perfect Gaussian,
  - 135 e (no sensor).
  - agrees with threshold scan!

One pixel with test pulse xdb



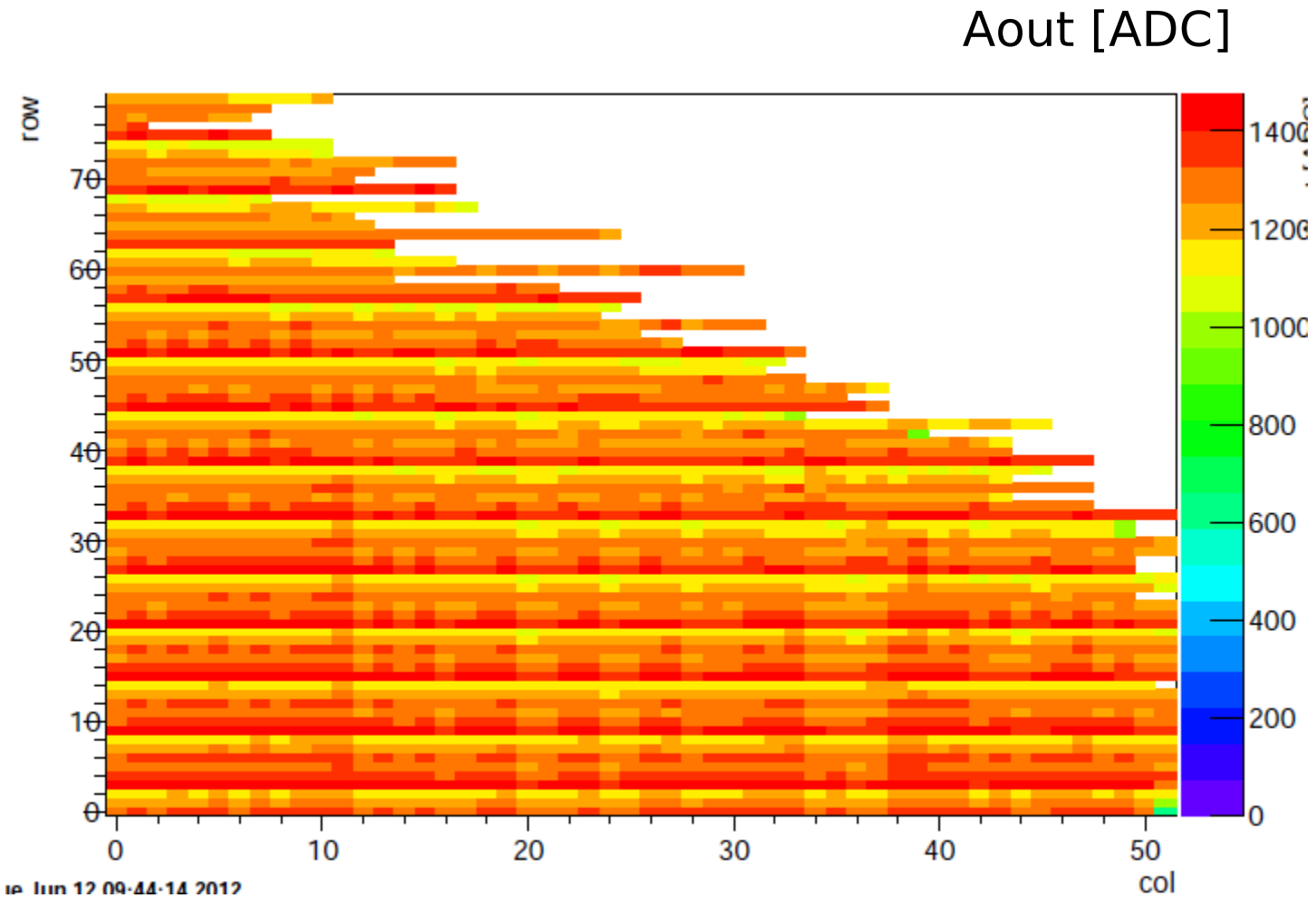
- one pixel.
- 25k triggers
- Width = 6 ADC counts
- CtrlReg 4

Pixel map Chip 5



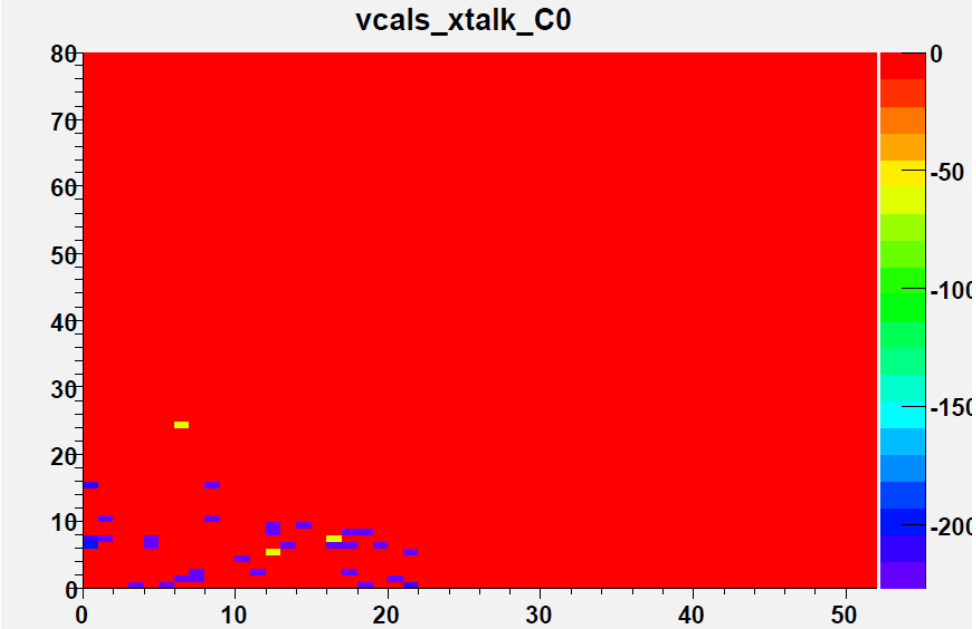
- 52 × 80 = 4160 pixel per chip.
- Vcal = 200 DAC
- VthrComp = 80
- Strong pulse height variation:
  - gain?
  - timing?

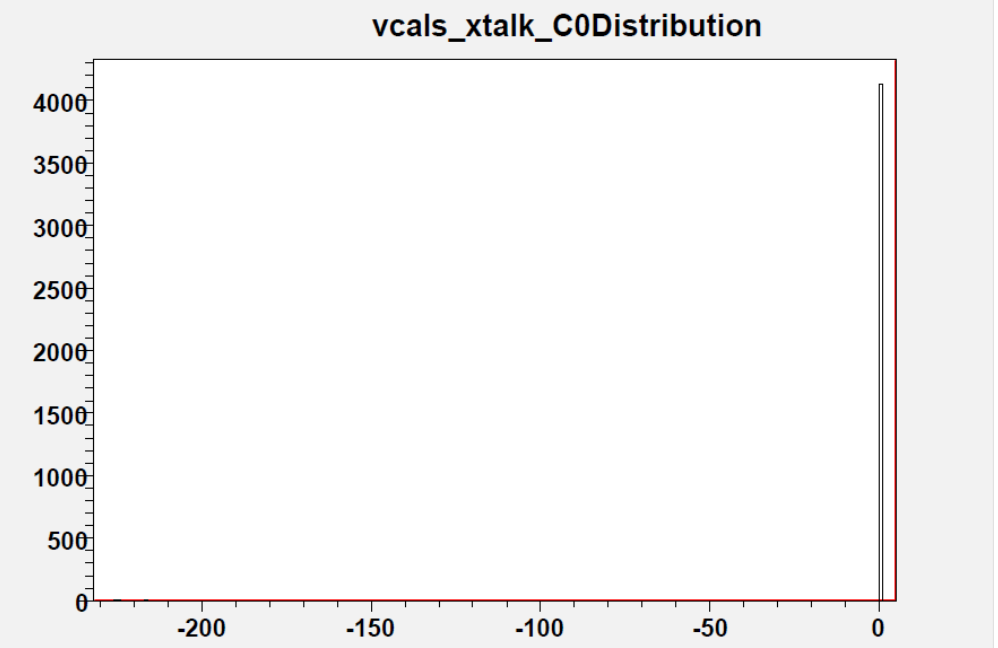
Pixel map xdb



- 52 × 80 = 4160 pixel per chip.
- Vcal = 200 DAC
- VthrComp = 72
- CtrlReg 4
- Strong pulse height variation

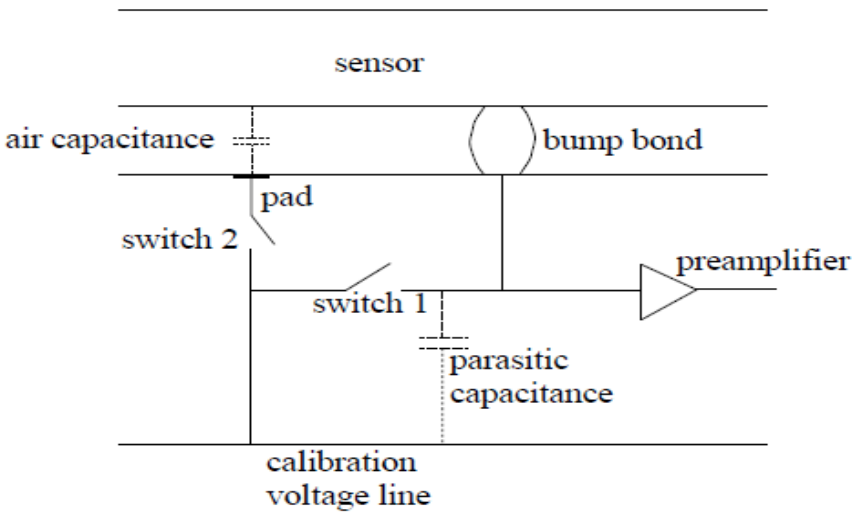
Bump Bonding test xdb



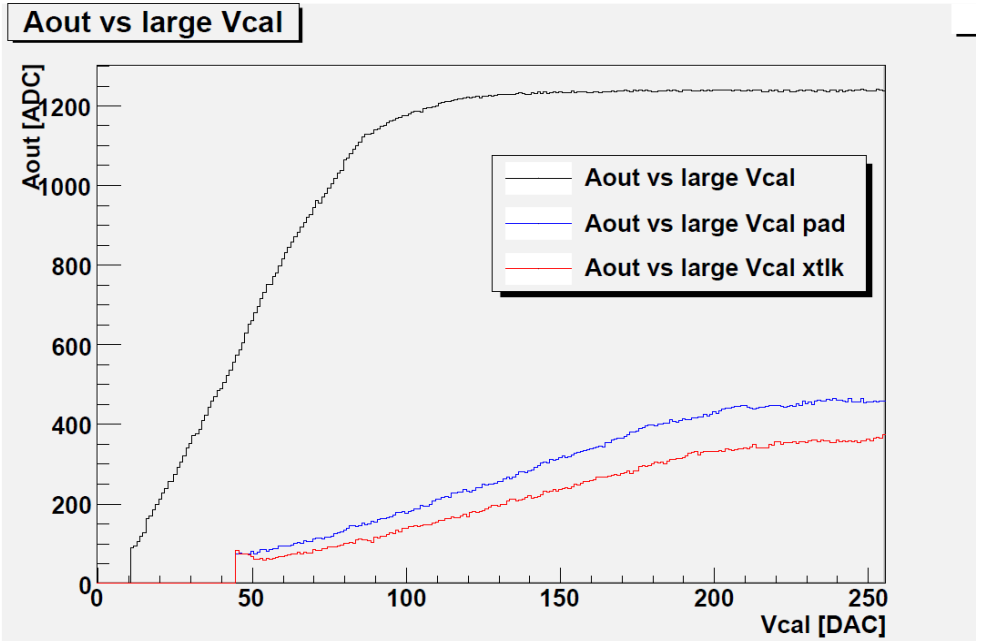


|Vcal_Thr1 – Vcal_Thr2| < 5 DAC units
→ defect bump bonding

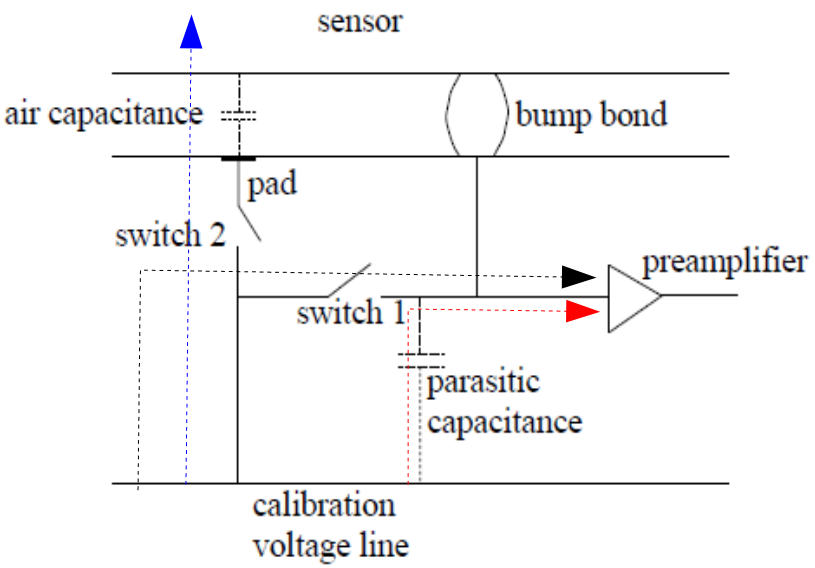
ΔThreshold peak at 0:
we do not see the sensor ?



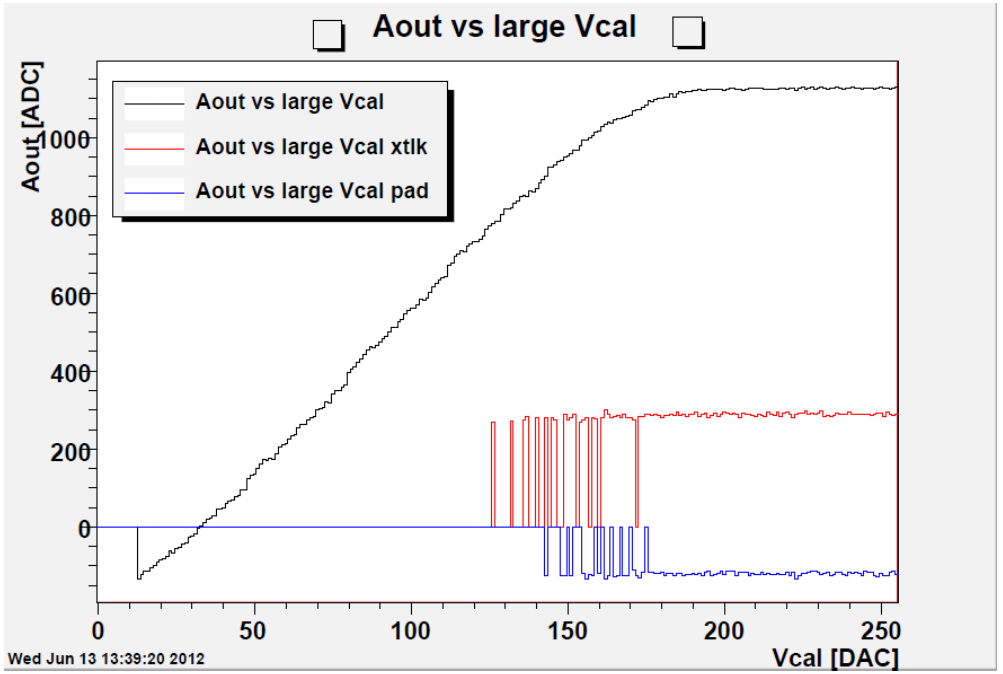
Arm, Pad, xtalk for Chip 8

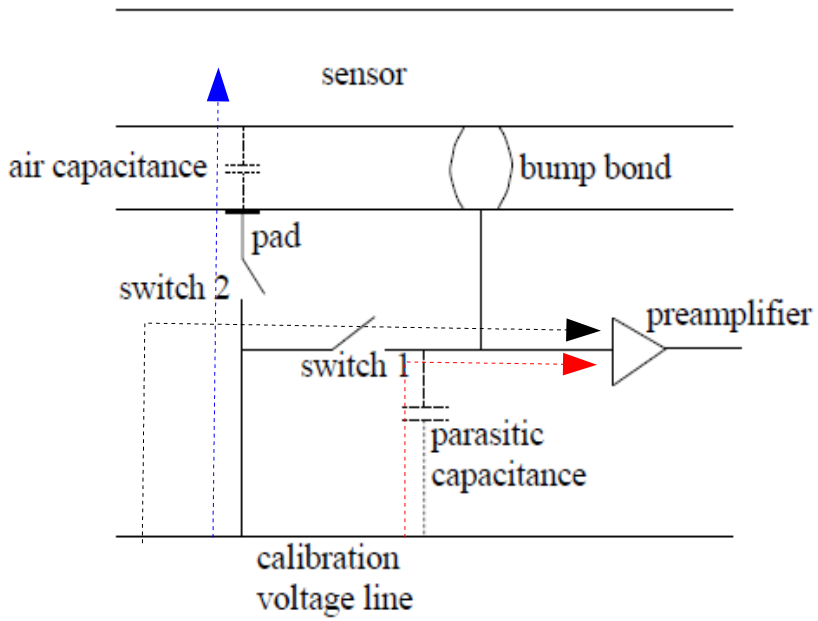


- Use three different capacitances to inject charge: **direct**, **via sensor**, and **crosstalk**:
  - $Q = C_x \cdot Vcal$
- One pixel activated
- Draw PH [ADC] vs calibrate amplitude for large Vcal (450 e/DAC)
- Use sensor type ROC



Arm, Pad, xtalk for xdb





- Use three different capacitances to inject charge: **direct**, **via sensor**, and **crosstalk**:
  - $Q = C_x \cdot Vcal$
- One pixel activated
- Draw PH [ADC] vs calibrate amplitude for large Vcal
- Significant difference between sensor and crosstalk ways

Summary

- The xdb chip works (Last DAC responds, Aout responds). No DACs 5,6,8 now
- Ia is almost linear vs Vana (was quadratic)
- Pretest and Trimming procedure works
- PixelMap shows strong variation between left and right halves of the ROC (first 26 vs last 26 columns)
- After trimming, both halves are alive, but the thresholds differ a lot
- Tests are done with large Vcal (CtrlReg 4)
- Aout vs Vsf is different: rather flat instead of sharp valley
- Better linearity degree vs Vsf. Smaller ID dependence on Vsf
- Aout vs Vcal has smaller slope now
- Aout vs Vcal reacts very little to Vbias on or off
- Aout has a maximum at VhldDel=255
- Only narrow region of comparator threshold can be used

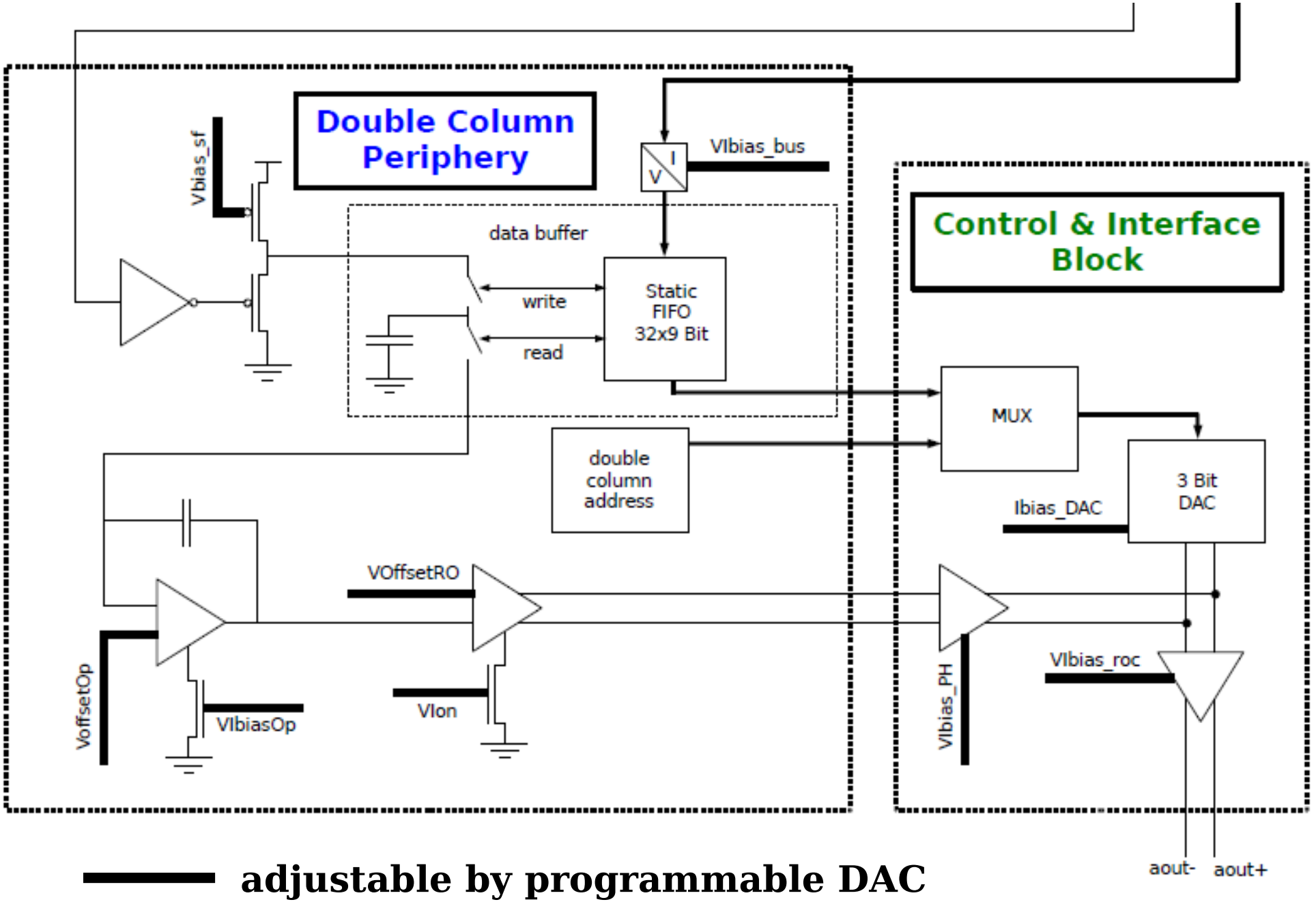
Summary (continue)

- Time walk is different between left and right halves
- Up to 48 data buffers filled per double column
- Strong Pulse height variation in Aout map
- Bump bonding test shows peak at 0 only
- Strong reaction to light (right half)

- Problem: we don't see pulses from a Ru106 (3 MeV e-) source with TakeData

Back up

psi46 pixel readout chip



adjustable by programmable DAC

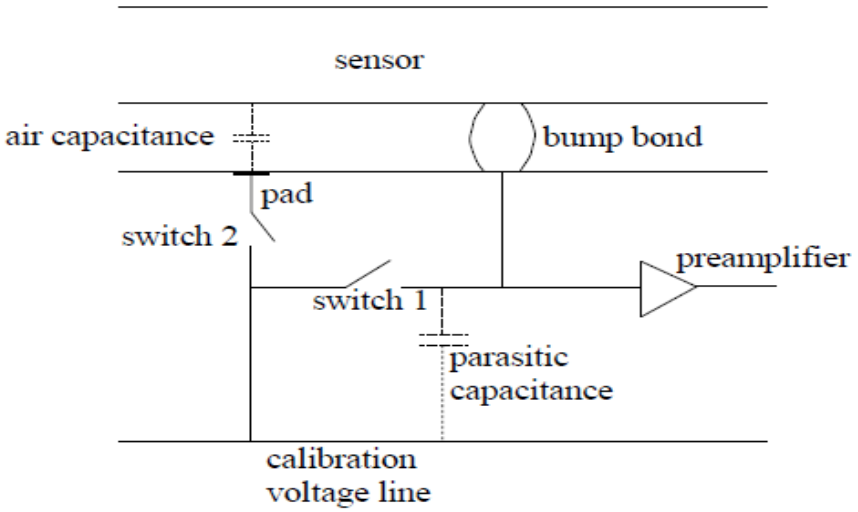
psi46 DACs

1	Vdig	6
2	Vana	150
3	Vsf	160
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	7
12	VthrComp	124
253	CtrlReg	0
254	WBC	20

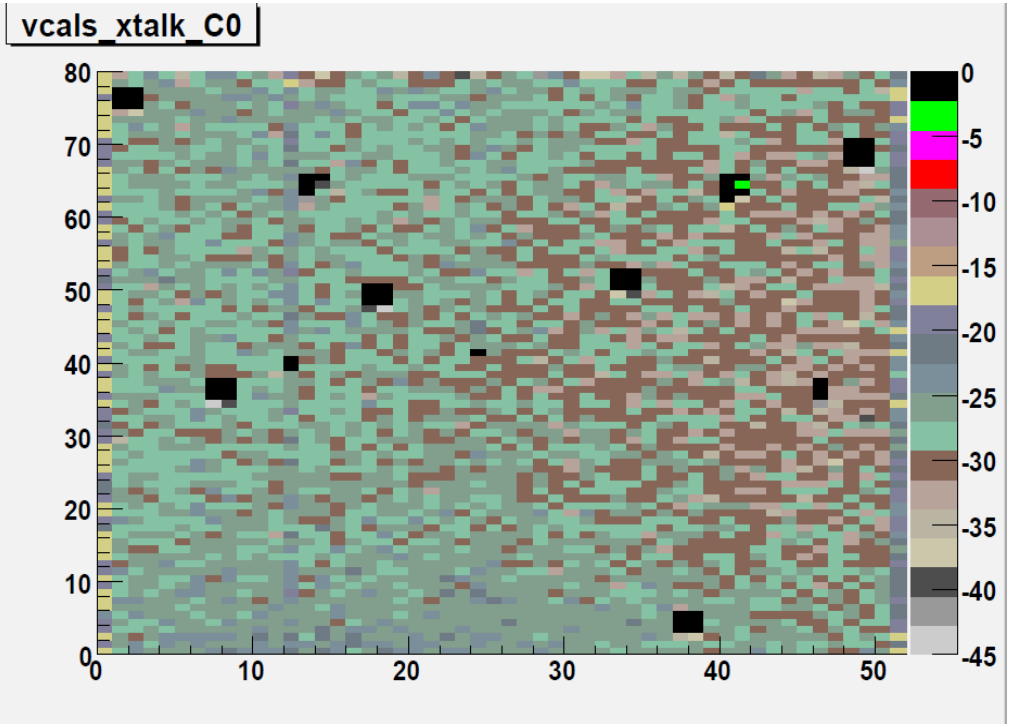
13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

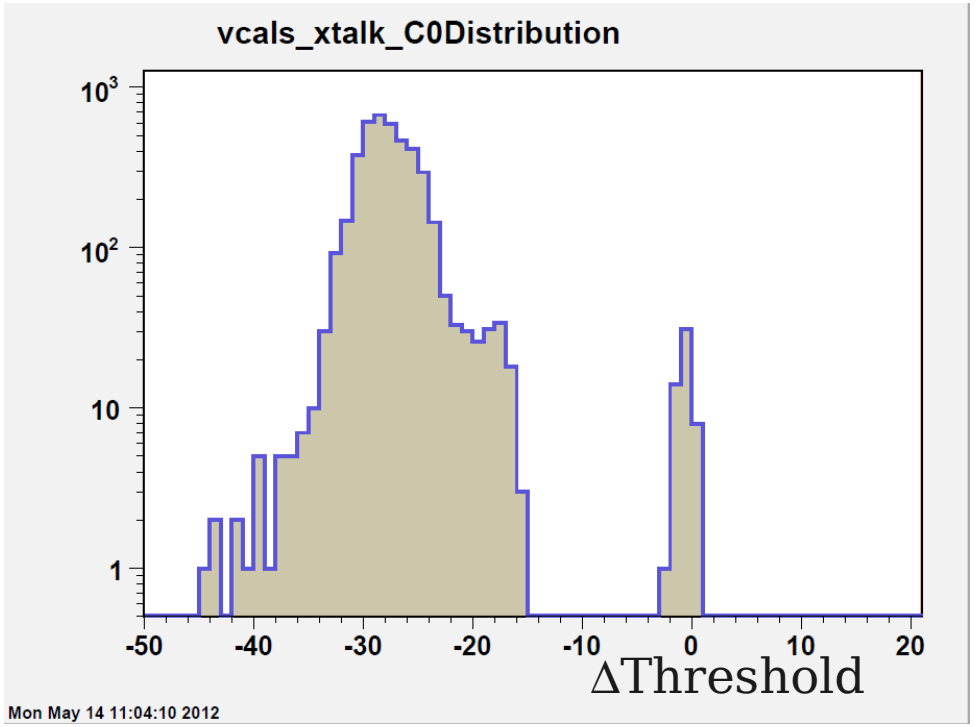
Bump Bonding Test Procedure

- Vcal to switch 2 induces a signal in sensor. If bump bond (bb) is present it is seen by preamplifier: missing bb can be identified
- Problem: cross-talk via a parasitic coupling between the calibration voltage line and preamplifier can fake a signal even without bb
- Determine Vcal_Thr2 for the signal injection through the sensor
- Measure Vcal_Thr1 for the parasitic cross-talk (with both switches open)
- |Vcal_Thr1 – Vcal_Thr2| < 5 DAC units → defect bump bonding



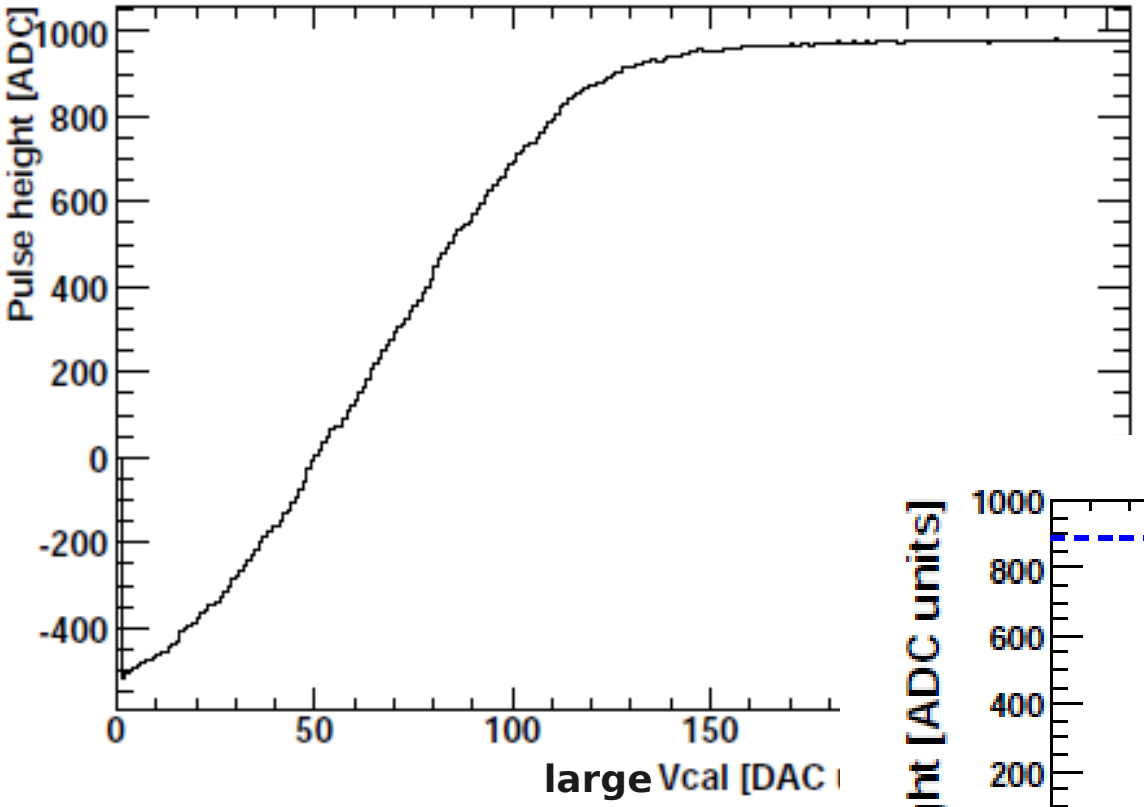
Bump Bonding Test Results, chip11





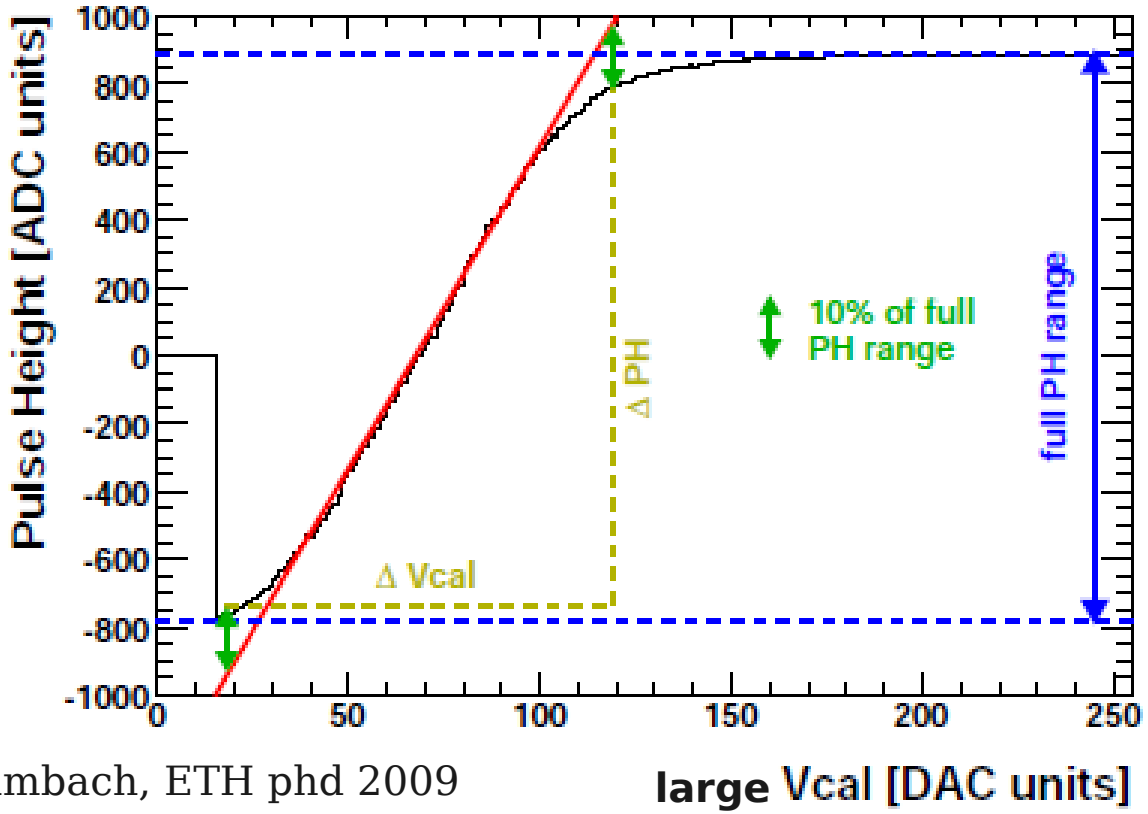
- Threshold difference: expected defects from beam test are correctly identified by 'psi46expert'
- Peak at ΔThreshold ~ -25 → good bump bonds. Peak at ΔThreshold ~ 0 → bad bump bonds

linear range and saturation at PSI



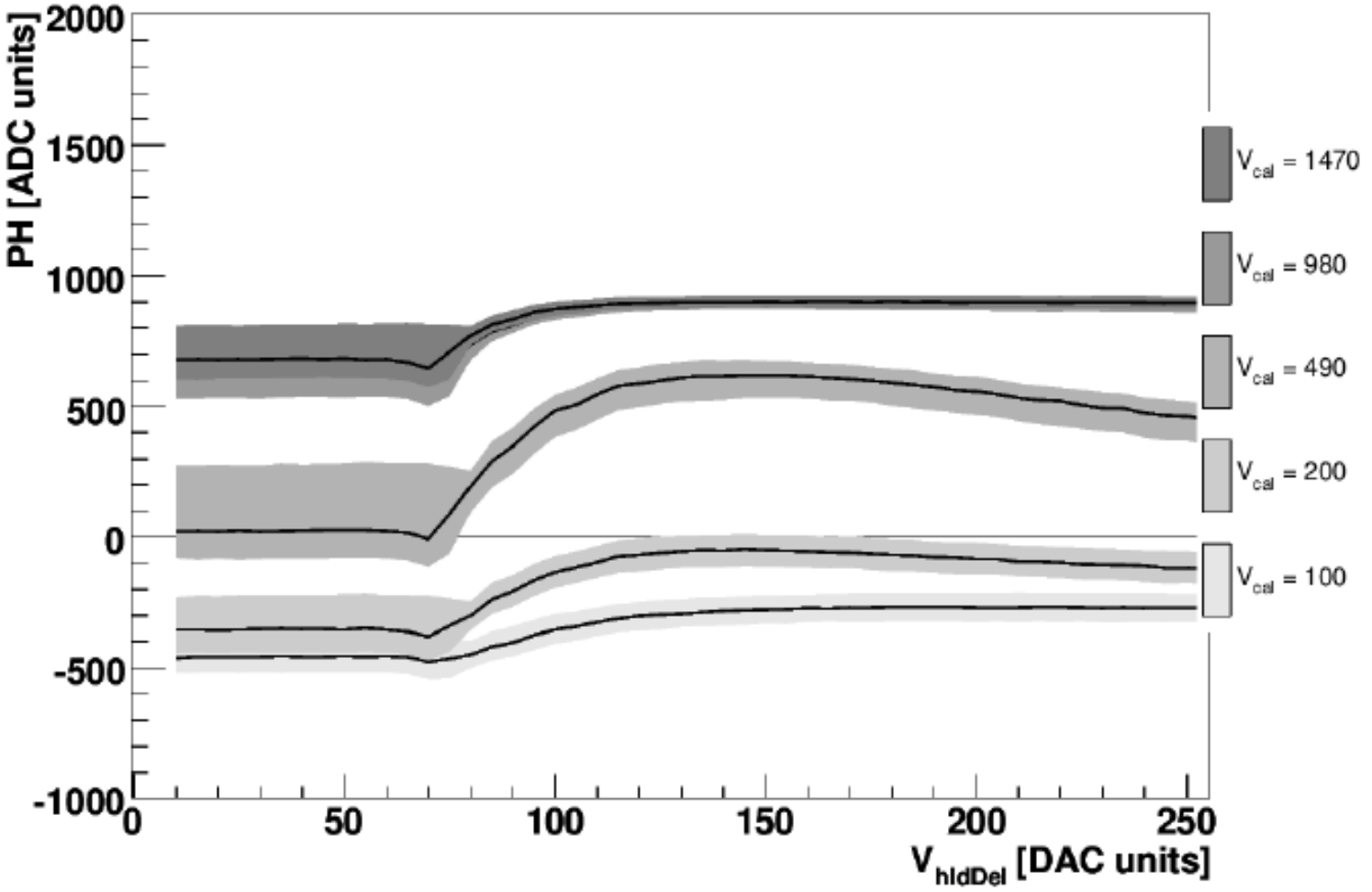
P. Trüb, ETH phd 2008

- Taken at PSI:
  - looks similar.
  - somewhat larger linear range
  - different working point?



S. Dambach, ETH phd 2009

Sample and hold timing at PSI



- Similar observations
- Somewhat different working point.

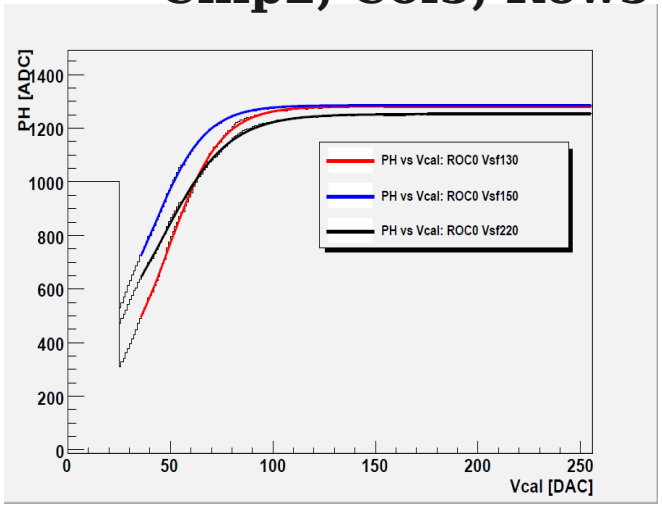
S. Dambach, ETH phd 2009

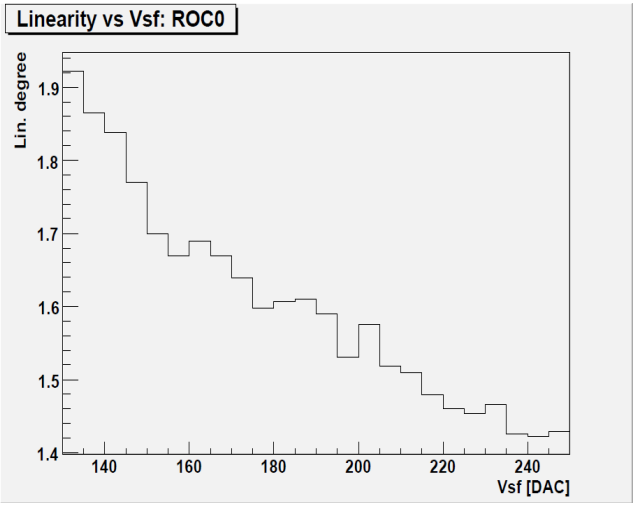
Vsf scan [VsfScan] Chip2

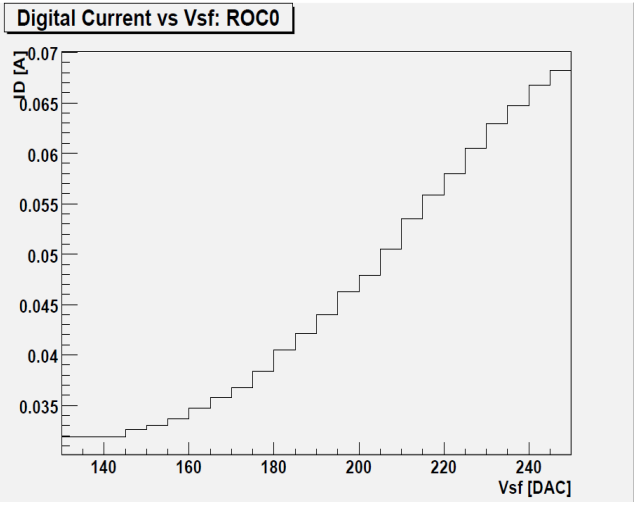
- Set high Vcal (CtrlReg=4) and default Vsf
- Fix 1 row. Check 5 columns in the row and find the one with a smallest deviation of linearity parameter from its mean (calculated from 5 col.)
  - Measure PH for Vcal [25 – 256]
  - Fit the curves with hyperbolic tangent function
  - Par(1) is a linearity degree (=1 if linear)
  - Find col. with a min. difference between mean and linearity parameter
- Arm one pixel in chosen column. Scan Vsf [130 – 250] with step=5
- Measure PH for Vcal [25 – 256] for each Vsf value
- Fit the curves with hyperbolic tangent function
- Plot linearity degree and ID since Vsf affects the digital current
- ~1 min. test

$$y = P3 + P2 * \tanh(P0 * x - P1)$$

Chip2, Col5, Row5







PSI46 test board at DESY