XDB ROC Tests 2

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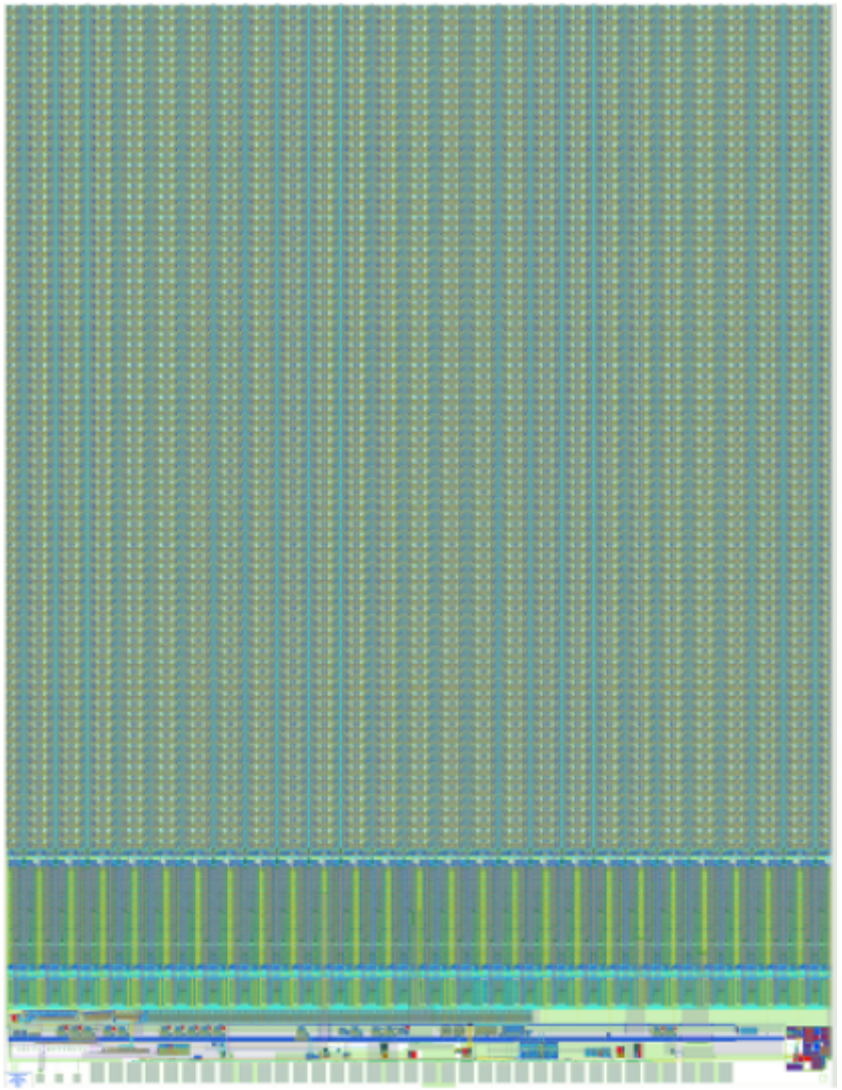
Pixel upgrade, 29.6.2012



- DESY setup
- Various tests
- Summary

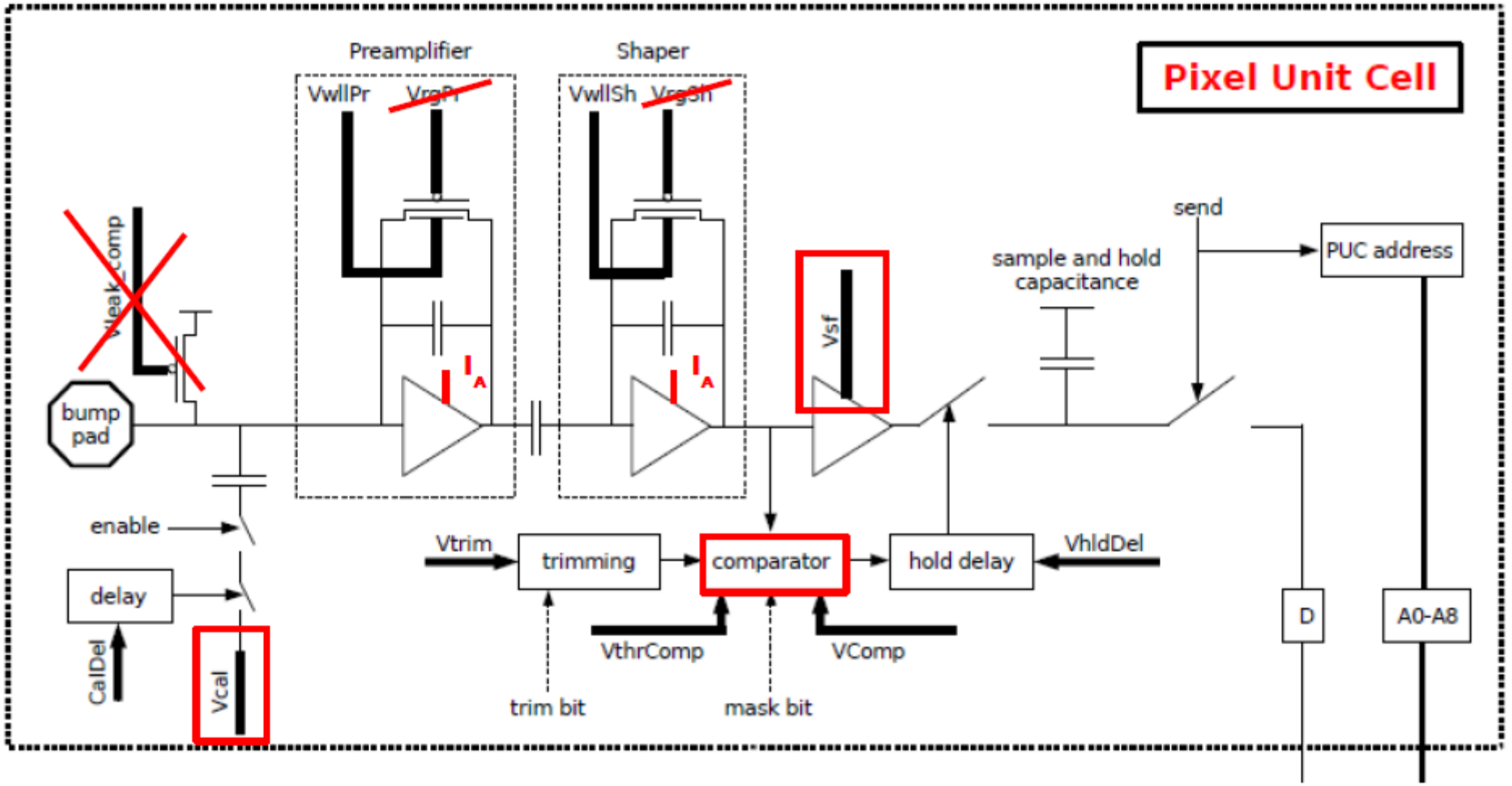
Configuration at DESY

- Another xdb ROC with sensor arrived from PSI 4 days ago
- PSI test board, with Aug 2010 FPGA firmware (binary file from Beat Meier downloaded using ALTERA USB Blaster via JTAG connector)
- run in 40 MHz mode
- Dell laptop running Ubuntu 10.10 Linux.
- psi46expert software compiled using gcc-4-5-2 in AMD 64 bit.
- libftd2xx1.0.2 for USB interface from FTDI: http://www.ftdichip.com/Drivers/D2XX.htm

PSI46expert software at DESY

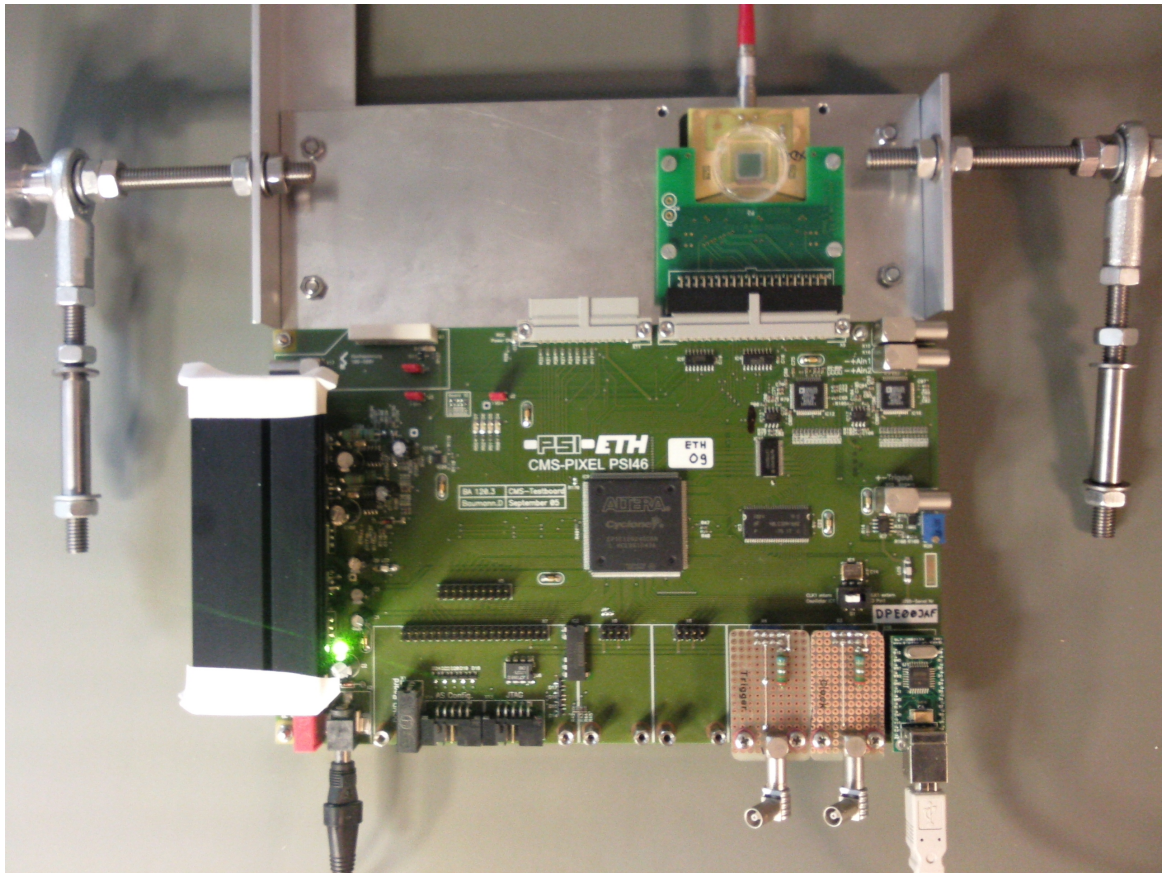
- Several new routines written:
  - DAC scans, noise maps, address decoding…
- DAC and TB settings for new chip are determined from Pretest.
- Threshold trimming is applied
- New slope of 0.15 A/DAC is measured
- FullTest confirms the determined parameters except BumpBonding test and AddressDecoding test (for part of the ROC)
- More individual tests are ongoing

PSI46xdb pixel unit cell



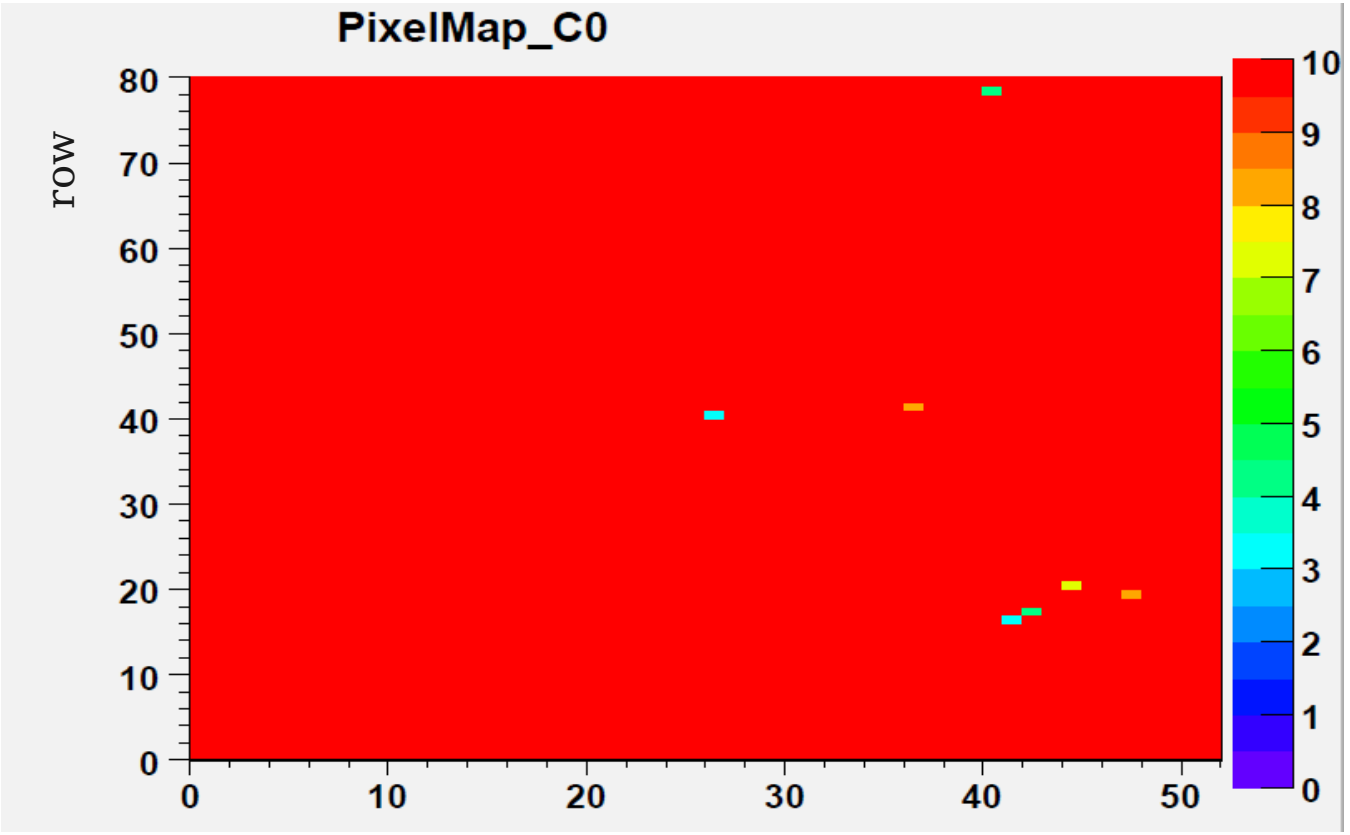
modified in PSI46xdb

Test setup at DESY



- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
- Use the same analog signal path as before

Pixel Alive test xdb2

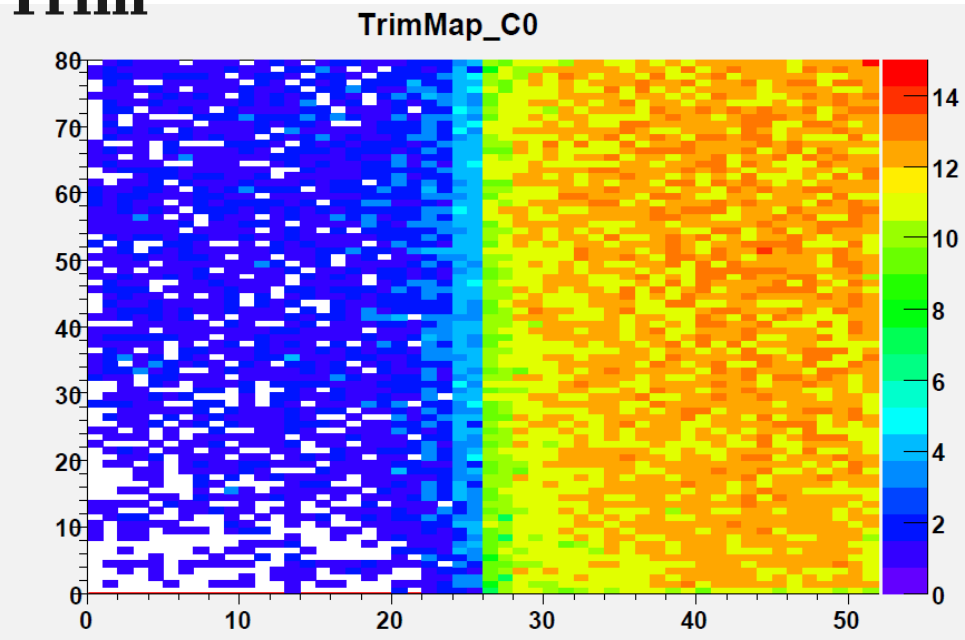


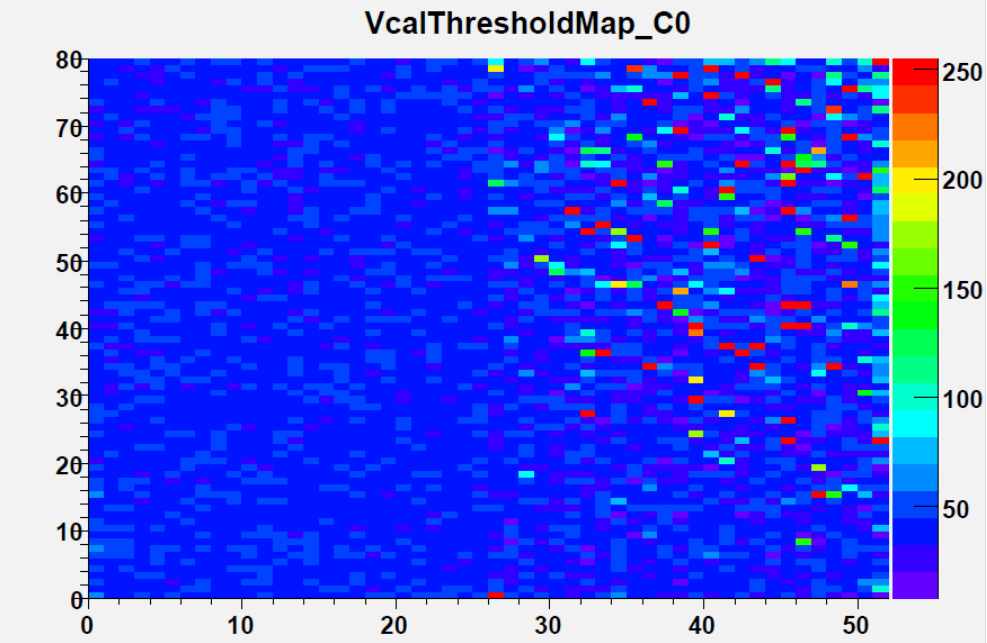
Pixmap

Charges above threshold are injected into all pixels in a ROC and the correct response of each pixel is verified

Maps after trimming xdb1 (15/06/2012)

Trim



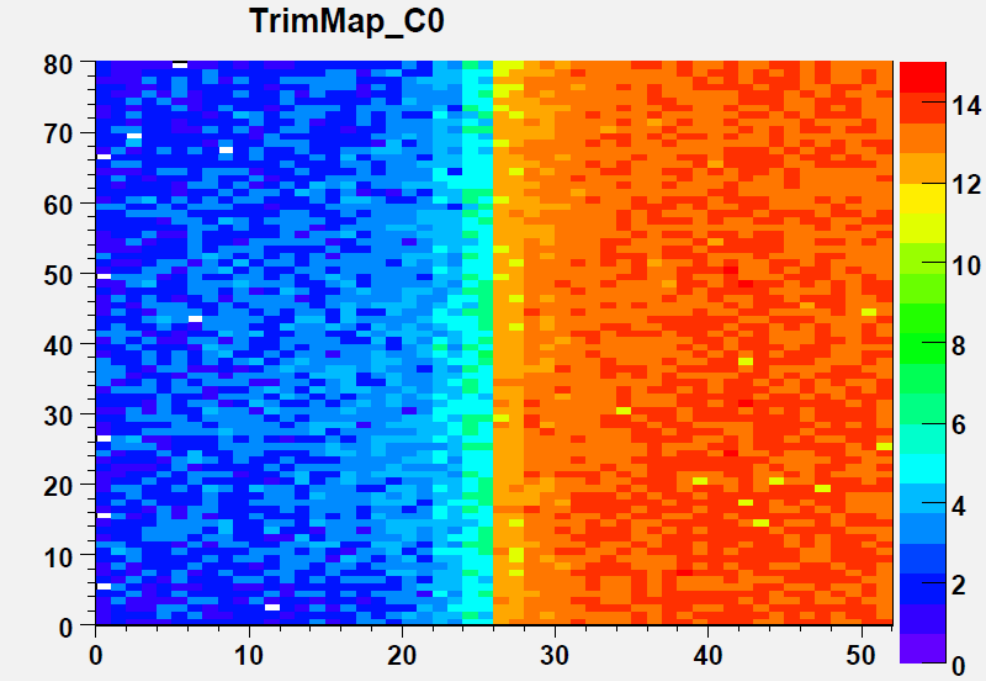


Trim bits map

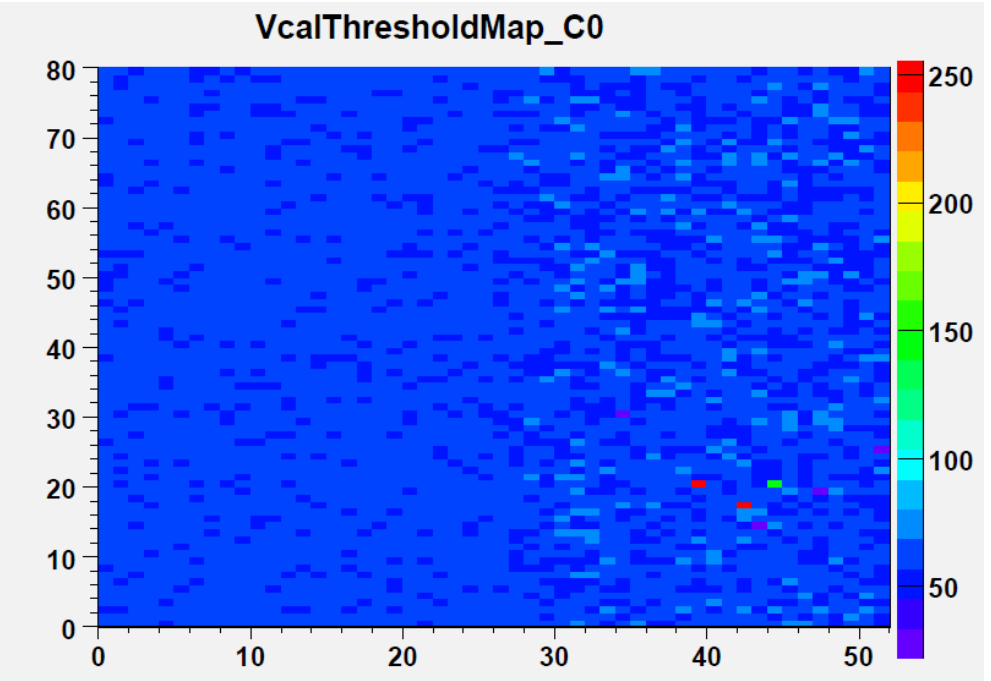
Vcal thresholds map

Big difference in trim bits and thresholds for 2 halves. Some thresholds are set to maximum – underflow bins ?

Maps after trimming xdb2



Trim bits map

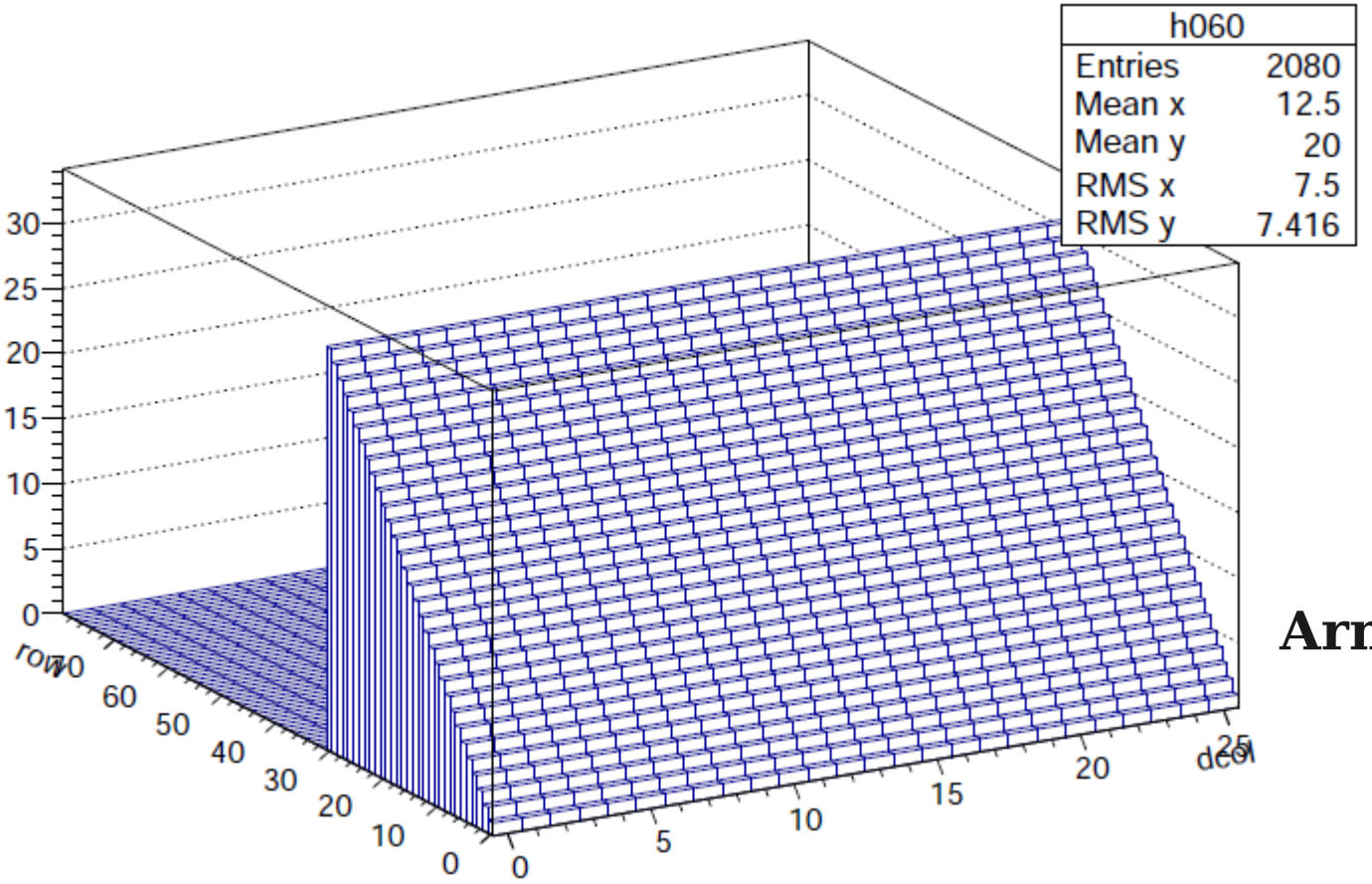


Vcal thresholds map

Big difference in trim bits for 2 halves. Almost all thresholds are set properly. Ia=40 mA, Target Vcal=60

New DAC and Trim files are prepared for various goal Ia and Vcal for the test beam

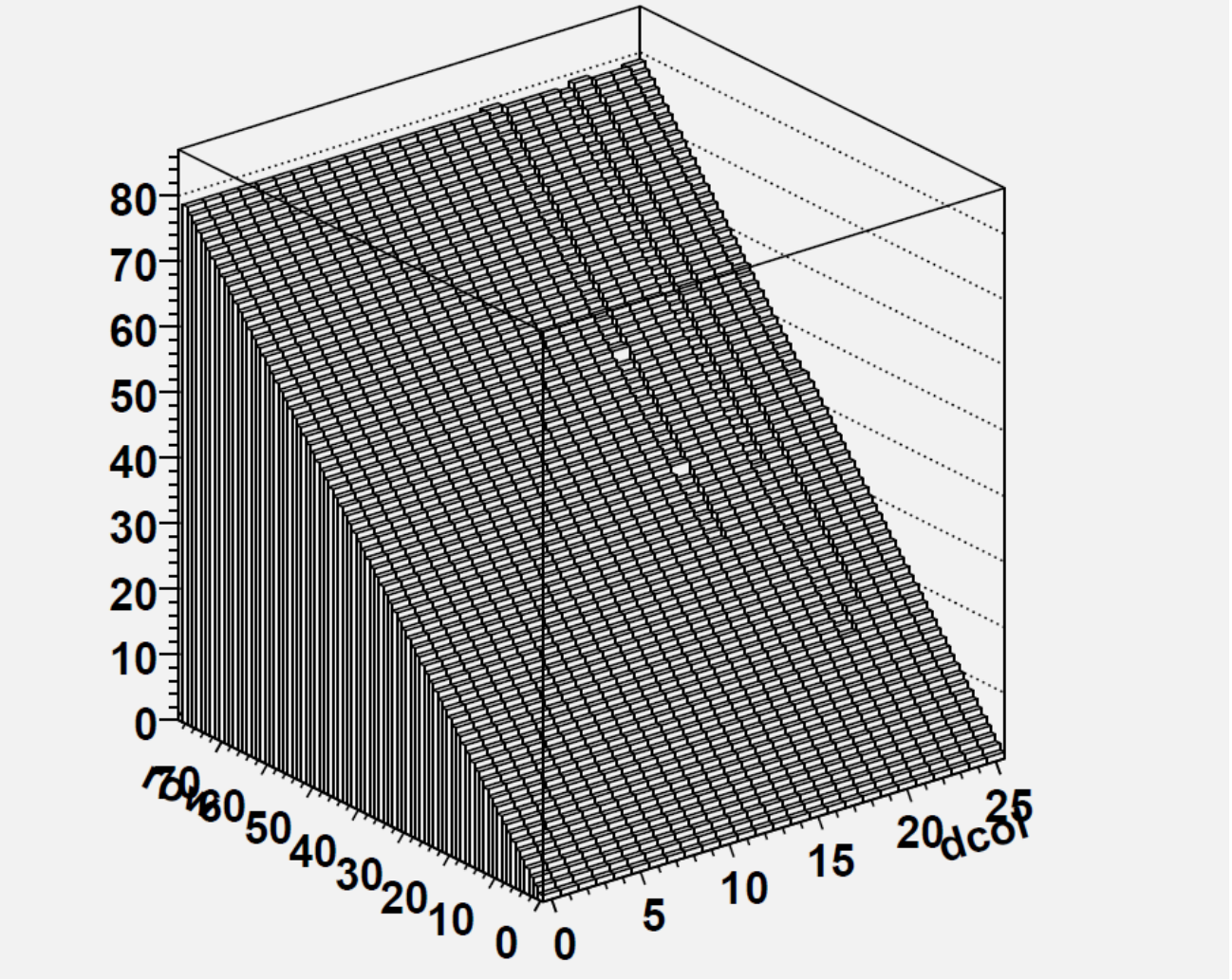
Data buffer test Chip 5 (old)



Armrow2d

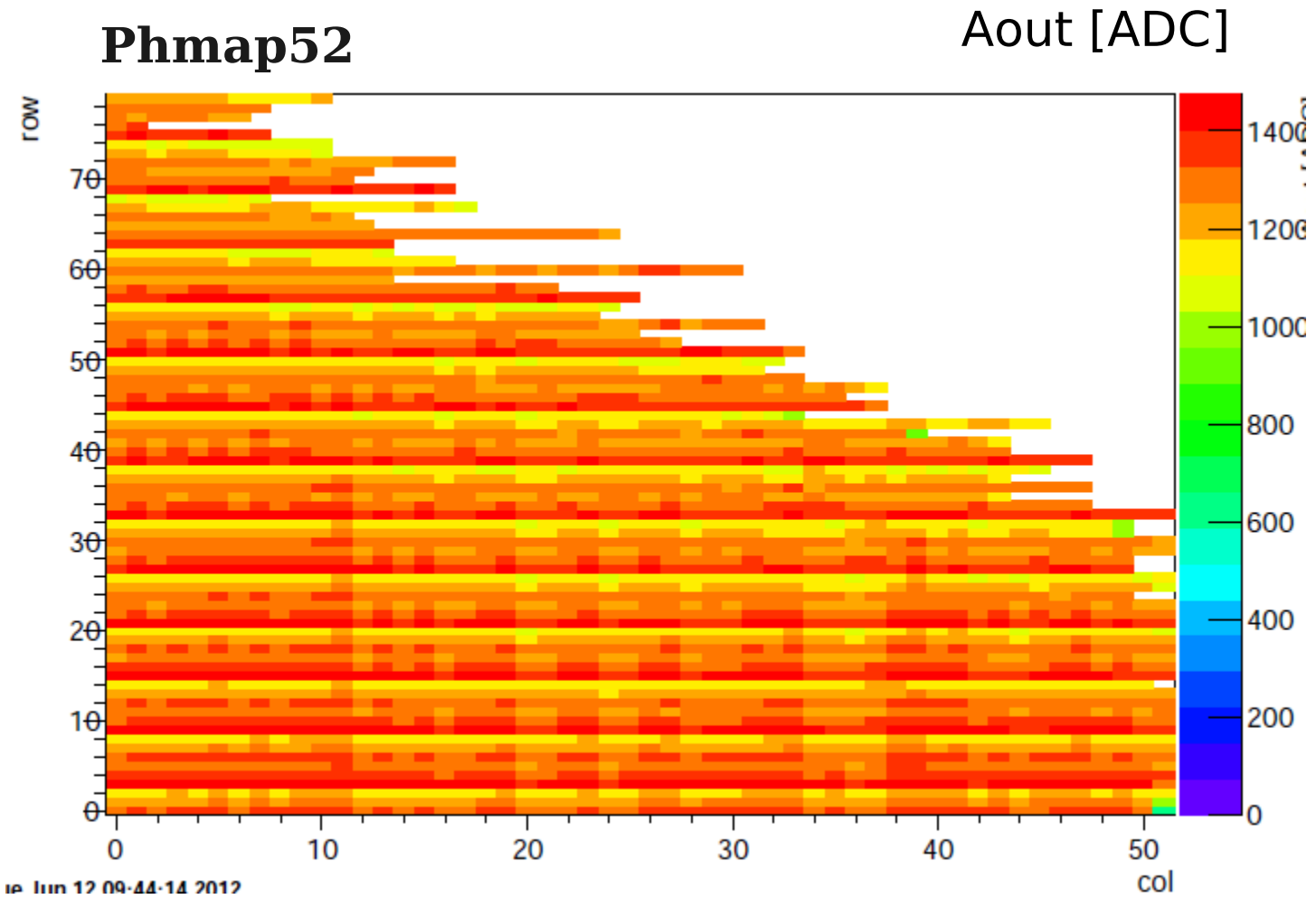
- Enable rows for each double column and count pixels
- Expect one pixel per activated row – until the data buffer is filled
- Up to 31 data bufferes for each double column are filled – OK

Data buffer test xdb2



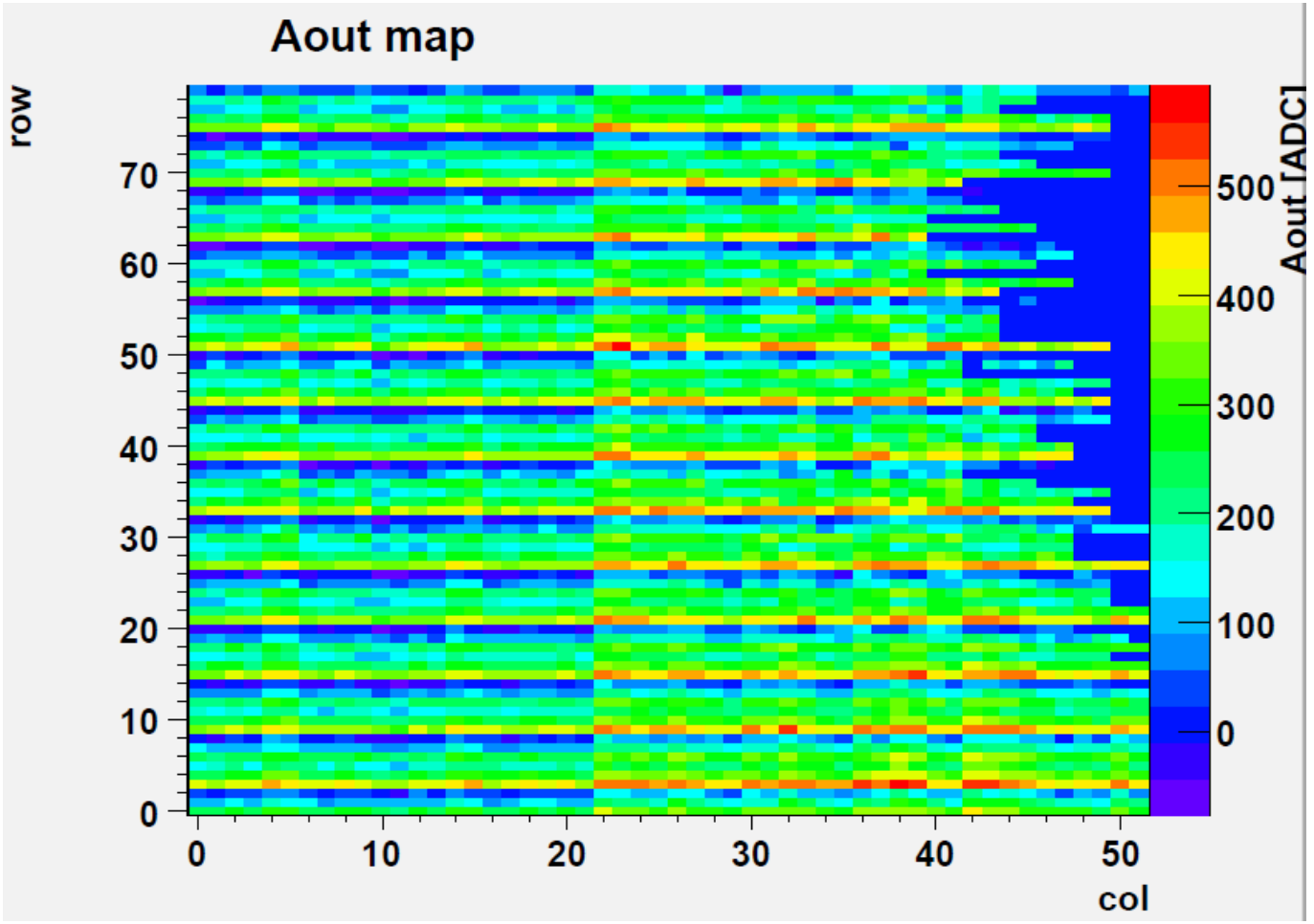
- Enable rows for each double column a count pixels
- Expect one pixel per activated row – until the data buffer is filled
- Up to 79 data bufferes for each double column are filled – OK!
- WBC > 160
- 2 BC/pixel

Pixel PH map xdb1 (15/06/2012)



- 52 × 80 = 4160 pixel per chip.
- Vcal = 255 DAC
- VthrComp = 72
- CtrlReg 4
- Strong pulse height variation

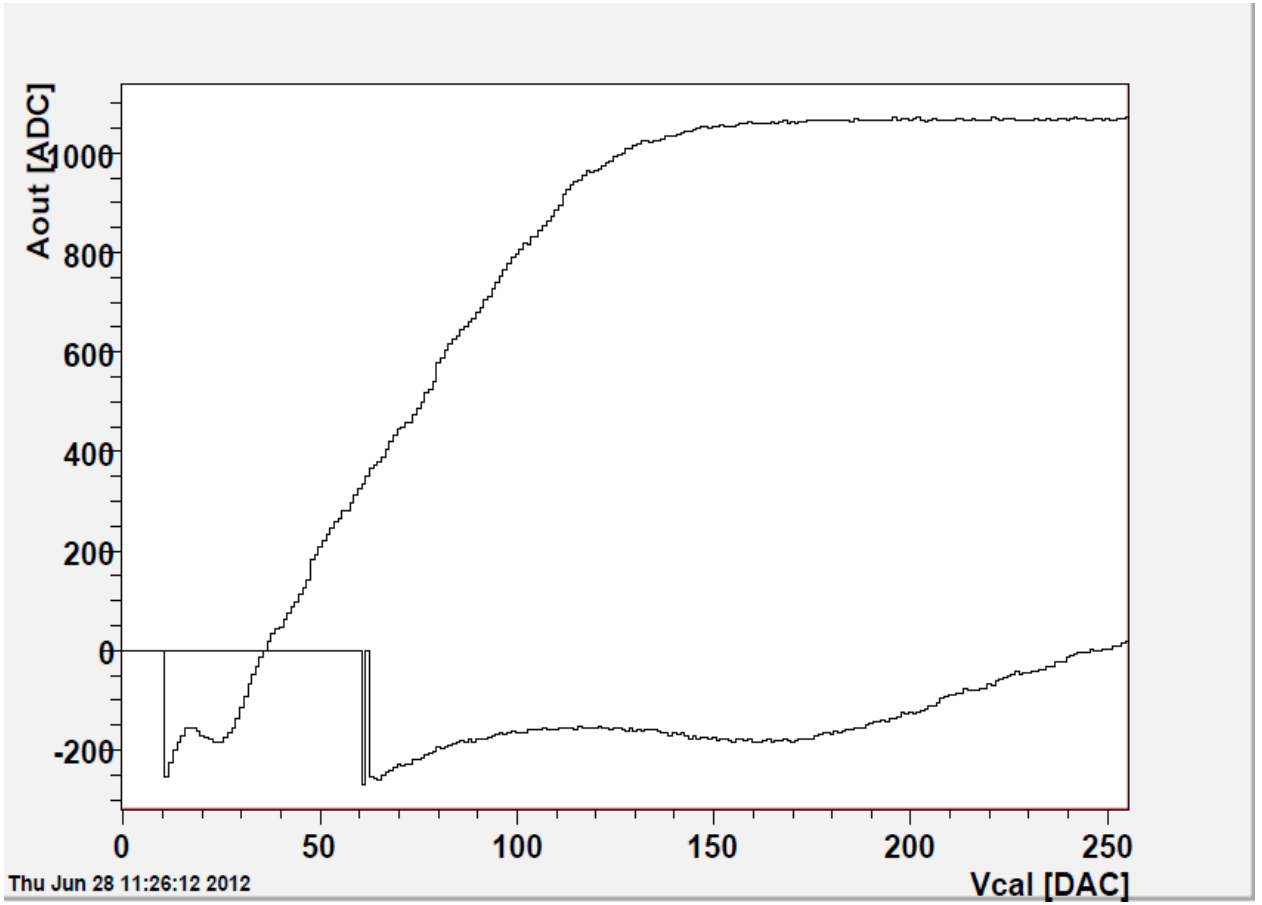
Pixel PH map xdb2



- 52 × 80 = 4160 pixel per chip.
- Vcal = 255 DAC
- VthrComp = 82
- CtrlReg 0
- Strong pulse height variation

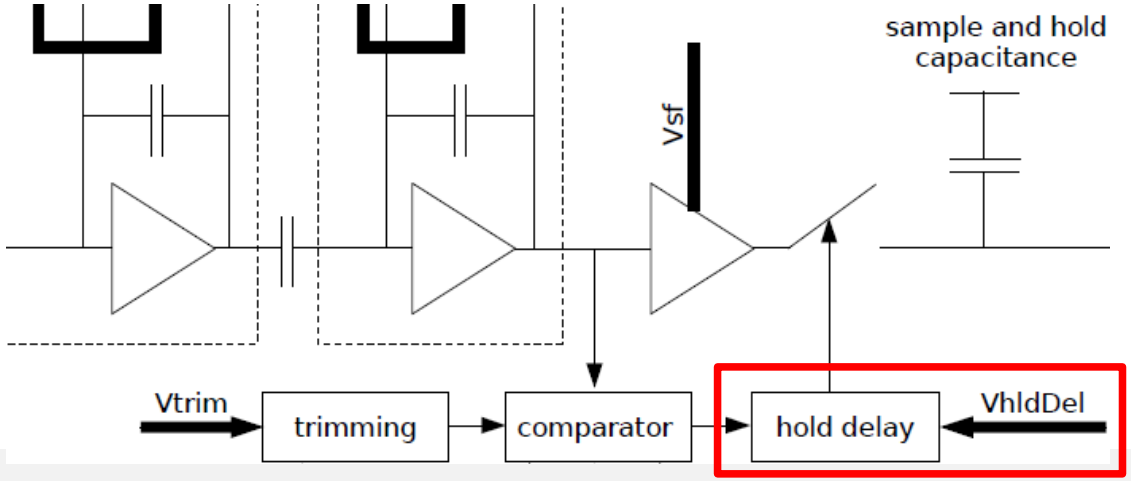
Gain and linear range xdb2

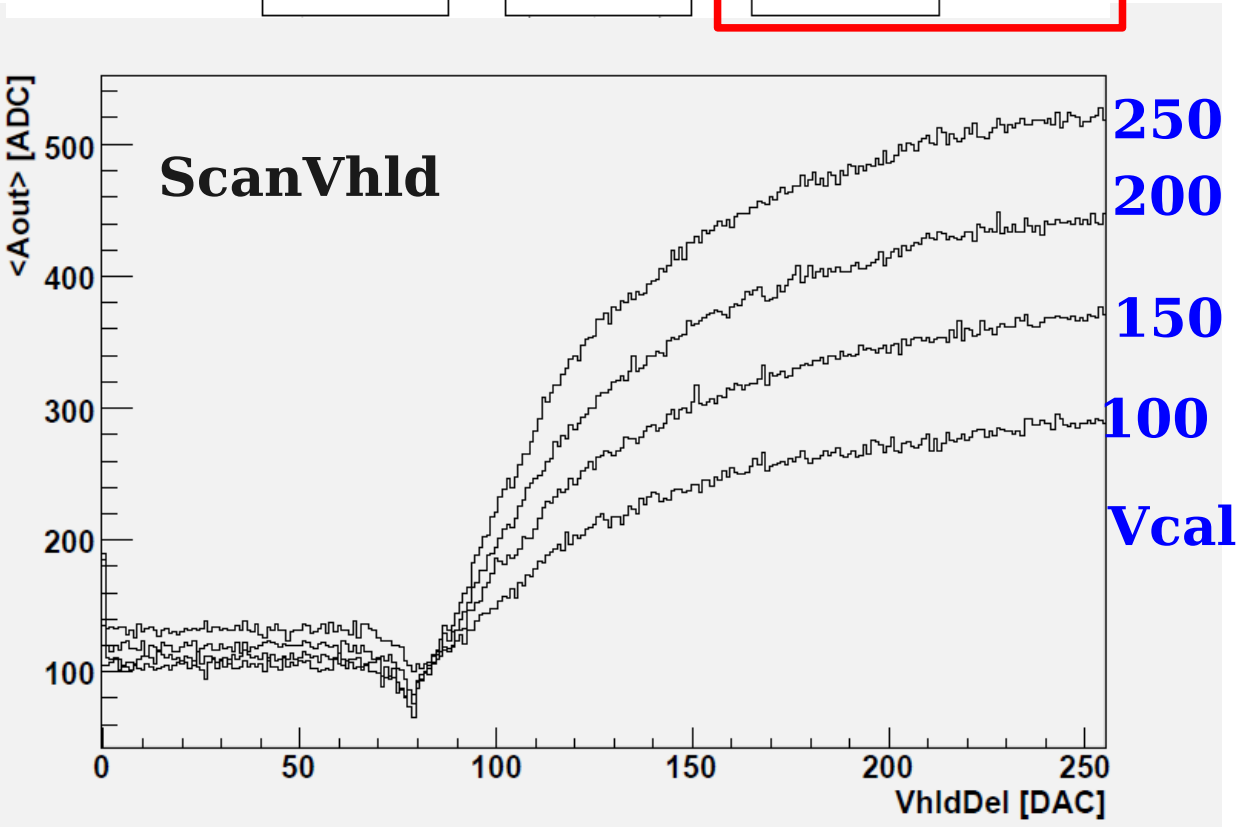
ScanVcal, pixel 2 2



- One pixel.
- 2 Vcal ranges:
  - CtrlReg 0 or 4,
- 42(47) e/DAC for small Vcal. ETH: Mo, Ag, Sn, Ba targets
- Saturation at higher Vcal and non-linearity at small Vcal
- Trimming was done for CtrlReg 0

Sample and hold timing xdb2





- One pixel.
- Position of maximum is at VhldDel=255

Summary

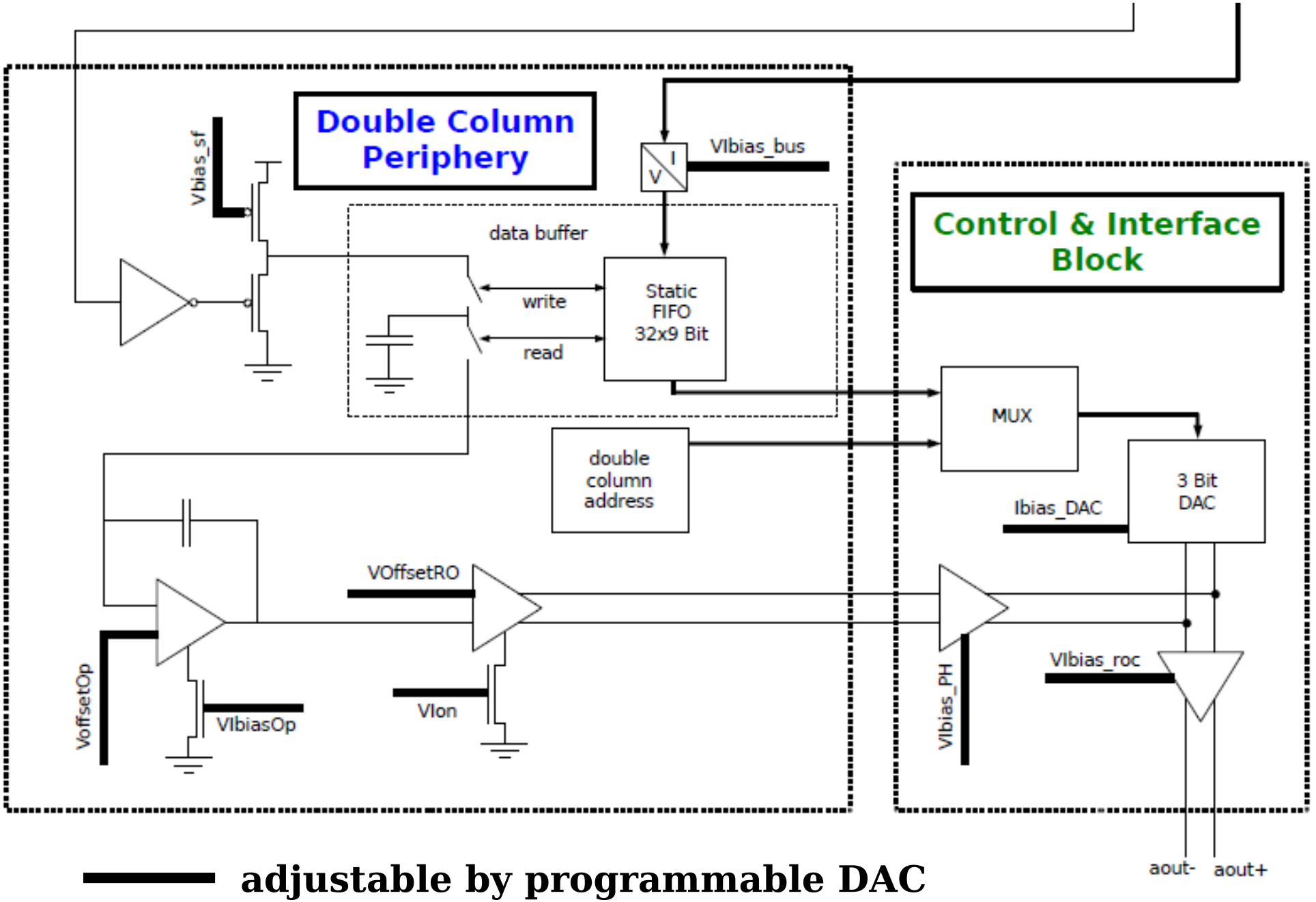
- New xdb chip reacts to bias Voltage. DACs can be programmed
- Pretest and Trimming procedure works
- PixelMap shows strong variation between left and right halves of the ROC (first 26 vs last 26 columns)
- Max of VhldDel distribution is at 255
- Up to 79 data buffers for each dcolumn can be filled
- Strong Pulse height variation in Aout map

Plans

- Run a Time Walk test
- Modify a Bump Bonding test
- Improve PH linearity
- Continue with a test beam for the next 2 weeks

Back up

psi46 pixel readout chip



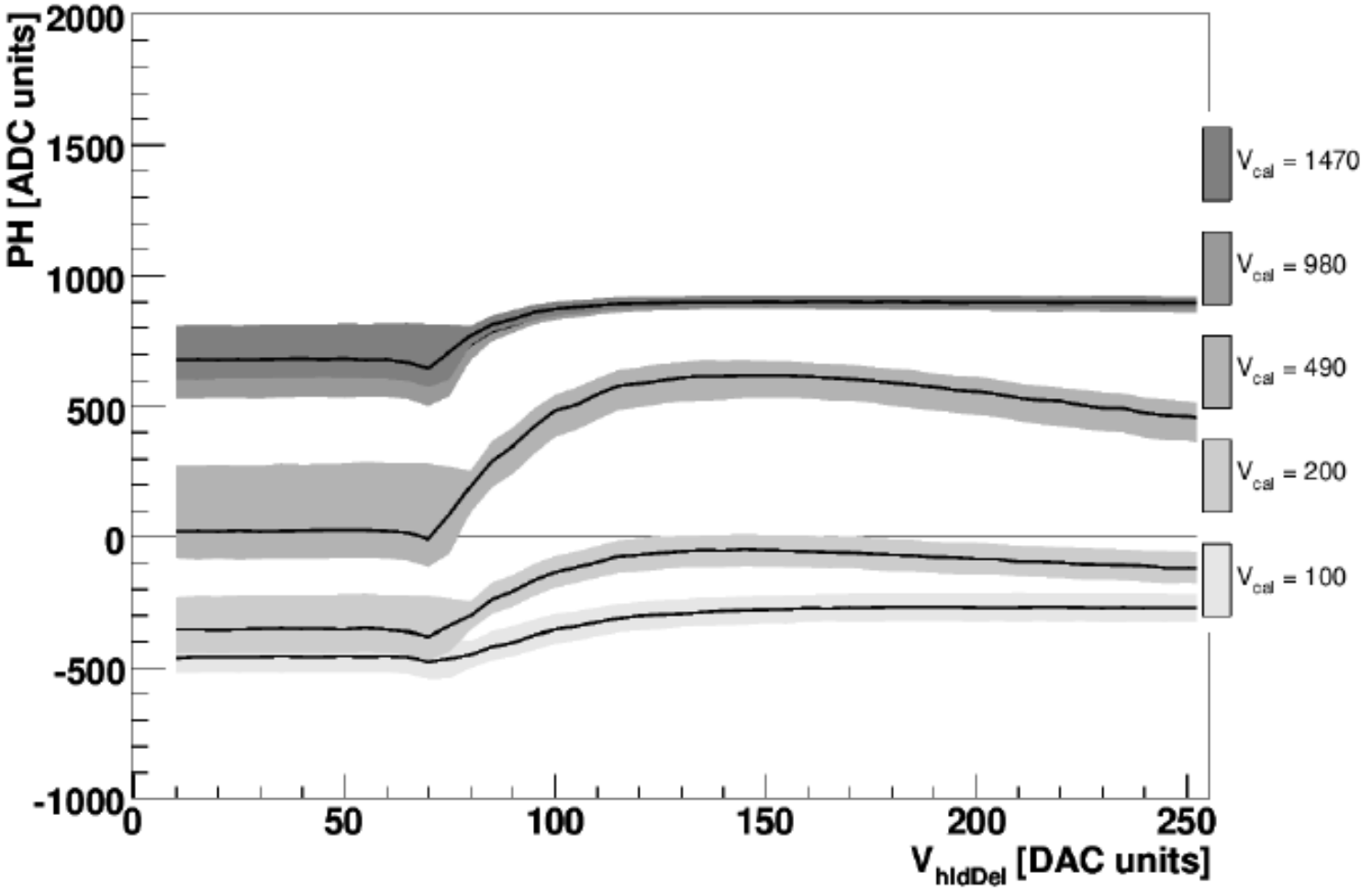
adjustable by programmable DAC

psi46 DACs

1	Vdig	6
2	Vana	150
3	Vsf	160
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	130
11	Vtrim	7
12	VthrComp	124
253	CtrlReg	0
254	WBC	20

13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	55
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	115
19	VIbias_PH	130
20	Ibias_DAC	122
21	VIbias_roc	220
22	VIColOr	100
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	125
27	RangeTemp	0

Sample and hold timing at PSI

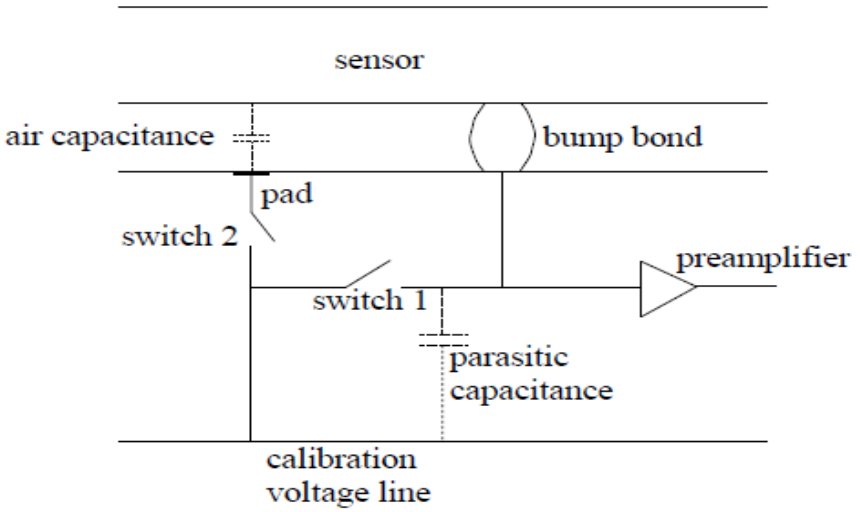


- Similar observations
- Somewhat different working point.

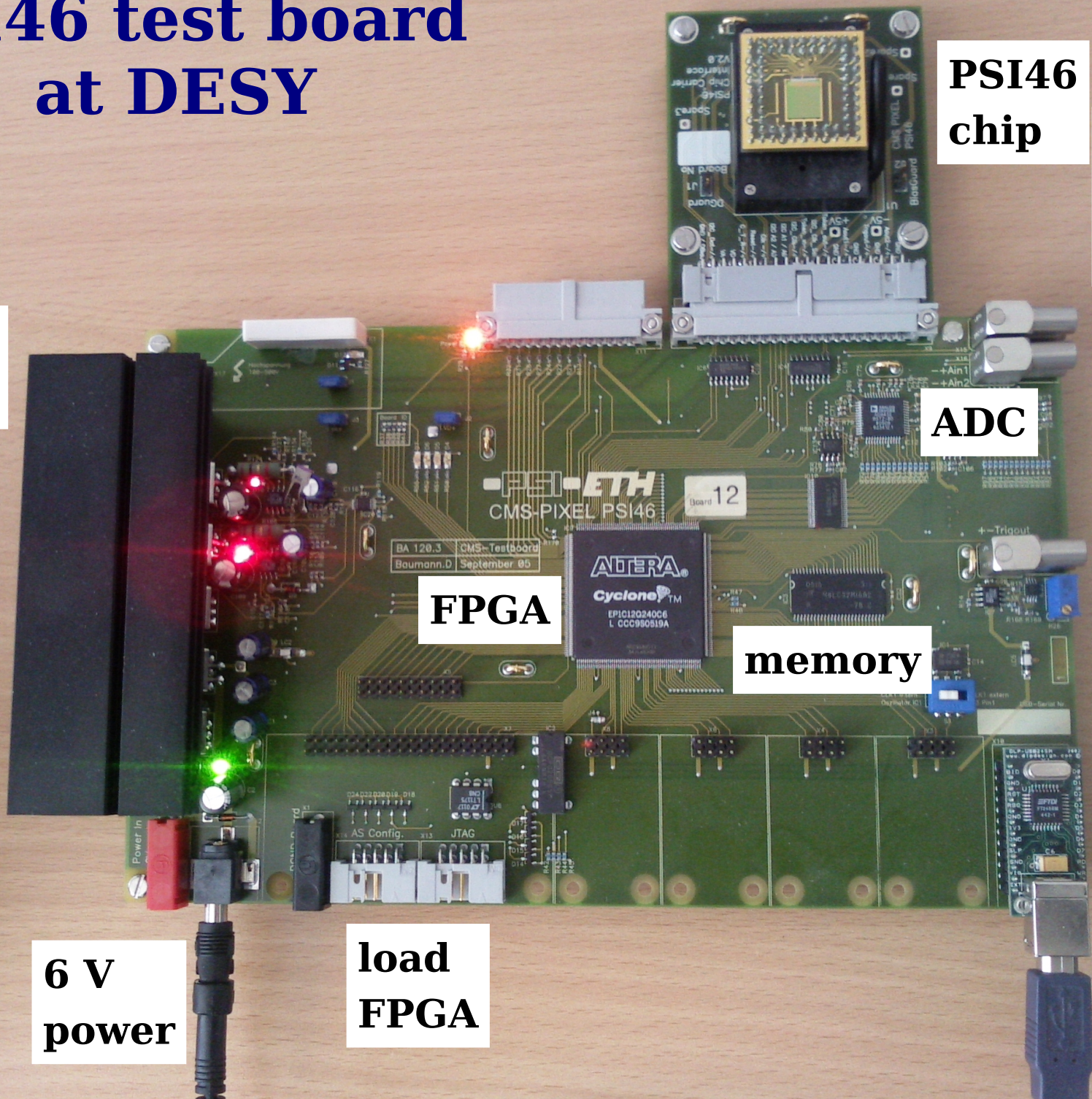
S. Dambach, ETH phd 2009

Bump Bonding Test Procedure

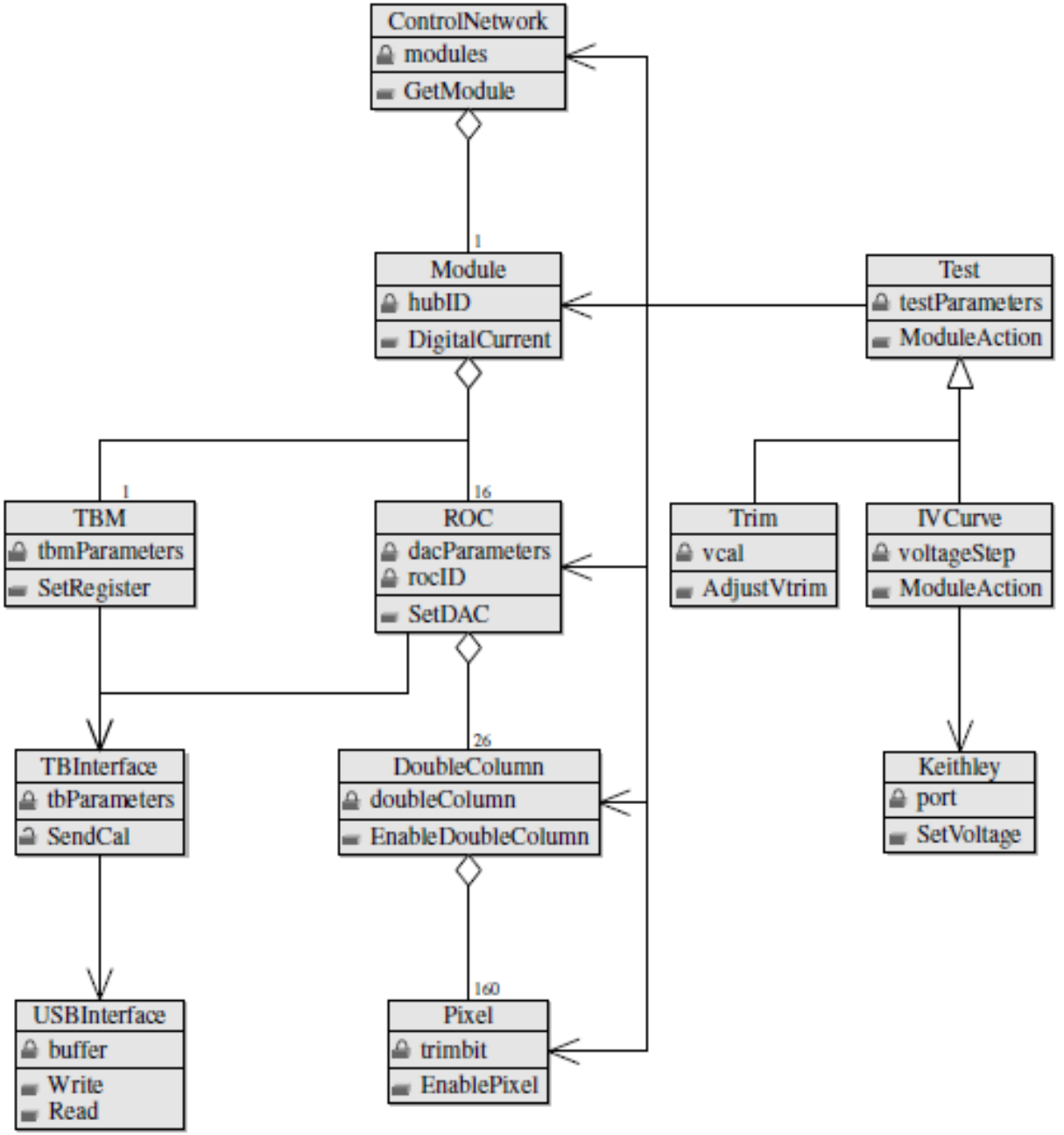
- Vcal to switch 2 induces a signal in sensor. If bump bond (bb) is present it is seen by preamplifier: missing bb can be identified
- Problem: cross-talk via a parasitic coupling between the calibration voltage line and preamplifier can fake a signal even without bb
- Determine Vcal_Thr2 for the signal injection through the sensor
- Measure Vcal_Thr1 for the parasitic cross-talk (with both switches open)
- |Vcal_Thr1 – Vcal_Thr2| < 5 DAC units → defect bump bonding



PSI46 test board at DESY



psi46expert software



- C++ class library.
- Written by Peter Trüb (ETH, 2005-2007) for Scientific Linux (32 bit).
- Now compiled with g++ 4.4.5 under Ubuntu 10.10 (64 bit).
- USB interface required some changes (long → int).
- All tests were working properly with old ROC