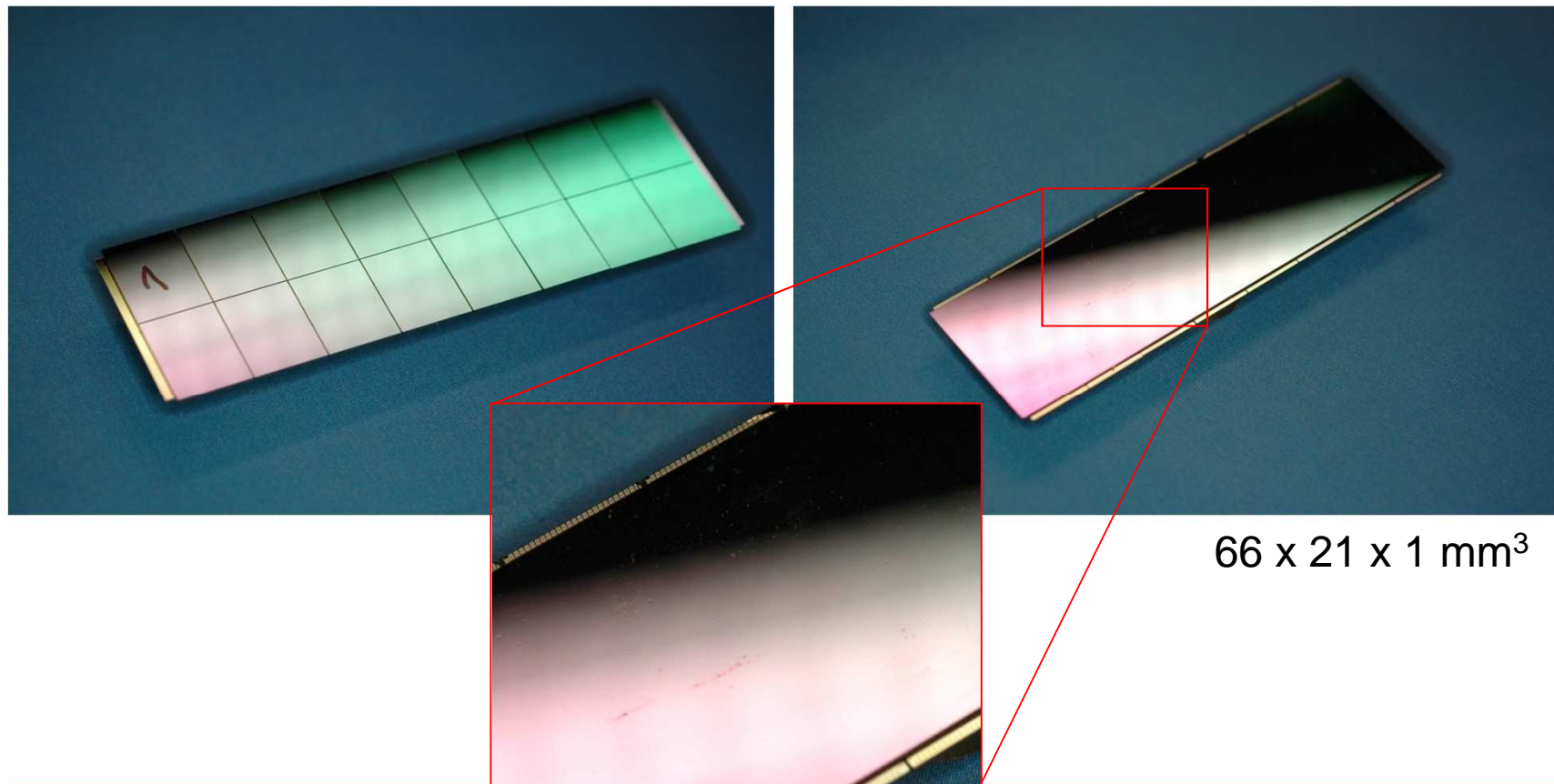


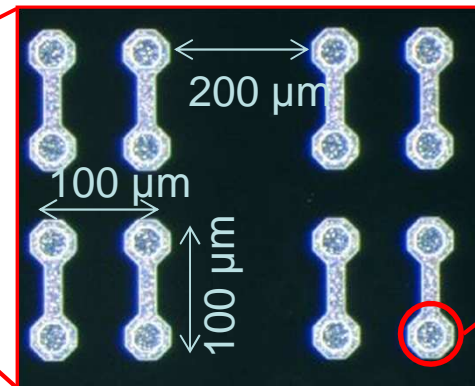
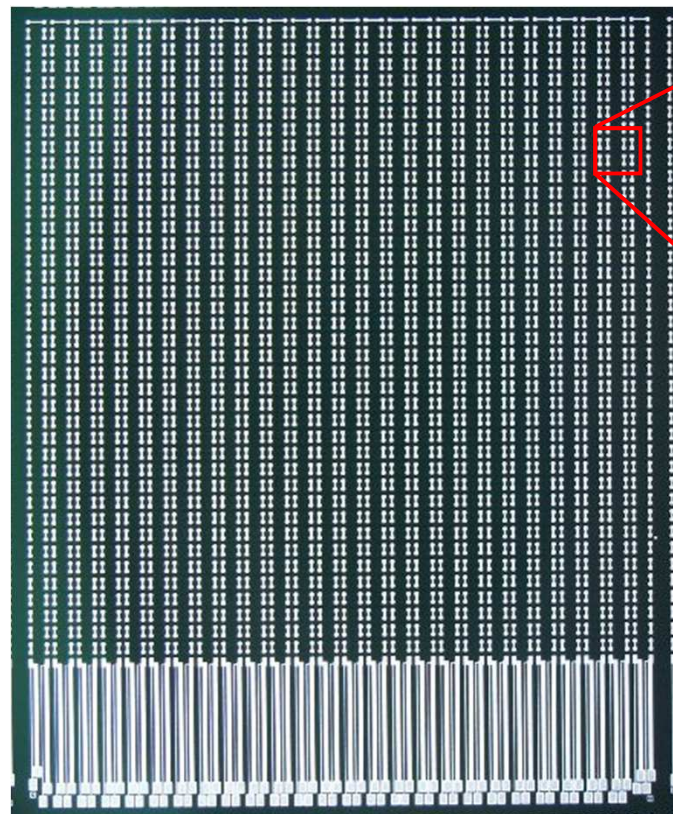
CMS BPIX dummy modules for in-house Flip-Chip technology tests

PICTURES OF A FABRICATED DUMMY MODULE



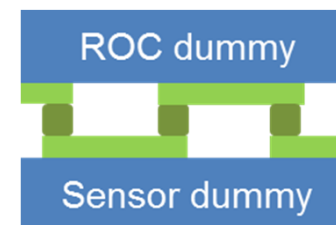
Dummies mimic the crucial parts for bump bonding of the CMS pixel sensors and ROCs

MICROGRAPH OF ONE CHIP AND ZOOM TO DAISY CHAIN PADS



Copy of the CMS contact pad and its pitch

Pad pitch = 100 μm / 200 μm
Pad metal = 50 μm
Passivation opening = 30 μm

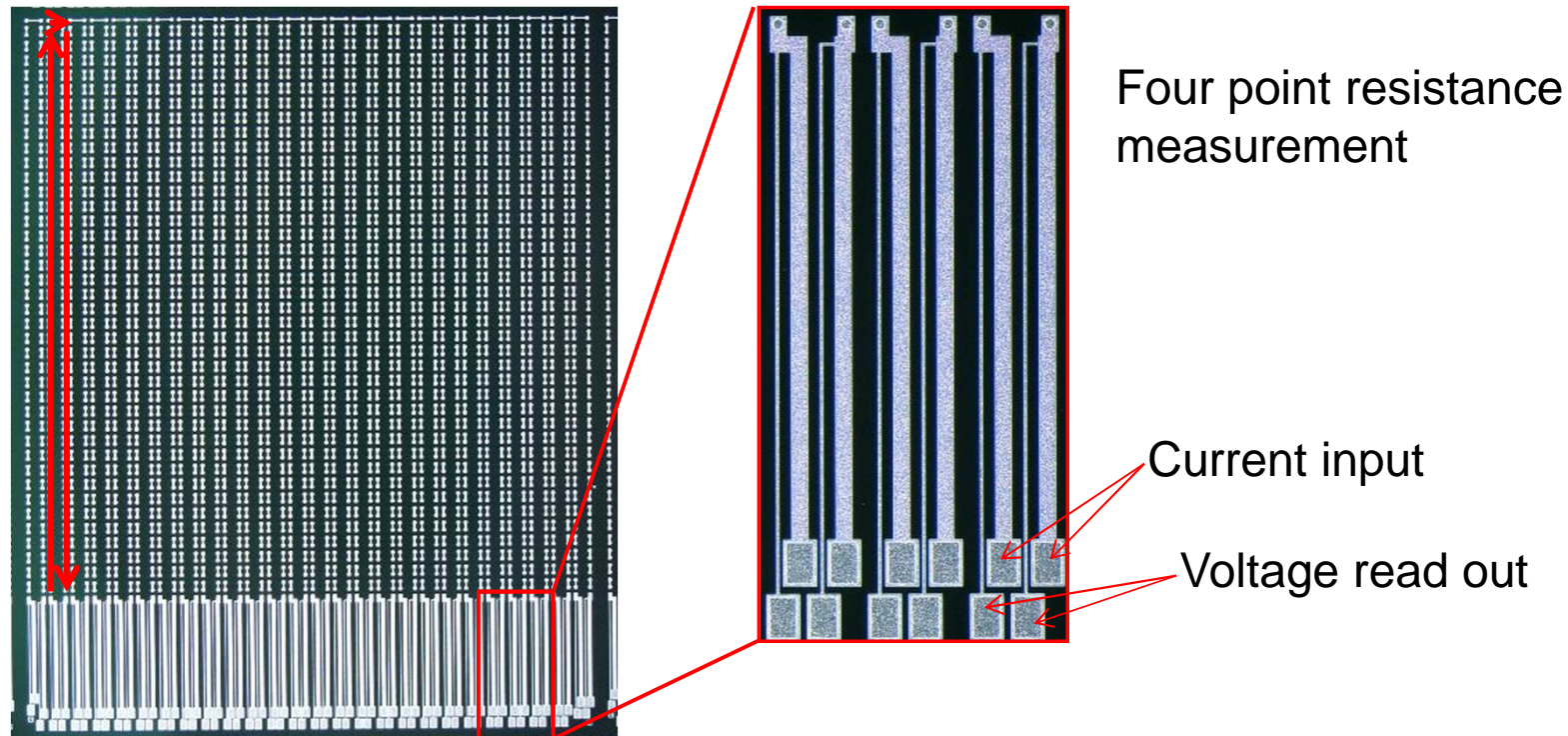


4160 contacts per chip
26 double columns per chip
66560 per substrate

- daisy chain pad structure for tests
- sensor provides the missing pieces of the electrical path to the ROC

26 daisy chains (comparable to double columns) per chip are resistance measured

MICROGRAPH OF ONE CHIP AND ZOOM TO CONNECTOR PADS



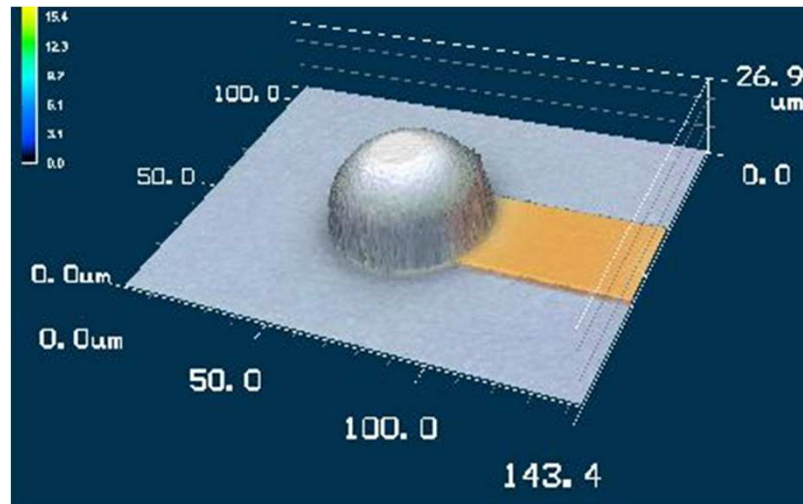
Chain resistance comprises

- metal path between the pads
- 160 bumps per chain

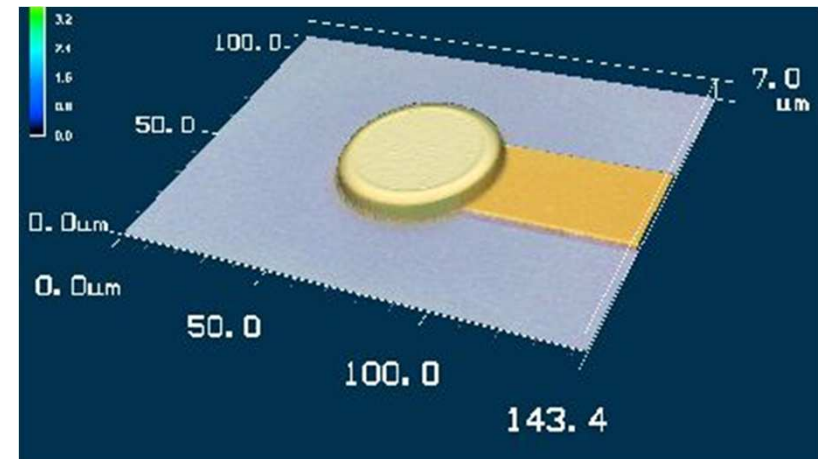
One „dead pixel“ → open circuit

UBM and solder is deposited on each pad

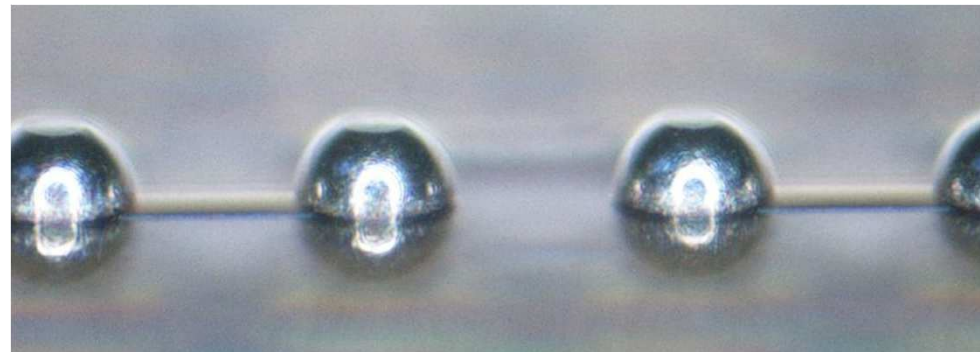
LASER SCAN AND OPTICAL MICROSCOPE PICTURES



Pad bumped with 40 μm solder ball



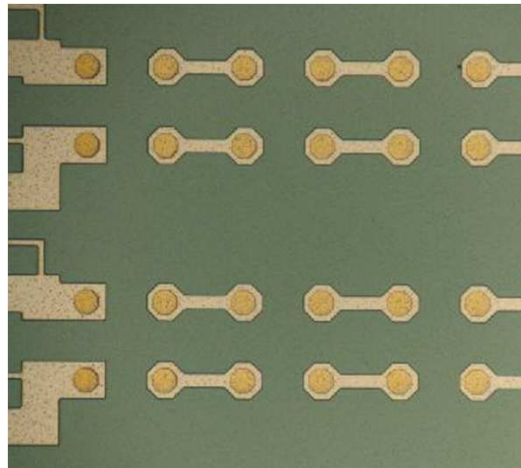
Pad with processed UBM



Side view of bumped daisy chain structure on chip

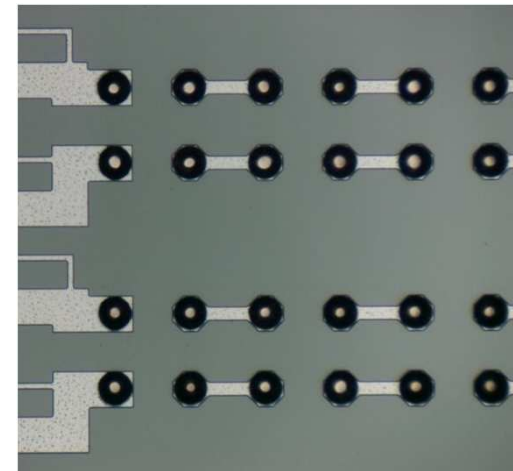
First soldering tests with the Pac Tech SB² solderball jet have been successful

MICROGRAPHS OF DUMMY-ROC



Dummy-ROC with UBM

ENEPIG UBM:
40 μm diameter
5 μm Ni (layer)
200 nm Pd (layer)
50 nm Au (layer)

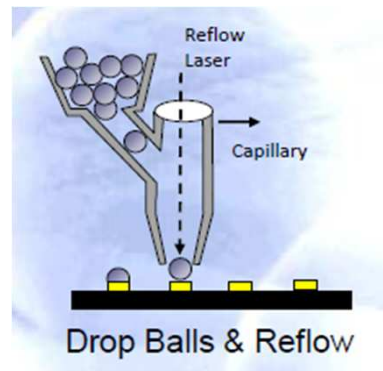


Dummy-ROC after solder placement

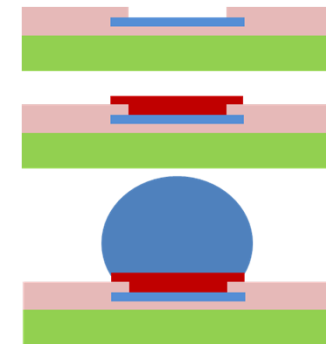
SAC solder:
Sn 96.5%_{wt}
Ag 3%_{wt}
Cu 0.5%_{wt}



UBM at Pac Tech



SB² Jet
(to be
purchased)

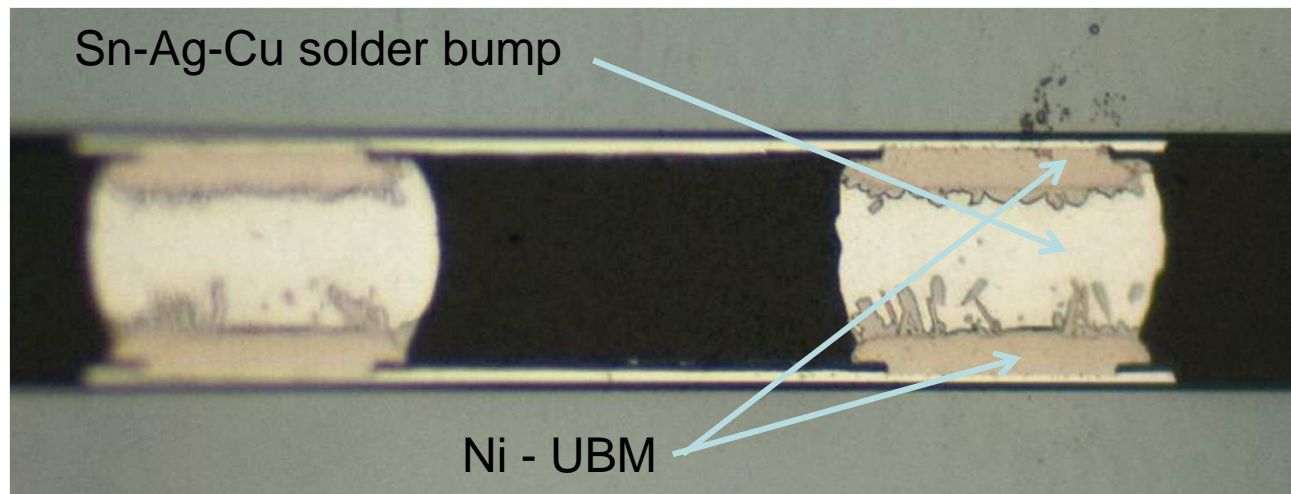


Older tests already showed fine bump bond connections

CROSS SECTIONAL VIEWS TO BONDED DUMMY ROCS



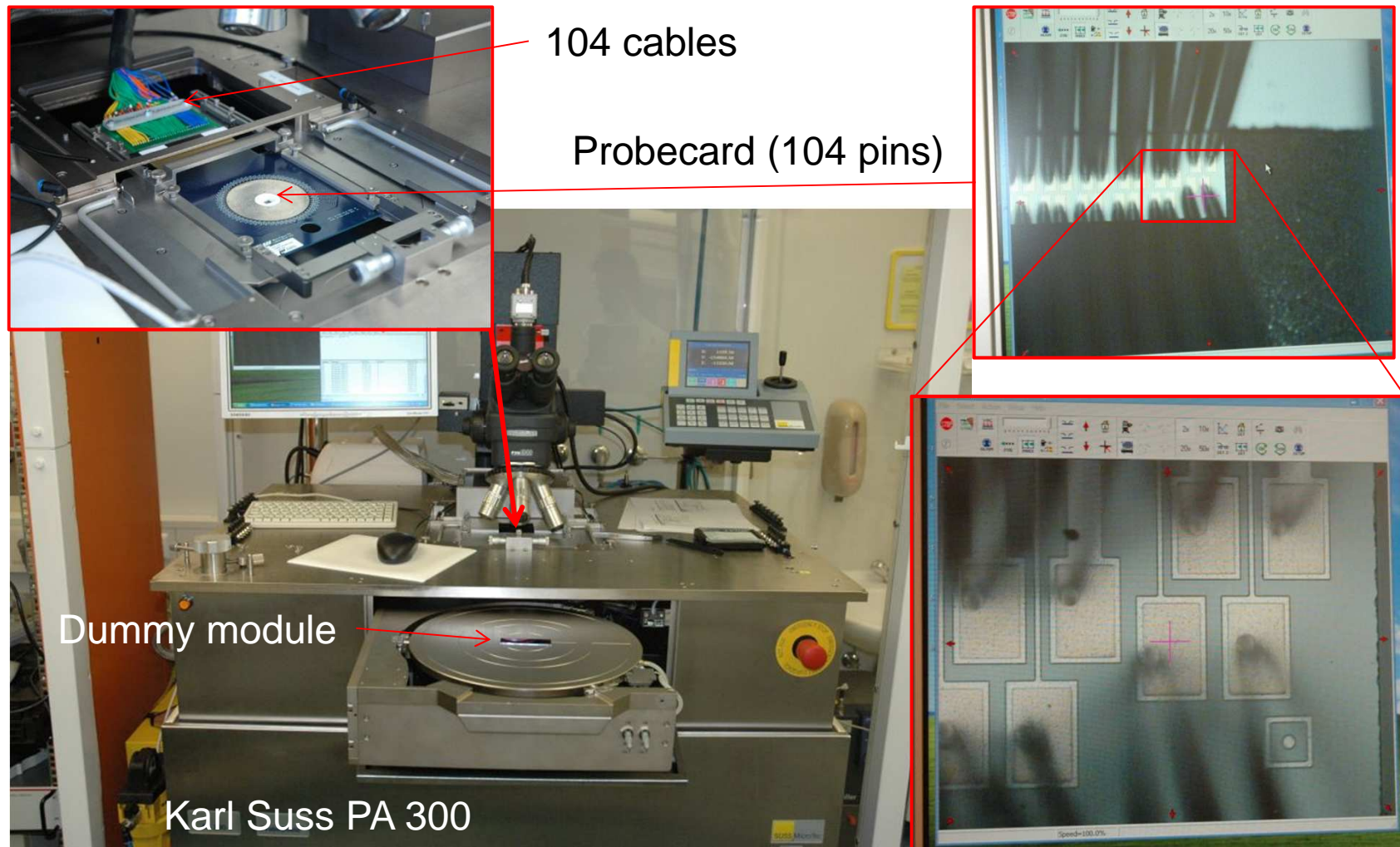
First ROC to
ROC bond
test cross
sections



40 μm diameter
25 - 30 μm height
4160 per chip
80 per column

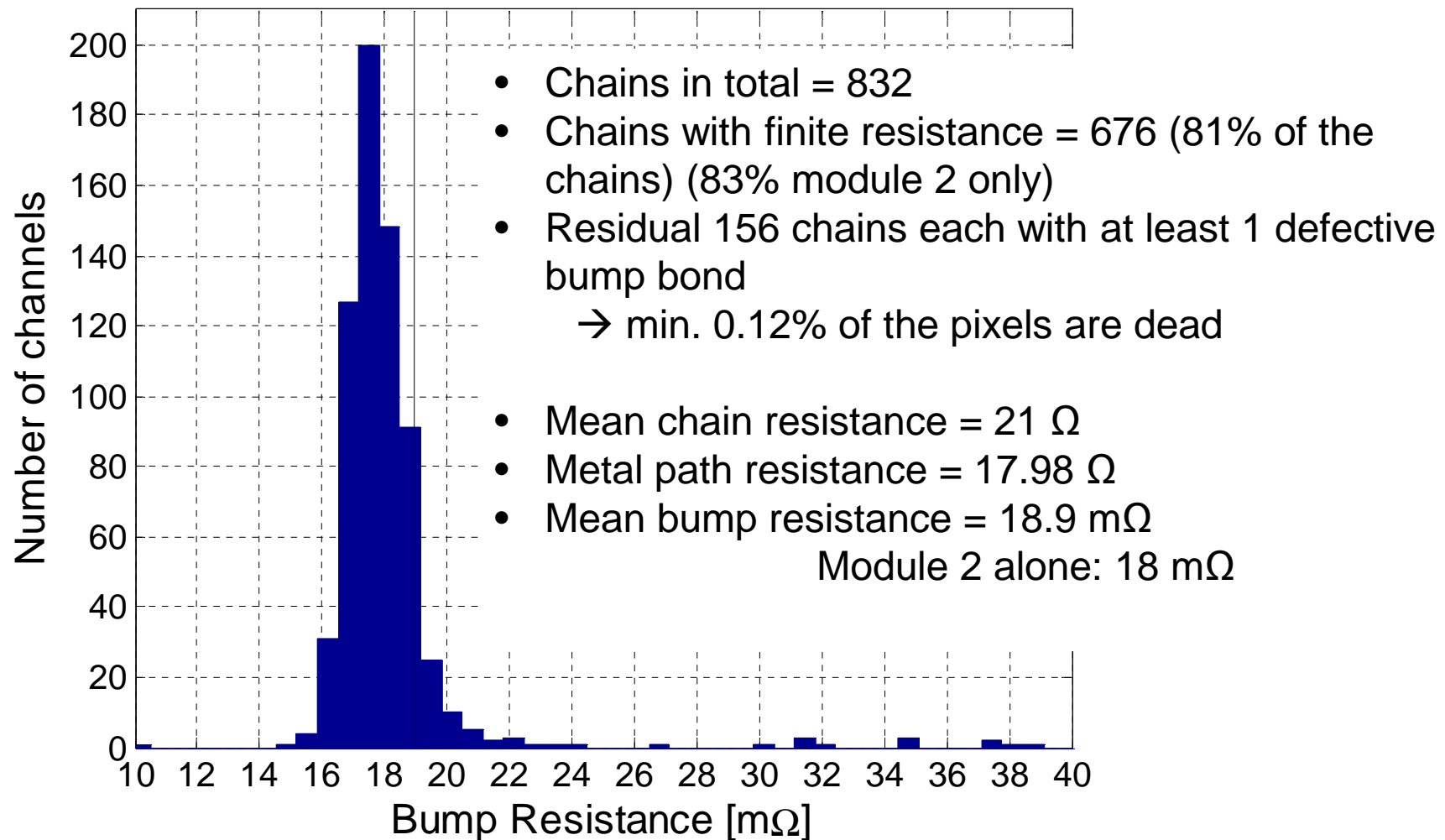
Dummy ROCs are contacted with a probecard according to their 104 pads each

PICTURES FROM THE PROBING STEPS



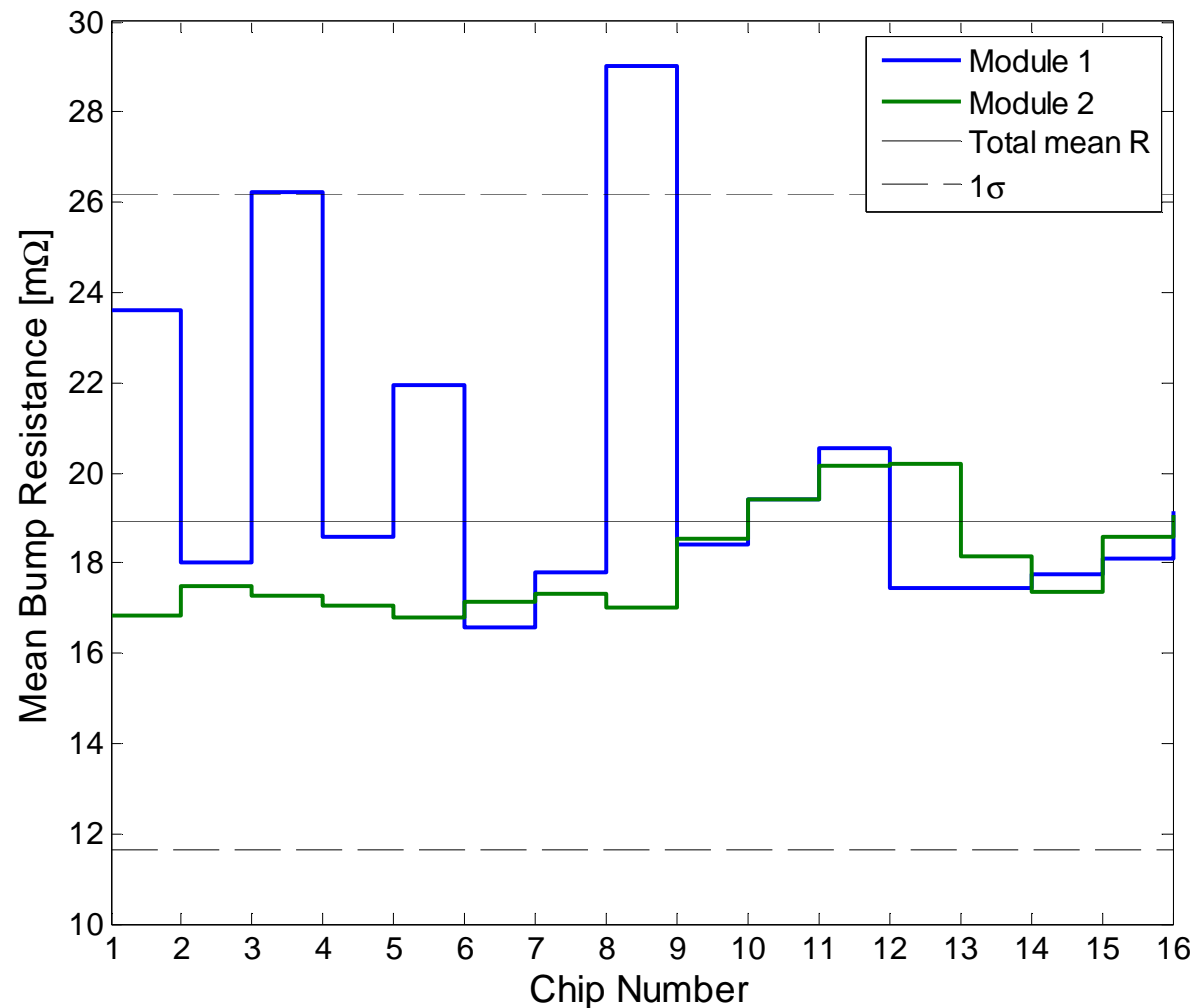
Bump resistance is around 18.9 mΩ

FEMTO TEST-JUNE2012-MODULE 1 + 2, HISTOGRAM



Low variance of mean bump resistance per chip

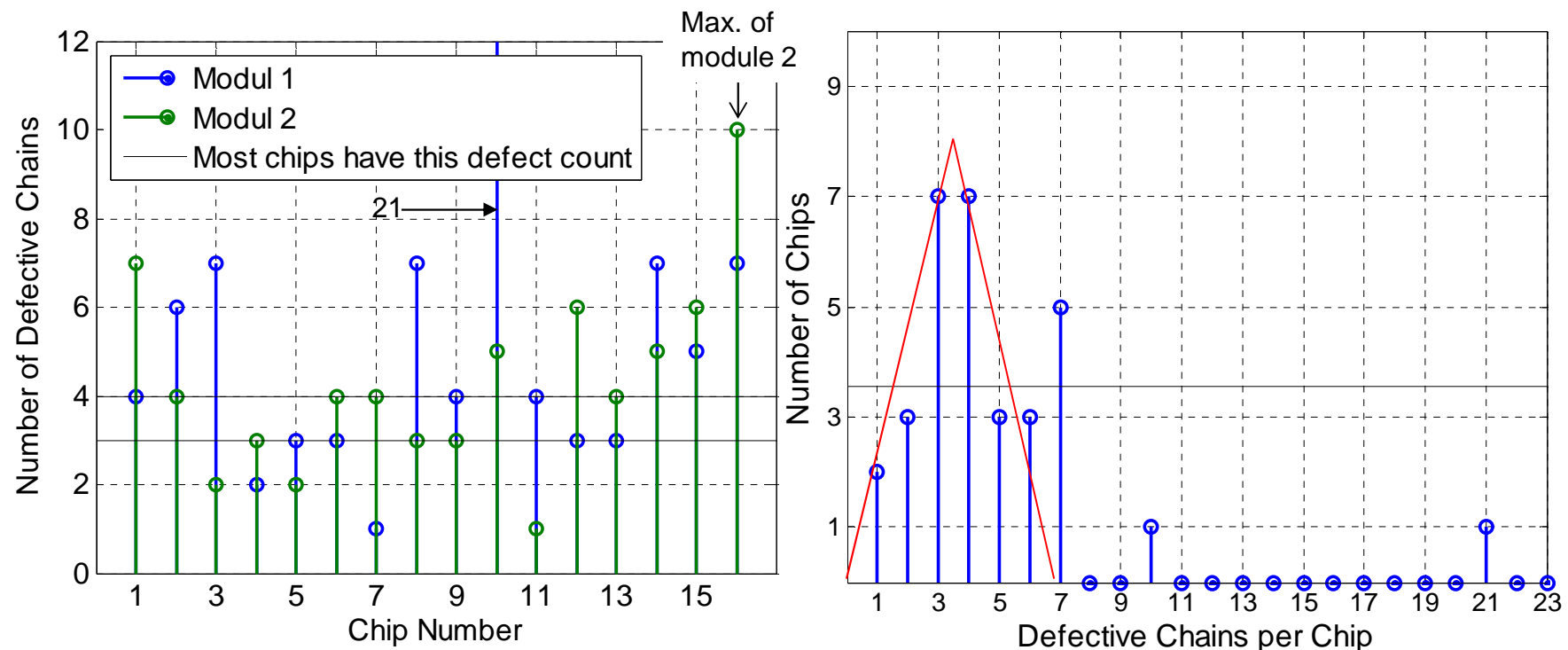
FEMTO TEST-JUNE2012-MODULE 1 + 2, BUMP RESISTANCE PER CHIP



First 8 chip areas of module 1 have been used in several attempts to find correct bonding parameter

The defect rate of 4 chains per chip (min. 0.1% dead pixels) is found for most of the chips

FEMTO TEST-JUNE2012-MODULE 1 + 2, DEFECT STATISTICS

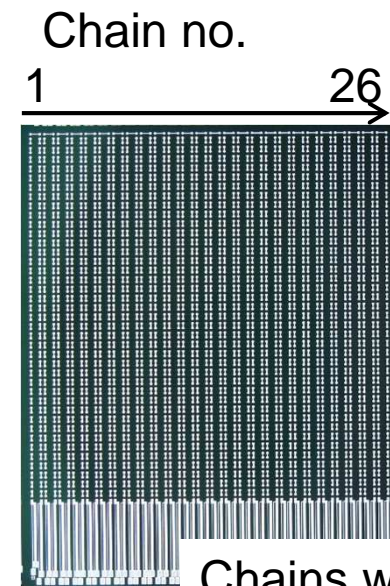
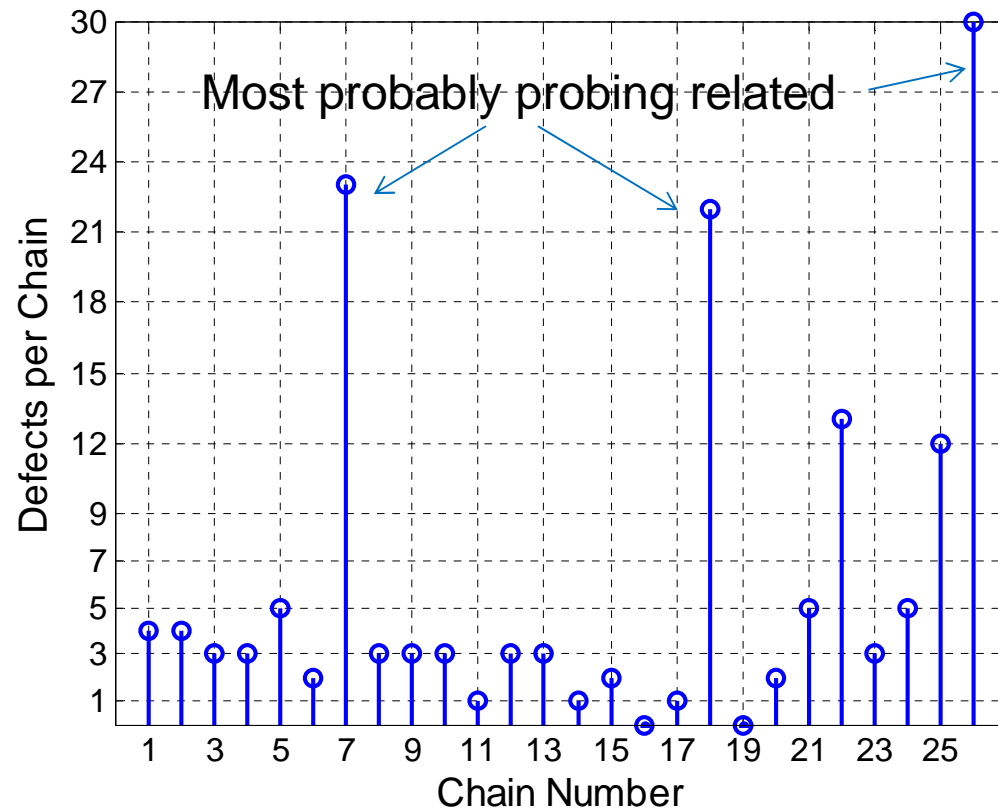


- Max. number of defects = 21 (1 Chip)
- Min. number of defects = 1 (2 Chip)
- Most chips (7 each) have 4 or 3 defects
- 13 chips with more defects
- 5 chips with less defects

Distribution around 4 defects per chip \rightarrow 0.1%

Spatial defect distribution may indicate small misleveled bonding

FEMTO TEST-JUNE2012-MODULE 1 + 2, NUMBER OF DEFECTS PER CHAIN

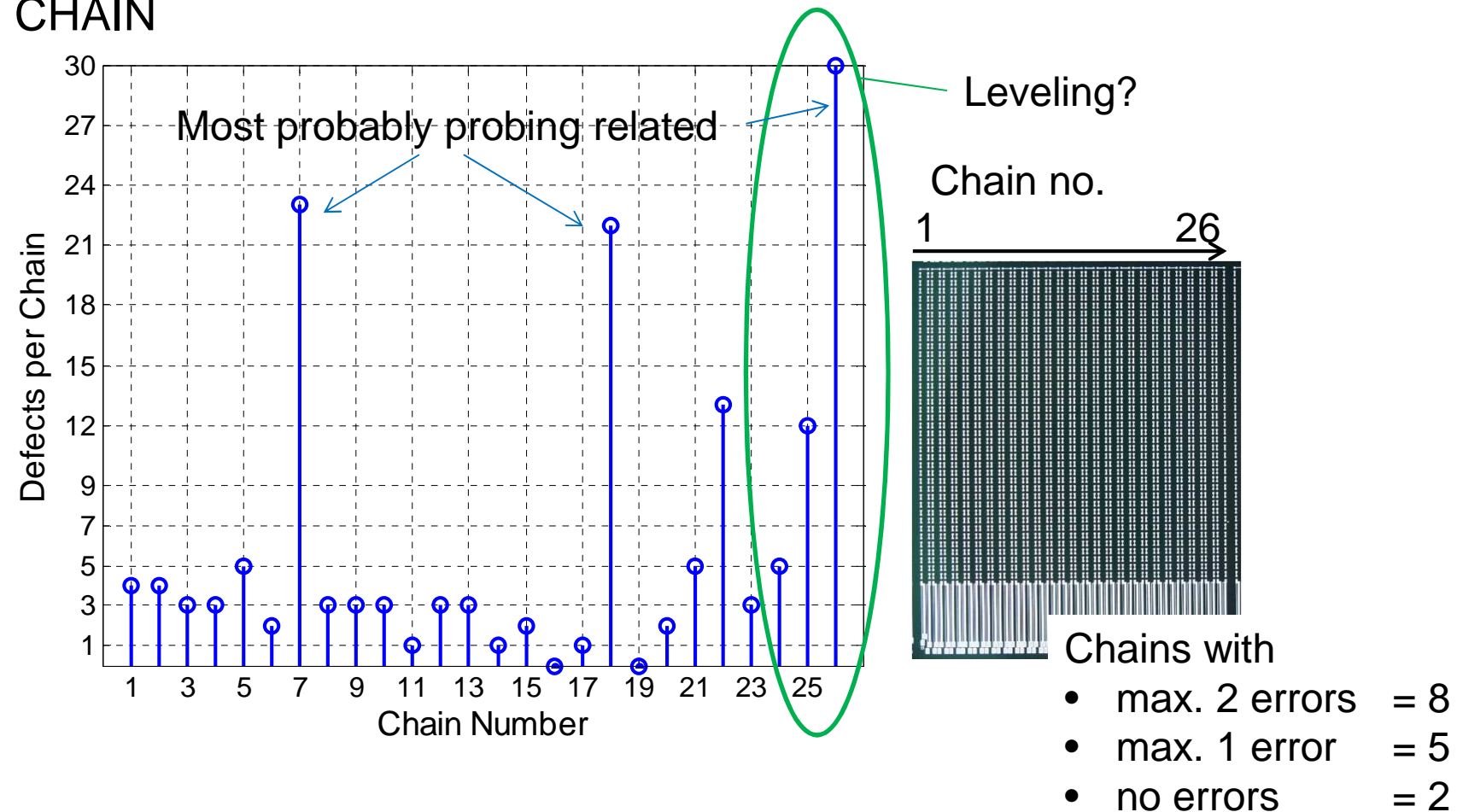


Chains with

- max. 2 errors = 8
- max. 1 error = 5
- no errors = 2

Spatial defect distribution may indicate small misleveled bonding

FEMTO TEST-JUNE2012-MODULE 1 + 2, NUMBER OF DEFECTS PER CHAIN



3D X-ray investigation (CT) of the latest module tests within the next 4 weeks