

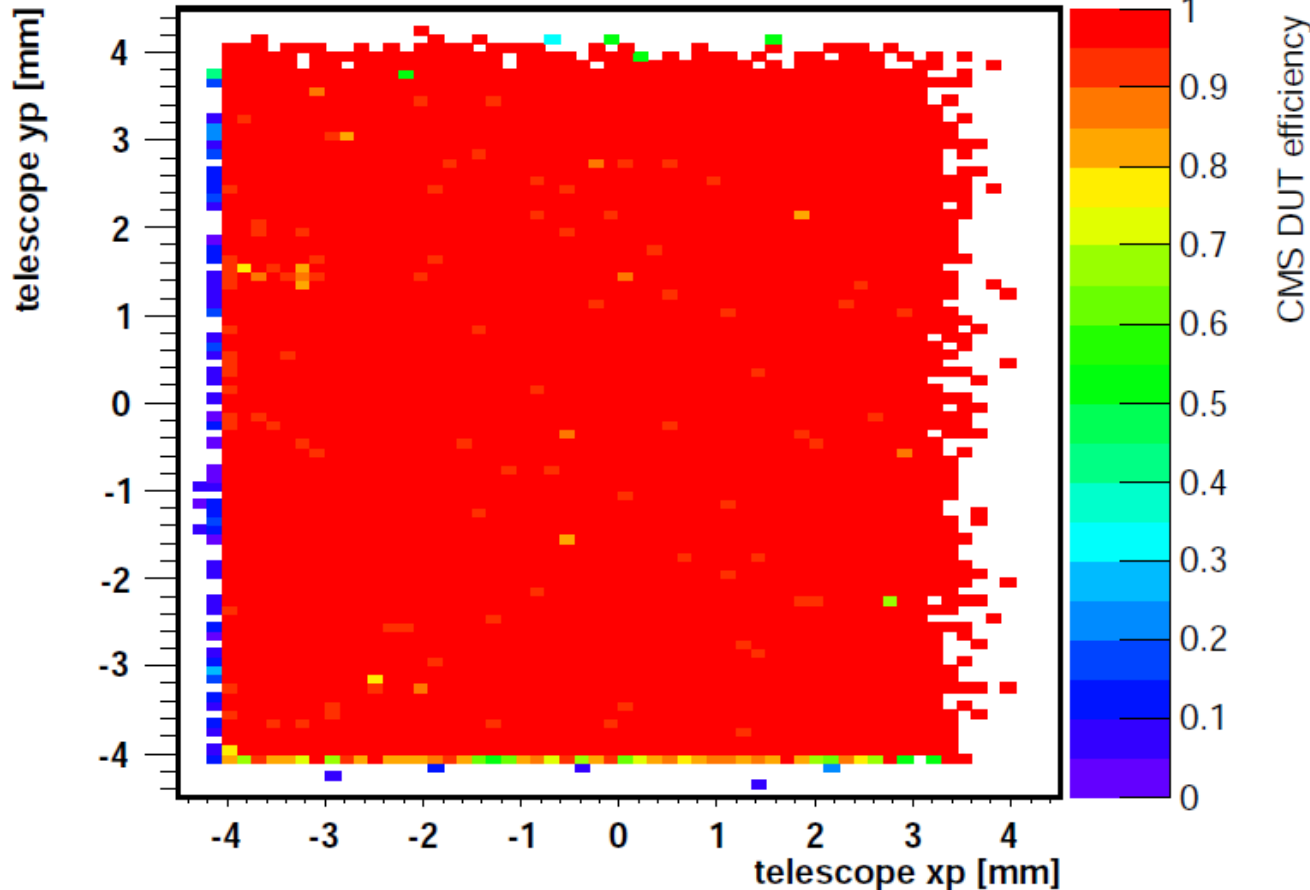
# PSI46xdb pixel chip in the DESY test beam: the first 3 days

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DESY CMS Phase I pixel upgrade, 29.6.2012

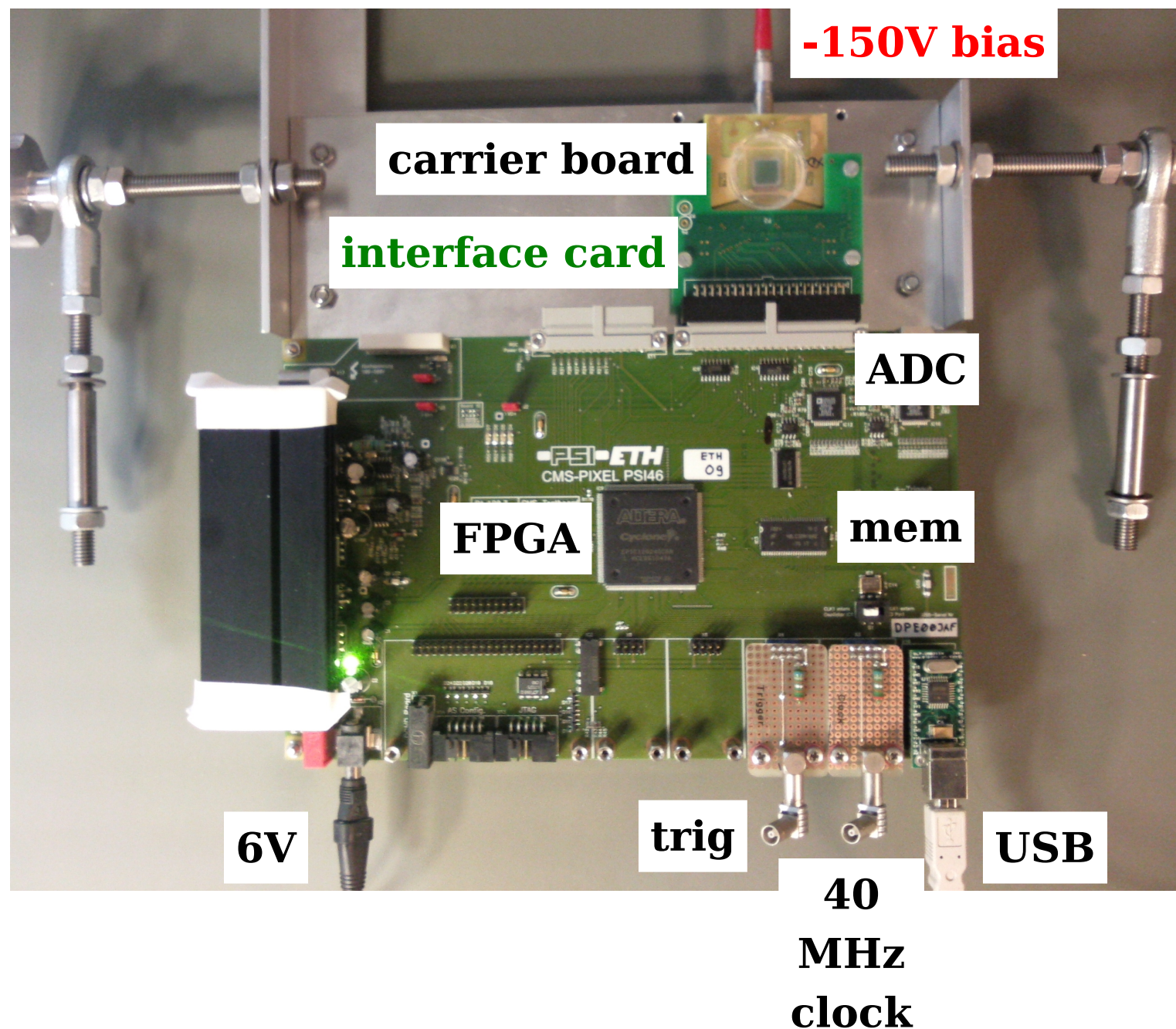
DUT efficiency

Entries 64389



- PSI46xdb
- setup and plan
- first results

# psi46xdb and test board at DESY



- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to test board
  - xdb 2 arrived 25.6.
- Use the same board, firmware, software as for psi46

# PSI46xdb

## Data Rate, Efficiency:

- Extended data buffer 32 → 80 cells
- Extended time stamp buffer 16 → 24

## Crosstalk, threshold uniformity:

- 6 metal layer (process option)
- Thick top metal (LM instead of MZ process option, +37%)
  - better power and ground distribution (lower resistance)
  - better threshold uniformity
- New routing for calibrate signal → less crosstalk of calibrate signal
- Better decoupling of comparator and digital voltage → less crosstalk
- Different other minor layout changes to reduce crosstalk

# PSI46xdb

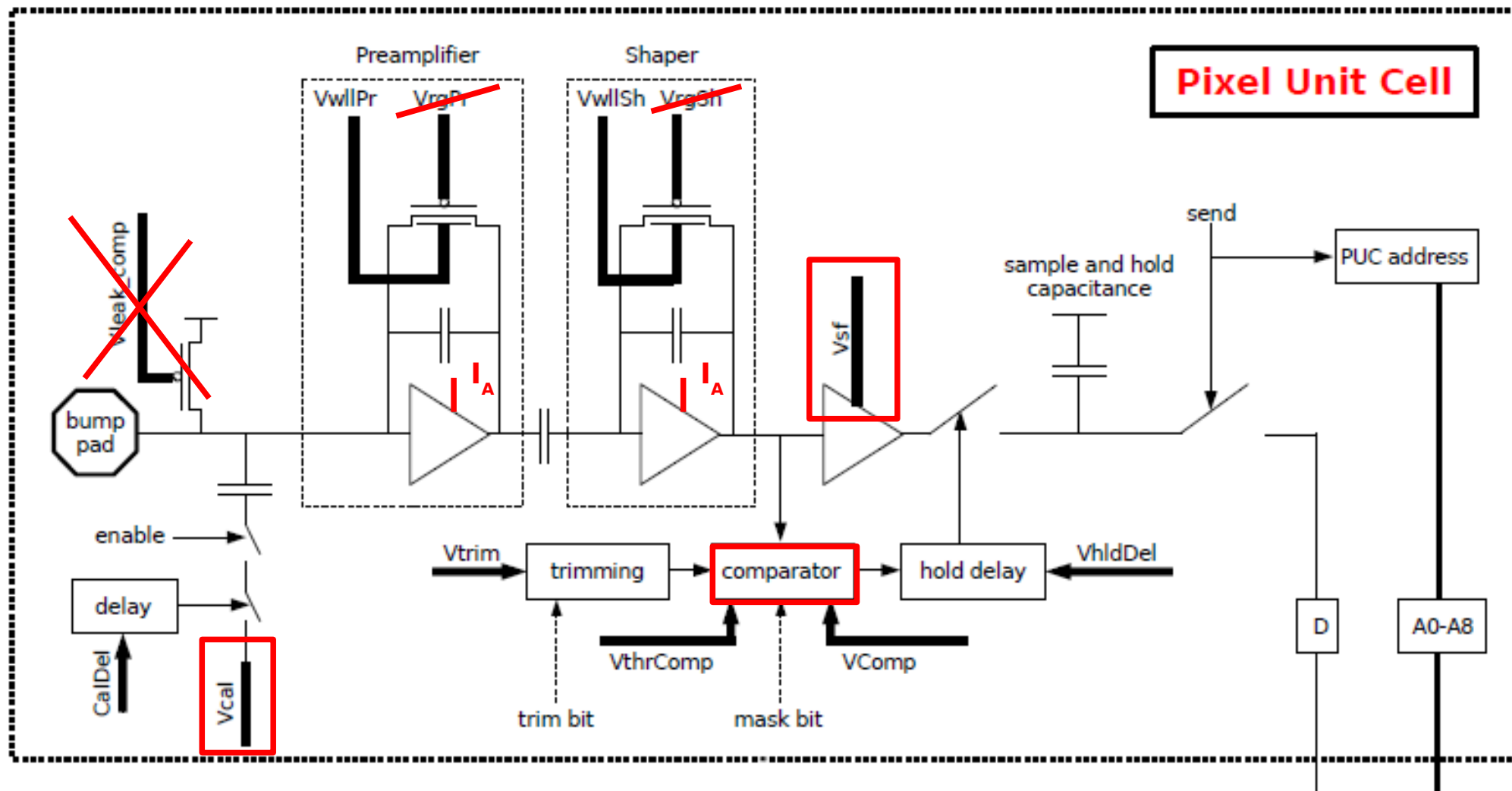
## DAC:

- 3 DACs removed: VRGPR, VRGSH and Vleakage
- All DAC's with power on reset for low power ROC configuration
- **Current control** instead of voltage control for **S&H and analog power supply** → easier and independent setup

## Timing:

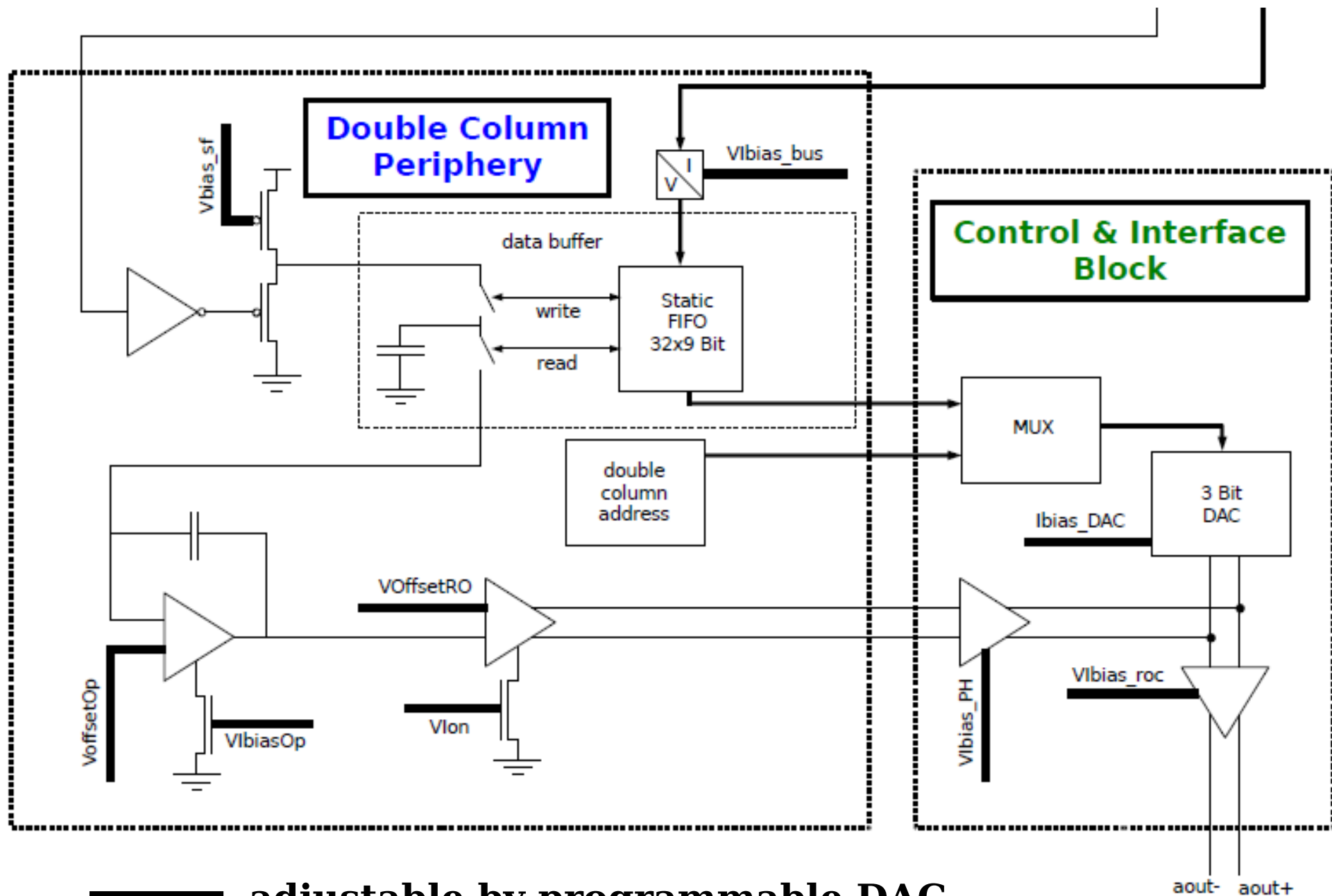
- Small performance optimization in column drain mechanism (timing)
- Modified comparator with **reduced timewalk**
- Same analog read out as PSI46 → **same test board**
- **Comparison possible between PSI46 and PSI46xdb**

# PSI46xdb pixel unit cell



  **modified in PSI46xdb**

# psi46 pixel readout chip



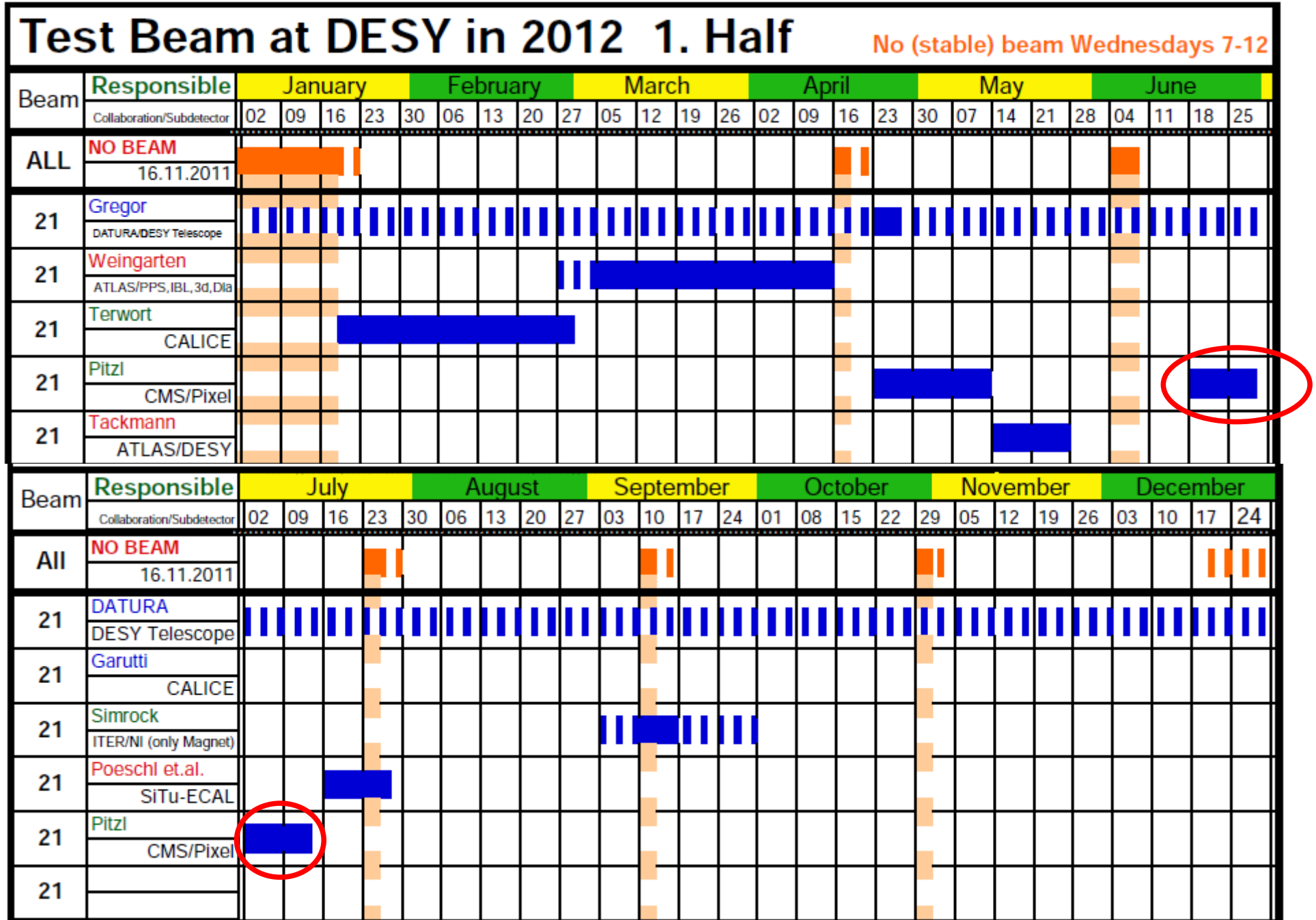
# psi46xdb DACs

|     |          |     |    |            |     |
|-----|----------|-----|----|------------|-----|
| 1   | Vdig     | 6   | 13 | VIBias_Bus | 30  |
| 2   | Vana     | 166 | 14 | Vbias_sf   | 10  |
| 3   | Vsf      | 30  | 15 | Voffset0p  | 57  |
| 4   | Vcomp    | 10  | 16 | VIbias0p   | 115 |
|     |          |     | 17 | V0ffsetR0  | 120 |
|     |          |     | 18 | VIon       | 115 |
| 7   | VwllPr   | 60  | 19 | VIbias_PH  | 130 |
|     |          |     | 20 | Ibias_DAC  | 83  |
| 9   | VwllSh   | 60  | 21 | VIbias_roc | 190 |
| 10  | VhldDel  | 250 |    |            |     |
|     |          |     | 25 | Vcal       | 200 |
| 11  | Vtrim    | 130 | 26 | CalDel     | 155 |
| 12  | VthrComp | 74  | 27 | RangeTemp  | 0   |
|     |          |     |    |            |     |
| 253 | Ctr1Reg  | 0   |    |            |     |
| 254 | WBC      | 20  |    |            |     |

# CMS Pixel in the DESY test beam

<http://adweb.desy.de/~testbeam/>

29.05.2012



# CMS pixel planes in the telescope

3 planes  
downstream

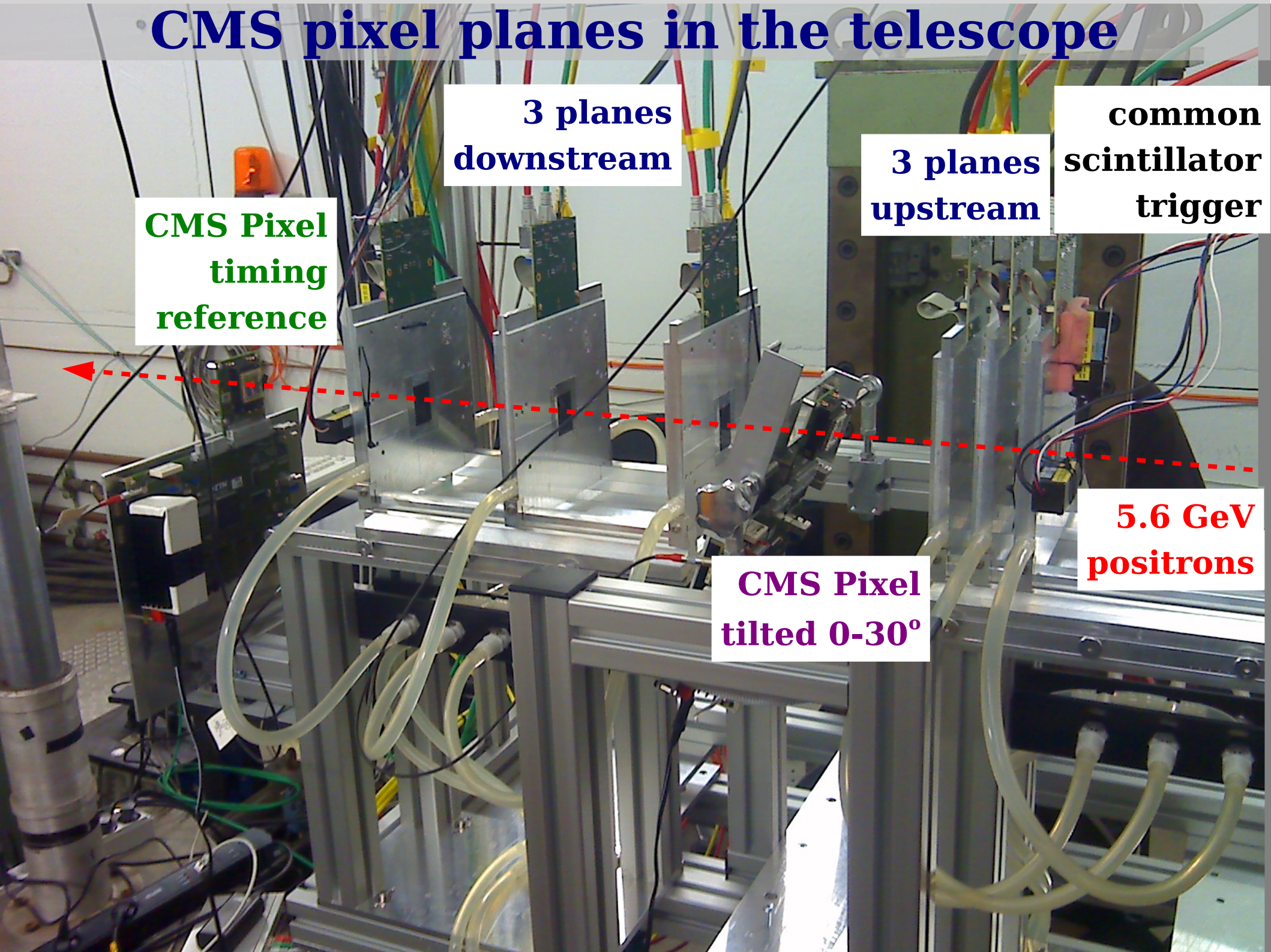
3 planes  
upstream

common  
scintillator  
trigger

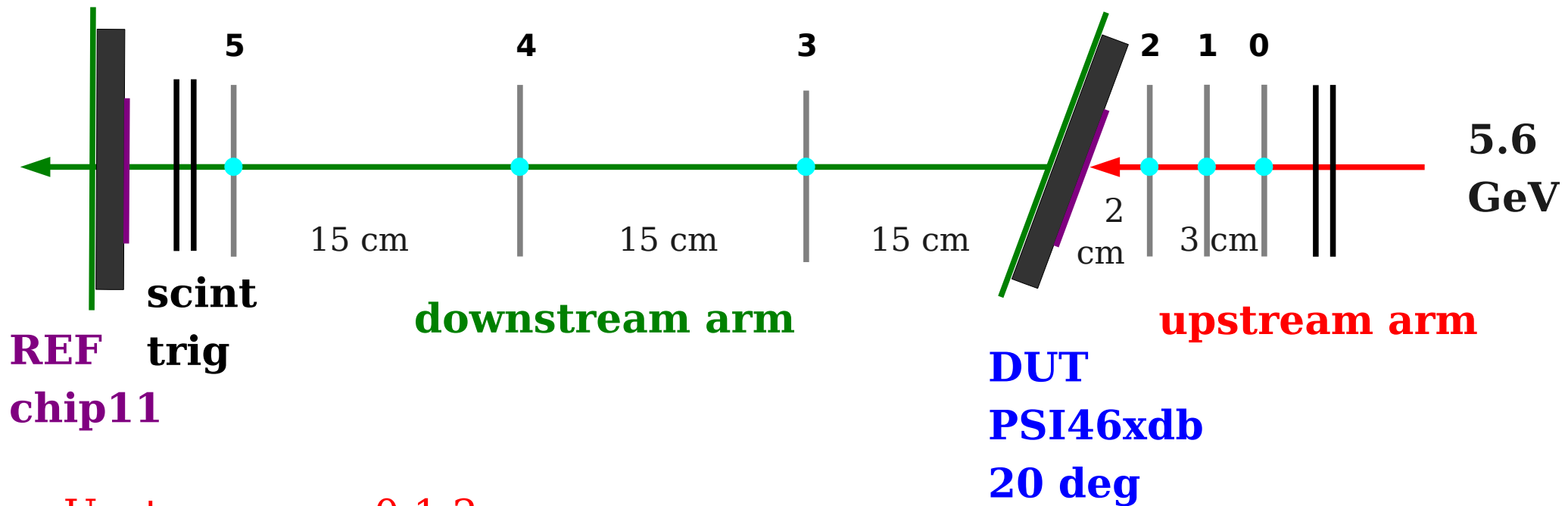
CMS Pixel  
timing  
reference

5.6 GeV  
positrons

CMS Pixel  
tilted 0-30°



# Default set up

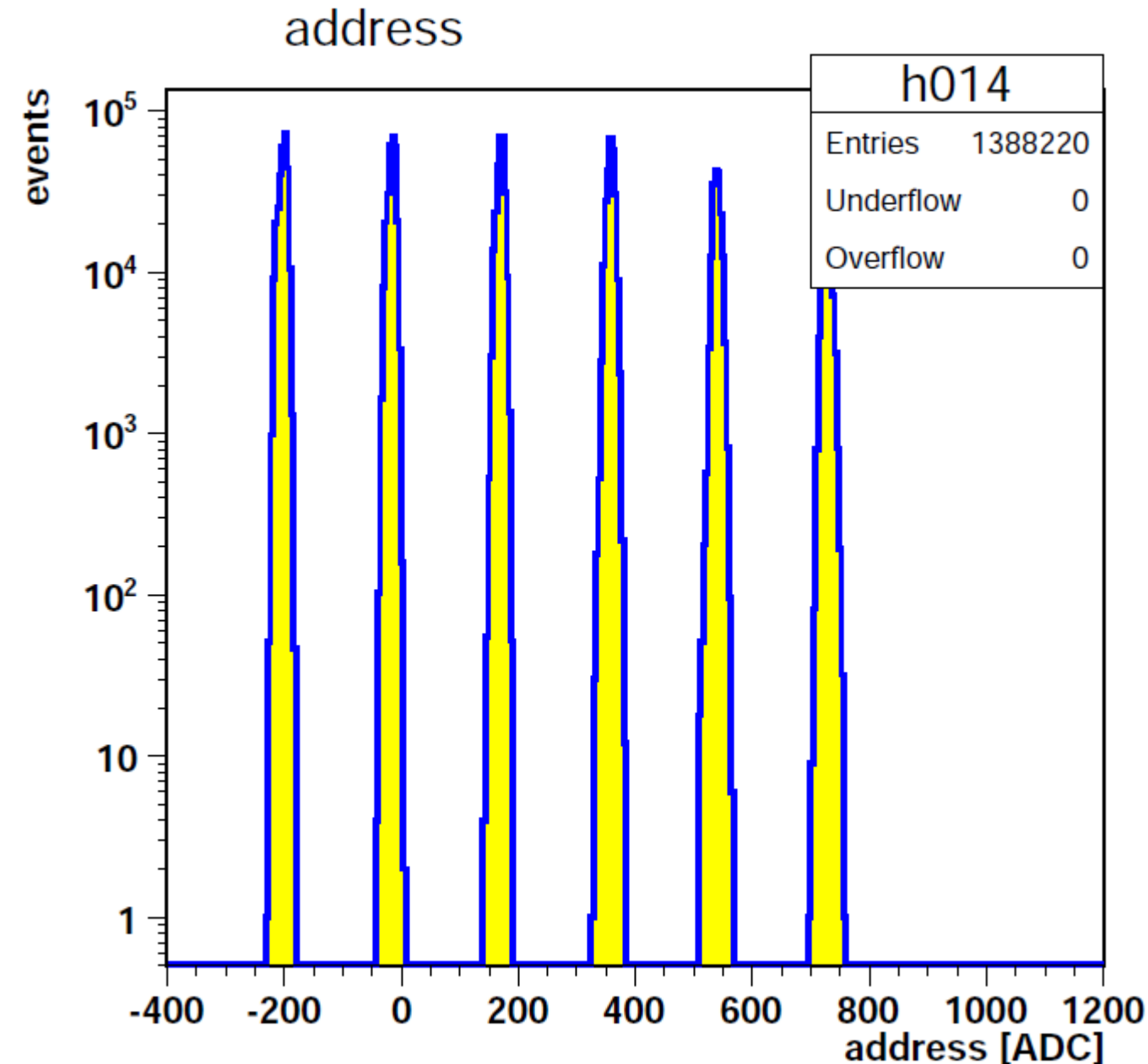


- Upstream arm 0-1-2:
  - as close as possible to DUT, but allow for tilting (open for insertion)
- DUT = single chip module, tilted by up to 30°,
- Downstream arm 3-4-5:
  - equally spaced between DUT and REF, allow for DUT tilting
- REF = single chip module for timing, as close as possible behind scint
- trigger: 2-fold coincidence (config: TLU AndMask 12)

# PSI46xdb test beam goals

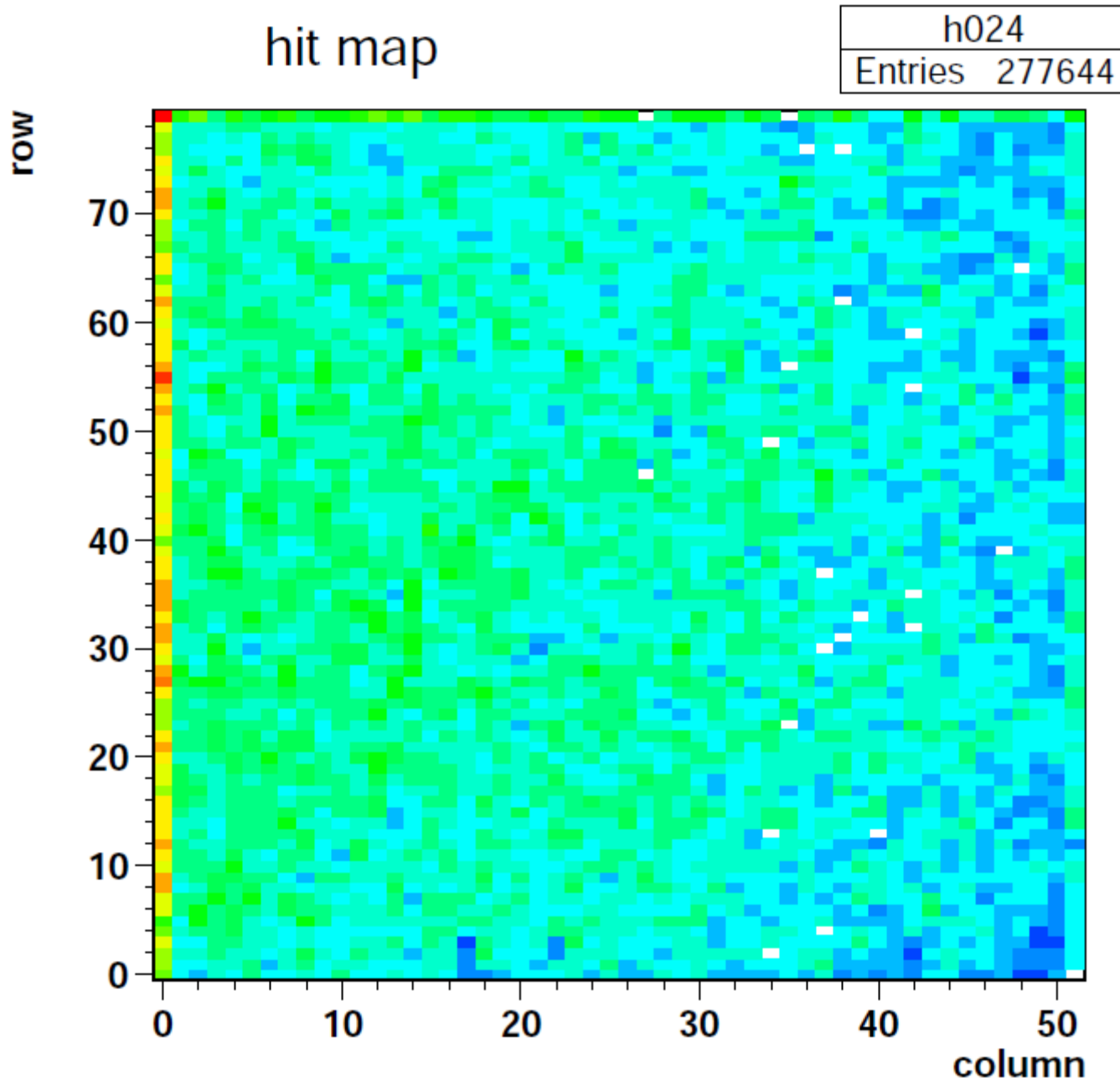
- Measure efficiency
  - present ROC reached 99.9%
- Measure resolution
  - present ROC reached 7  $\mu\text{m}$  at 20° tilt
  - new ROC might be better with lower thresholds
- Measure gain:
  - calibration from Landau peak vs tilt angle
- Study any problems
- Give feedback to chip designers at PSI
- Present results in CMS meetings and at conferences
- Publish

# xdb2 address levels



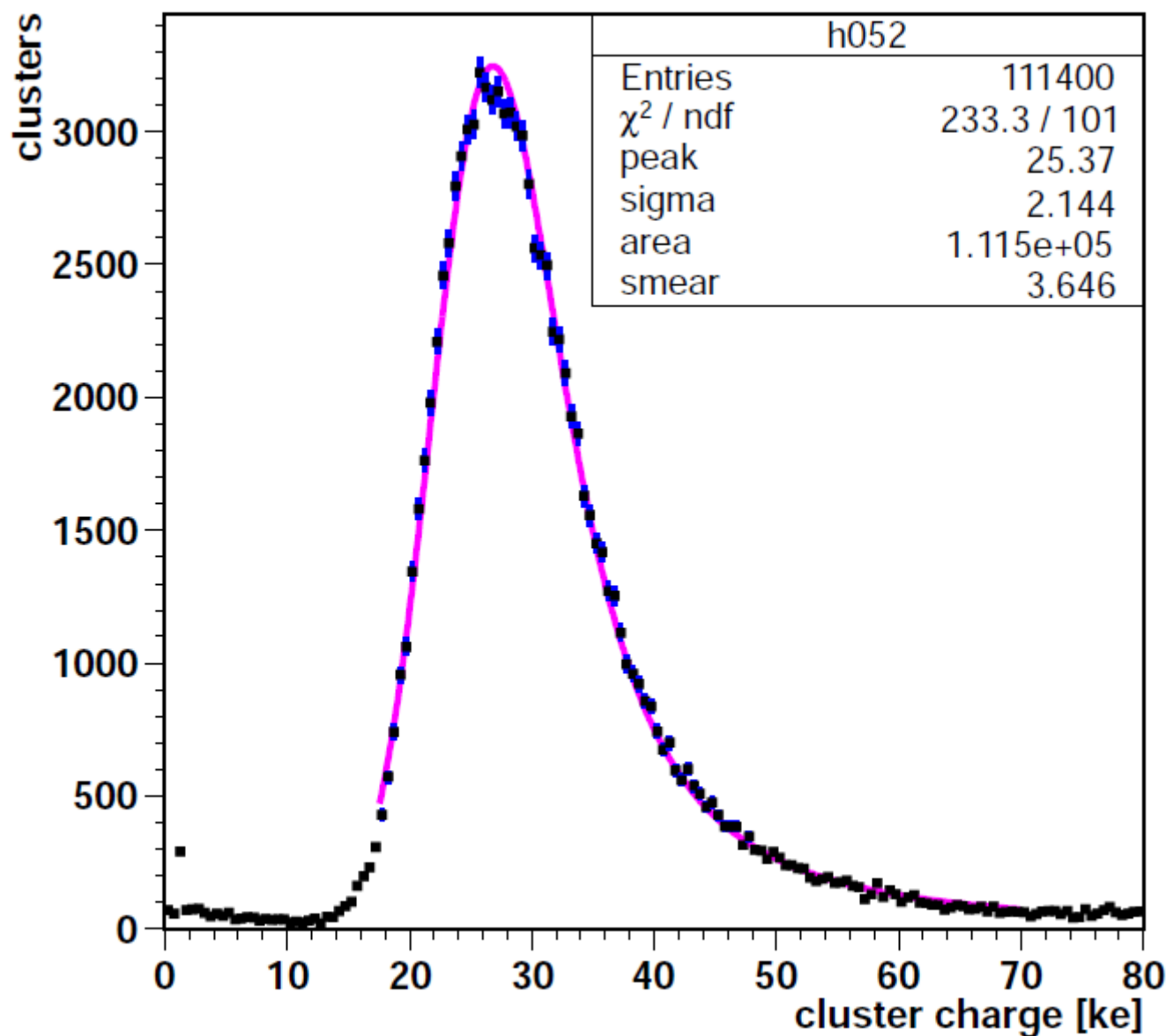
- analog transfer of pixel column and row address:
  - hexal encoding
- 6 levels clearly separated
- no noise
- perfect

# xdb2 hit map in beam



- xdb2
- run 2392:
  - 600 s
  - 5.6 GeV
  - tilt  $22^\circ$
- beam profile  
from left to right
- some dead pixels  
in the right half:
  - thresholds?
  - bumps?

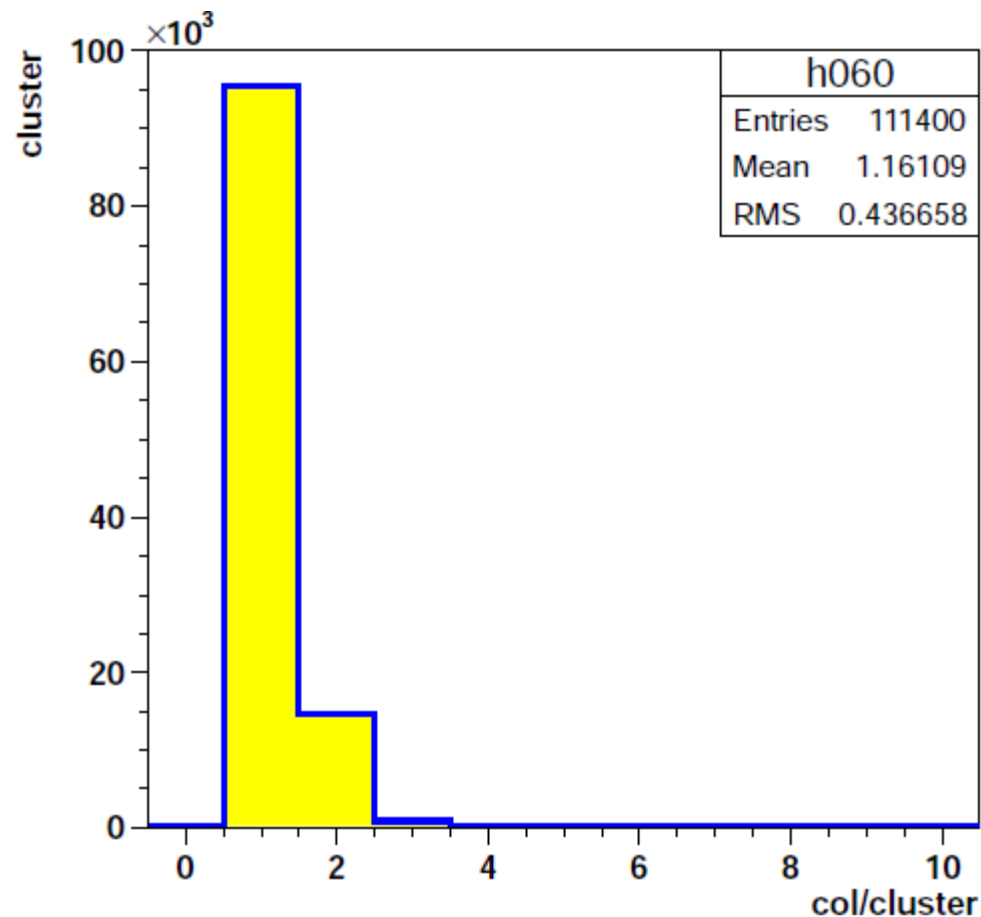
# xdb2 Landau distribution



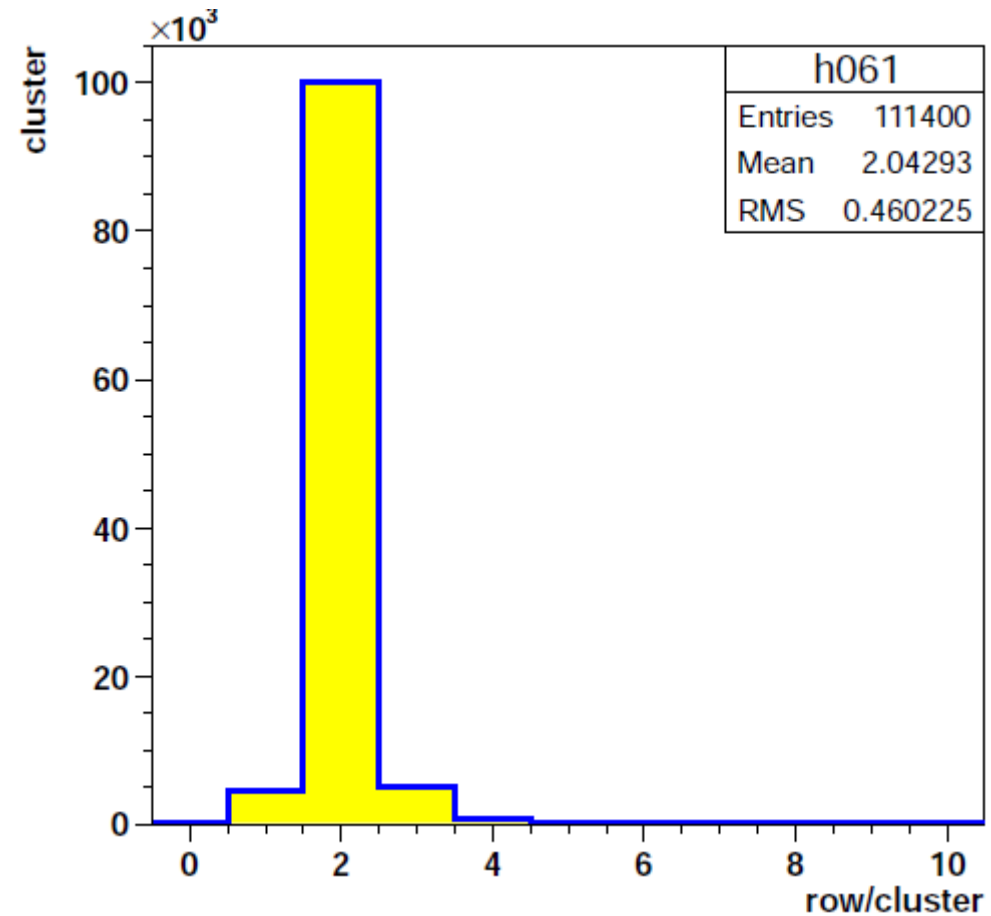
- xdb2
- run 2392:
  - tilt 22°
- Weibull gain calibration applied
- Cluster charge distribution fit by Landau  $\otimes$  Gauss
  - peak position and width OK
  - too much Gaussian smearing needed

# xdb2 cluster size

**column direction:**  
**no tilt**  
**mostly 1-col clusters**

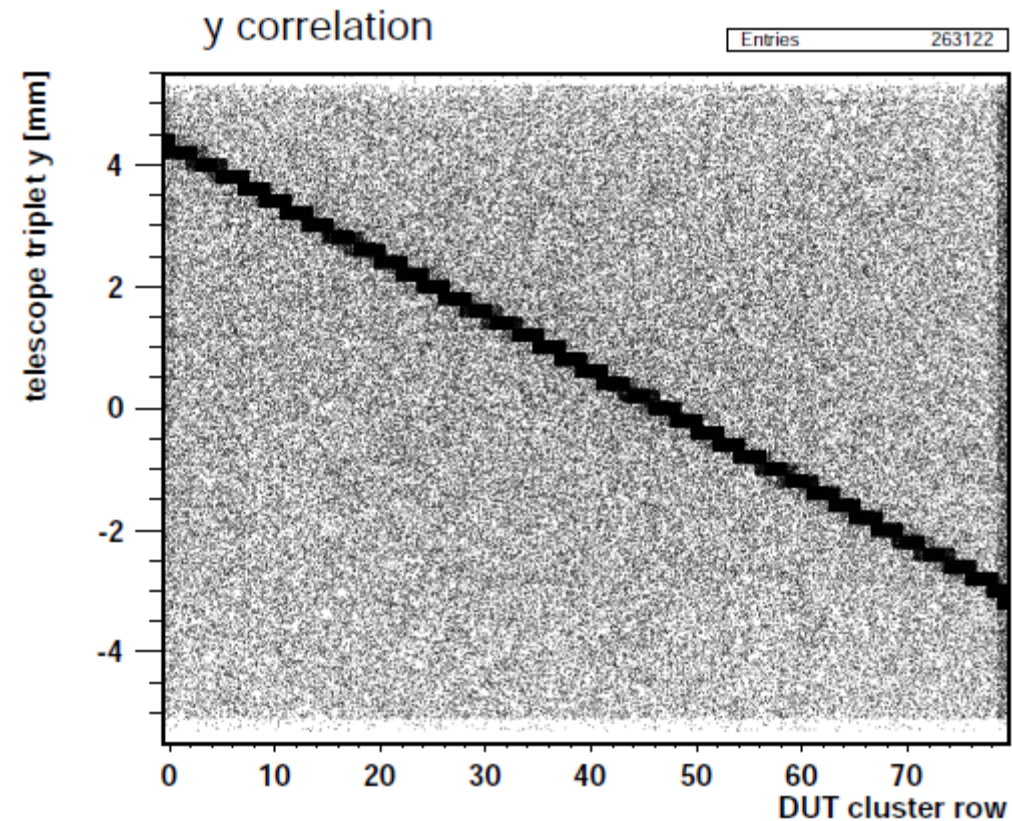
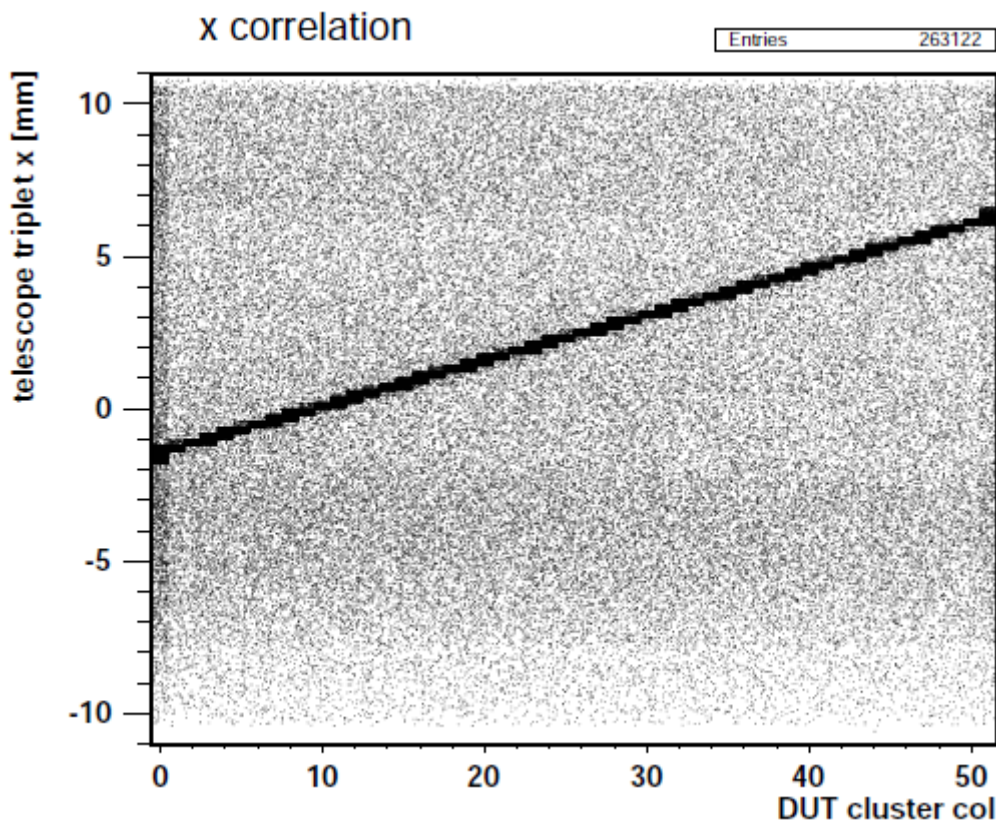


**row direction:**  
**22° tilt**  
**mostly 2-row clusters**



# xdb2 clusters vs telescope tracks

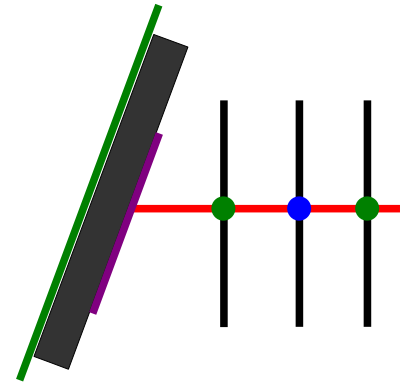
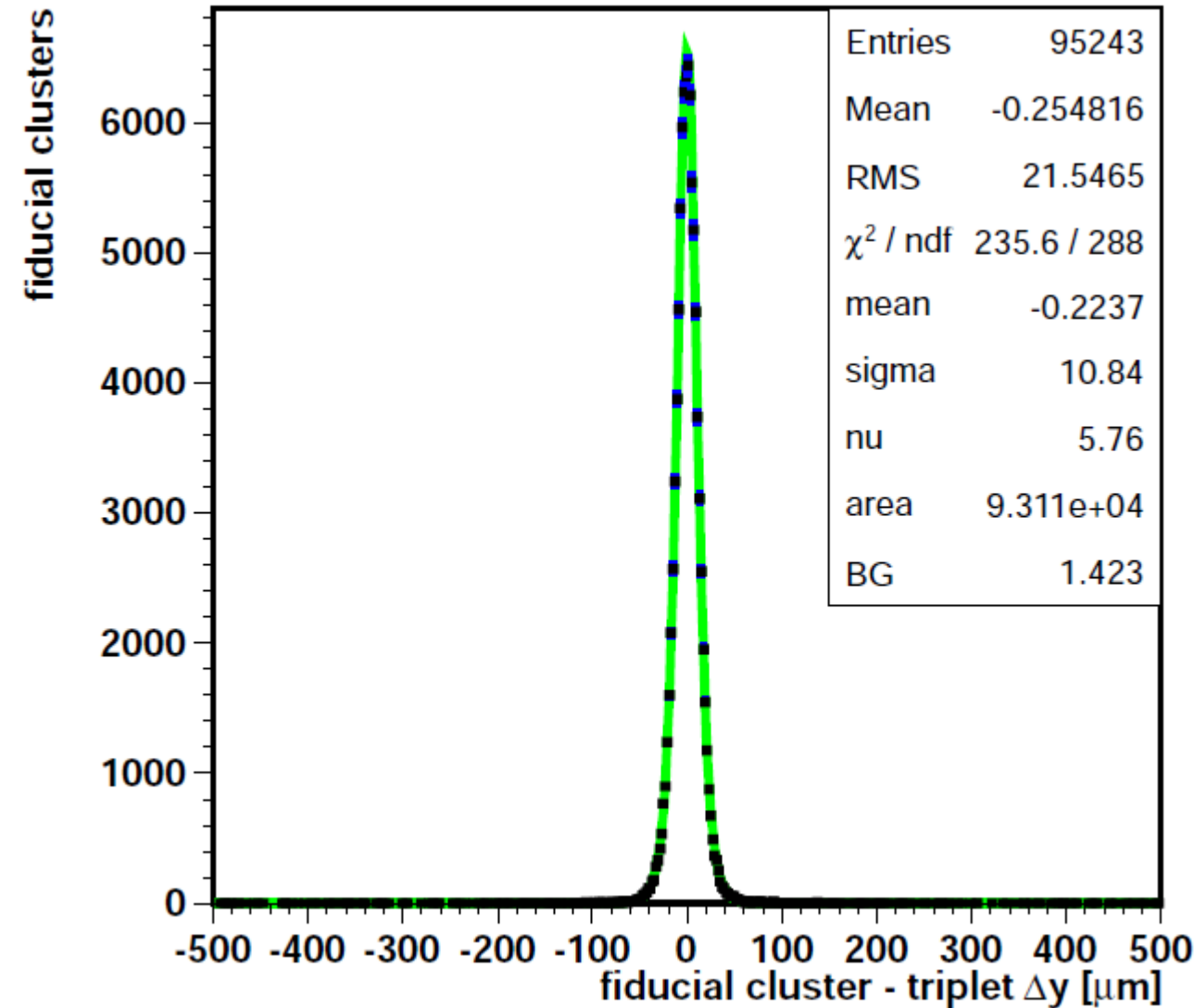
**correlations!**



**aligned in space and time**

# CMS pixel row resolution

run 3702, 5.6 GeV, 22° tilt

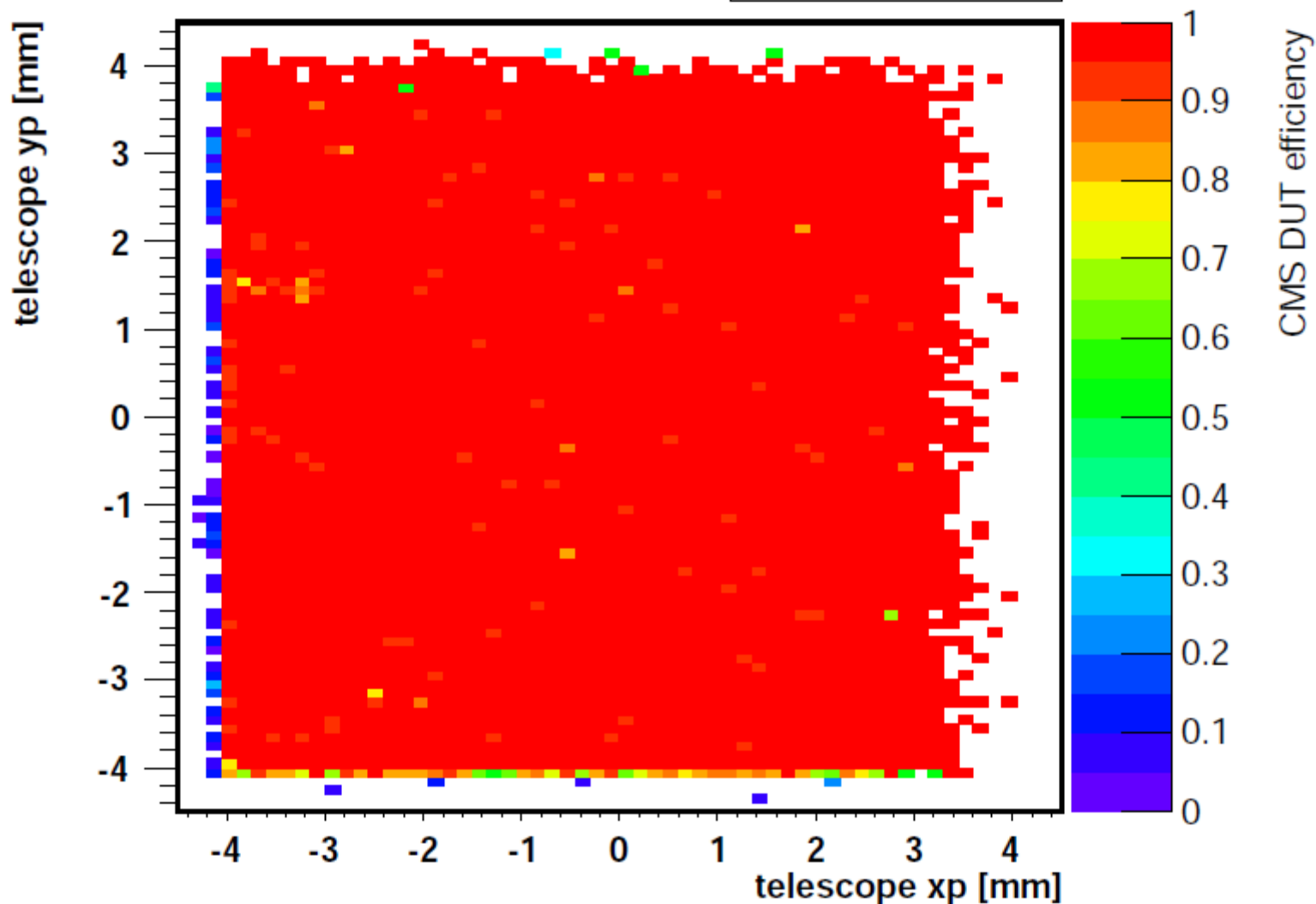


- Vertical = rows
  - CMS pixel = 100  $\mu\text{m}$ .
- Residual:
  - $\sigma = 10.8 \mu\text{m}$ ,
  - telescope extrapolation: 4.5  $\mu\text{m}$ ,
  - **xdb resolution: 10  $\mu\text{m}$**
  - **previous: 7  $\mu\text{m}$**

# Efficiency map

$\text{eff} = (\text{xdb linked hits}) / (\text{telescope tracks with REF hit})$

DUT efficiency

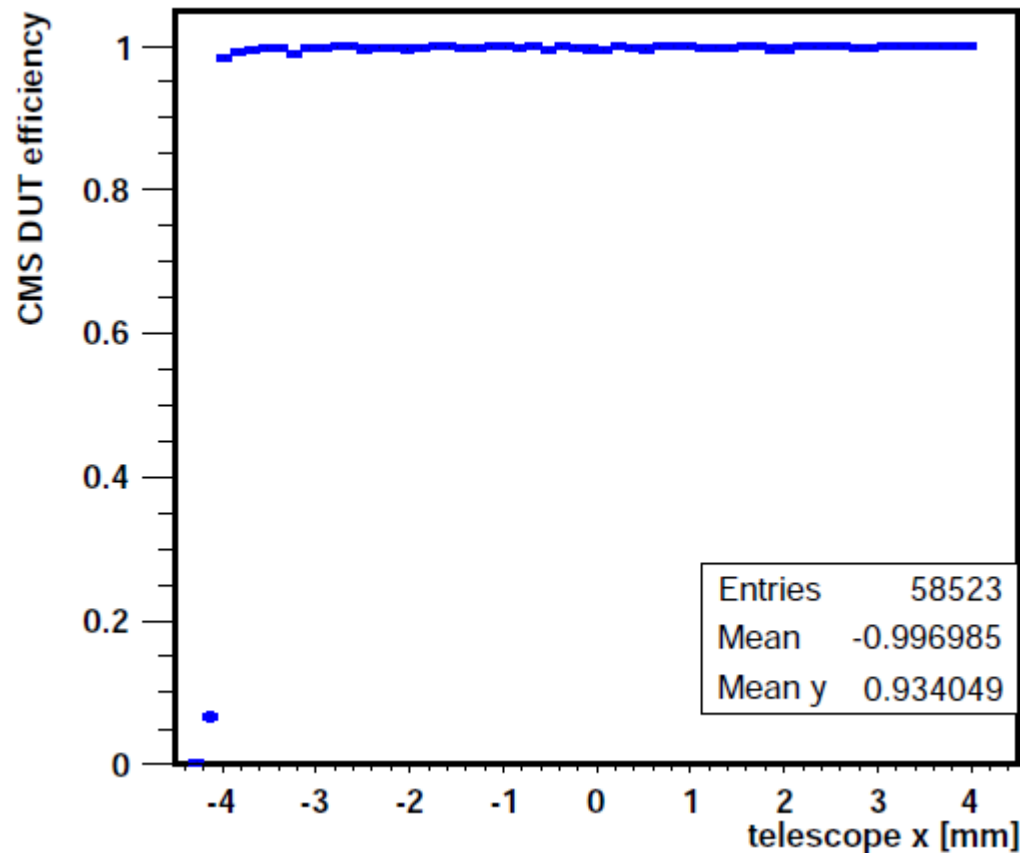


- xdb 2
- run 3702
  - first 350 s
- 5.6 GeV
- tilt 22°
- 99.7% in fiducial volume

# Efficiency profiles

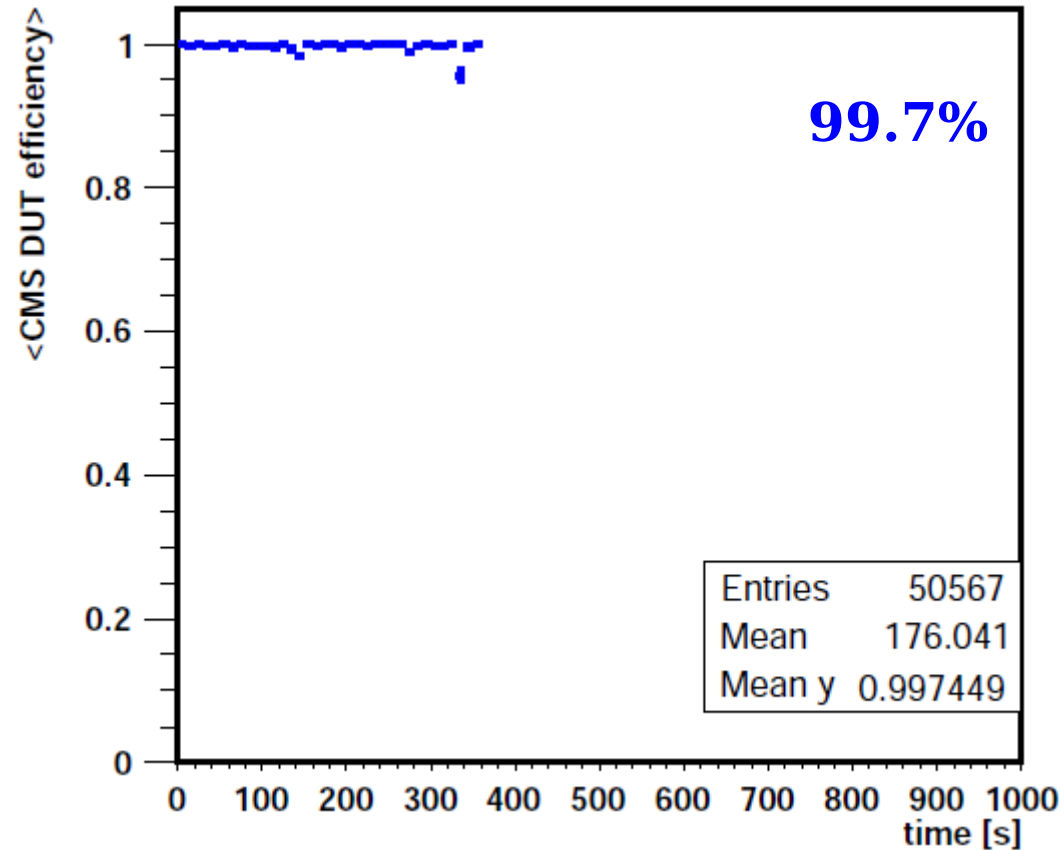
xdb 2, 22°, run 3702

**efficiency vs x after  
fiducial cuts in y**



**x: 52 columns**

**Efficiency vs time after  
fiducial cuts in x and y**



**first 350 s (then drop)**

# Summary and outlook

- One analog PSI46xdb bump bonded to a single chip pixel sensor operated at the DESY test beam:
  - procedures established
  - efficiency good, resolution can be improved
- Improve:
  - Timing stability (Hanno)
- Next 2 weeks: efficiency and resolution scans:
  - vs threshold, vs analog current
  - vs tilt, vs bias voltage
- During Summer:
  - test PSI46dig

# April TB program

- Defaults: DUT at 20°, bias -150 V, softest threshold, optimal delays
- Optimize rate in test beam by adjusting position ½ day
- Clock delay scan: 0..24 ns, 4 ns steps, finer at edges (~10 runs) ½ day
- Bias voltage scan: -150 to -10 V, 20 V steps (8 runs) ½ day
- DUT tilt scan: 0°, 5°, 10°, 15°, 18°, 20°, 22°, 25°, 30° (9 long runs) 1.5 day
- Threshold scan: `vthrComp` 97 to 7 step 10 (10 long runs) 1.5 day
- gain calibrations each day
- scan Vana (less power), always re-optimize other DACs 2 days
  - possibly repeat delay and threshold scans
- another chip as DUT 1 day
- repeat problematic runs 1 day
- reserve 1 day + weekends + extension week