Development of CMOS Pixel Sensors for High-Precision Vertexing & Tracking Devices

M. Winter (PICSEL team of IPHC-Strasbourg)

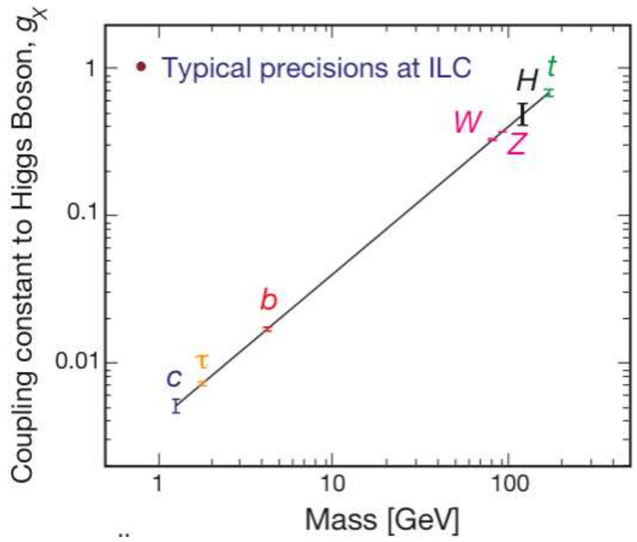
- **Sensor design** : coll. with IRFU-Saclay - (ALICE-MFT)
- **Ladder design** : coll. with DESY - Oxford - Bristol
- **Tests** : coll. with LBNL/STAR - Frankfurt/CBM - CERN-INFN/ALICE - DESY/AIDA

DESY – 3rd May 2012

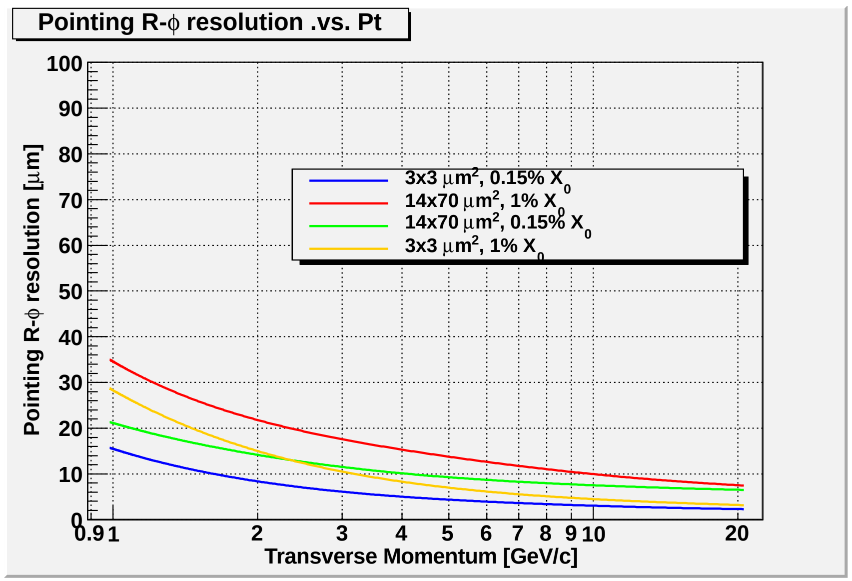
Contents

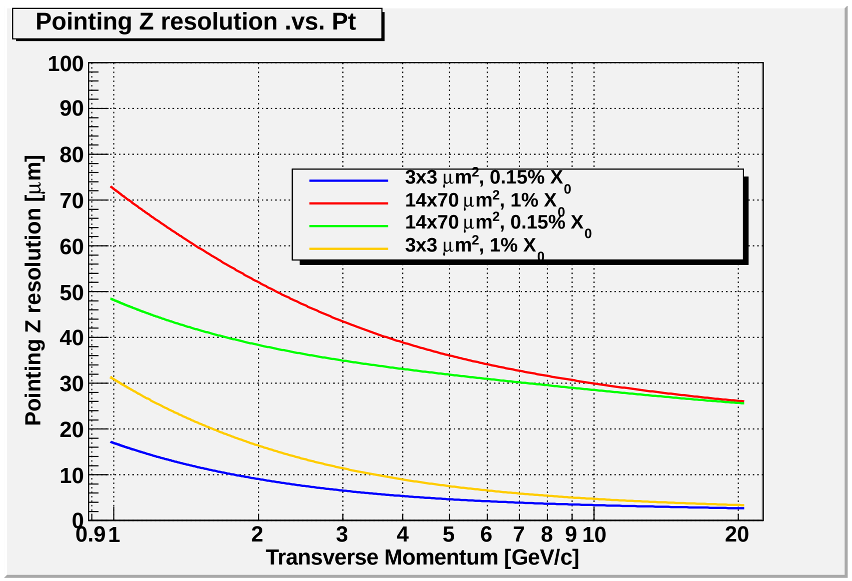
ILC Vertexing Performance Goals

- CMOS PIXEL SENSORS **(CPS) devt triggered by ILC vertex detector requirements :**
  - ⋇ unprecedented granularity & material budget (very low power)
  - ⋇ much less demanding running conditions than at LHC
    - ⇛ alleviated read-out speed & radiation tolerance requests



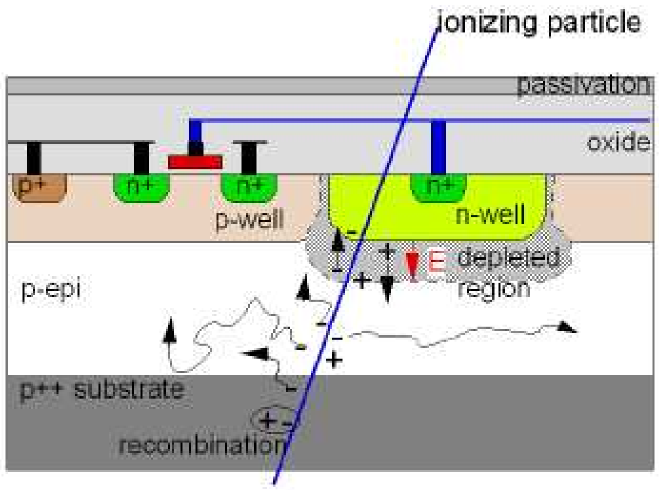
- **Vertexing goal:**
  - ⋇ achieve high efficiency & purity flavour tagging ⟼ charm & tau !!!
  - $\hookrightarrow \sigma_{R\phi,Z} \leq 5 \oplus 10/p \cdot sin^{3/2}\theta\ \ \mu m$ ▷ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta$
  - ▷ Comparison: $\sigma_{R\phi,Z}$(ILD) with VXD made of ATLAS-IBL or ILD-VXD pixels:





CMOS Pixel Sensors: Main Features

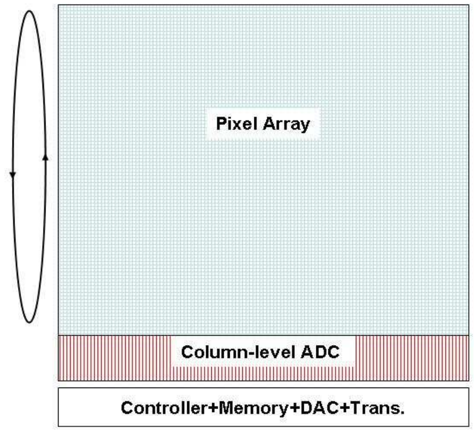
- **Prominent features of CMOS pixel sensors:**
  - ⋇ high granularity ⇛ excellent (micronic) spatial resolution
  - ⋇ very thin (signal generated in 10-20 μm thin epitaxial layer)
  - ⋇ signal processing μ-circuits integrated on sensor substrate
    - ⇛ impact on downstream electronics (⇛ cost)



- **CMOS pixel sensor technology has the highest potential**

⇛ R&D largely consists in trying to exploit potential at best with accessible industrial processes

- **Organisation of MIMOSA sensors:**
  - ⋇ manufactured in 0.35 μm OPTO process (mainly)
  - ⋇ signal sensing and analog processing in pixel array
  - ⋇ mixed and digital circuitry integrated in chip periphery
  - ⋇ read-out in rolling shutter mode
    (pixels grouped in columns read out in //)
    - ⇛ impact on power consumption

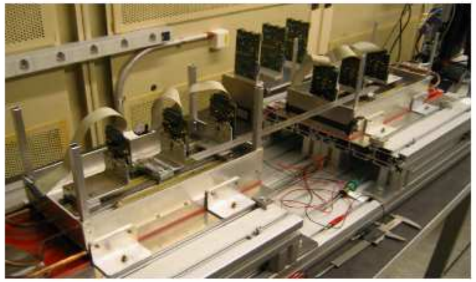


CPS R&D: A Long Path with Numerous Intermediate Steps

- Main objective: ILC, with staggered performances
  - MAPS applied to other experiments with intermediate requirements

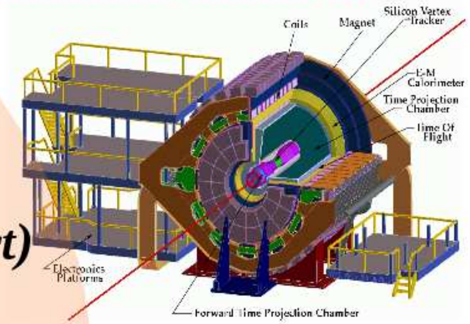
EUDET 2006/2010

Beam Telescope



STAR 2012

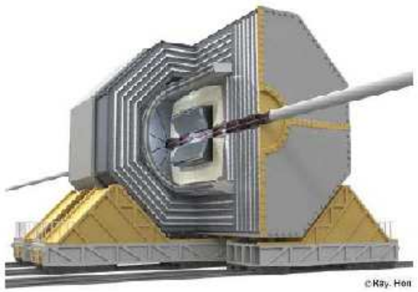
Solenoidal Tracker at RHIC



EUDET (R&D for ILC, EU project)
STAR (Heavy Ion physics)
CBM (Heavy Ion physics)
ILC (Particle physics)
HadronPhysics2 (generic R&D, EU project)
AIDA (generic R&D, EU project)
FIRST (Hadron therapy)
ALICE/LHC (Heavy Ion physics)
EIC (Hadronic physics)
CLIC (Particle physics)
SuperB (Particle physics)
...

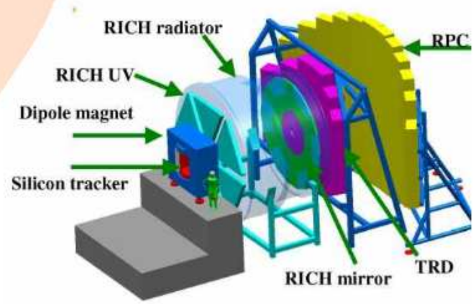
ILC >2020

Internatinal Linear Collider



CBM 2017

Compressed Baryonic Matter



➔ Spinoff: Interdisciplinary Applications, biomedical, space …

CMOS Pixel Sensors: Established Architecture

- **Main characteristics of MIMOSA-26 sensor equipping EUDET BT:**

  ⋇ 0.35 μm process with high-resistivity epitaxial layer (coll. with IRFU/Saclay)

  ⋇ column // architecture with in-pixel amplification (cDS) and end-of-column discrimination, followed by $\emptyset$

  ⋇ binary charge encoding

  ⋇ active area: 1152 columns of 576 pixels (21.2×10.6 mm^2)

  ⋇ pitch: 18.4 $\mu m \rightarrowtail \sim$ 0.7 million pixels

  ▷ charge sharing $\Rrightarrow$ $\sigma_{sp} \sim$ 3.-3.5 μm

  ⋇ t$_{r.o.} \lesssim$ 100 μs ($\sim$10^4 frames/s) suited to $>$10^6 part./cm^2/s

  ⋇ JTAG programmable

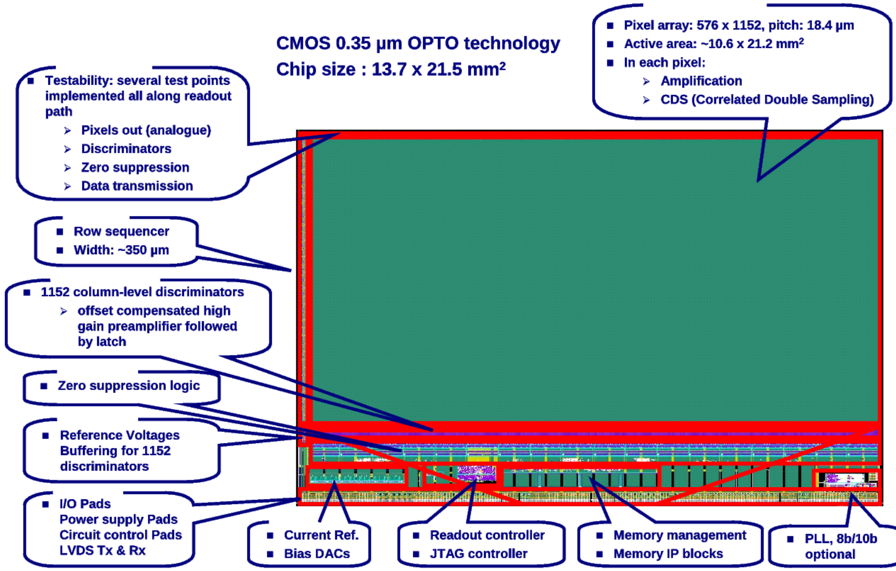
  ⋇ rolling shutter architecture

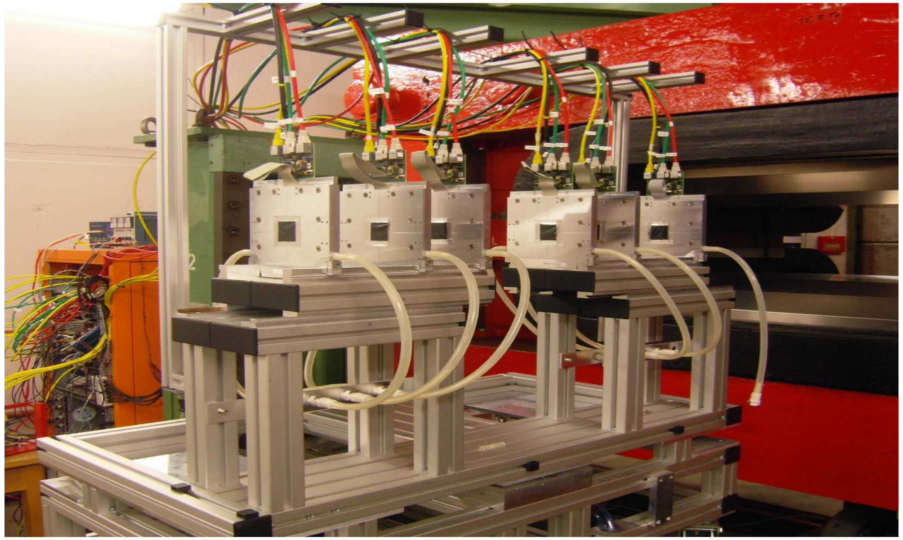
  $\Rrightarrow$ full sensitive area dissipation $\cong$ 1 row

  ▷ $\sim$ 250 mW/cm^2 power consumption (fct of N$_{col}$)

  ⋇ thinned to 50 μm

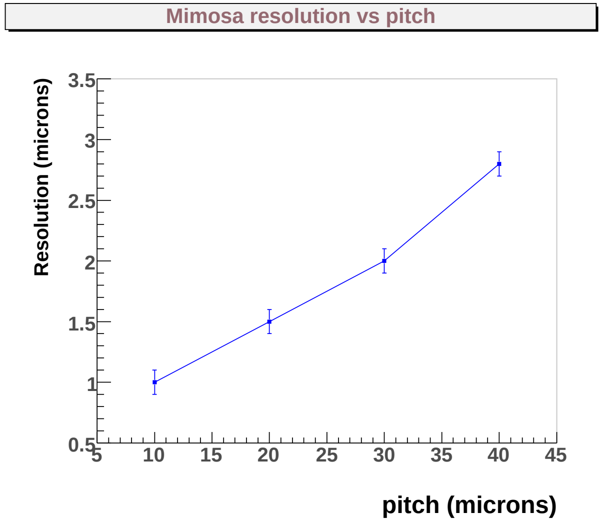
  ⋇ various appli. : VD demonstr., NA63, oncotherapy, dosimetry, ...





Measured Spatial Resolution

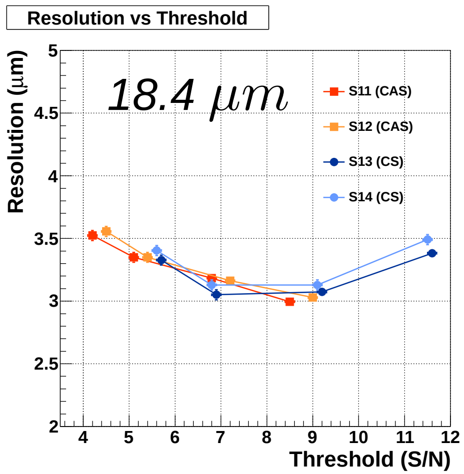
- **Compare position of impact on sensor surface predicted with BT to hit reconstructed with sensor under test :**
  clusters reconstructed with eta-function,
  exploiting charge sharing between pixels

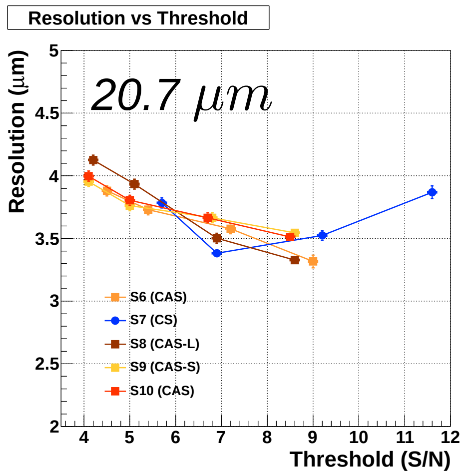


- **Impact of pixel pitch (analog output) :** ▷▷▷
  $\boldsymbol{\sigma_{sp} \sim 1\ \mu m}$ (10 μm pitch) $\rightarrowtail$ $\boldsymbol{\lesssim 3\ \mu m}$ (40 μm pitch)

- **Impact of charge encoding resolution :** ▷▷▷
  ▷ ex. of 20 μm pitch $\Rrightarrow$ σ_{sp}^{digi} = pitch/$\sqrt{12} \sim 5.7\ \mu m$

Nb of bits	**12**	**3-4**	**1**
Data	*measured*	*reprocessed*	*measured*
σ_{sp}	$\lesssim 1.5\mu m$	$\lesssim 2\mu m$	$\lesssim 3.5\mu m$





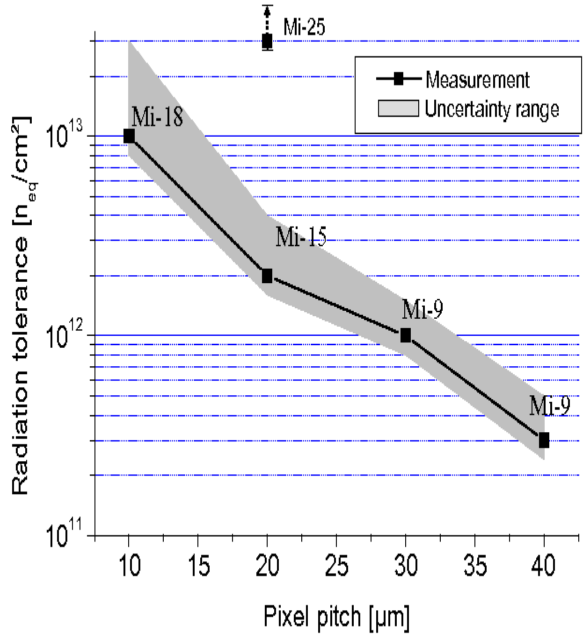
Observed Radiation Tolerance

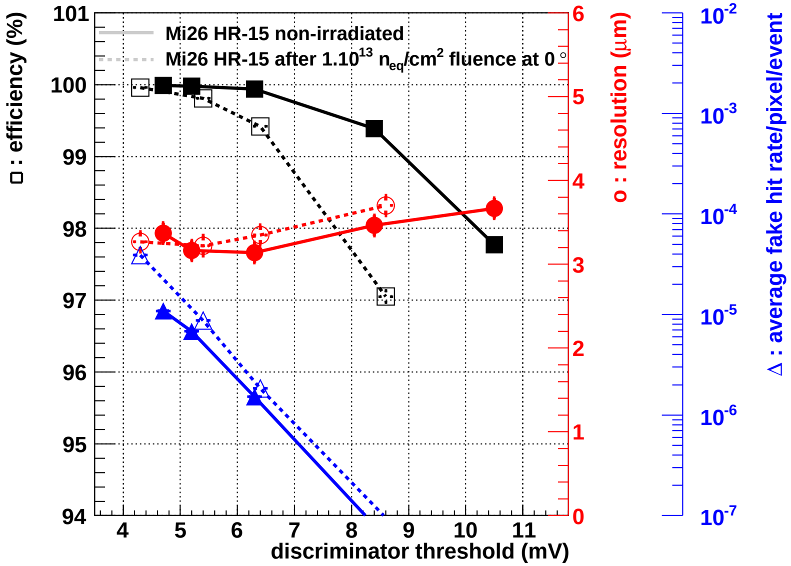
- **Introductory remarks :**
  - ⋇ still evolving (csq of CMOS industry process param. evolution)
  - ⋇ CMOS technology expected to tolerate high ionising radiation doses ($>>$ 10 MRad), in particular at $< 0^{\circ}$C and short t_{integ}
  - ⋇ main a priori concern : NON-ionising radiation (in absence of thick depleted sensitive volume)

- **Influence of pixel pitch :** ▷▷▷
  - ⋇ fig: all measts done with low resistivity epitaxial layer, but 1
  - ⇛ high density sensing diodes ($\equiv$ small pitch) improves non-ionising radiation tolerance

- **Influence of epitaxial layer resistivity :**
  - ⋇ ex: 1 k$\Omega \cdot cm$ & O(1)V depletion voltage ▷▷▷
  - ⋇ trend : $\gtrsim 1\ k\Omega \cdot cm$ & $>>$ 10 V

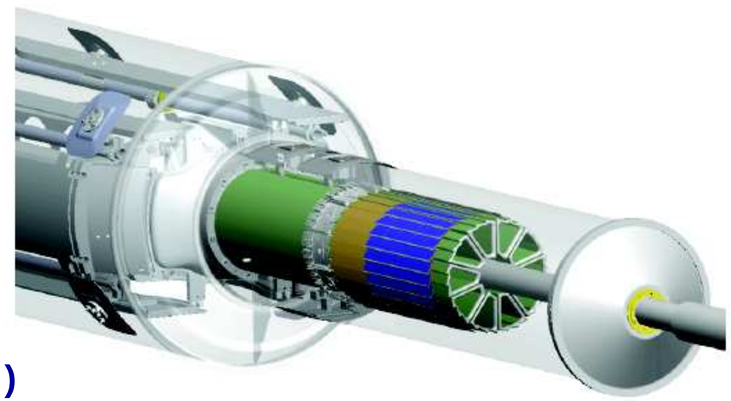
⇛ **tolerance to $\gtrsim 10^{14-15}$ n_{eq}/cm^2 not excluded**

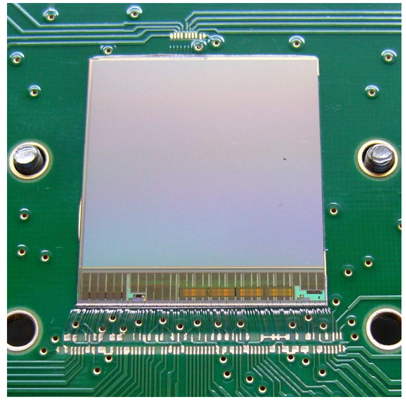




State-of-the-Art: MIMOSA-28 for the STAR-PXL

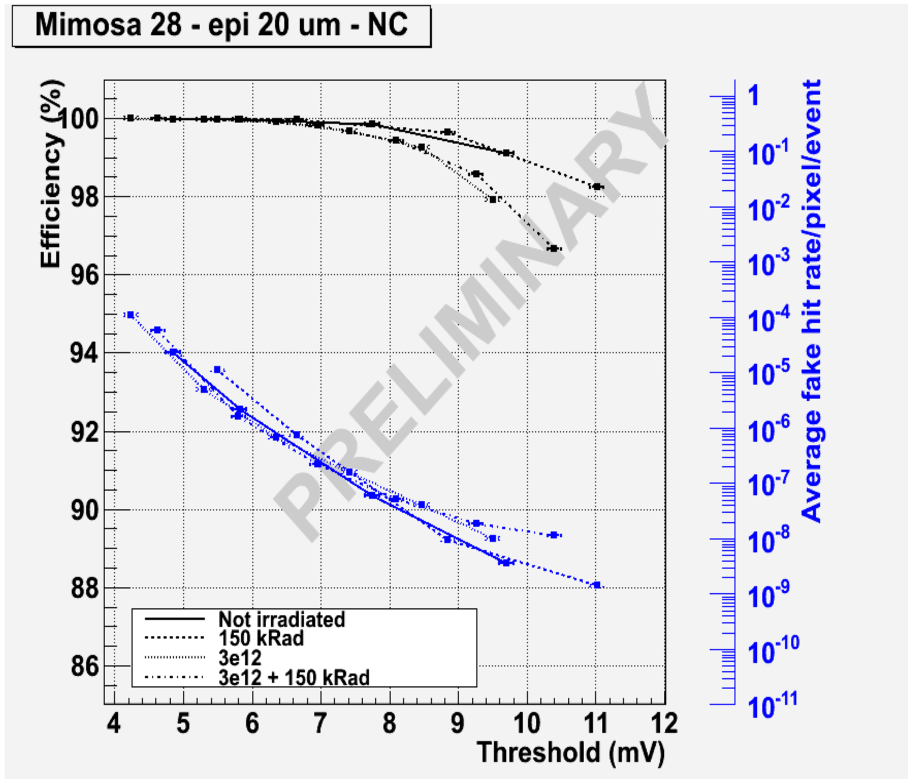
- **Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):**
  - ⁜ 0.35 μm process with high-resistivity epitaxial layer
  - ⁜ column // architecture with in-pixel cDS & amplification
  - ⁜ end-of-column discrimination & binary charge encoding
  - ⁜ on-chip zero-suppression
  - ⁜ **active area: 960 colums of 928 pixels (19.9$\times$19.2 mm^2)**
  - ⁜ **pitch: 20.7 μm $\rightarrowtail$ $\sim$ 0.9 million pixels**
    $\hookrightarrow$ **charge sharing $\Rrightarrow$ σ_{sp} $\gtrsim$ 3.5 μm**
  - ⁜ JTAG programmable
  - ⁜ **t$_{r.o.}$ $\lesssim$ 200 μs ($\sim$ 5$\times$10^3 frames/s) $\Rrightarrow$ suited to $>$10^6 part./cm^2/s**
  - ⁜ 2 outputs at 160 MHz
  - ⁜ **$\lesssim$ 150 mW/cm^2 power consumption**





▷▷▷ **Sensors fully evaluated :** (50 μm thin)

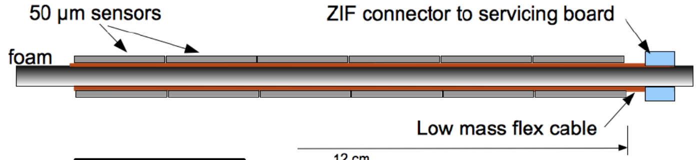
- ⁜ N $\lesssim$ 15 e$^-$ ENC at 30-35°C (as MIMOSA-22AHR)
- ⁜ ϵ_{det}, fake & σ_{sp} as expected
- ⊸ **Rad. tol. validated (3·10^{12}n$_{eq}$/cm^2 & 150 kRad at 30°C)**
- ⊸ All specifications are met $\Rrightarrow$ 40 ladders under construction

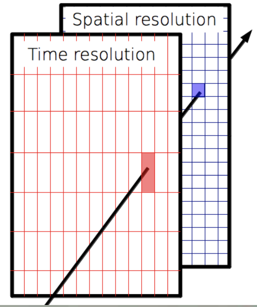


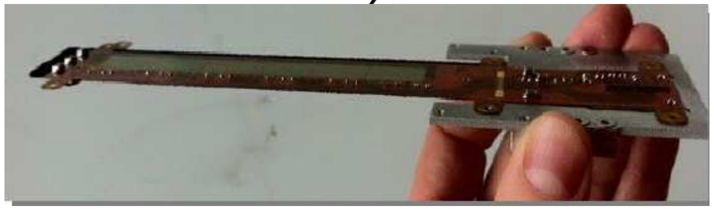
▷▷▷ **Start of data taking early 2013**

Sensor Integration in Ultra Light Devices

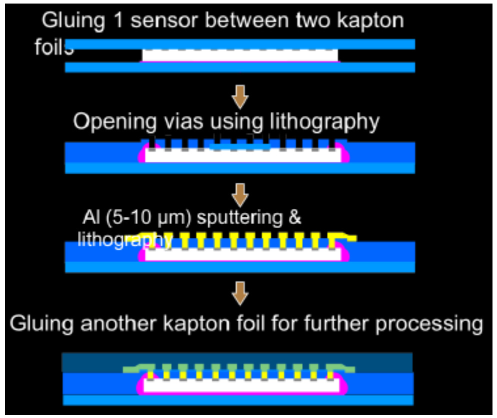
- **2-sided ladders with time stamping for the ILD-VXD :**
  - ⋇ manyfold bonus expected from 2-sided ladders:
    compactness, alignment, pointing accuracy (shallow angle), redundancy, etc.
  - ⋇ studied by PLUME coll. (Oxford, Bristol, DESY, IPHC) & AIDA (EU)
    $\hookrightarrow$ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - ⋇ square pixels for single point resolution on beam side
  - ⋇ elongated pixels for 4-5 times shorter r.o. time on other side
  - ⋇ correlate hits generated by traversing particles
  - ⋇ expected total material budget $\sim$ 0.3 % X_0
    $\hookrightarrow$ 1st proto. (0.6 % X_0) fabricated & operationnal
    - ▷ beam tests at CERN-SPS (traversing m.i.p.) in Nov. '11

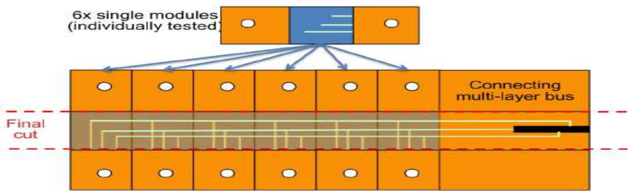




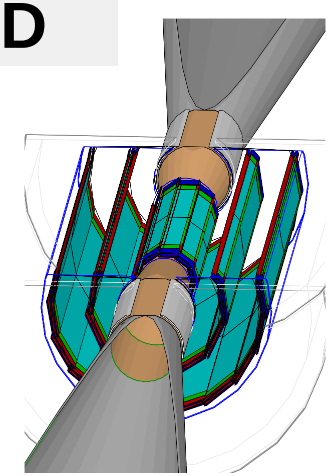


- **Unsupported ladders (Hadron Physics 2 / FP-7)**
  - ⋇ 50 μm thin CMOS sensors embedded in thin kapton and cabled
    with redistributed connections $\rightarrowtail$ suited to curved surfaces ?
  - ⋇ expected total material budget $\lesssim$ 0.15 % X_0
  - ⋇ 1st single sensor mechanical prototype fabricated
  - ⋇ 1st 3-sensor electrical proto. expected by Summer 2012

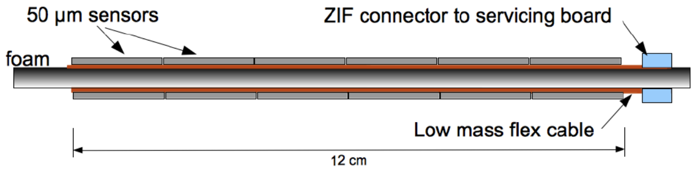




CMOS Pixel Sensors for the ILD-VXD

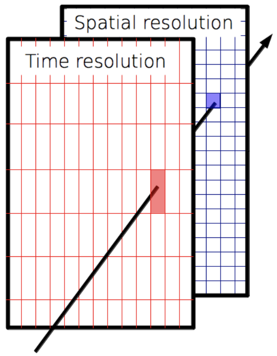


- **Two types of CMOS Pixel Sensors (CPS):**
  - ⋇ **Inner layers** ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 6 μm
  - ⋇ **Outer layers** ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm
  - ⋇ Total VXD instantaneous/average power $<$ 700/20 W (0.35 μm process)



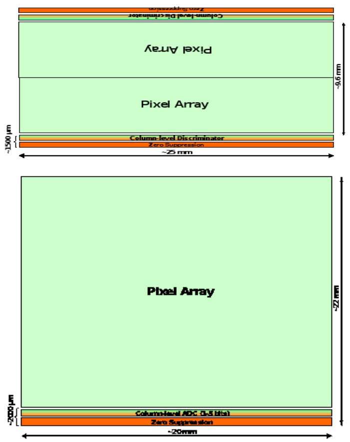
- **2-sided ladder concept for inner layer :**
  - ⋇ *S*quare pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} < 3\ \mu m$)

    & *E*longated pixels (16×80 μm^2) on external ladder face ($t_{r.o.} \sim 10\ \mu s$)



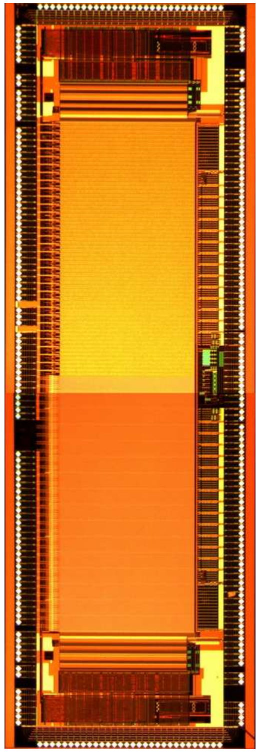
- **Sensor final prototypes :** fabricated in Q4/2011
  - ⋇ **MIMOSA-30:** inner layer prototype with 2-sided read-out ▷ ▷ ▷
    - ↪ one side : 256 pixels (16×16 μm^2)

      other side : 64 pixels (16×64 μm^2)
  - ⋇ **MIMOSA-31:** outer layer prototype ▷ ▷ ▷
    - ↪ 48 col. of 64 pixels (35×35 μm^2) ended with 4-bit ADC

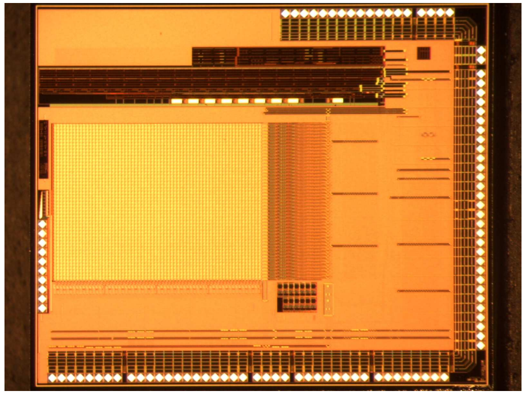


CMOS Pixel Sensors: Status of Baseline Devt

- **MIMOSA-30: prototype for ILD-VXD innermost layer** ▷ ▷ ▷
  - ⋇ 0.35 CMOS μm process with high-resistivity epitaxy
  - ⋇ in-pixel CDS, rolling shutter read-out, binary sparsified output
  - ⋇ **high resolution side : pixels of 16×16 μm^2 $\Rrightarrow$ expect $\sigma_{sp} <$ 3 μm**
    - 128 columns (discri) & 8 col. (analog) of 256 rows (final scale)
    - read-out time $\lesssim$ 50 μs
  - ⋇ **time stamping side : pixels of 16×64 μm^2 $\Rrightarrow$ $t_{r.o.} \sim$ 10 μs**
    - (expect $\sigma_{sp} \sim$ 6 μm)
    - 128 columns (discri) and 8 col. (analog) of 64 rows (final scale)
    - lab tests positive : N $\sim$ 15 e$^-$ENC & discri. all OK for $t_{r.o.} = 10 \mu s$
  - ⋇ beam tests (CERN-SPS) in June/July '12 $\Rrightarrow$ σ_{sp}, ϵ_{det}, fake rate

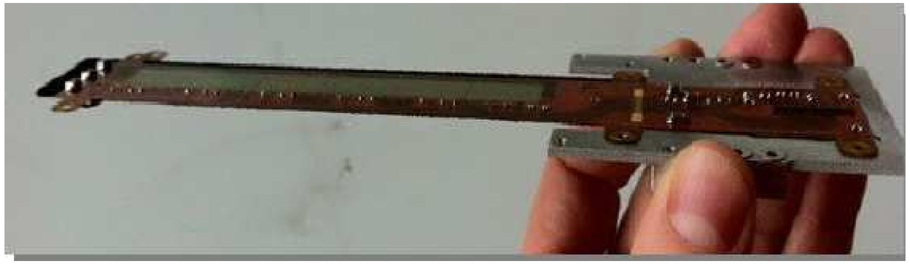


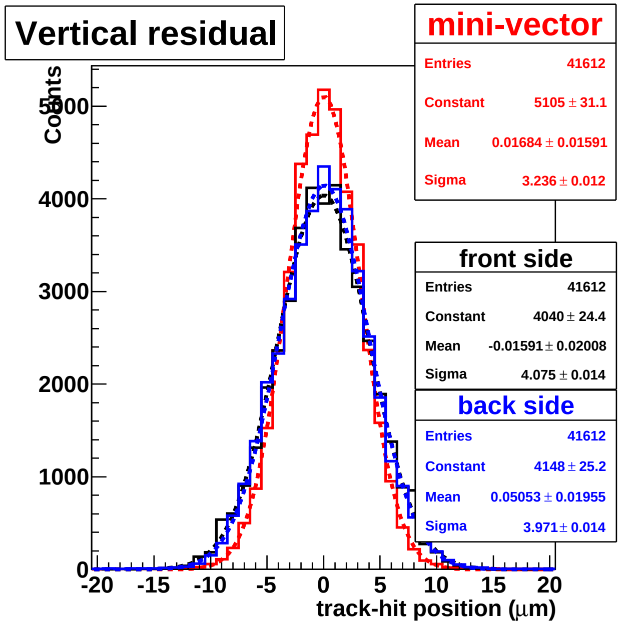
- **MIMOSA-31: prototype for ILD-VXD outer layers** ▷ ▷ ▷
  - ⋇ pixels of 35×35 μm^2 (power saving)
  - ⋇ 48 columns of 64 pixels ended with 4-bit ADC (1/10 of full scale chip)
    - $\hookrightarrow$ expect $\sigma_{sp} \lesssim$ 3.5 μm
  - ⋇ $t_{r.o.} \sim$ 10 μs (1/10 of complete column)
  - ⋇ beam tests (DESY) in Q1/2013 $\Rrightarrow$ σ_{sp}, ϵ_{det}, fake rate

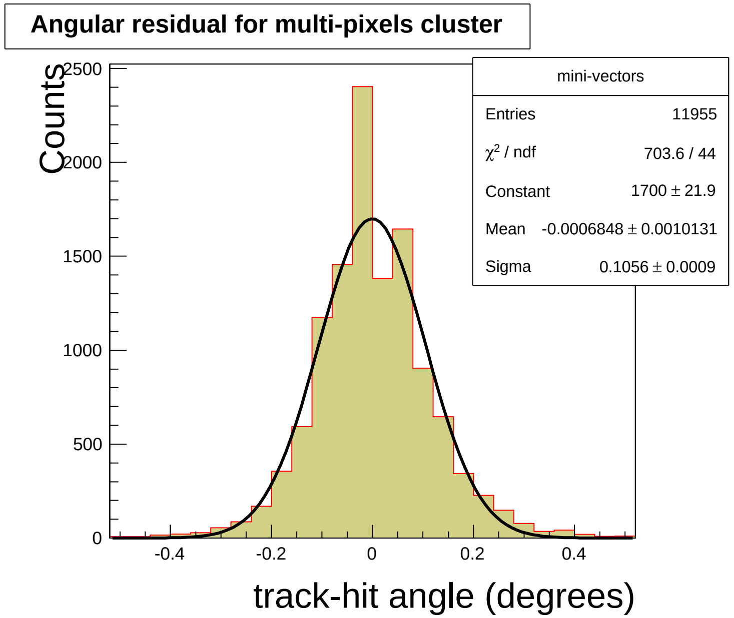


2-Sided Ladder Beam Test Results

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**
  - ⋇ *Beam telescope : 2 arms, each composed of 2 MIMOSA-26 sensors*
  - ⋇ *DUT : 1 PLUME ladder prototype (0.6 % X_0)*
    - $\hookrightarrow$ *6 MIMOSA-26 sensors on each ladder face ($>$ 8 Mpixels)*
  - ⋇ *CERN-SPS beam : $\gtrsim$ 100 GeV "π^-" beam*
  - ⋇ *BT (track extrapolation) resolution on DUT $\sim$ 1.8 μm*
  - ⋇ *Studies with PLUME perpendicular and inclined ($\sim$ 36°) w.r.t. beam line*
  - ⋇ *Preliminary results (no pick-up observed): combined impact resolution & pointing resolution*



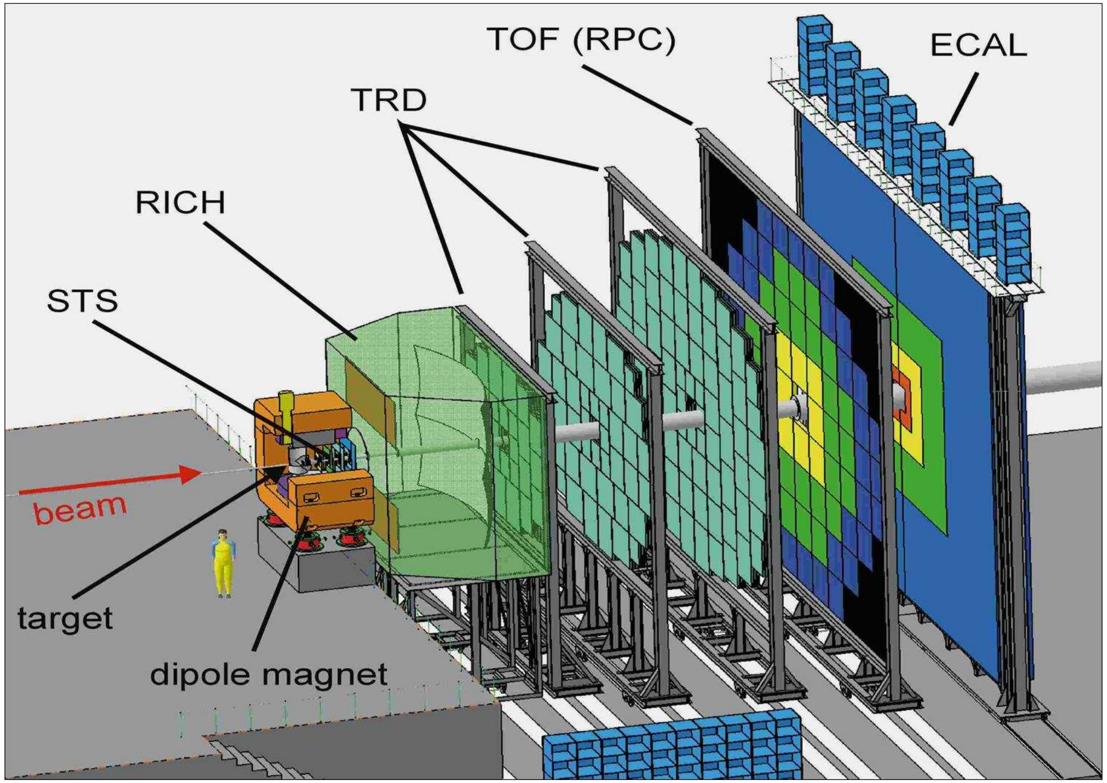




- **New PLUME proto. under construction with 0.35 % X_0** (X-sect.) $\longrightarrow$ **beam tests in Q4/2012** (SPS ?)

Applications of CPS : the CBM H.I. Experiment

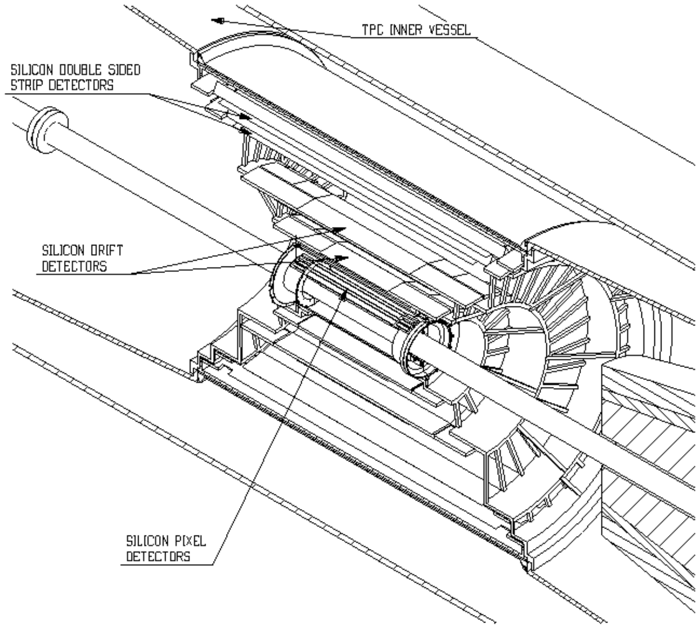
- **Cold Baryonic Matter (CBM) experiment at FAIR/GSI:**
  - ⋇ Micro-Vertex Detector (MVD) made of 2 or 3 stations located behind fixed target
  - ⋇ double-sided stations equipped with CMOS pixel sensors
  - ⋇ **operation a negative temperature in vacuum**
  - ⋇ each station accounts for $\lesssim$ 0.5 % X_0
  - ⋇ sensor architecture close to ILC version



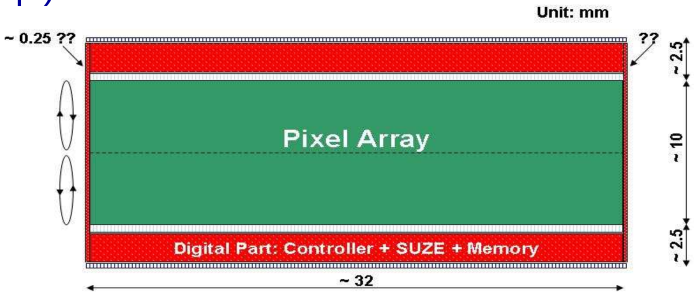
- **Most demanding requirements :**
  - ⋇ ultimately ($\gtrsim$ 2020): 3D sensors
    $\lesssim$ 10 μs, $>$ $10^{14} n_{eq}/cm^2$, $\gtrsim$ 30 MRad
  - ⋇ intermediate steps: 2D sensors
    $\lesssim$ 30-40 μs, $>$ $10^{13} n_{eq}/cm^2$, $\gtrsim$ 3 MRad
  - ⋇ 1st sensor for SIS-100 (data taking $\gtrsim$ 2018)

Applications of CPS : ALICE-ITS Upgrade

- **ITS upgrade :** envisionned for "2017-18" LHC long shutdown
  - ⋇ exploits space left by replacement of beam pipe with small radius (19 mm) section
  - ⋇ consists (at least) in adding L0 at $\sim$ 22 mm radius (potentially : replace part of the ITS)
  - ⋇ 2 main pixel options considered (CDR) :
    - ◇ Hybrid pixel sensors with reduced material budget & pitch
    - ◇ CPS derived from STAR-PXL (ULTIMATE/MIMO-28)



- **Differences w.r.t. ULTIMATE/M-28 :**
  - ⋇ $>$ 1 MRad & 10^{13}n$_{eq}$/cm^2 at T = 30°C (target values)
    $\hookrightarrow$ 0.18 μm triple-well HR-epi techno. (instead of 0.35 μm double-well hR-epi)
  - ⋇ $\sim$ 1$\times$3 cm^2 large sensitive area (instead of 2$\times$2 cm^2)
  - ⋇ double-sided read-out (instead of single-sided) $\rightarrowtail$ $\lesssim$ 10 μs
  - ⋇ 1 or 2 output pairs at $\gtrsim$ 300 MHz (instead of 1 output pair at 160 MHz)
  - ⋇ possibly: 2-sided ladder derived from PLUME ($<$ 0.5 % X$_0$)

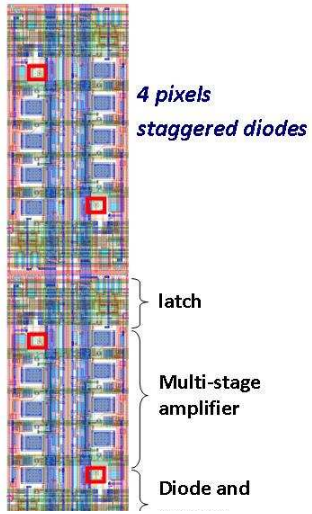


▷▷▷ **Conceptual Design Report delivered to LHCC in March 2012** ▷ ▷ ▷ **techno. choice $\lesssim$ Q1/2013 (?)**

$\hookrightarrow$ **includes Muon Forward Tracker (MFT) based on CPS**

Read-Out Acceleration

- **Motivations (w.r.t. occupancy) :**
  - ⋇ required for ALICE-ITS & -MFT and CBM-MVD (and SuperB-SVT)
  - ⋇ robustness w.r.t. predicted hit rates (e.g. beam BG)
    - $\hookrightarrow$ ILC beam BG ($\gtrsim$ 1 TeV) $\gtrsim 3\times$BG (500 GeV)
  - ⋇ standalone inner tracking capability (e.g. soft tracks)

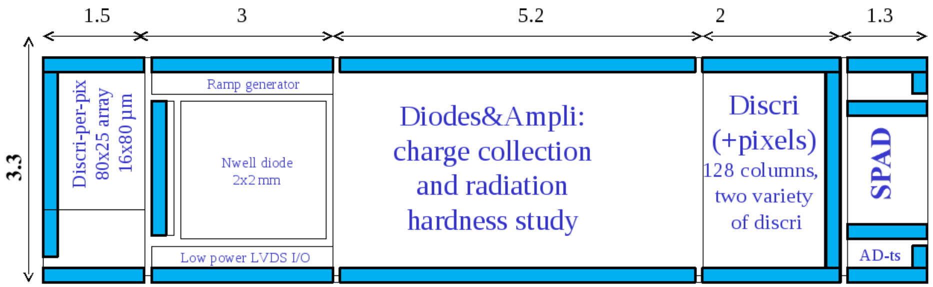


- **How to accelerate the elongated pixel read-out**
  - ⋇ elongated pixel dimensions allow for in-pixel discriminators $\Rrightarrow$ $\geq$ 2 faster r.o. ▹ ▷
  - ⋇ read out simultaneously 2 or 4 rows $\Rrightarrow$ 2-4 faster r.o./side
  - ⋇ subdivide pixel area in 4-8 sub-arrays read out in // $\Rrightarrow$ 2-4 faster r.o./side
  - ▷ 0.18 μm CMOS process needed
    - $\hookrightarrow$ 6-7 ML, Ion. Rad. tol., design compactness, in-pixel PMOS T, ...

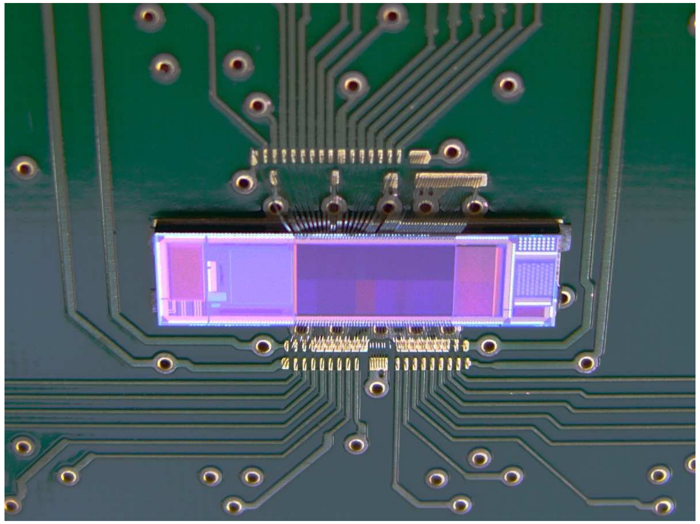
  - ⋇ conservative step: 2 discri./column **end** (22 μm wide)
    - $\Rrightarrow$ read out 2 rows simultaneously
    - $\hookrightarrow$ 1st stage improvement: 50/10 $\mu s \rightarrowtail$ 25/5 μs
    - (5 μs also achievable with 0.35 μm technology)

MIMOSA-32 : Prototyping a 0.18 μm Process

- **0.18 μm imaging technology options used :**
  - ⋇ Epitaxial layer: **High-Resistivity (1-5 $k\Omega \cdot cm$)** & "18 μm" thick $\Rrightarrow$ SNR, rad. tol., ...
  - ⋇ Quadruple well: deep P-type skin embedding N-well hosting P-MOS transistors $\Rrightarrow$ compactness, power, ...
  - ⋇ MIM capacitors
  - ⋇ start with 4 Metal Layers (6 ML run in 2012 chips)
  - ⋇ etc.



- **Prototype sub-divided in several blocks :** ▷ ▷ ▷
  - ⋇ Sensing elements and in-pixel amplifiers :
    - ⊸ pixel dimensions : 20×20/40/80 μm^2
    - ⊸ 2 different types of sensing elements : diodes of ∼ 9–15 μm^2
    - ⊸ N-MOS and P-MOS transistor based amplifiers
  - ⋇ Discriminators :
    - ⊸ Col. // pixel array ended with 1 discriminator/col. (2 variants)
    - ⊸ Pixel array with in-pixel discriminator (16×80 μm^2 pixels)
  - ⋇ Total surface ∼ 43 mm^2



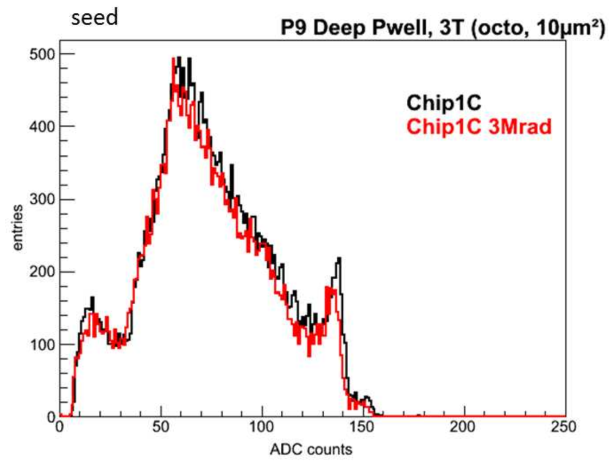
- **Mimosa-32 fabricated in Q4/2011 $\Rrightarrow$ Laboratory tests since April '12**

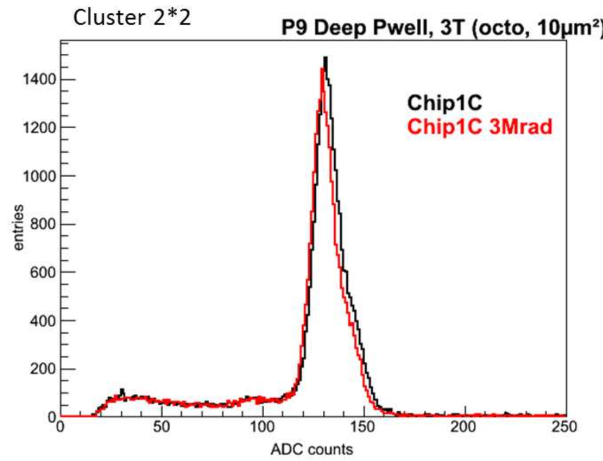
Preliminary 0.18 μm Process Test Results

- **MIMOSA-32 lab tests (^{55}Fe source) of pixel matrix with analog output $\rightarrowtail$ Very preliminary results :**
  - ⋇ Read-out time of each sub-matrix = 32 μs
  - ⋇ Observed CCE (20×20 μm^2 pixels) :
    - ∘ seed pixel : ∼ 40–50 % ▷ ▷ ▷ ▷
    - ∘ 2×2 pixel cluster : nearly 100 % ▷ ▷ ▷ ▷

      $\Rrightarrow$ confirms Epi. layer 1-5 $k\Omega \cdot cm$
    - ∘ No parasitic charge coll. seen with Deep P-well
    - ∘ CCE of 20×40 μm^2 pixels

      ↪ seed ∼ 30 % and with 1st crown ∼ 75 %



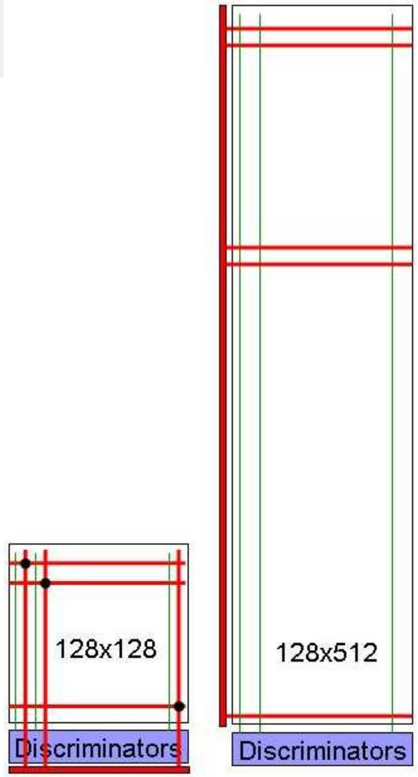


  - ⋇ Noise ∼ 20 e$^-$ ENC at 20°C , unchanged at 35°C **(tbc !)**
  - ⋇ Irradiation: 0.4/1/3 MRad $\rightarrowtail$ ∼ no effect up to 35°C **(tbc !)**
  - ⋇ Difficult to find operating regime of in-pixel ampli. due to inaccurate simul. **models** $\Rrightarrow$ pixel design optimisation ?

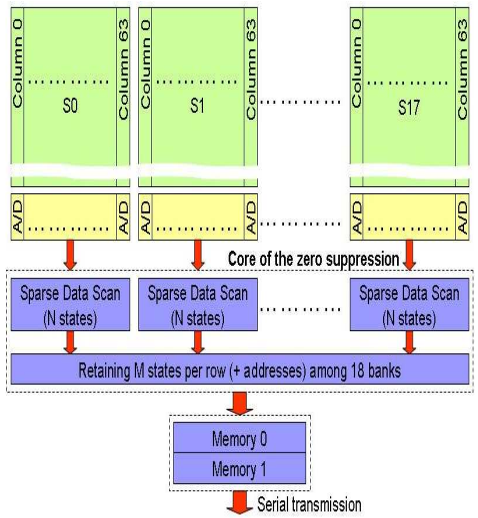
- **Next steps :**
  - ⋇ Beam tests of pixel matrix foreseen in June-July 2012 (incl. NI radiation tolerance assessment)
  - ⋇ Lab and beam tests of digital matrix through Summer 2012
  - ⋇ Lab tests of in-pixel discriminator array in Q3-Q4/2012 (tbc)
  - ⋇ **MIMOSA-32bis** fab. in Spring'12 with standard epitaxial layer $\rightarrowtail$ lab tests in Summer 2012
  - ⋇ **Submission of MIMOSA-32ter** (July 2012) with alternative in-pixel amplification schemes

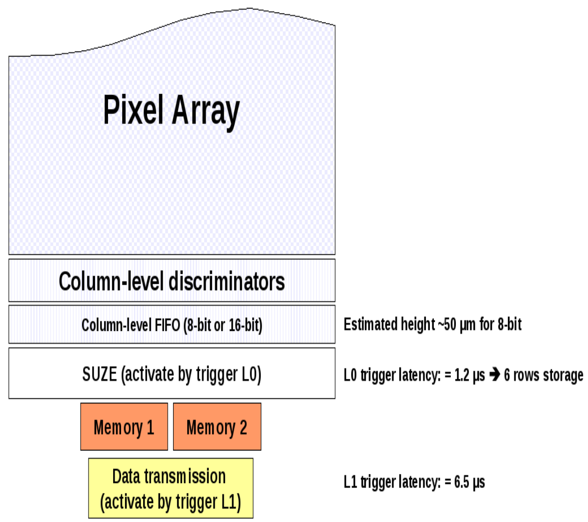
MISTRAL: 0.18μm Architecture Prototyping

- **1st Objective : MISTRAL ≡ MIMOSA FOR THE INNER SILICON TRACKER OF ALICE**
- **MIMOSA-22THR (Upstream part of MISTRAL) :**
  - ⁜ Col. // pixel array with in-pixel ampli + pedestral subtraction (cDS)
  - ⁜ Each of 128 columns ended with discriminator + 8 columns without discri.
  - ⁜ Pixel array sub-divided in sub-arrays featuring different pixel designs (22×22/44 μm^2)
  - ⁜ 2 options for July'12 submission :
    - ○ end of column discriminator ≡ translation of MIMOSA-22AHR (0.35 techno.)
    - ○ simultaneous 2-row encoding & 2 discriminators/column ⇛ twice faster



- **AROM-1 (Accelerated Read-Out Mimosa)**
  - ⁜ in-pixel discri. & simultaneous 4-row encoding ⇛ 8 times faster
  - ⁜ submission in Octobre'12
- **SUZE-02 (Downstream part of MISTRAL) :**
  - ⁜ ∅ μ-circuits & output buffers (≡ SUZE-01)
  - ⁜ add trigger L0 info after discriminators for data filtering ⇛ flow & power reduction
  - ⁜ add trigger L1 downstream of output buffers for further filtering ⇛ flow & power
  - ⁜ submission in Octobre'12

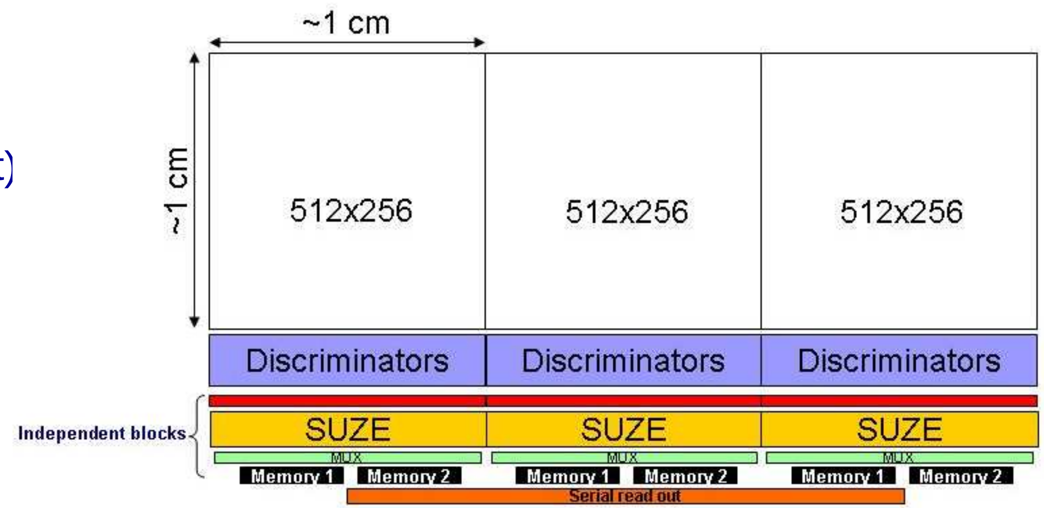




MISTRAL : Final Steps

- **FSBB (Full Scale Basic Block) :**
  - ⋇ Composition :
    - ⊸ Pixel array with $\sim$ final pixel design ($\sim$ 1 cm^2)
    - ⊸ Final r.o. circuitry ($\emptyset$, filtering, data transmission, ...)
    - ⊸ All read-out circuitry split in elementary blocks according to **stitching** design rules ⟼ AIDA-BT
  - ⋇ Submission : Summer 2013 (?)

- **MISTRAL :**
  - ⋇ Composition :
    - ⊸ 3 full-size adjacent FSBB (1-sided read-out) or 6 half FSBB (2-sided read-out)
    - ⊸ Complemented with serial r.o. circuitry
  - ⋇ Submission : Summer 2014 (?)

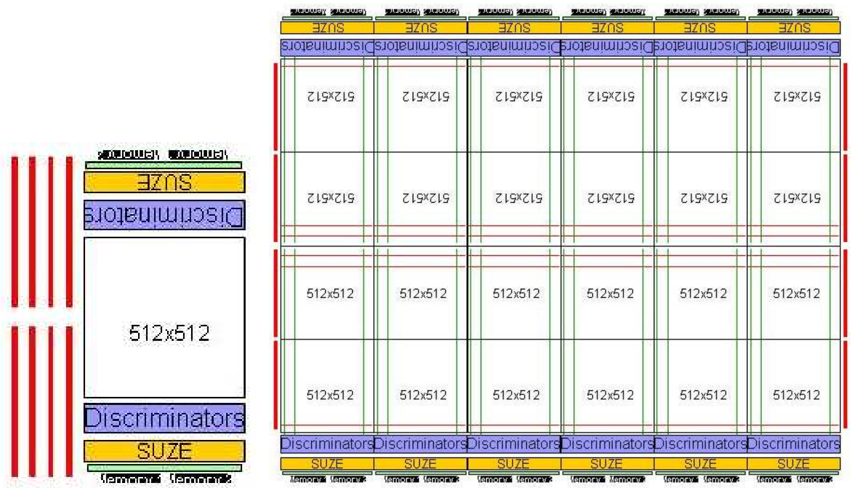


- **Start MIMAIDA & MIMOSIS designs (+ others ?) :**

  ↪ submission in 2015

AIDA Project : Assessment of Stitching & 2-Sided Ladder

- **Single Arm Large Area Telescope (SALAT) :**



✳ *2048×3072 pixels (∼ 20 μm pitch)*

$\Rrightarrow$ *4×6 cm^2 sensitive area, ∼ 3.5 μm spatial resolution*

✳ *requires combining several reticules (based on FSBB)*

$\Rrightarrow$ *stitching process* $\Rrightarrow$ *establish proof of principle*

✳ *2-sided read-out of 1024 rows in ∼ 200 μs*

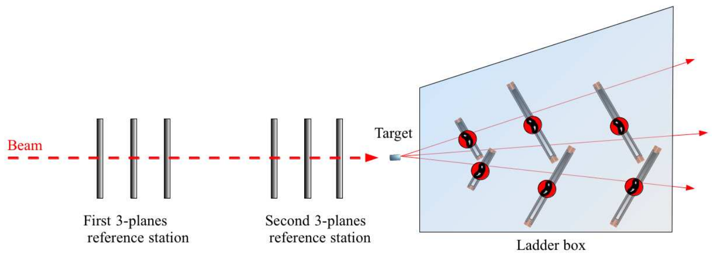
$\Rrightarrow$ *3 planes of Large Area Telescope for AIDA project (EU-FP7)*

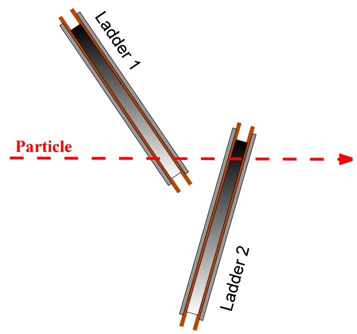
✳ *windowing of $\lesssim$ 1×6 cm^2 (collimated beam)*

$\Rrightarrow$ *∼ 50 μs r.o. time*

✳ *50-100 μm pitch variants under consideration (trackers)*

- **Alignment Investigation Device (AID) :**





✳ *box allowing to mount 3-4 pairs of ladders arranged in 3-4 consecutive layers ≡ VTX sector*

✳ *can be equipped with PLUME (2-sided) ladders*

✳ *ladders mounted on movable micrometric supports*

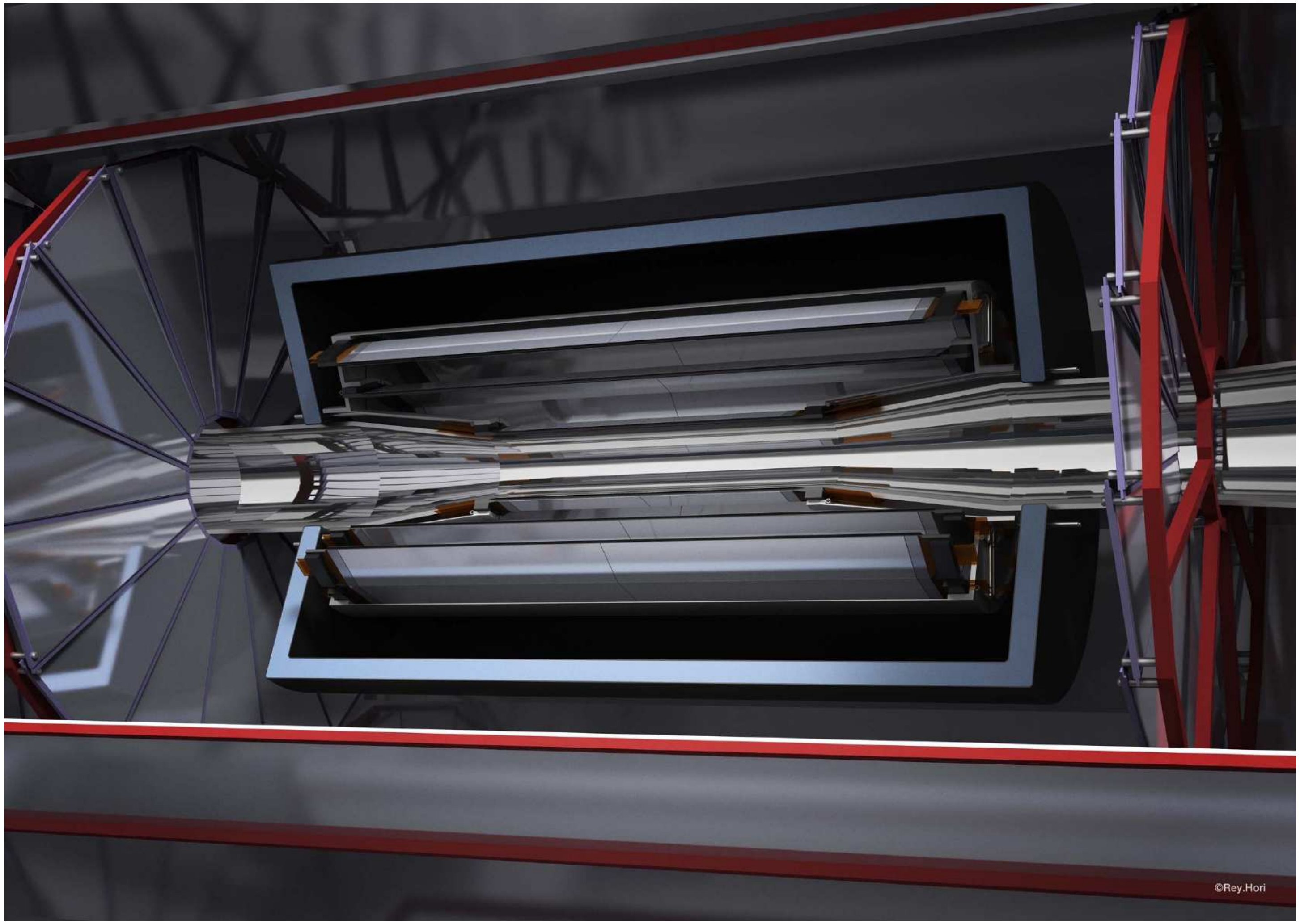
$\Rrightarrow$ *investigate alignment with particles traversing overlapping regions of neighbouring ladders*

✳ *allows developing clustering, tracking & vertexing algo. with particle beams*

Synergy with ILC Vertex Detectors

- **Specs of ALICE-ITS/-MFT, CBM-MVD, SuperB-SVT, AIDA, ... overlap those of ILC Vertex Detectors**

Example of ILD-VXD



MIMOSA & AROM Sensors for an ILC Vertex Detector

- **Assuming MIMOSA and AROM variants to equip innermost and outer layers**
  - ⋇ MIMOSA-in and AROM-1 equip innermost layer
  - ⋇ MIMOSA-out and AROM-2 equip outer layers

Sensor version	**MIMOSA-in**	**MIMOSA-out**	**AROM-1**	**AROM-2**
Active area dimensions $[\text{mm}^2]$	8.7×31.0	19.6×31.0	10.9×31.0	20.8×31.0
Pixel dimensions $[\mu m^2]$	17×17	34×34	17×85	34×72
Single point resolution $[\mu m]$	$\lesssim 3$	$\lesssim 4$	5-7	~ 10
Read-out time $[\mu s]$	50	~ 100	1.5	7
Power consumption: instantaneous [W]	~ 1.8	~ 0.6	2.7	0.7
average [mW]	36	12	55	14

- **Power consumption (average value stands for 5 ms long power-on periods $\equiv$ 2% duty cycle):**
  - ⋇ layer 1: 250 W (inst.) $\Rrightarrow$ 5 W (average)
  - ⋇ layer 2: 120 W (inst.) $\Rrightarrow$ 2.4 W (average)
  - ⋇ layer 3: 200 W (inst.) $\Rrightarrow$ 4 W (average)

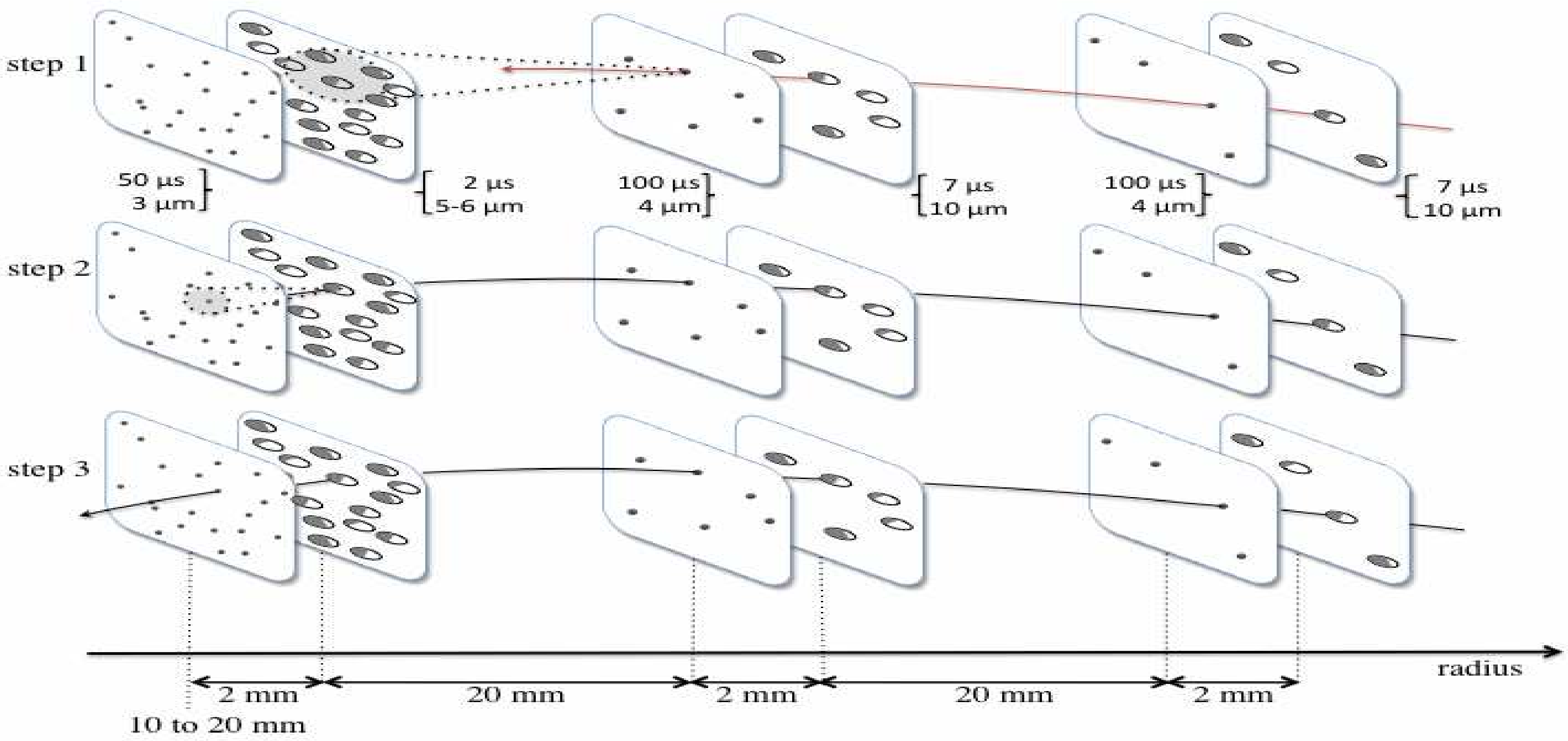
$\Rrightarrow$ **Complete detector instantaneous power $\lesssim$ 600 W $\Rrightarrow$ $<$12 W in average $\Rrightarrow$ air cooling OK**

▷ ▷ ▷ power cycling still needs being investigated $\longmapsto$ power $>$ 100 ladders ($<$10 g) with $\sim$200 A in 3.5 T !!!

Tracking through ILD-VXD

- **Tracking from outside towards IP combining MIMOSA spatial resolution & AROM timestamp**

  ⋇ MIMOSA provides < 3 or 4 μm spatial resolution   ⋇ AROM provides < 2 or 7 μs time stamping



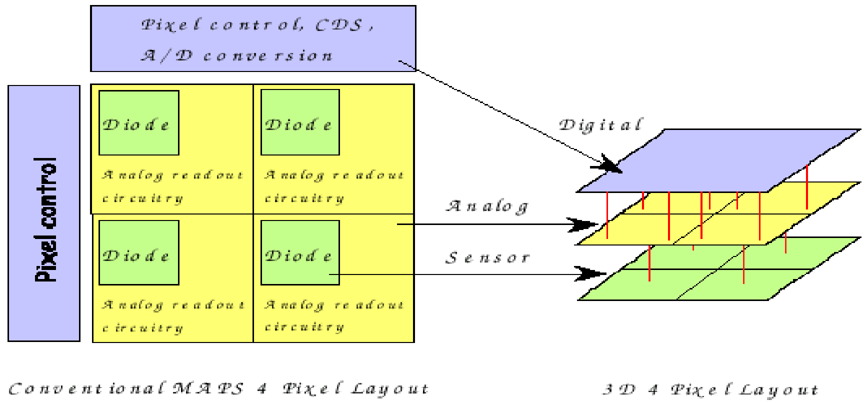
	M-in	A-1	M-out	A-2	M-out	A-2
Pixel occupancy [%] :	0.9	0.1	0.3	0.04	0.06	0.01
with safety factor 3 [%] :	2.6	0.3	0.9	0.1	0.2	0.03

Using 3DIT to reach Ultimate CMOS Sensor Performances

- 3D Integration Technologies allow integrating high density signal processing μcircuits inside **small** pixels by stacking ($\sim$ 10 μm) thin tiers interconnected at pixel level

- 3DIT are expected to be particularly beneficial for CMOS sensors :
  - ⋇ combine different fab. processes $\Rrightarrow$ chose best one for each tier/functionnality
  - ⋇ alleviate constraints on peripheral circuitry and on transistor type inside pixel, etc.

- Split signal collection and processing functionnalities :
  - ⋇ *Tier-1: charge sensing*
  - ⋇ *Tier-2: analog-mixed μcircuits*
  - ⋇ *Tier-3: digital μcircuits*



- **The path to nominal exploitation of CMOS pixel potential :**
  - ⋇ fully depleted 10-20 μm thick epitaxy $\Rrightarrow$ $t_{collect} \lesssim$ 5 ns, rad. hardness $>$ Hybrid Pixel Sensors ???
  - ⋇ FEE with $\leq$ 10 ns time resolution $\rightarrowtail$ solution for CLIC & HL-LHC specifications ???

- **3DIC coordinated by FNAL produced painfully 1st generation of chips (debugging process)**

  Devt of CAIRN $\equiv$ **C**MOS **A**ctive pixel sensors with vertically **I**ntegrated **R**ead-out & **N**etworking functionnalities

SUMMARY (MIMOSA/AROM based Subatomic Phys. Trackers)

- **Increasing demand for highly granular & thin (low power) pixel devices (charm tagging) :**

  $\Rrightarrow$ CPS offer the highest potential for these applications (also for large areas $\rightarrowtail$ cost, power)

- **R&D of 1st generation CPS (0.35 μm) $\sim$ completed:** STAR-PXL, CBM-MVD1, ...

  $\hookrightarrow$ **ILD-VXD sensors** comply with all specs for 500 GeV : σ_{sp}, thickness, rad.tol., speed, power

- **2-sided ladder (0.3% X_0) & unsupported ladder (0.15 % X_0) devts progressing :** PLUME, SERNWIETE

  $\hookrightarrow$ allows for $<$ 3 μm / 2 μs in ILD-VXD innermost layer ($<$ 3.5 μm / 7 μs in outer layers)

- **R&D of 2nd generation CPS (0.18 μm) started with MIMOSA-32: radiation tol. & read-out speed**
  - Several MIMOSA-32 lab test results encouraging : CCE, Ion. Rad. tol., noise at 35°C
  - Beam tests in Summer 2012 for m.i.p. detection performance assessment (incl. NI rad. tol.)
  - Present sources of investigation : inaccurate in-pixel μcircuitry modeling, noise $\gtrsim$ 30 % too high at 20°C

- **Next steps of 0.18 μm based sensor devt $\equiv$ important milestones :**
  - Establish high-performance in-pixel signal amplification μ-circuitry in Q3/Q4 2012
  - Mid-scale prototypes validating architectures (MIMOSA-22THR, AROM-1, SUZE-02) in Q3/Q4 2012
  - Full Scale Basic Block (FSBB) expected to be fabricated in 2013
  - Dedicated sensors $\gtrsim$ 2014: ALICE-ITS/-MFT, CBM-MVD2/-MVD3, **ILC-500/1000**, AIDA, SuperB-SVT, eIC, ...

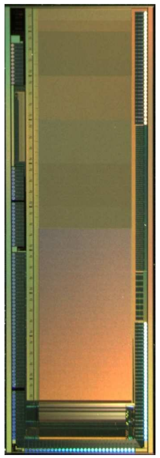
- **Long term R&D : 3D sensors for CLIC, HL-LHC, etc. $\rightarrowtail$ CAIRN chips under devt**

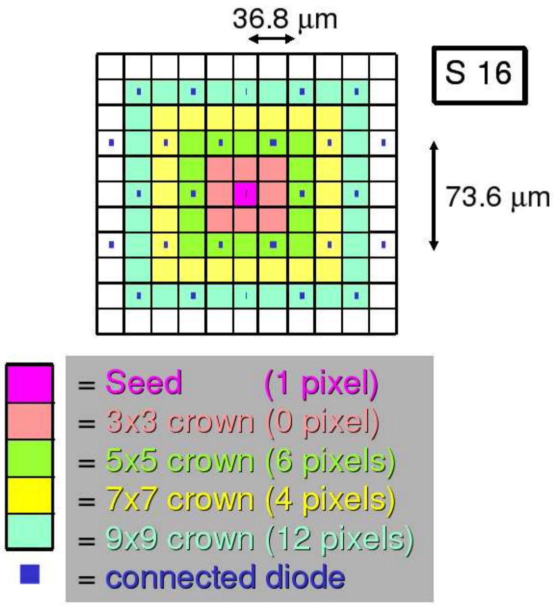
Towards a Large Pitch

- **Large pitch : Motivations**
  - ⋇ elongated pixels allow faster read-out
  - ⋇ trackers (e.g. ILD-SIT) require $\sigma_{sp} \gtrsim 10\ \mu m$
  - $\Rightarrow$ minimise number of pixels for the sake of power dissipation, integration time and data flow

- **Large pitch : Limitations (besides spatial resolution)**
  - ⋇ DANGER: increasing distance inbetween neighbouring diodes
    - $\Rightarrow$ particles traversing sensor "far" from sensing diodes may not be detected because of e^- recombination
  - ⋇ "fragile" detection efficiency, exposed to losses due to irradiation, high temperature operation & "slow" read-out

- **Elongated pixels : Test results**
  - ⋇ elongated pixels allow minimising the drawbacks of large pitch
  - ⋇ concept evaluated with MIMOSA-22AHR prototype,
    composed of a sub-array with 18.4×73.6 μm^2 pixels ▷▷▷
  - ⋇ m.i.p. detection performances assessed at CERN-SPS (T $\sim$ 15°C)
    - —o $\epsilon_{det} \sim 99.8$ %
    - —o $\sigma_{sp} \sim$ 5-6 μm (binary charge encoding)





- **Square pixels : prototype back from foundry**
  - ⋇ MIMOSA-29 : fabricated on high-resistivity epitaxy in Summer '11
  - ⋇ pixels of 64×16/32/64 μm^2 and 80×16/48/80 μm^2
  - ⋇ chips back from foundry $\Rightarrow$ test preparation under way

VXD - SIT Variant Composed of CPS

- **ILD-SIT : baseline assumes 2 double-sided μstrip detector layers**
  - ⋇ try understanding if CMOS sensors could improve performance with their high spatial resolution
  - ⋇ advantage : spatial resolution ▷ 4×4 μm^2 instead of 7×50 μm^2

    ⇛ improved soft track reconstruction (p) and TPC link

    potentially : material budget, cost
  - ⋇ disadvantage : time resolution ▷ 7 μs instead of O(100)ns – Is power a pb ?
- **Variant of VXD–SIT design made of CMOS pixel sensors (other variants give similar performances)**

Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	**Occupancy [%]** w/o safey factor	**Power** inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs	0.9(2.6) / 0.1(0.3)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs	0.3(0.9) / 0.04(0.1)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs	0.06(0.2) / 0.01(0.03)	200/4 W
SIT-1	4 / 15 μm	100 / 7 μs	$\lesssim$ 0.01	$\sim$ 1.3 kW/26 W
SIT-2	4 μm	100 μs	$\lesssim$ 0.01	$\sim$ 2.5 kW/50 W

- **ILD-SIT : power consumption** (average $\lesssim$ 100 W for $\gtrsim$ 4 m^2 coverage) **seems affordable**

  ⇛ **need benchmark event study with beam BG to evaluate track reconstruction performance**