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DEPFET
Active Pixel Detector

DEPFET
Active pixel sensors

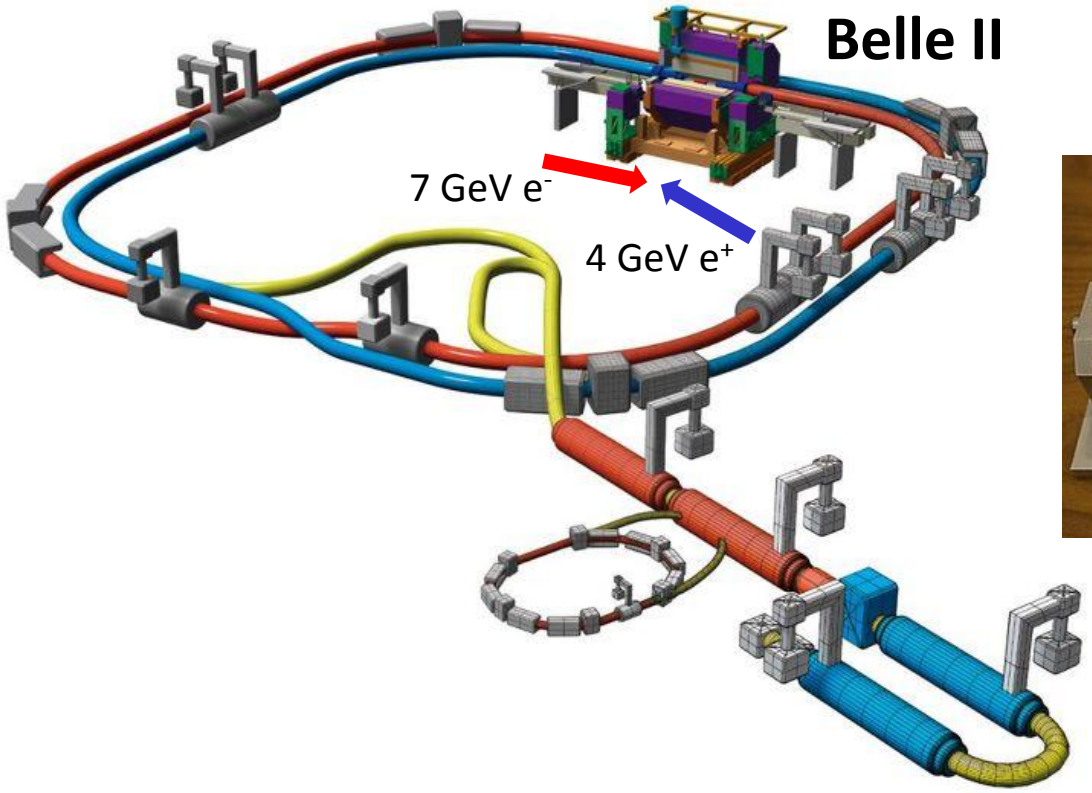
Carlos Marinas
University of Bonn

On behalf of the DEPFET Collaboration

Outline

- SuperKEKB and ILC
  - Common requirements
- DEPFET
  - Fundamentals
  - System elements
- Recent progress
  - PXD6 production
  - Test beam
  - Mechanics and cooling

KEKB upgrade plan: SuperKEKB Flavour Factory



- Asymmetric energy (4 GeV, 7 GeV) e^+e^- collider at the E_{cm}=m(Y(4S)) to be realized by upgrading the existing KEKB machine
- Final luminosity $8 \cdot 10^{35}$ cm^{-2} s^{-1}, 40 times higher than the existing KEKB Factory

The Belle II Collaboration decided on DEPFET as baseline for PXD

↘ Positive impact on DEPFETs for ILC

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ILC and Belle II

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- Both detectors have very similar requirements

	ILC	Belle II
Occupancy	0.13 hits/μm^2/s	0.1 hits/μm^2/s
Radiation	< 100 krad/year	2 Mrad/year
Duty cycle	1/200	1
Frame time	25-100 μs	20 μs
Momentum range	All momenta	Low momentum (< 1 GeV)
Acceptance	6º-174º	17º-155º

- ILC
  - Excellent single point resolution (3-5 μm) → Small pixel size 25 μm^2
  - Low material budget (0.1%X_0/layer)

- Belle II
  - Modest spatial resolution (10 μm) → Moderate pixel size (50 x 75 μm^2)
  - Few 100 MeV momenta → Lowest possible material budget (0.2% X_0/layer**)

** Including support Si, bumps and metal layers

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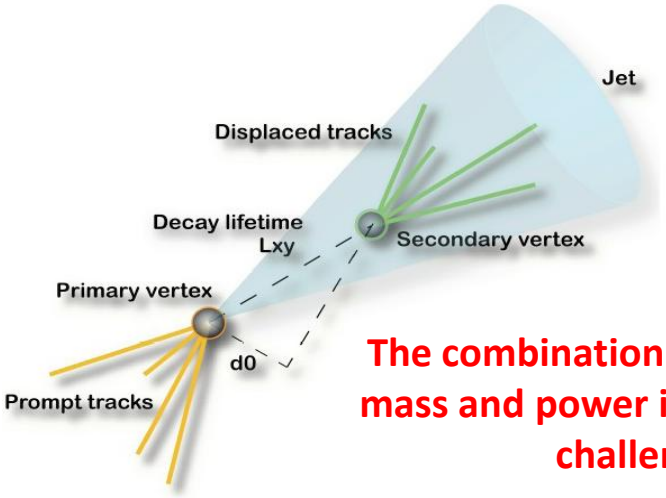
Vertexing requirements



The combination of resolution, mass and power is a substantial challenge

$$\sigma_{d0} \approx a \oplus \frac{b}{p \sin^{\frac{3}{2}} \theta}$$

	a (μm)	b (μm GeV c^{-1})
SLD	9	33
LEP	25	70
LHC	12	70
SuperKEKB	8.5	10
ILC	5	10

M. Winter

- Common requirements to both projects
  - First layer close to the IP
  - Low material budget
    - Reduced services
    - Low power dissipation
  - High granularity
    - Good spatial resolution
  - Fast readout
  - Radiation hardness

Highly pixelated

Transparent

Belle II PXD boosted the development of DEPFET sensors

DEPFET – DEpleted P-channel Field Effect Transistor

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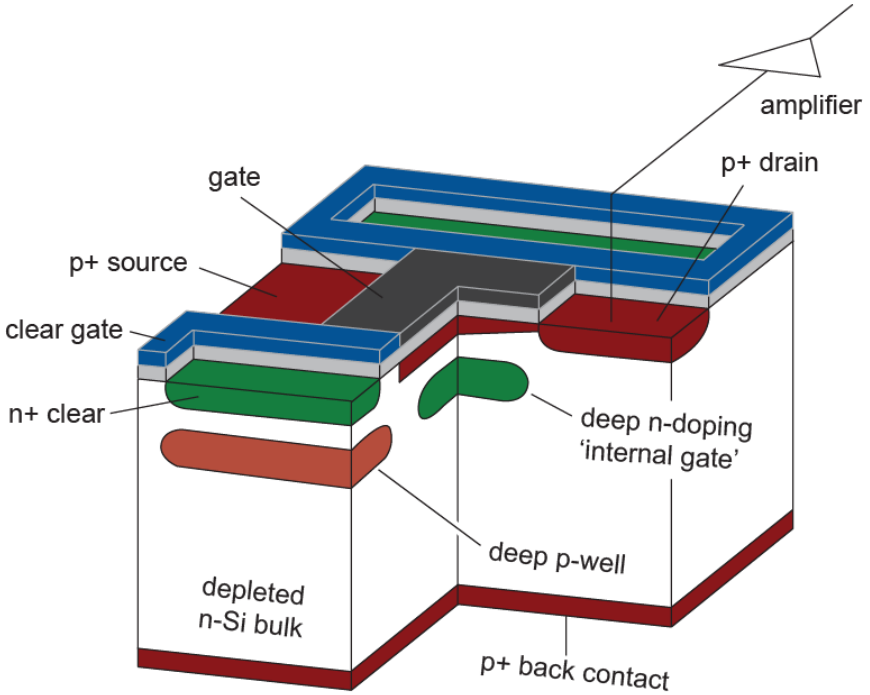
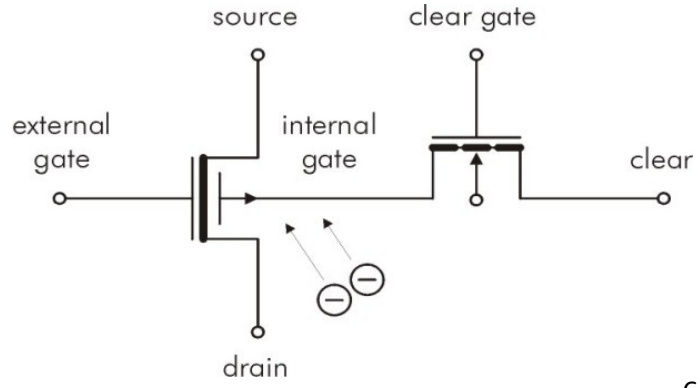
- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)



- Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \approx 400$ pA/e^-)
- Accumulated charge can be removed by a clear contact



- Detection, fast charge collection and internal amplification
- Excellent signal-to-noise ratio
- Low power consumption
- Thin detectors

Features

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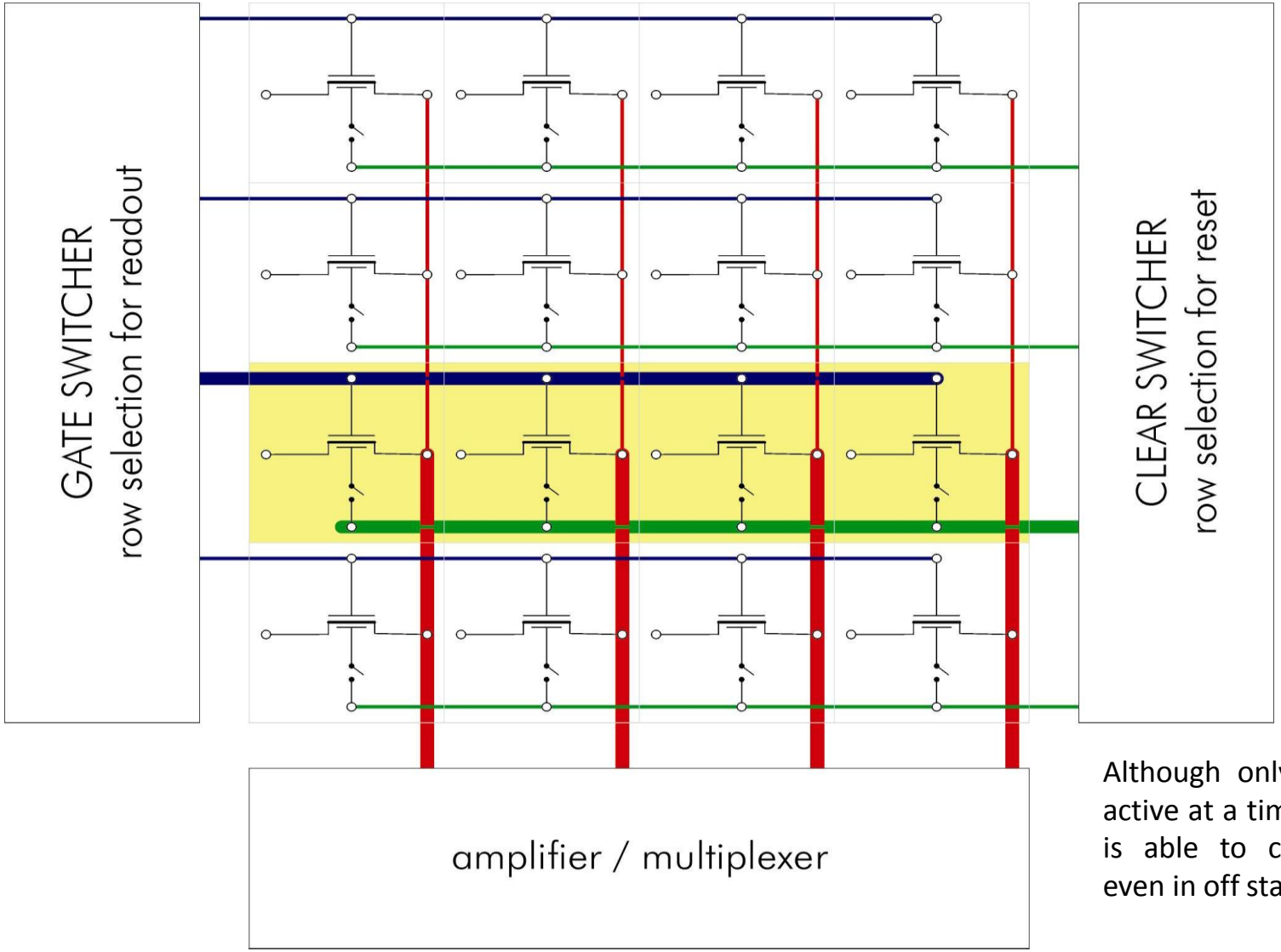
From a transistor to a detector



Although only one row is active at a time, the sensor is able to collect charge even in off state

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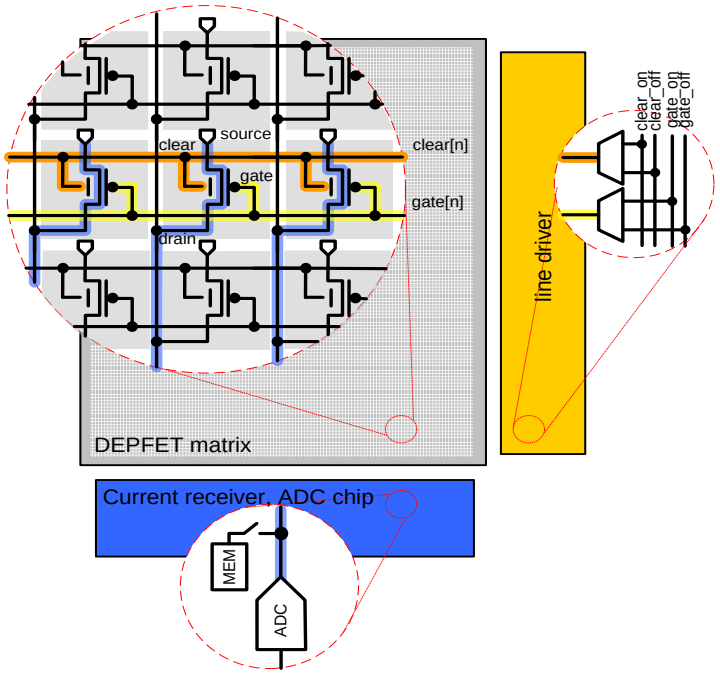
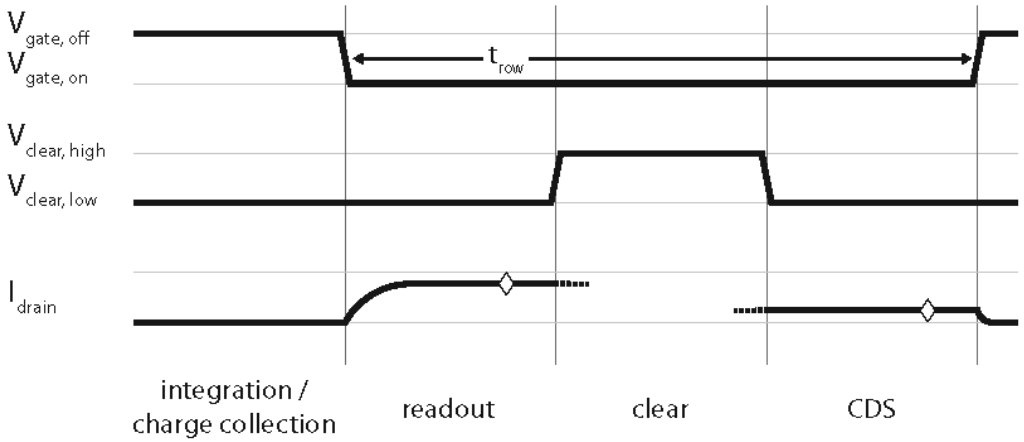
Operation mode: Row-wise readout



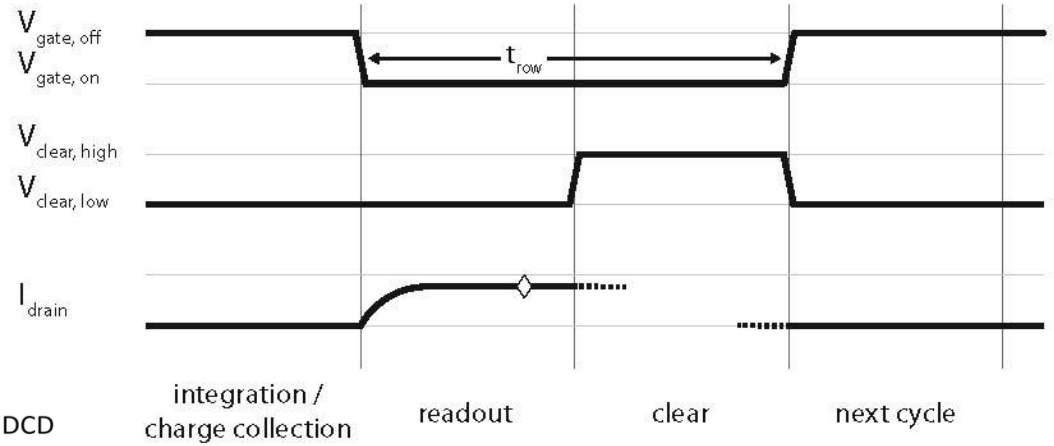


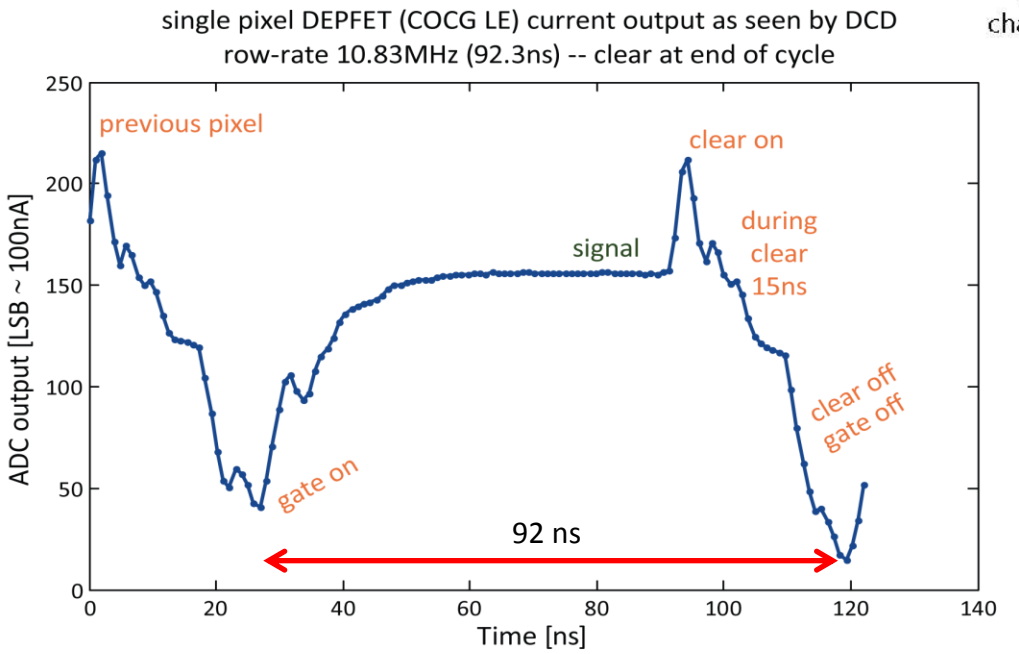
Row-wise readout (Rolling Shutter)

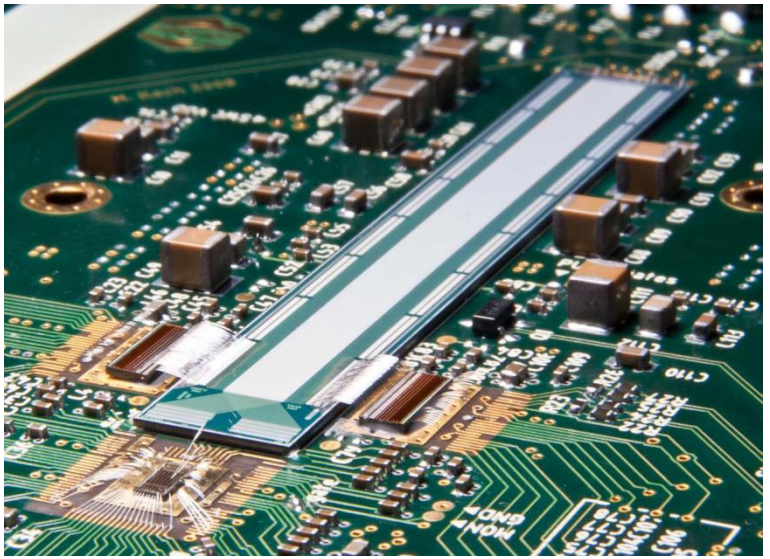
- (If CDS) Select a row, read the current (I_1), clear the DEPFET and read the current again (I_2). $I_{Signal}=I_1-I_2$
- Single sampling with pedestal substraction afterwards (Baseline)
- Low power consumption: Only one row is active at a time; readout on demand.
- Steering chips needed (Switchers) and limited frame rate.

Single sampling

- Abandon CDS in favour of speed, move clear to end of cycle
- Belle II PXD readout time: 20 µs (50 KHz frame rate)
- Read-clear cycle: 100 ns

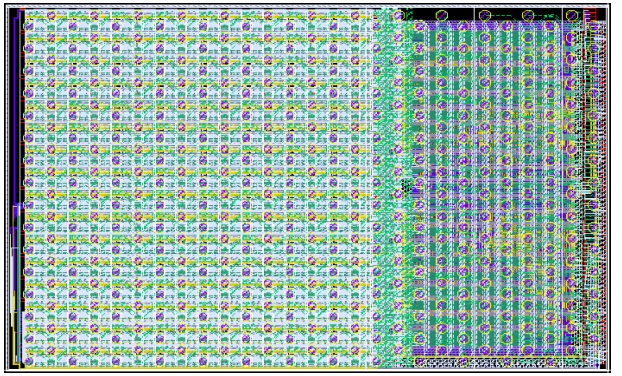






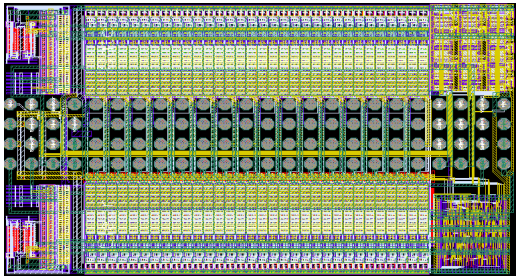
DEPFET auxiliary ASICs

DCDB (Drain Current Digitizer)
Analog frontend

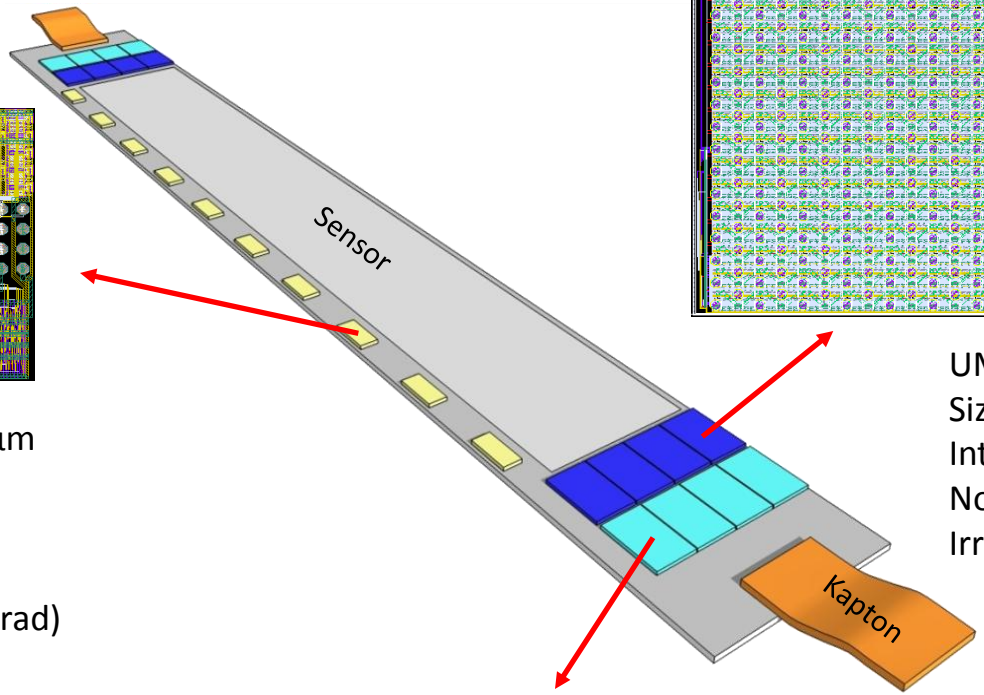


UMC 180 nm
Size 3.3 × 5.0 mm²
Integrated ADC
Noise 40 nA
Irradiation up to 7Mrad

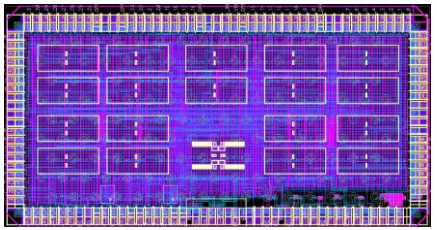
SwitcherB
Row control



AMS high voltage 0.35 µm
Size 3.6 × 2.1 mm²
Gate and Clear signal
Fast HV up to 30V
Rad. Hard proved (36 Mrad)



DHP (Data Handling Processor)
Processor



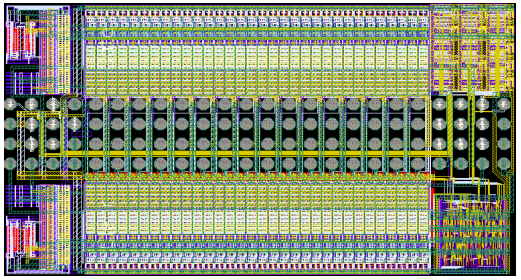
IBM CMOS 90 nm (TSMC 65 nm)
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation

DEPFET auxiliary ASICs

The full-size close to final versions of the ASICs are designed, produced and found to work

SwitcherB

Row control



AMS high voltage 0.35 µm
Size 3.6 × 2.1 mm²
Gate and Clear signal
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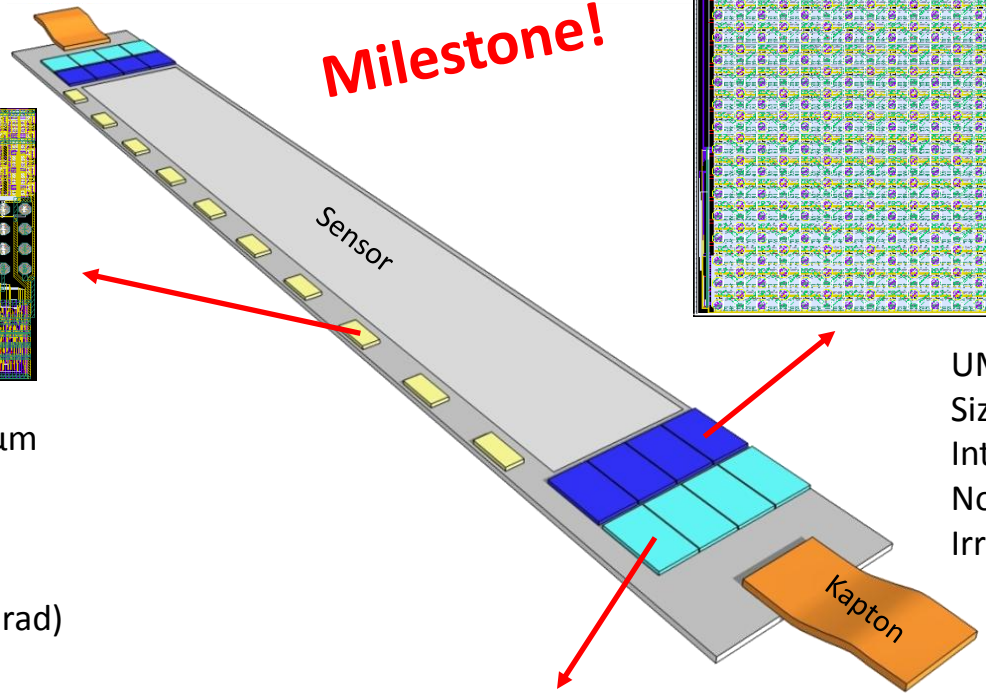
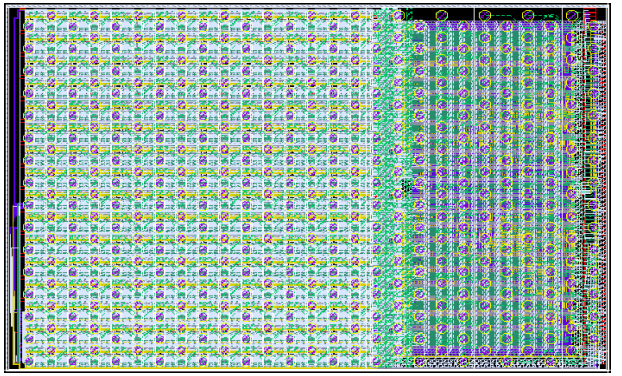
Milestone!



DCDB (Drain Current Digitizer)

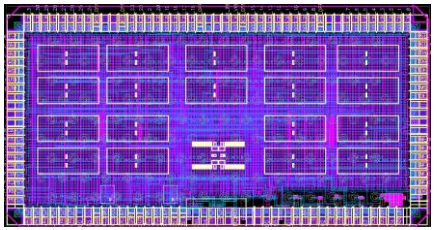
Analog frontend



UMC 180 nm
Size 3.3 × 5.0 mm²
Integrated ADC
Noise 40 nA
Irradiation up to 7Mrad

DHP (Data Handling Processor)

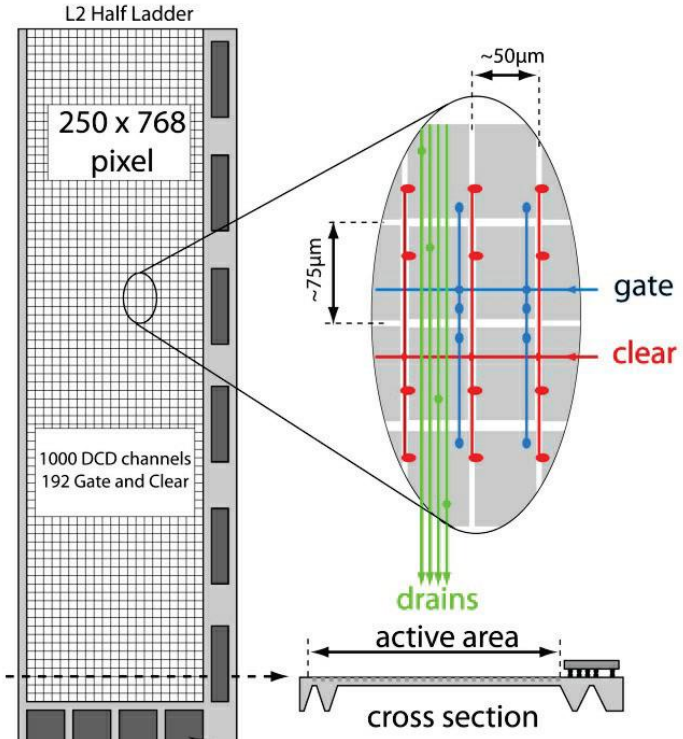
Processor



IBM CMOS 90 nm (TSMC 65 nm)
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation

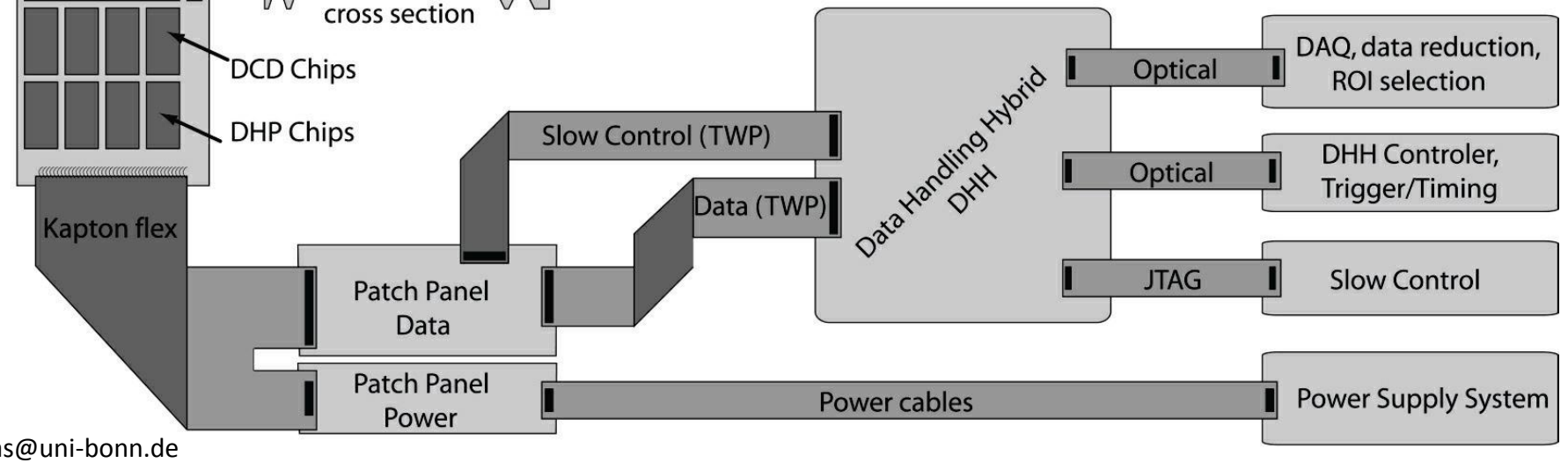
The layout of the module periphery is ready as well

Off-module signal flow



DHH (Data Handling Hybrid): interface with the outside world

- Electrical - optical interface
- Slow control master (JTAG)



Optimization: Full simulation chain

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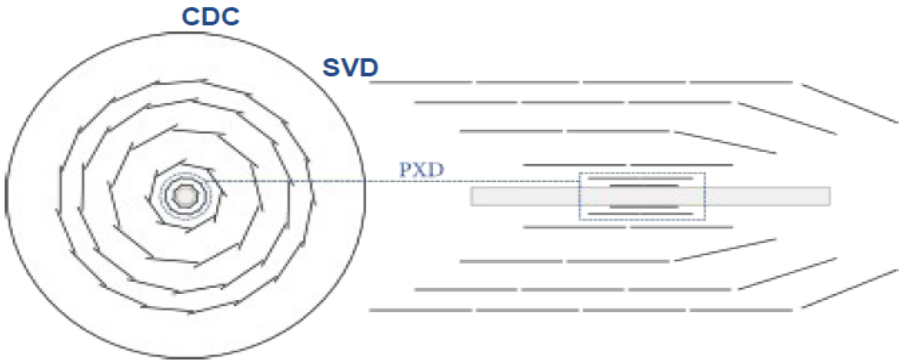
Particle gun (single event)
EvtGen (physics event)
Mokka geometry

Ionization points
Signal points
Electronic noise
Digitization and clustering

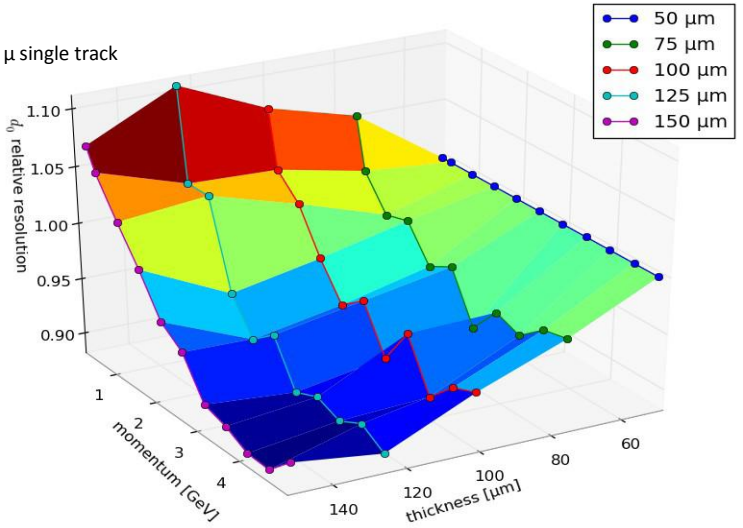
Marlin tracking
PXD+SVD+CDC

Physics channels



- Digitizer (Geant4) tuned with TBeam data:
  - Electric noise
  - Electric field in Si (charge collection time)
  - Lorentz angle in magnetic fields

Optimization studies:
- Sensor thickness
- Pixel size
- Inner layer radius



Optimization: Full simulation chain

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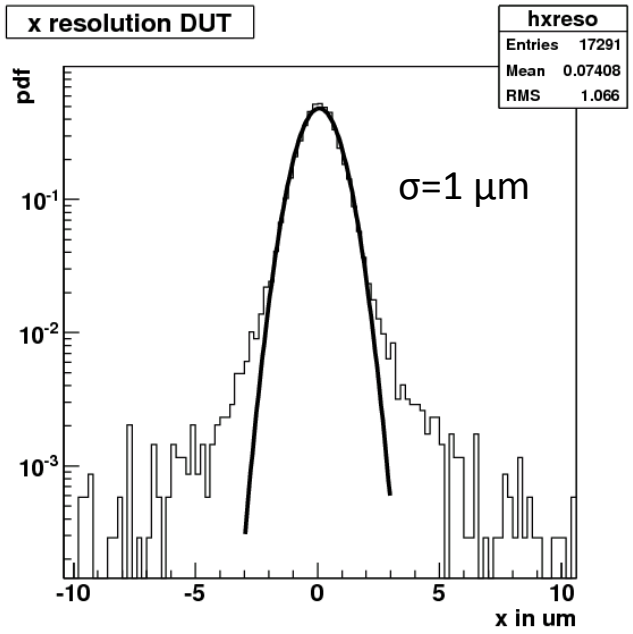
Detector simulation	PXD/SVD Simulation	Track reconstruction	Analysis
Particle gun (single event) EvtGen (physics event) Mokka geometry	Ionization points Signal points Electronic noise Digitization and clustering	Marlin tracking PXD+SVD+CDC	Physics channels

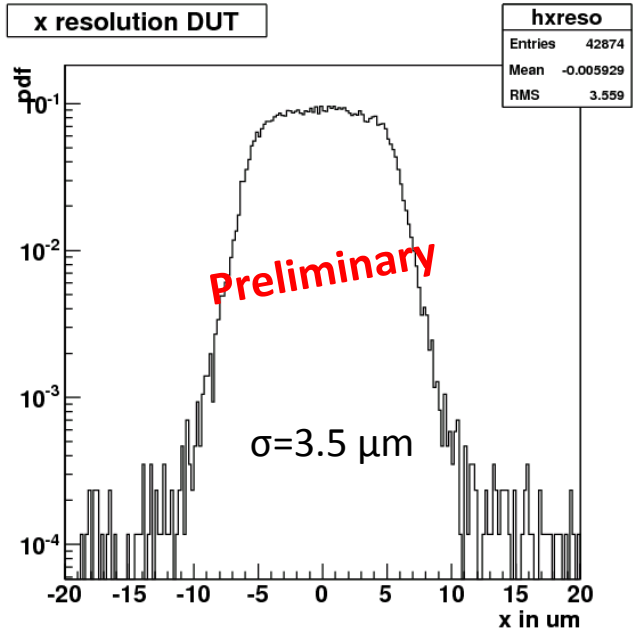
Test Beam Data
20x20x450 µm³
Single point resolution: 1 µm

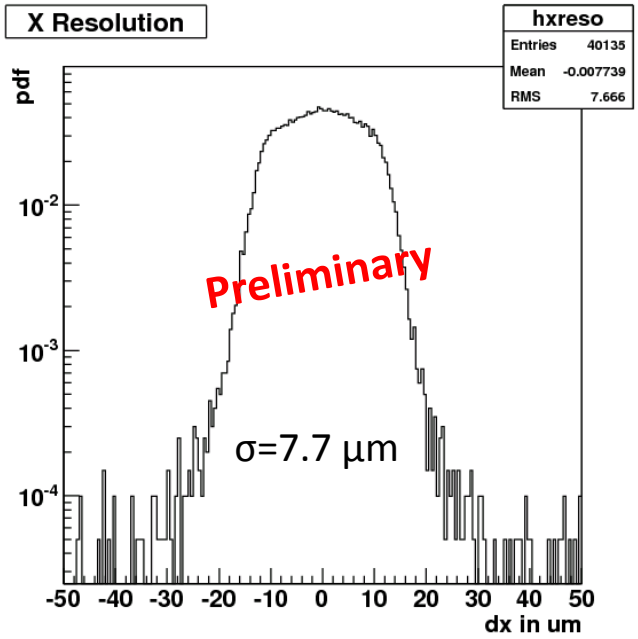
ILC (Simulation)
20x20x50 µm³
Single point resolution: 3.5 µm

Belle II (Simulation)
50x50x75 µm³
Single point resolution: 7.7 µm

→ See slide 20







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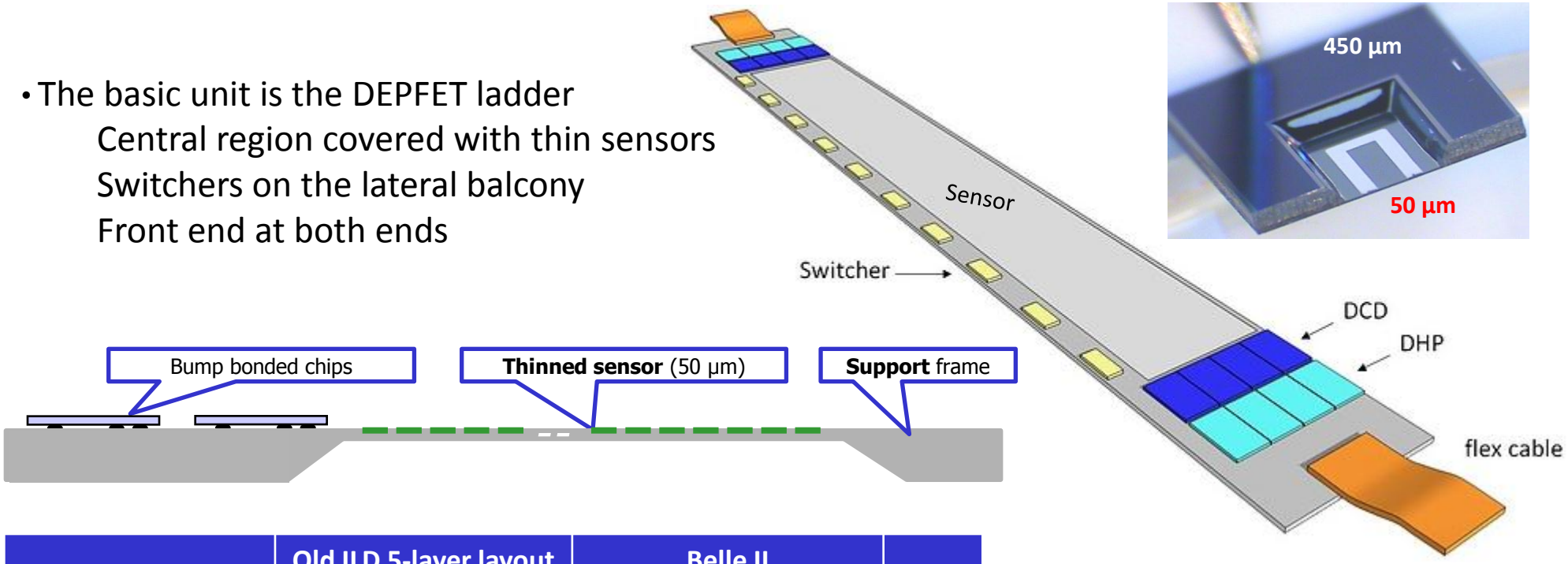
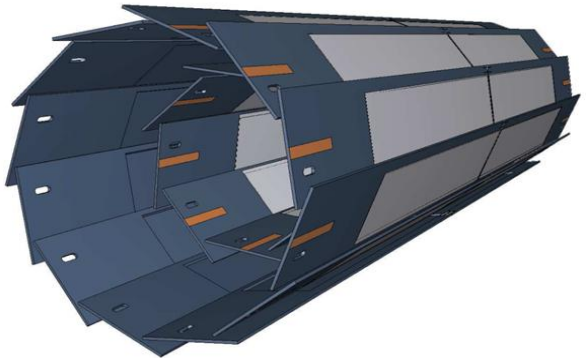
General layout of a DEPFET detector

- The basic unit is the DEPFET ladder
  - Central region covered with thin sensors
  - Switchers on the lateral balcony
  - Front end at both ends



	Old ILD 5-layer layout	Belle II	
Radii	15.5, 26, 38, 49, 60	14, 22	mm
Ladder length	100 (L0), 250 (L1-L4)	136 (L0), 169 (L1)	mm
Sensitive width	13 (L0), 22 (L1-L4)	12.5 (L0-L1)	mm
Number of ladders	8, 8, 12, 16, 20	8, 12	
Pixel size	25x25 (L0-L4)	50x50 (L0), 50x75 (L1)	μm^2
Row rate	40	10	MHz
Number of pixels	800	8	Mpix



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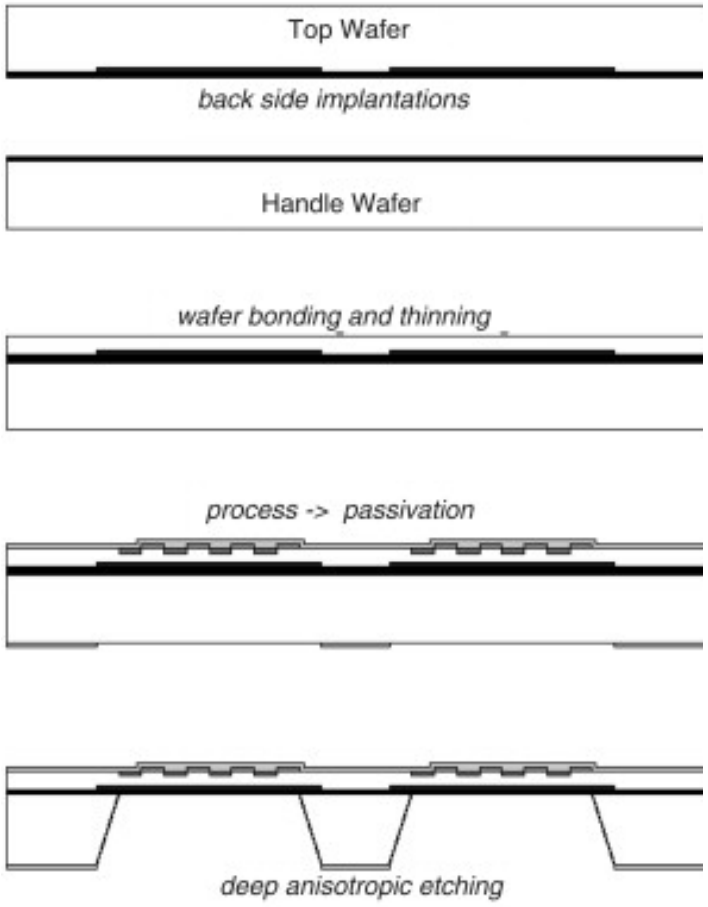
Thinning technology: All silicon sensors

Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor

→ One material uniform and small thermal expansion



- Oxidation and back side implant on sensor wafer
- Wafer bonding (with SiO_2 in between) and grinding/polishing of top wafer. Thin sensor side to the desired thickness
- Process DEPFET on top side → passivation
- Anisotropic deep etching opens “windows” in the handle wafer. Etch backside up to oxide/implant (etch stops SiO_2)

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Thinning technology

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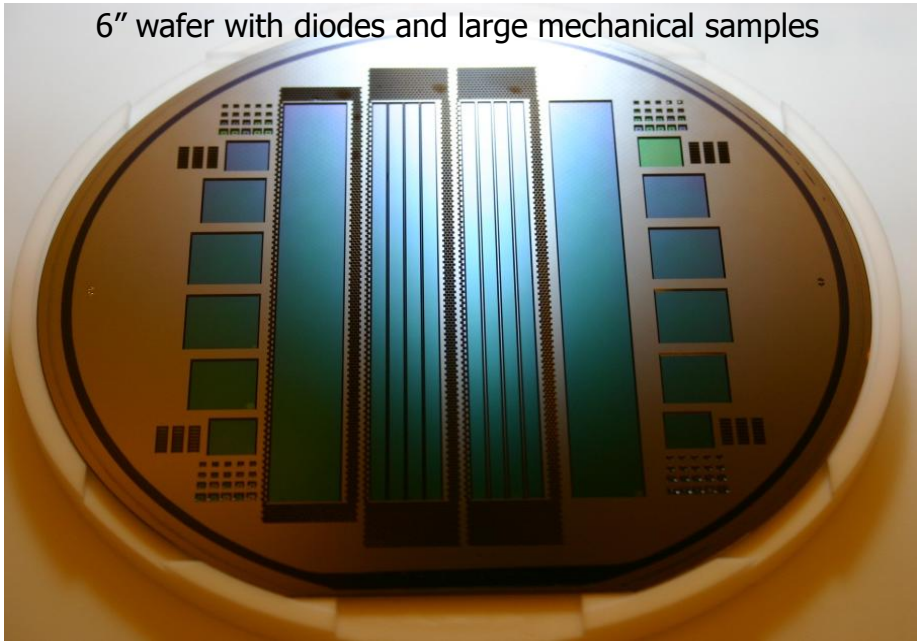
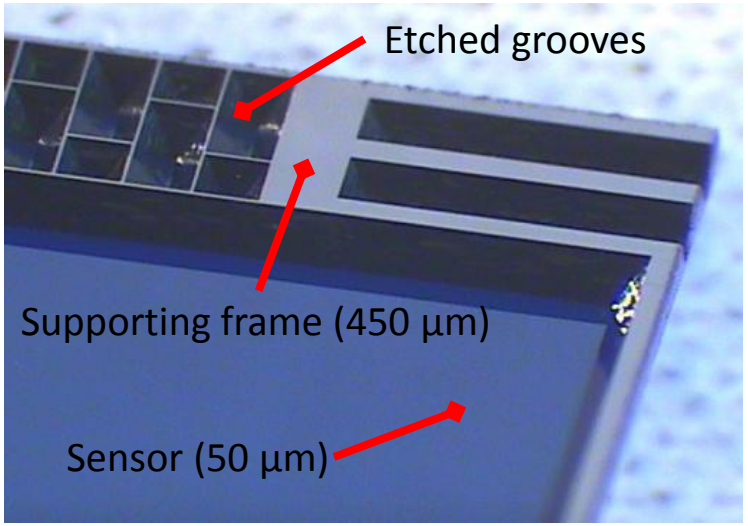
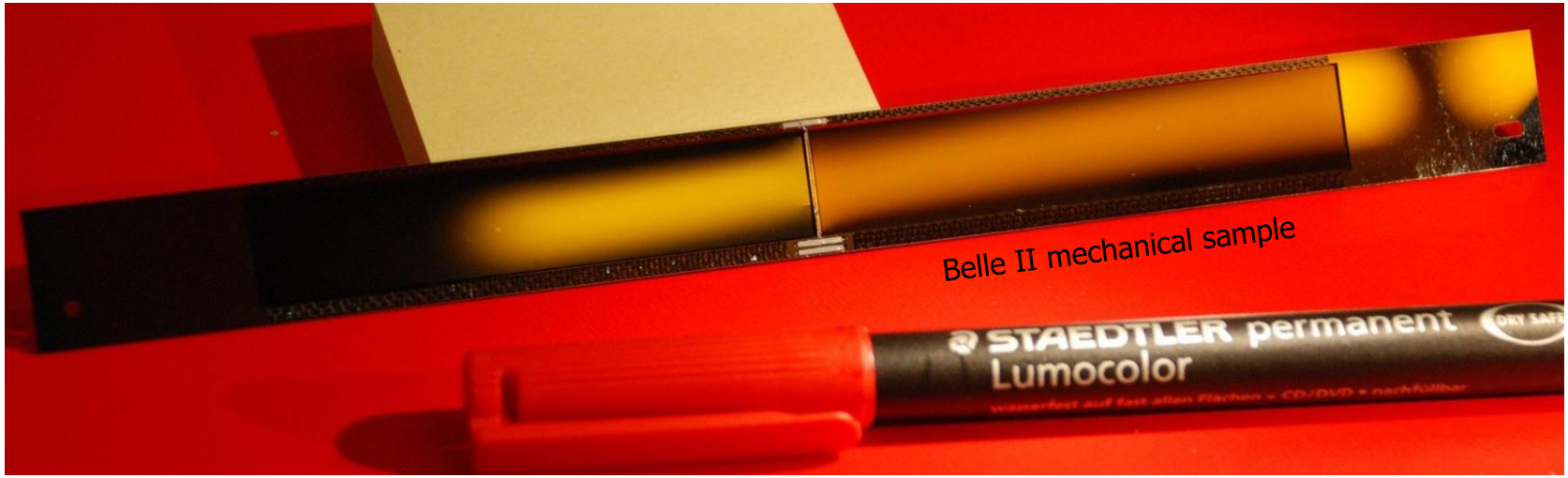
6” wafer with diodes and large mechanical samples

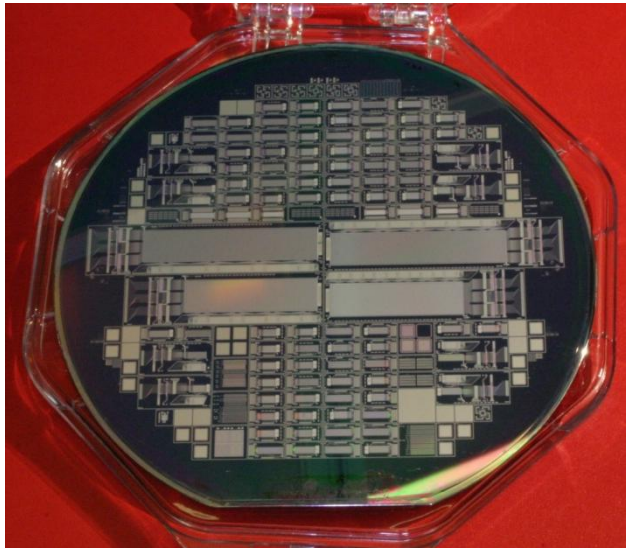


All-silicon sensors

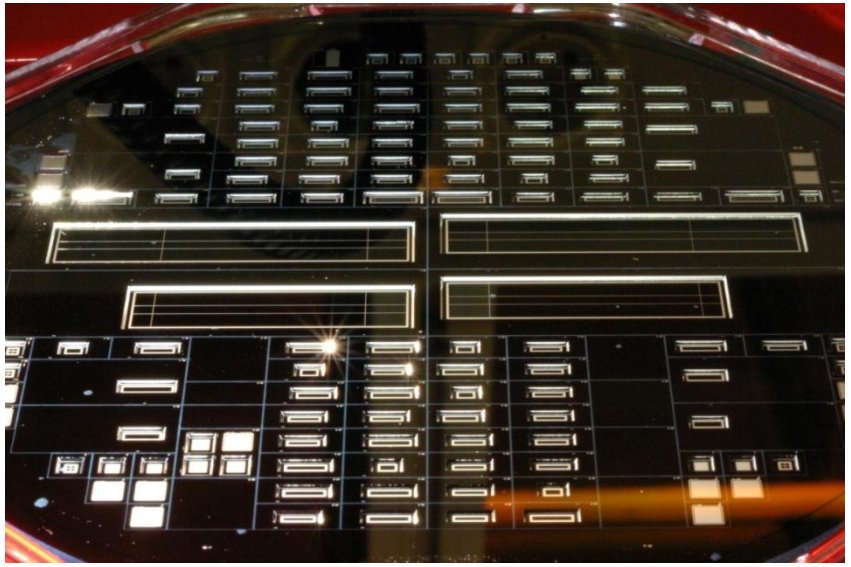


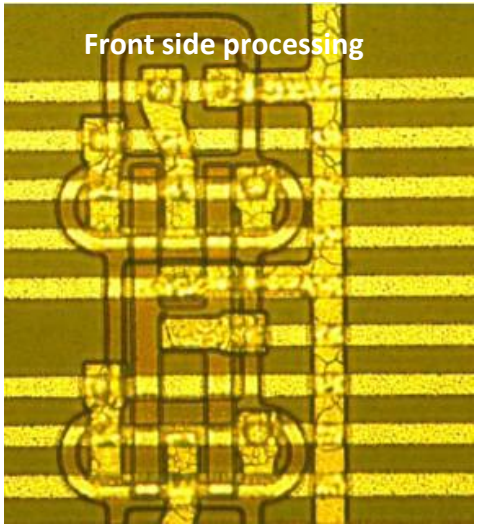


PXD6 prototype production



8 wafers with 50 µm thin sensors
- Small test matrices to test different pixel sizes (50-200 µm)
- Design variations: short gate lengths, clear structures, drift
- Full size sensors –half ladders for prototyping
- Technology variations on the wafer level





90 steps fabrication process:
- 9 Implantations
- 19 Lithographies
- 2 Poly-layers
- 2 Alu-layers
- Back side processing

First thin DEPFET sensors produced!

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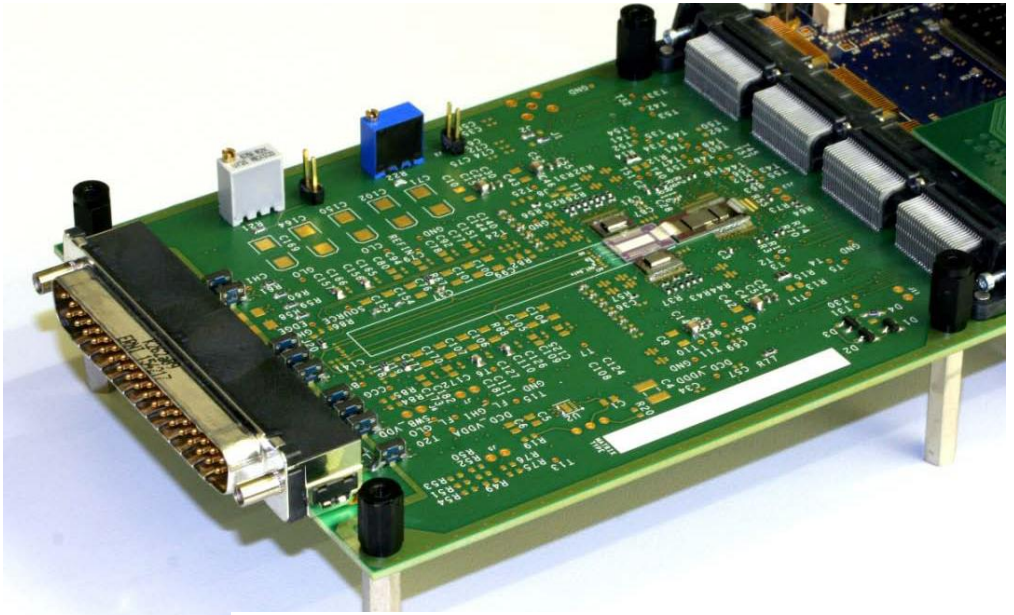
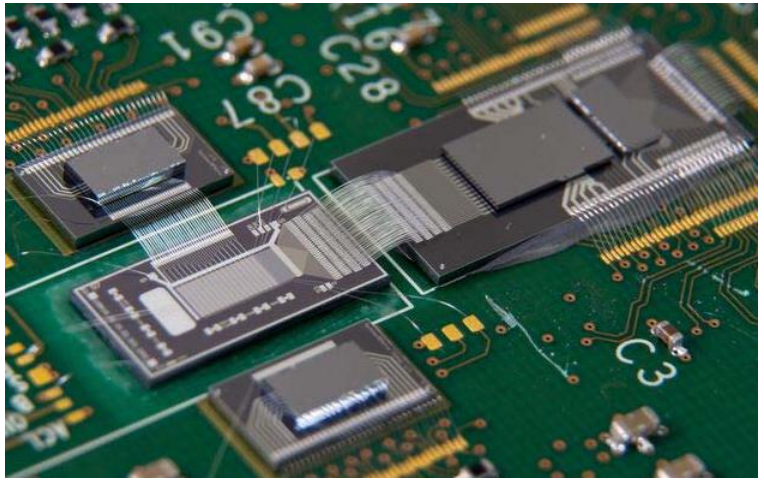
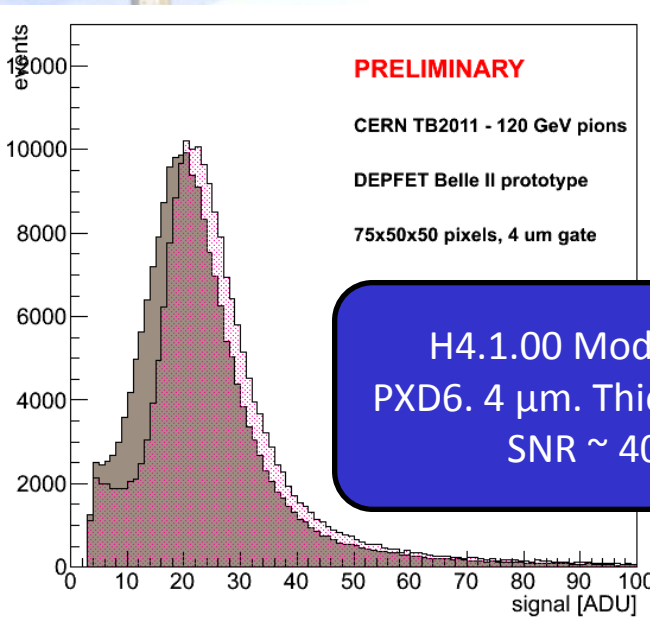
PXD6 - Beam Tests

Belle II design
Sensor 32x64 pixels
50x75x**50** μm^3
SwitcherB and DCDB at full speed
DCDB readout at 320MHz
100 ns row time

Close to final specs!



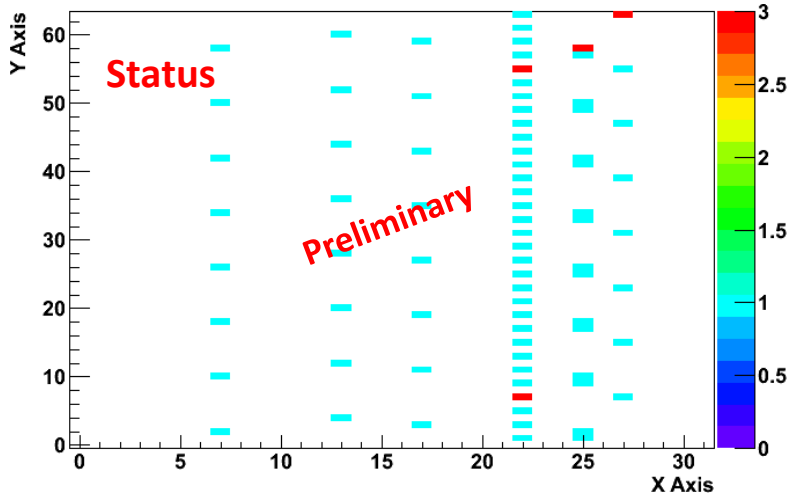




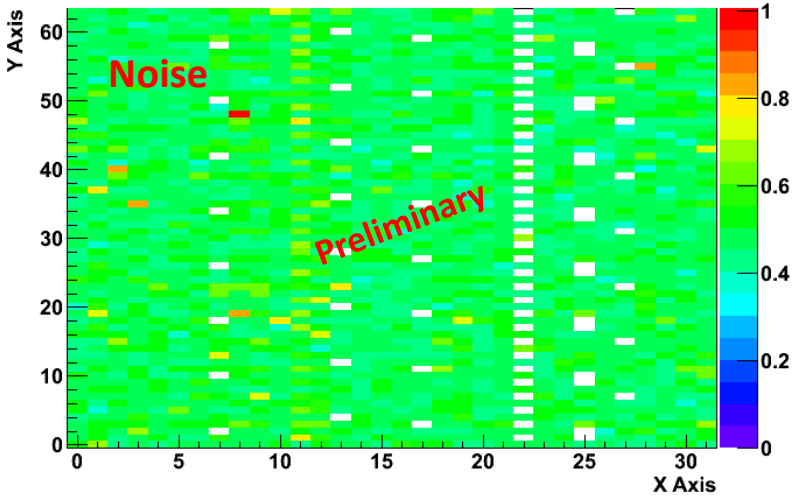
H4.1.00 Module B
PXD6. 4 µm. Thick oxide.
SNR ~ 40

Based on the valuable information obtained with the PXD6, the final Belle II production (PXD9) is already launched

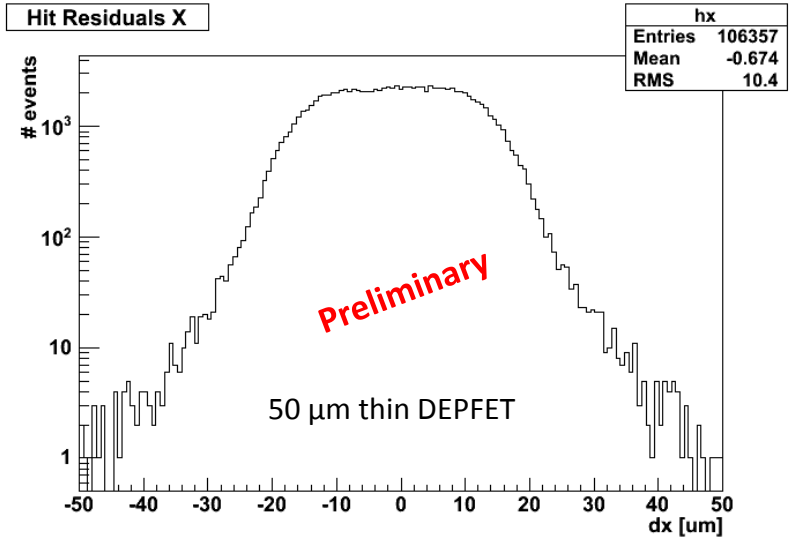
PXD6 - Noise, pedestals, residuals and seed signal



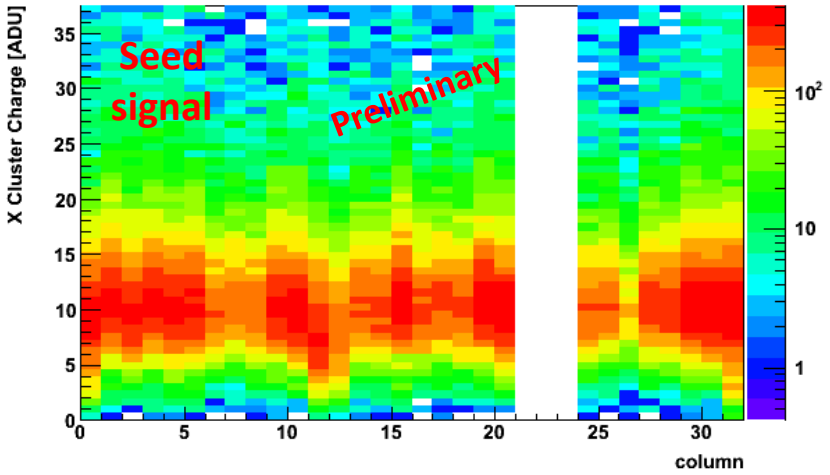
A few dead pixels due to brocken DCDBv1 channels



Homogeneous noise map (0.5 LSB at 100 MHz)



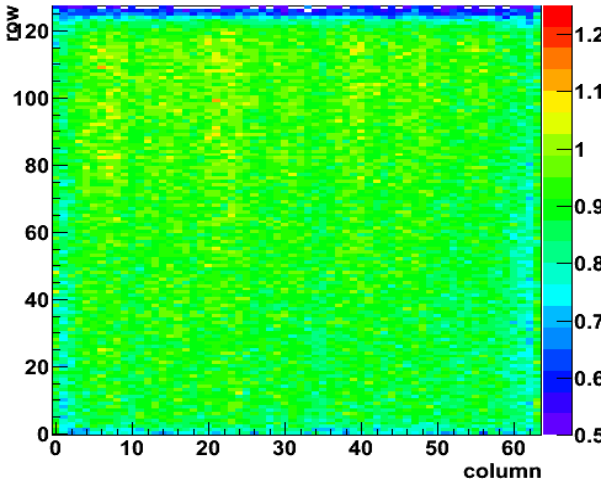
CoG residuals ~ 10 µm

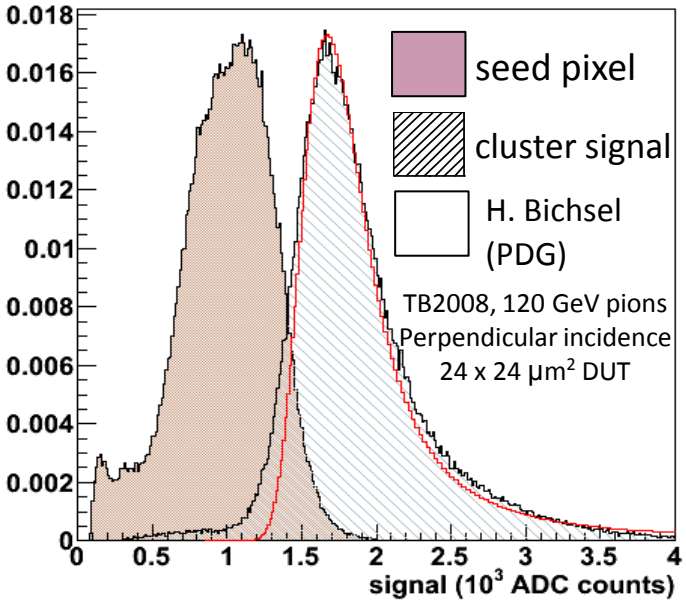


Column wise variations in the order 10%

TB 2008 and 2009: PXD5 ILC sensors

Gain map: Deviation from average seed signal

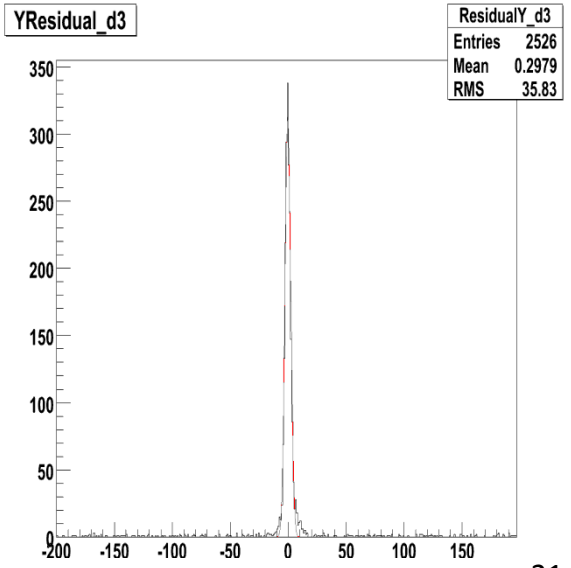




- 64x128, 24x24x450 µm^3 CCG, 6 µm (TB2008)
  g_q=363pA/e$^-$

- 64x256, 20x20x**450** µm^3 CCG, 5 µm (TB2009)
  g_q~650 pA/e$^-$

- Resolution **σ~1 µm**, 20x20x**450** µm^3, analog readout with charge interpolation



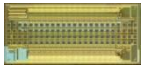
ILC Design

→ Extensively tested

Electronic MultiChip Module (E-MCM)

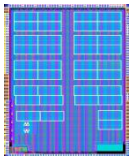
E-MCM: Everything but the DEPFET
Electrically active prototype of a half ladder

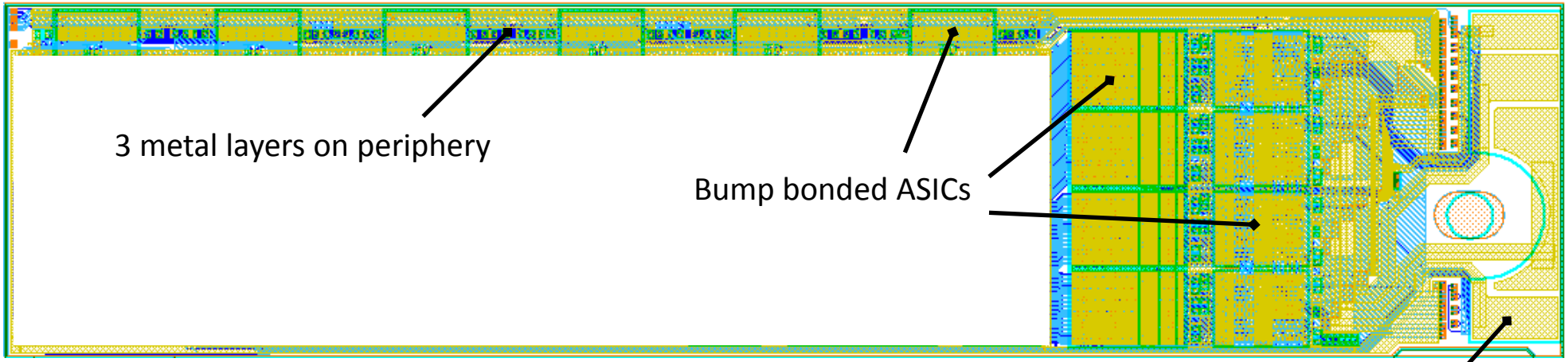
SW



DCD

DHP





Electronic MultiChip Module (E-MCM)

E-MCM: Everything but the DEPFET
Electrically active prototype of a half ladder

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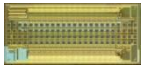
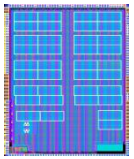
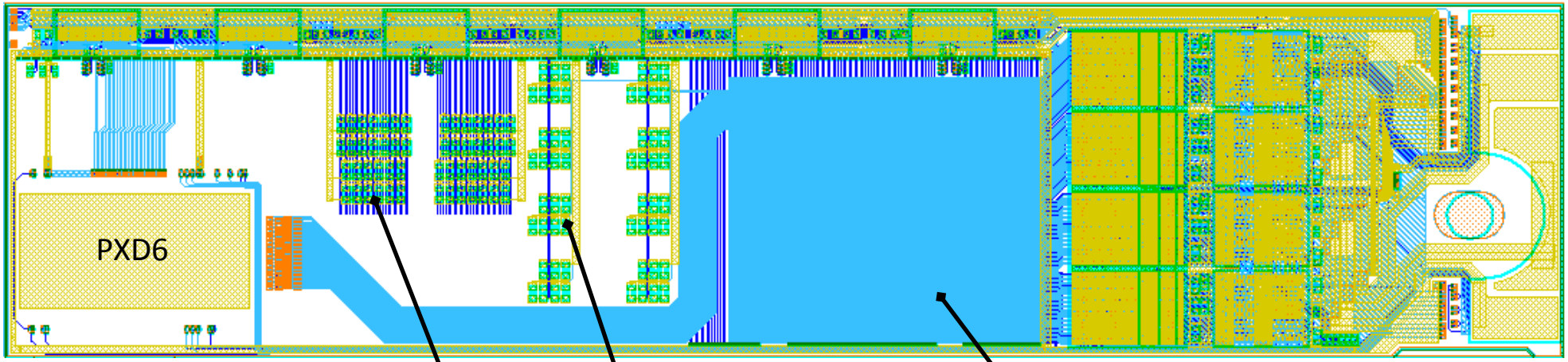


DCD

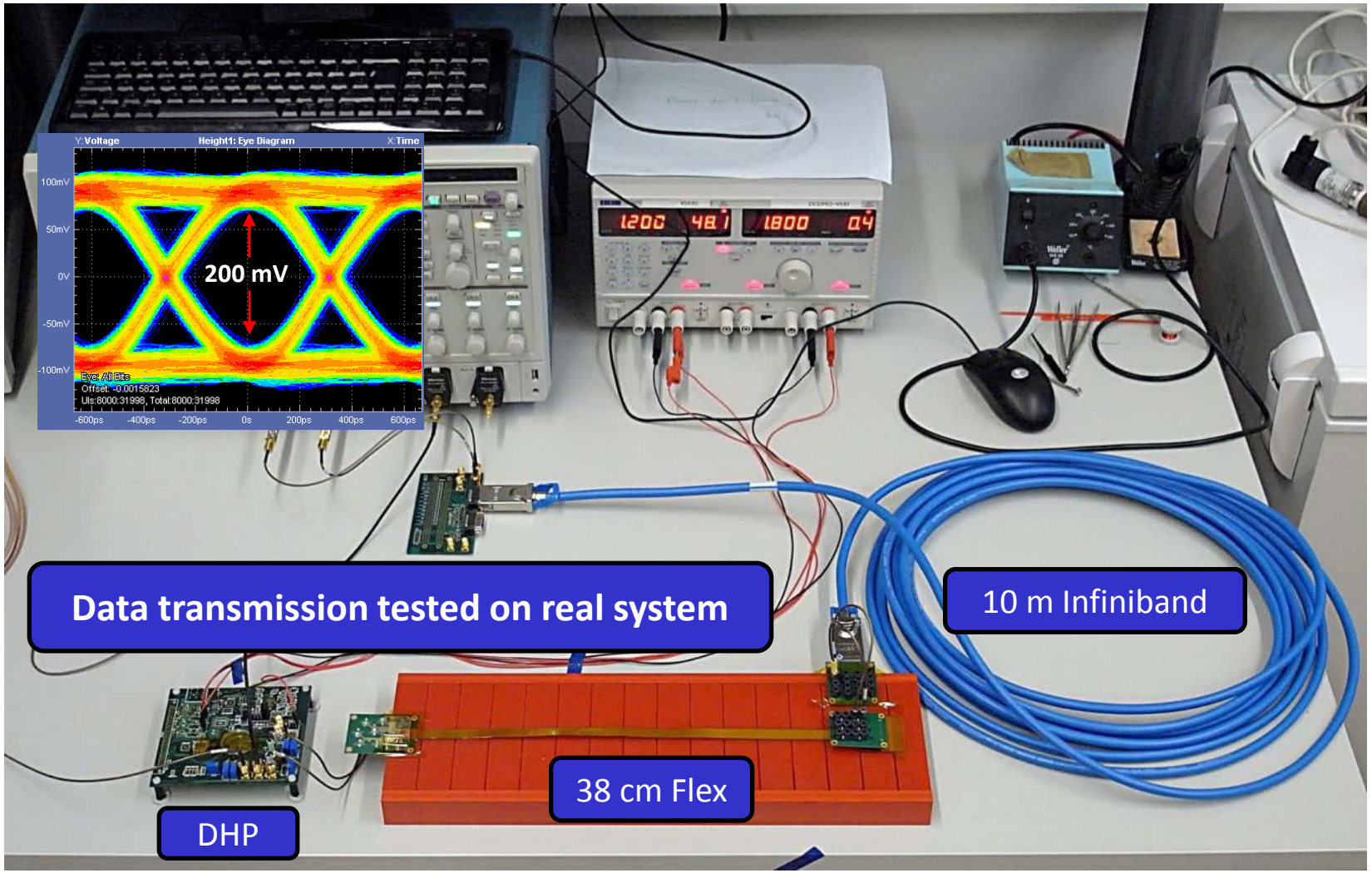
DHP





Metal system as close as possible to final → Electrical information

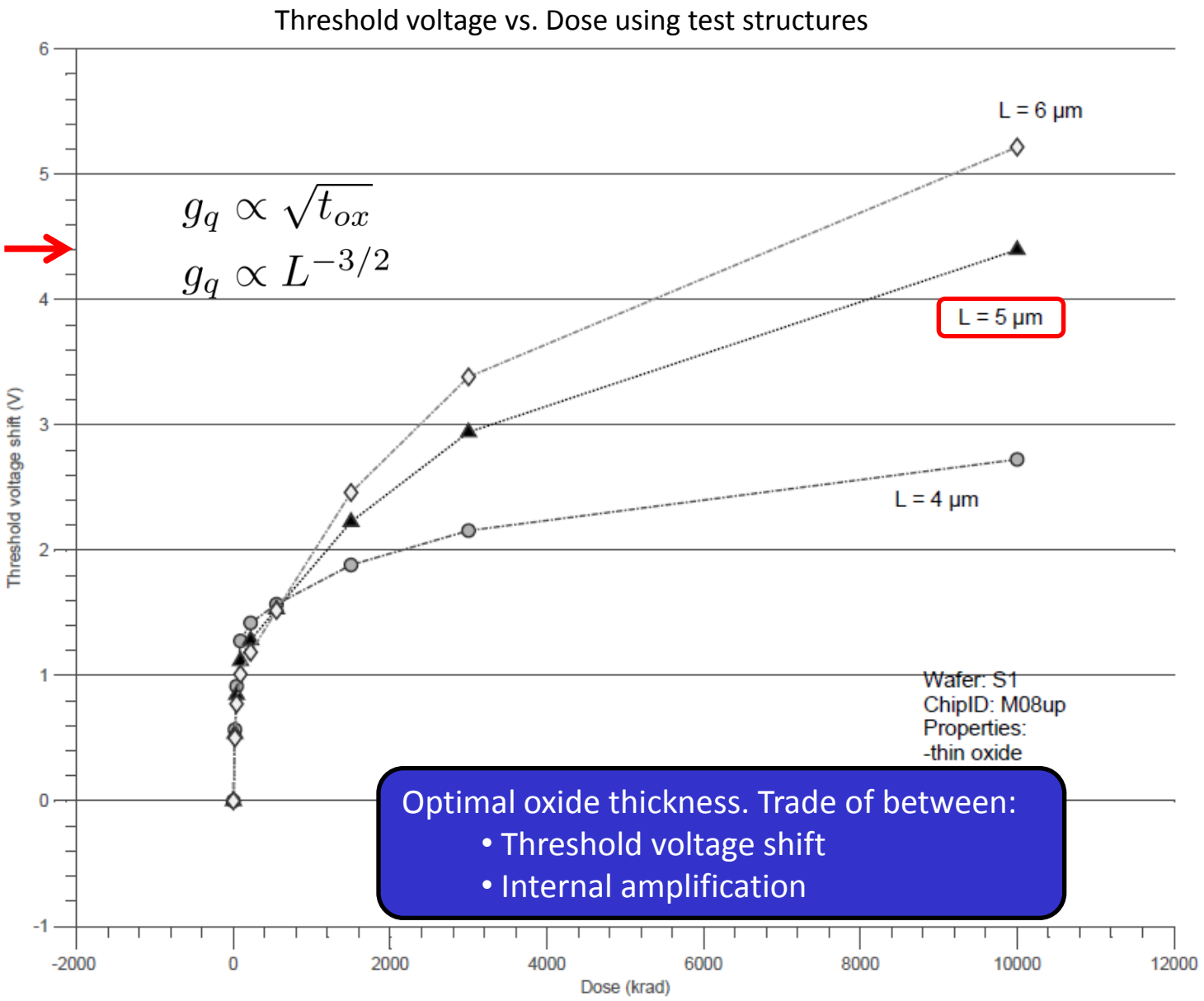
Signal integrity analysis



+ pre-emphasis

Radiation hardness

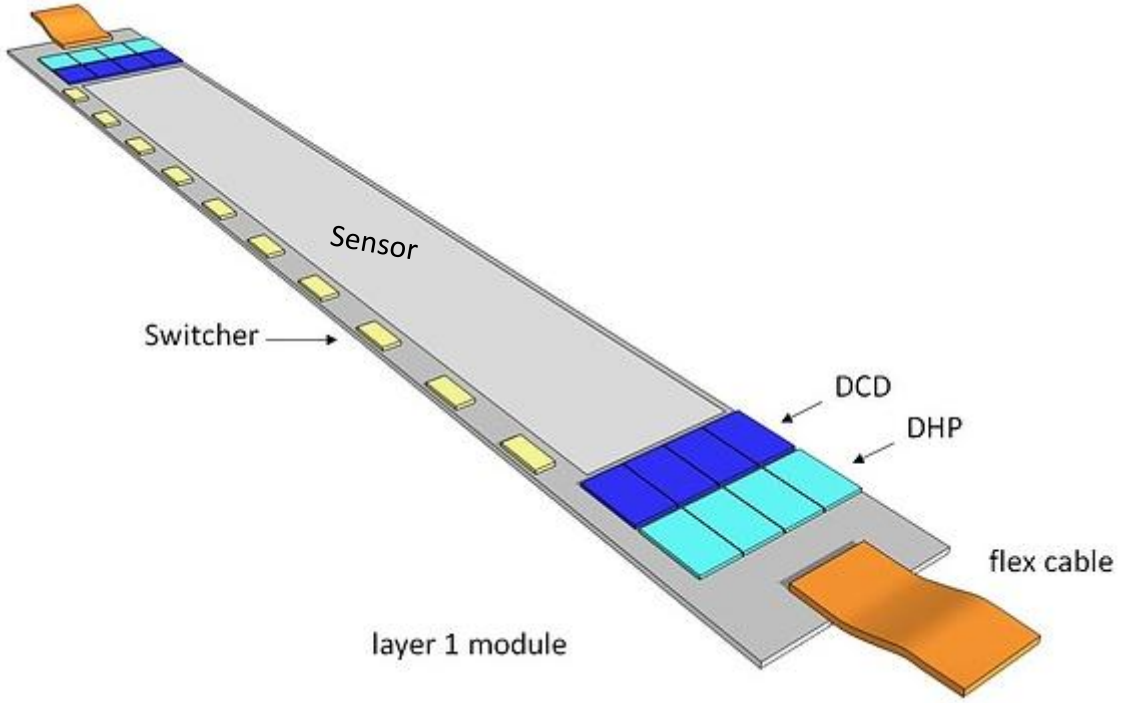
Small enough to be digested by the system

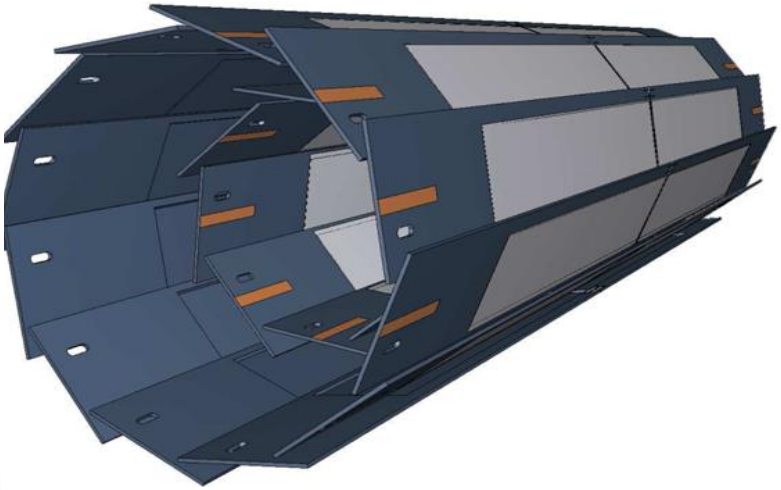


Optimal oxide thickness. Trade of between:
- Threshold voltage shift
- Internal amplification

Cooling strategy

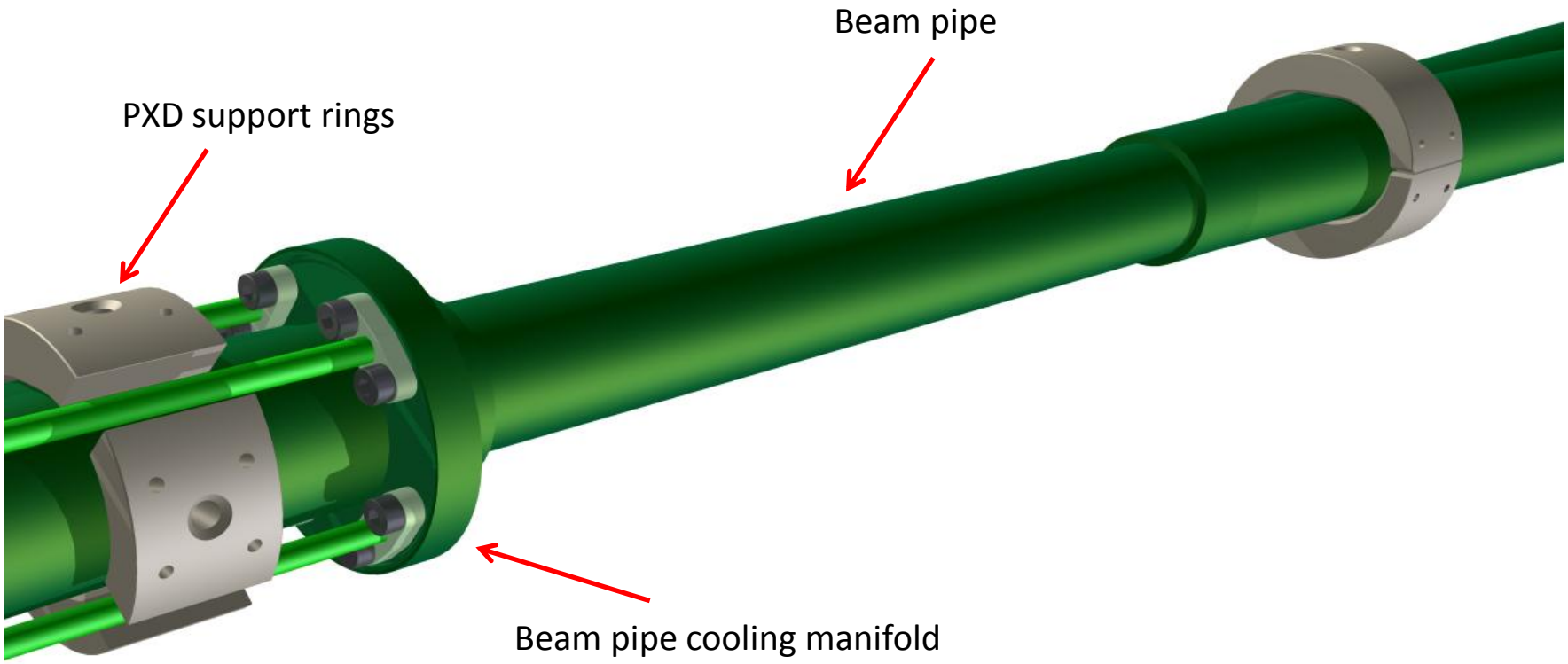
Remember the DEPFET detector unit, the ladder and how the ladders are assembled to form a vertex detector:





- The material budget must be minimal, no active cooling is allowed inside the acceptance
- The major amount of heat is dissipated in the readout chips, at both ends of the ladder
- The most straightforward solution:
  - Massive structures outside the acceptance to cool down the readout chips
  - The center of the ladder must be cooled using cold air

Building the Belle II PXD



- Thinner pipe
- Smaller radius
- Lighter materials

Building the Belle II PXD

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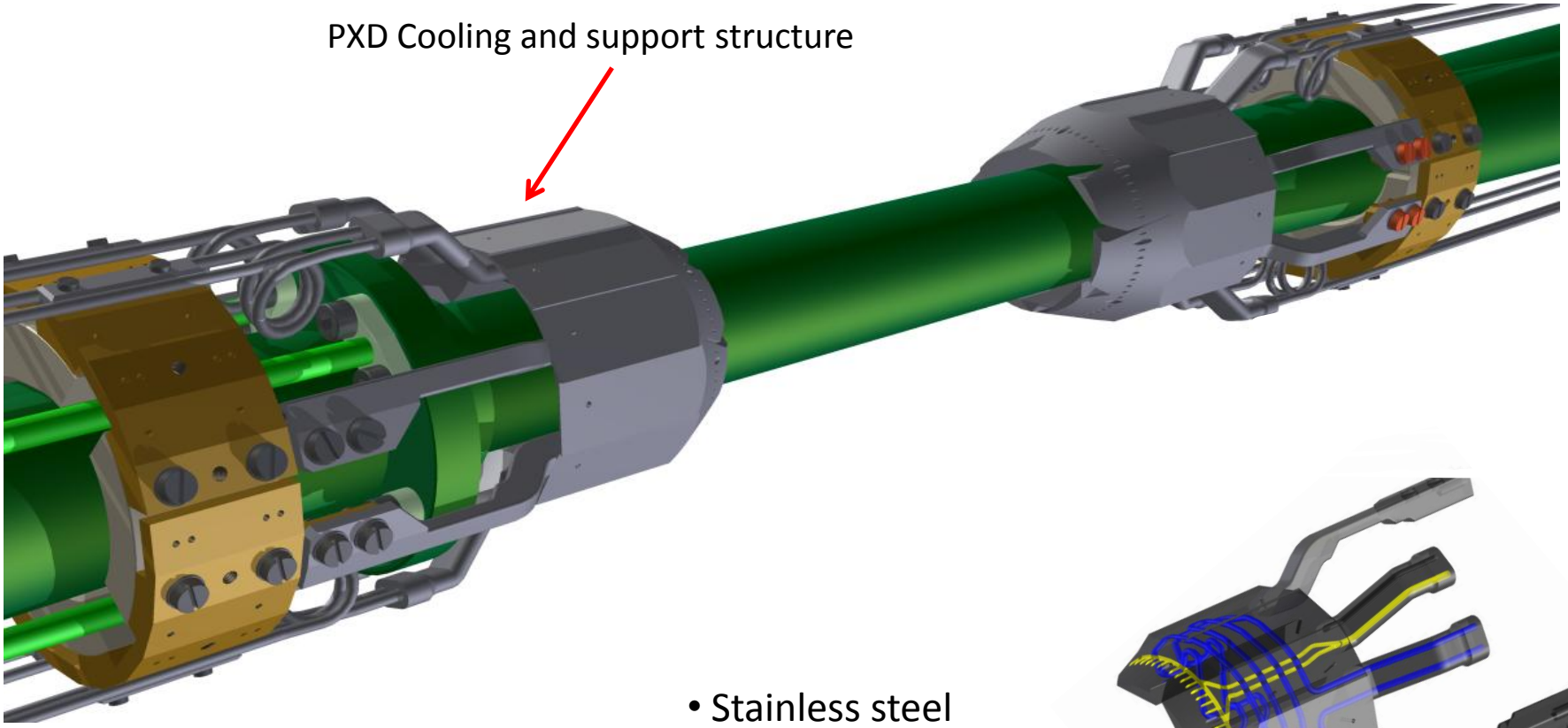
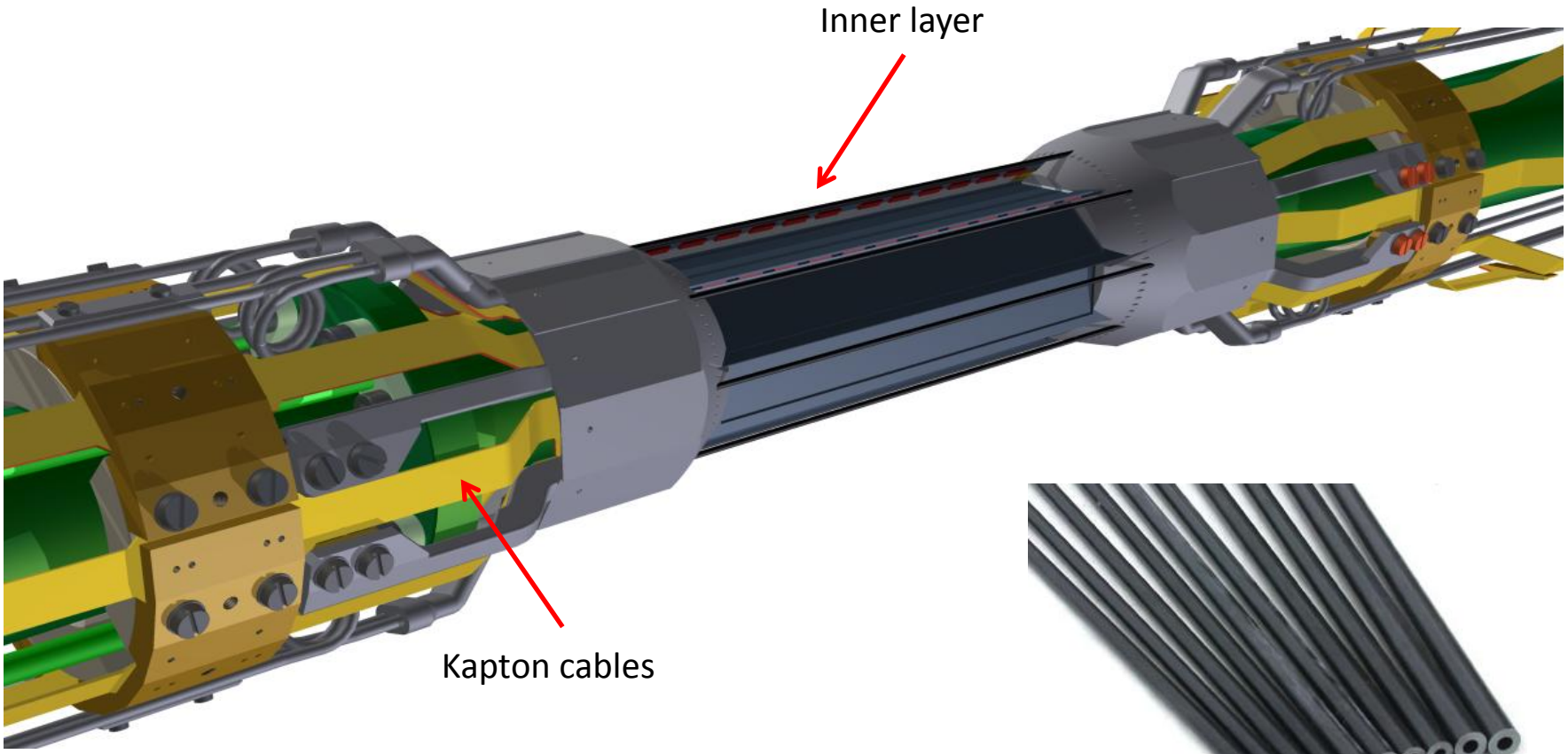
PXD Cooling and support structure



- Stainless steel
- Fast sintering
- Coolant: CO_2

Blue: CO_2 capillaries
Yellow: Air channels

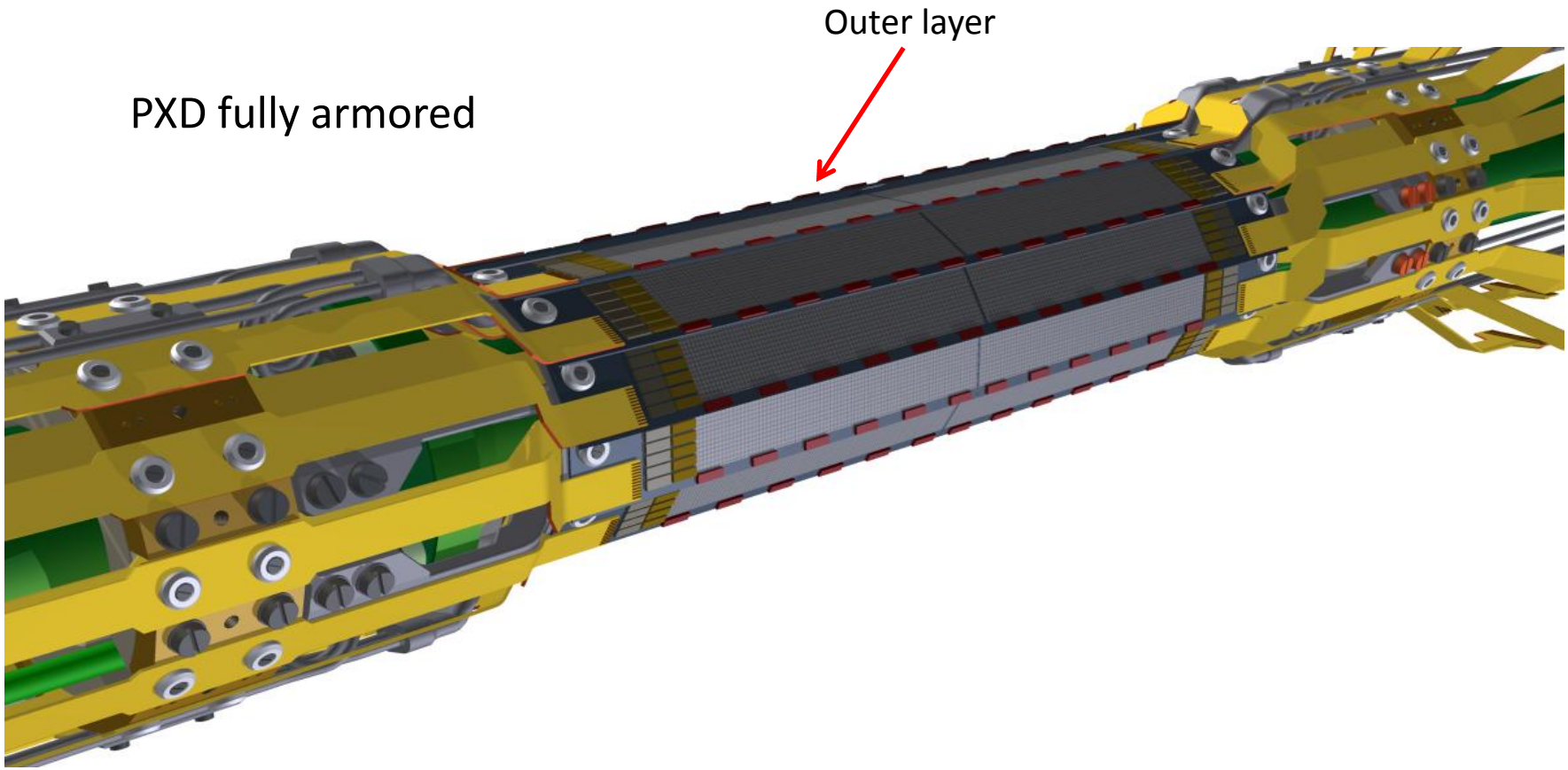
Building the Belle II PXD



Inner layer close to the IP (14mm)

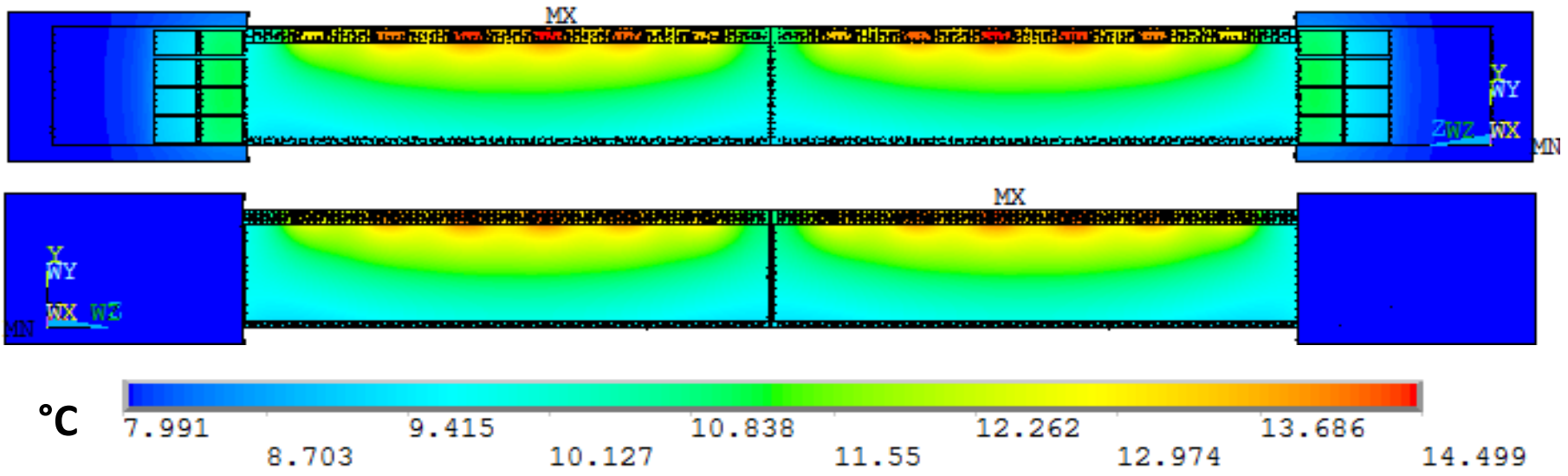
Additional carbon fibers capillaries to cool the Switchers, if needed (not tested yet)

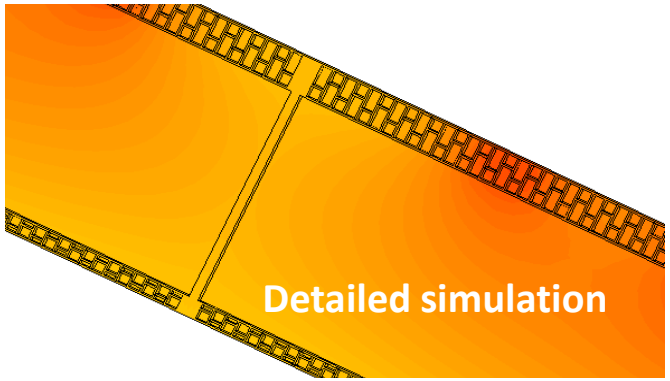
Building the Belle II PXD



- Low material budget cooling
  - Massive structures outside the acceptance to cool down the readout chips
  - The center of the ladder rely on cold air

Temperature distribution





Set of reasonable environment conditions

T_{env}=-5°C
T_{cb}=8°C

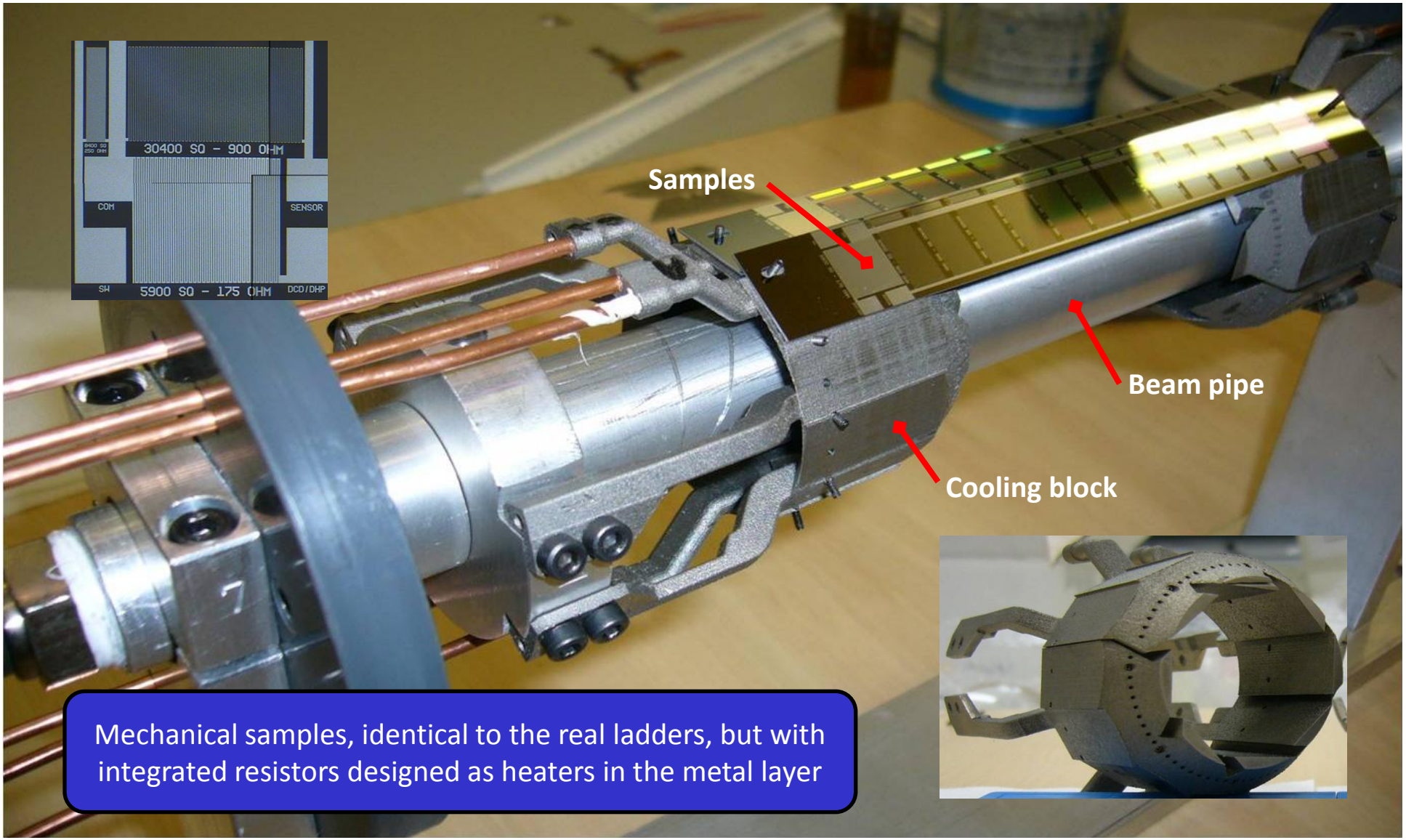
→

$T_{SENSORmax}$=14°C
DeltaT=4.7°C

$$\Delta L < 3\mu m$$

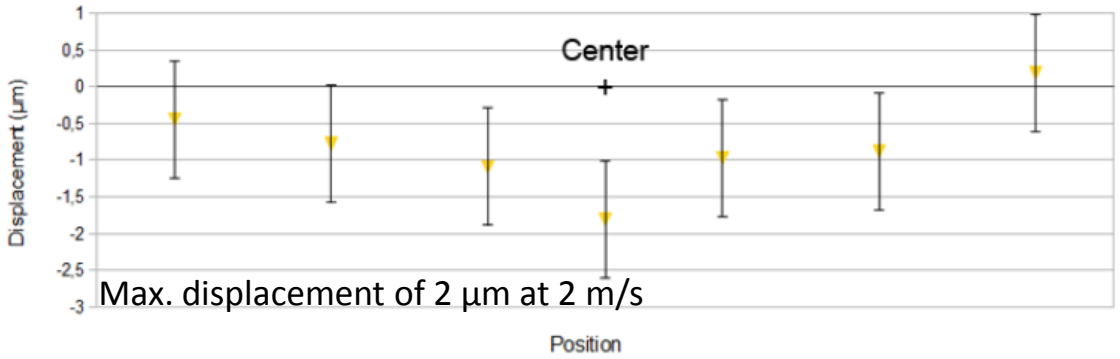
Just a gentle air flow (2 m/s) is enough to decrease and homogenize the temperature distribution

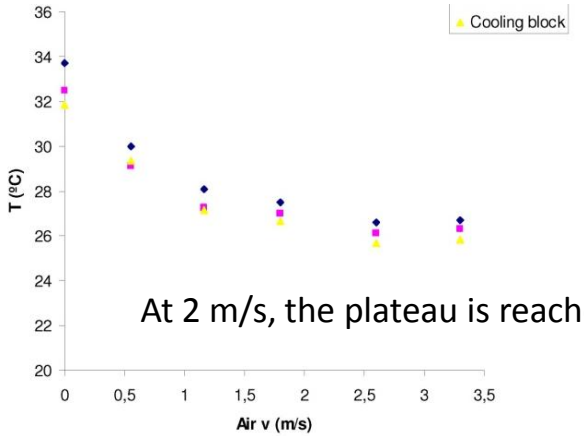
Measurements with mockup



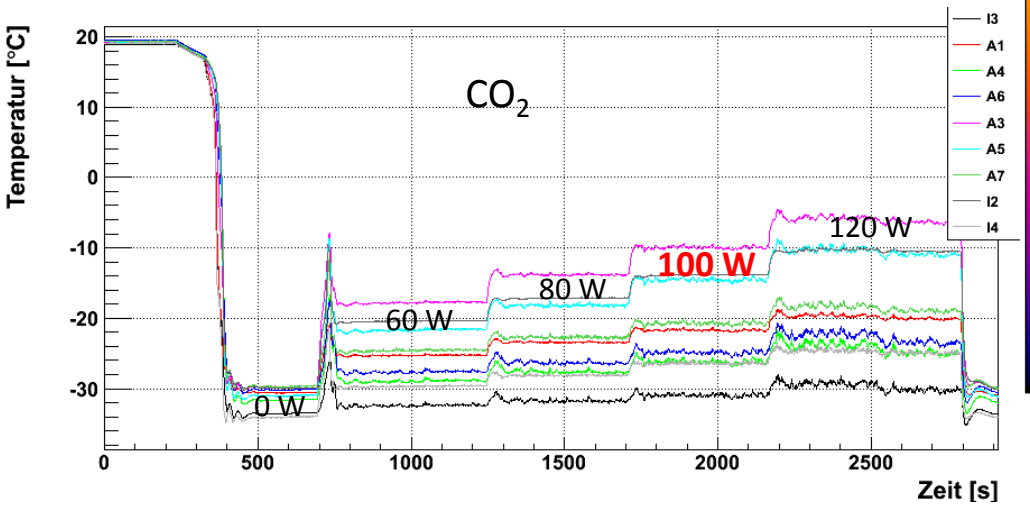
Mechanical samples, identical to the real ladders, but with integrated resistors designed as heaters in the metal layer

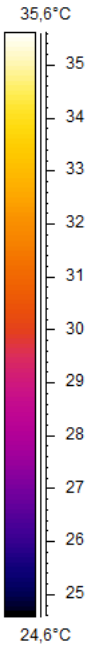
Thermo-mechanical measurements

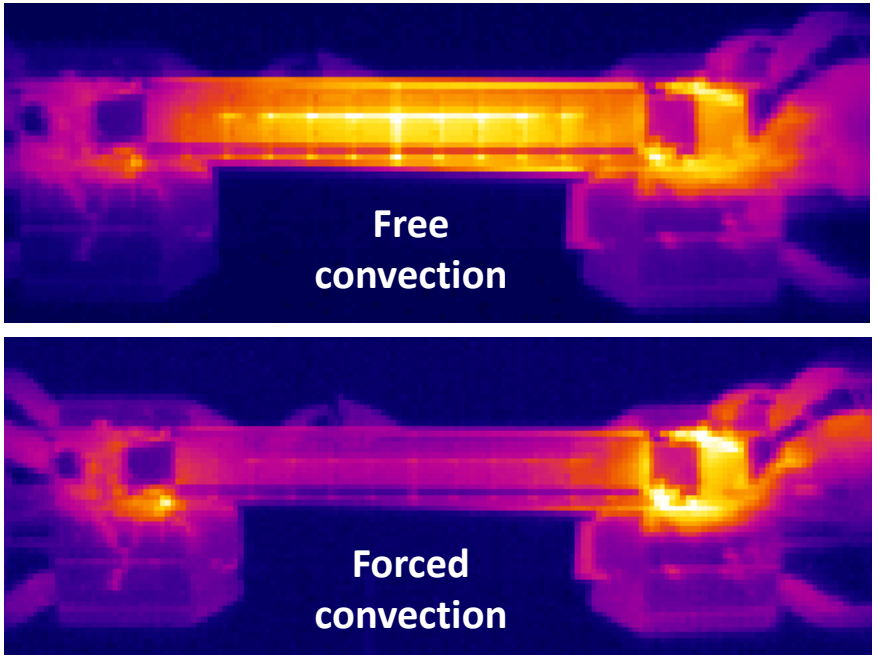




- Stainless steel
- Fast sintering
- Blue: CO_2 capillaries
- Yellow: Air channels







Cooling proof of principle

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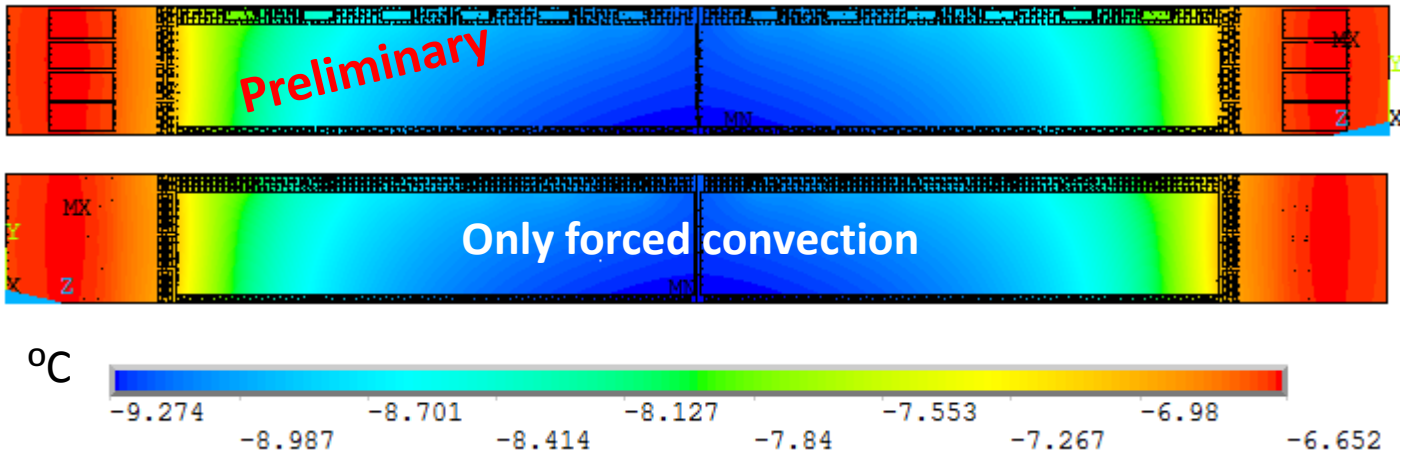
ILC scenario: Power cycle and air only

↘ Naïve approach using the XFEL hands-on:

• The power consumptions are weighted accordingly to the estimated duty cycle.

→ Completely shutting down the DEPFET and the analogue part of the electronics between trains → 1/25 power reduction if 1/100 duty cycle



• Tenv= -10 °C
• Vair=2 m/s

The air speed and temperature are not optimized to minimize the temperature distribution

P_{FE}=(0.5/25.) W / per chip
P_{Sw}=(0.1/25.) W / per chip
P_{Sensor}=(1./25.) W in total

↘ Although very preliminary, the cooling seems feasible so far

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Summary

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- The DEPFET Collaboration is developing pixel sensors with integrated amplification

- The good performance of the DEPFET detectors in terms of spatial resolution, sensor material and power consumption is demonstrated

- Transparent and precise vertex detectors for Belle II and ILC can be produced

- The Belle II PXD boosted the development of DEPFET detectors
  → Direct benefit in the ILC project

- Building a real system: Every detail (although not covered here) is being considered
  → Interconnection technologies, cooling, mechanics, ASICs, data transmission…

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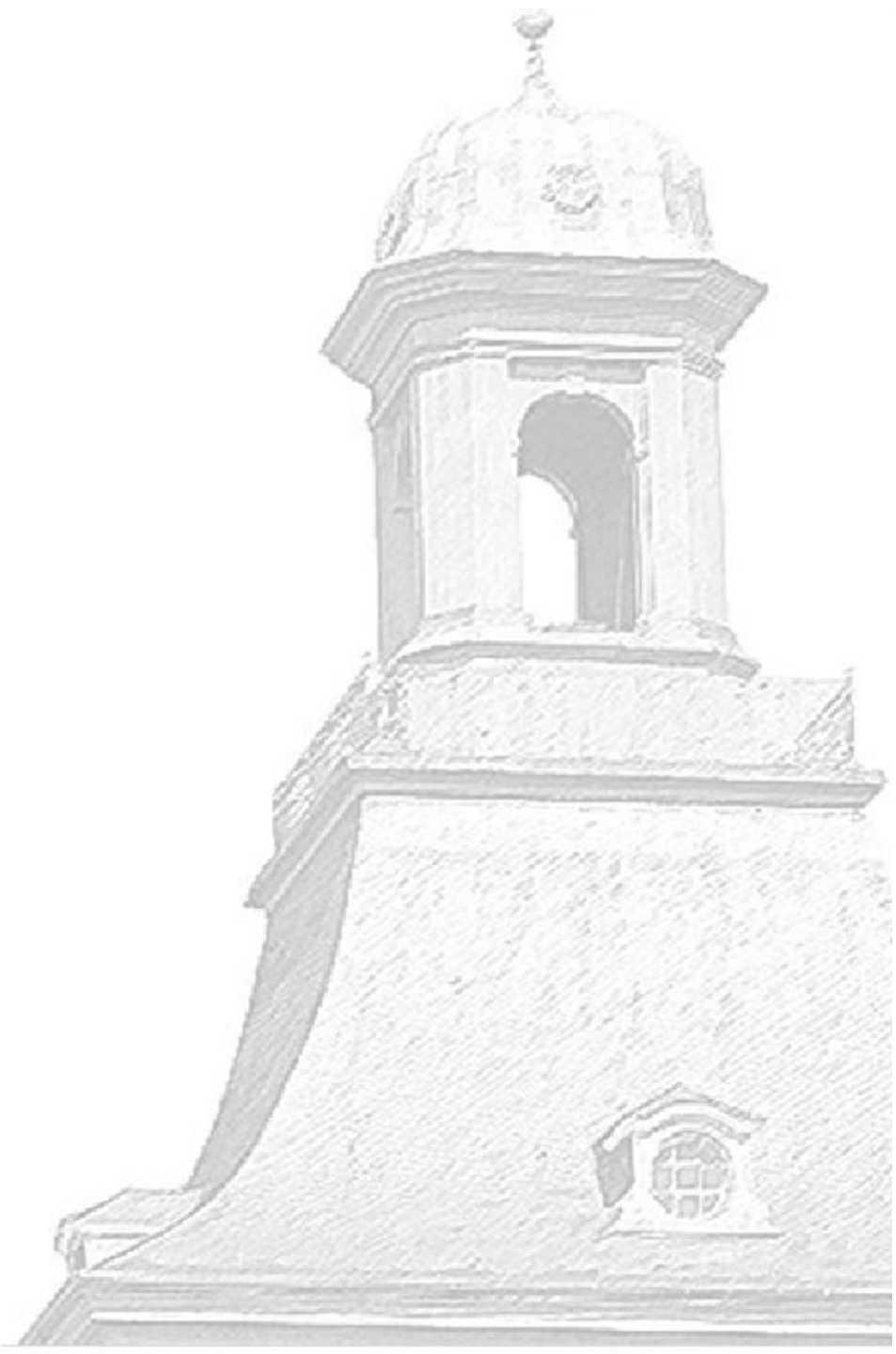
DEPFET

Active Pixel Detector

Thank you



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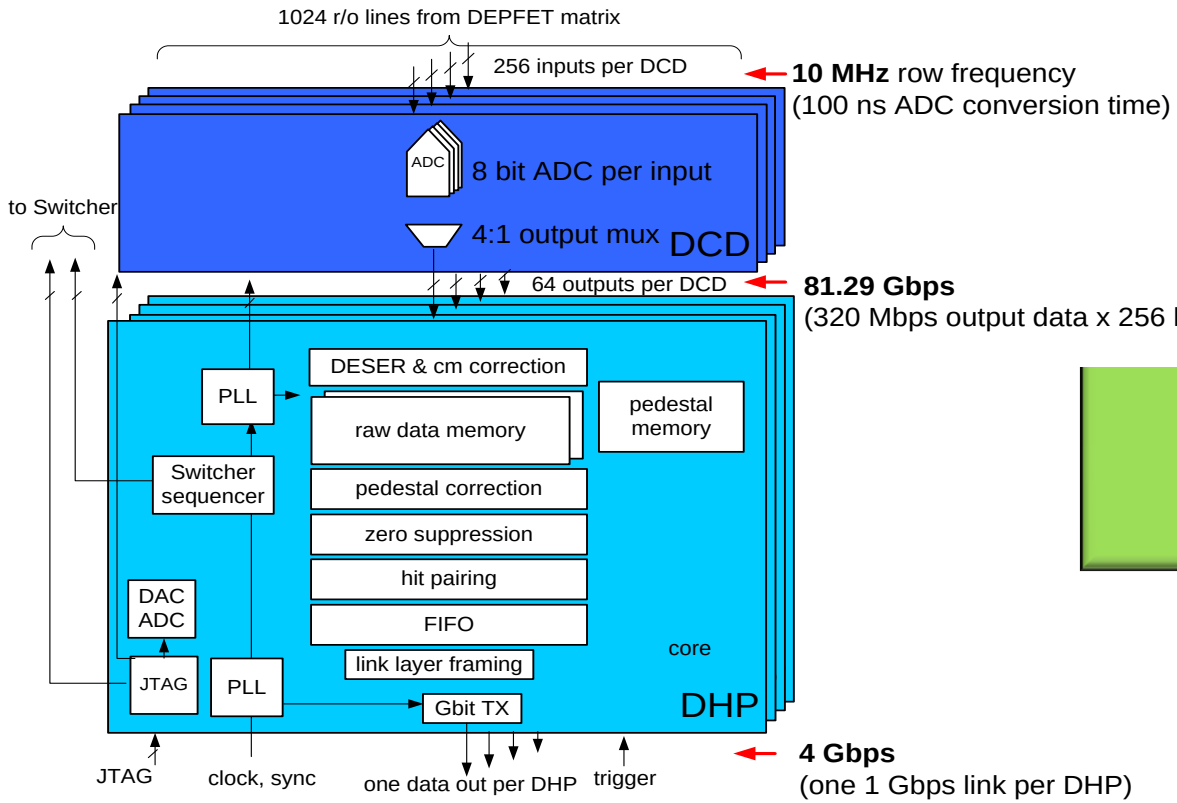
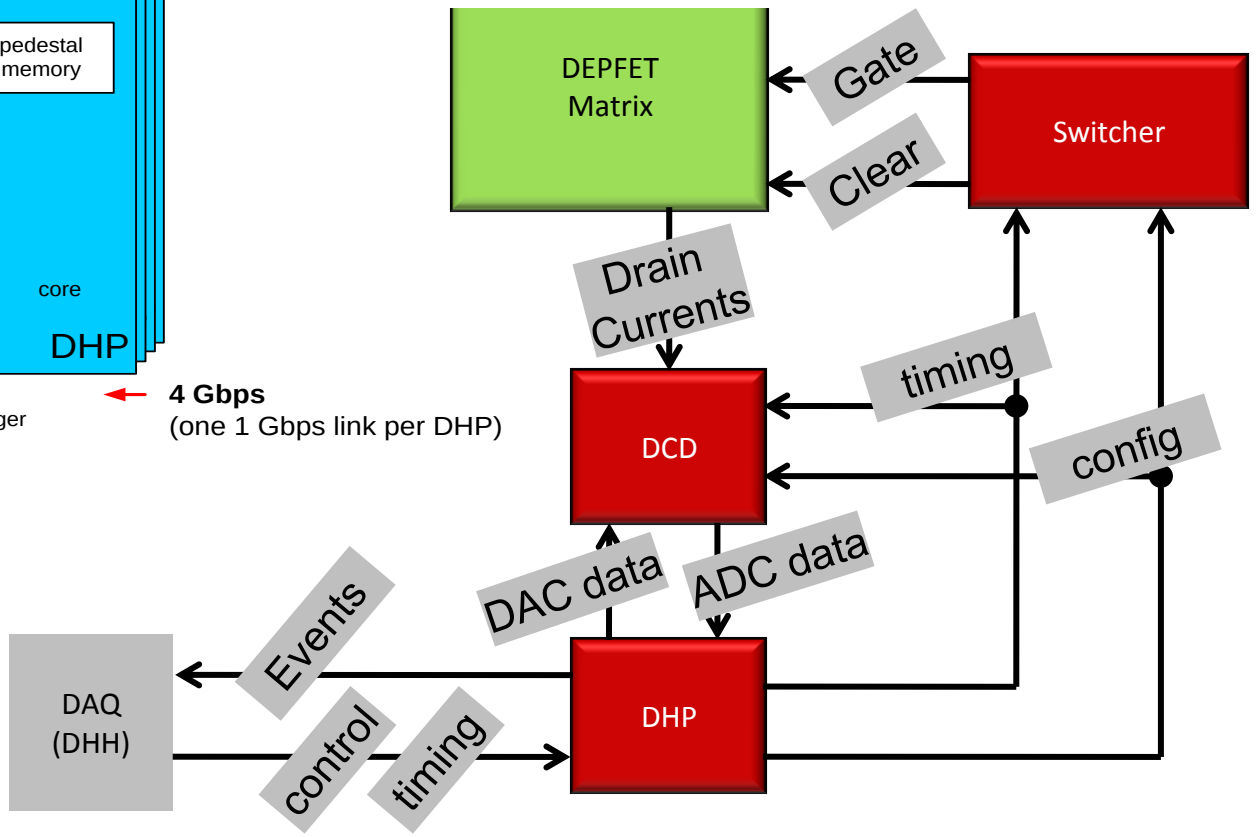
In-module signal flow





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