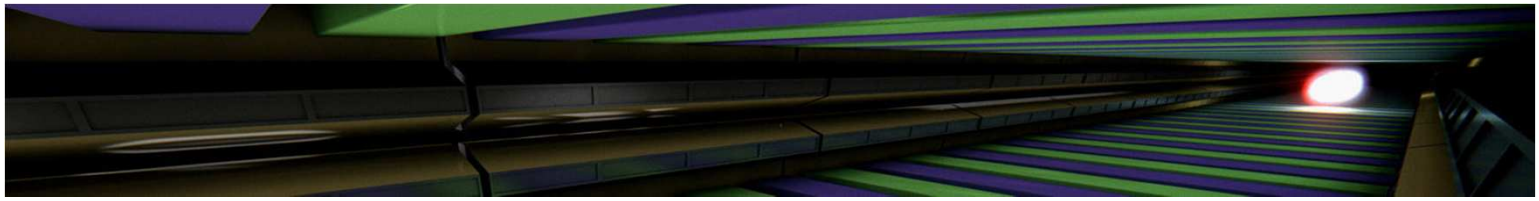


WP-76

XFEL Project Progress Report (1-2012)

C.Youngman

Comparison of forecasted and achieved progress: Jan. 12 → Mar. 12

- **PSP 20+30) DAQ and Data Management computing, storage and s/w**
  - **s/w (on schedule)**
    - First release of C++/Python Boost based s/w framework made
    - Now testing h/w (MPOD HV/LV, LPD, Timing Sync…) and s/w (PC layer…) devices
    - PyQt GUI first release made, integration with h/w and s/w devices started
    - HDF5 API developed and detector data format issues being addressed
    - Large amount of "other" work: Alfresco (K.Wrona)…
  - **Computing and storage slice test (on schedule)**
    - Computing, storage and 10GE h/w for slice test (vertical slice of DAQ and DM systems from online Front End Interface to offline compute and storage ordered
    - Network and compute systems delivered, setting up started in DESY CC
    - Storage h/w expected soon
    - Slice test aim : prove s/w and DAQ/DM architecture decisions
- **PSP 40) Beamline DAQ: control for optics, diagnostics and laser**
  - **Optics and diagnostics (on schedule)**
    - Beckhoff PLC h/w and f/w development continuing
    - Commercial camera station and DAQ requirements defined (WP74), PES follows
  - **Laser (delayed)**
    - Specification of s/w interface stalled waiting for s/w release, now restarted

PBS homogeneous s/w framework

Purpose – provide a single s/w environment for control, DAQ, DM and SC(analysis)

Solution – standards

- Proper standardization results in modular, scalable and homogeneous software
- use C++ / Boost / Python / PyQt as core technologies
- Do not re-invent the wheel, use high quality libraries: Boost (shared_ptr, any, msm, function, asio), PyQt, OpenMQ, Log4cpp, CImg, etc.

Issues of specific interest for control and DAQ

- s/w or h/w instances to control are called Devices = plugins created by factories in Device servers
- communication: use MOM broker (OpenMQ now) and p-2-p for large volume data transfer
- configuration and reconfiguration: XML and XSD (i.e. self-describing) driven (cmd line, file, DB)
- flow control: all devices are FSM enabled (message event driven)

Implementation – status

- first s/w release mid-March contains complete toolkit set
- Devices for h/w (MPOD, Beckhoff…) and s/w (PC layer, Data feeders…) online
- Generic GUI integration in progress

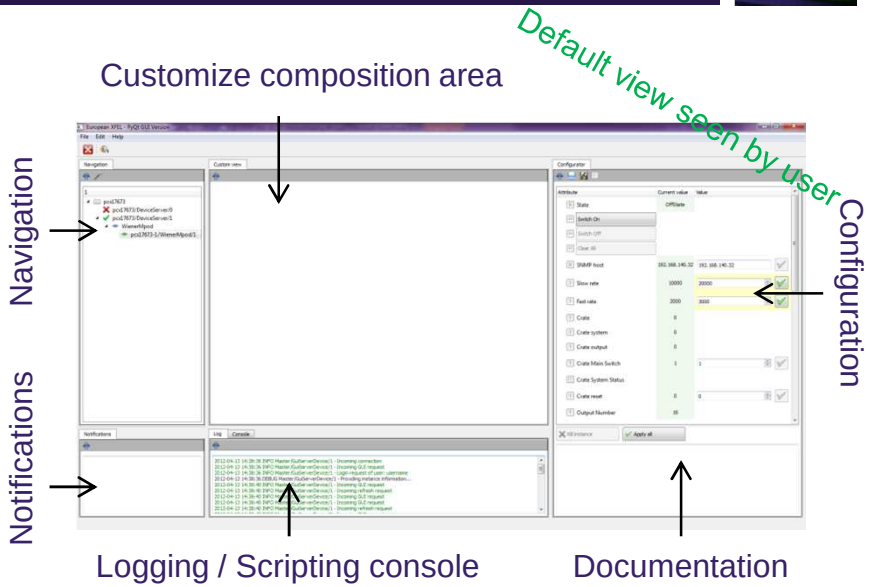
Outlook

- Final DB design and update of s/w API
- Upgrades driven by requirements (OpenMQ to ZeroMQ?)

PBS GUI development

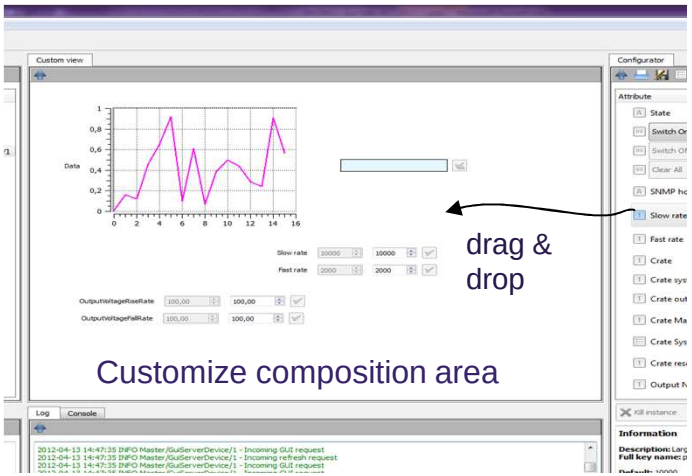
First time shown!

- generic, multi-purpose, cross-platform GUI
- remote control
- self explaining, default layout for any device
- highly customizable user panels
- Fully integrated with s/w framework
  - many features - not described
- Widgets are plugins – 3rd party ones can be used with a simple wrapper (e.g. Taurus?)



Generic GUI

- Framework XML and XSD usage = self description
- Configuration attributes immediately seen
- Device driven – no code generation



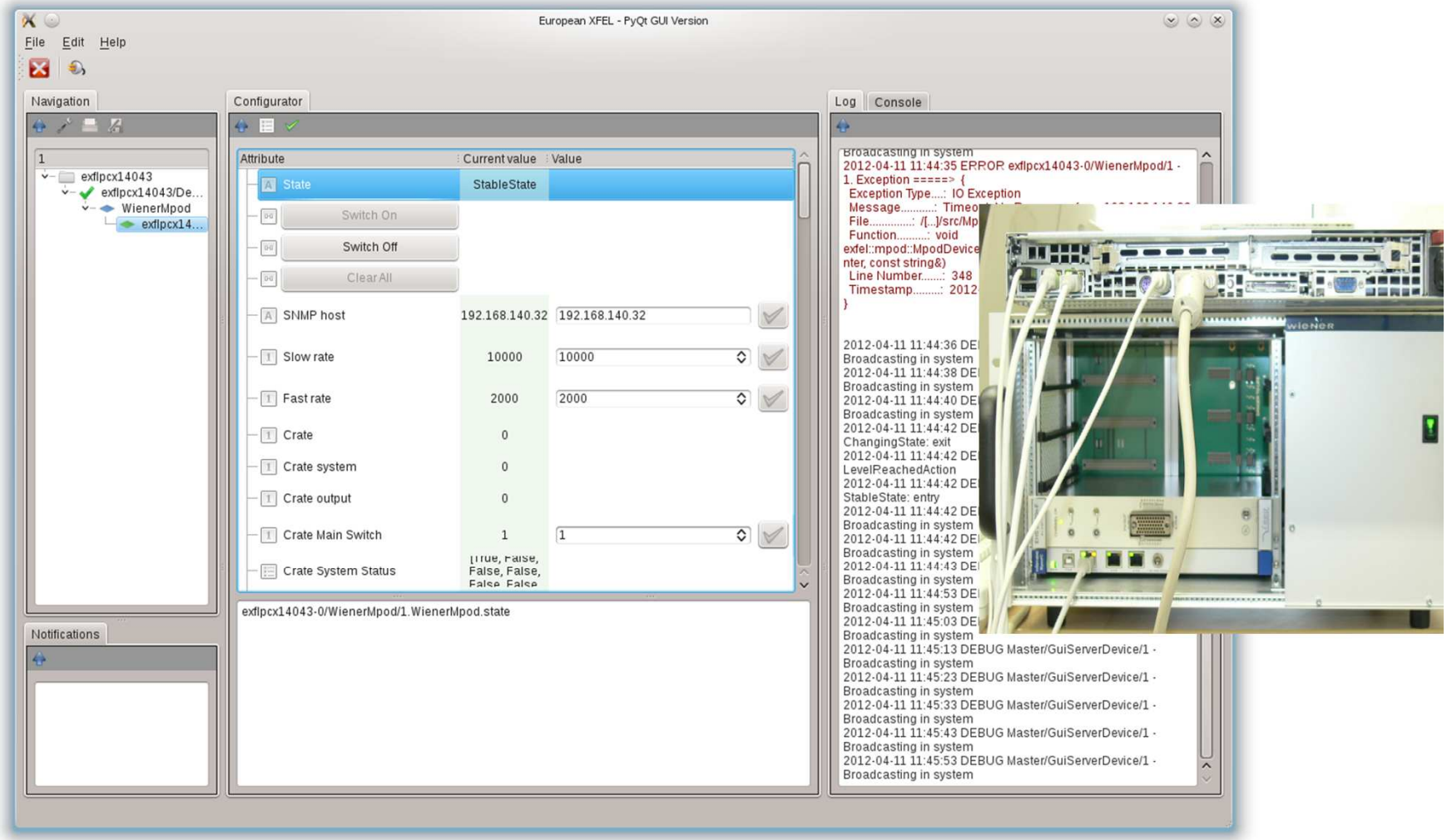
Outlook

- FSM visualization
- user-role driven (database)
- …

European XFEL

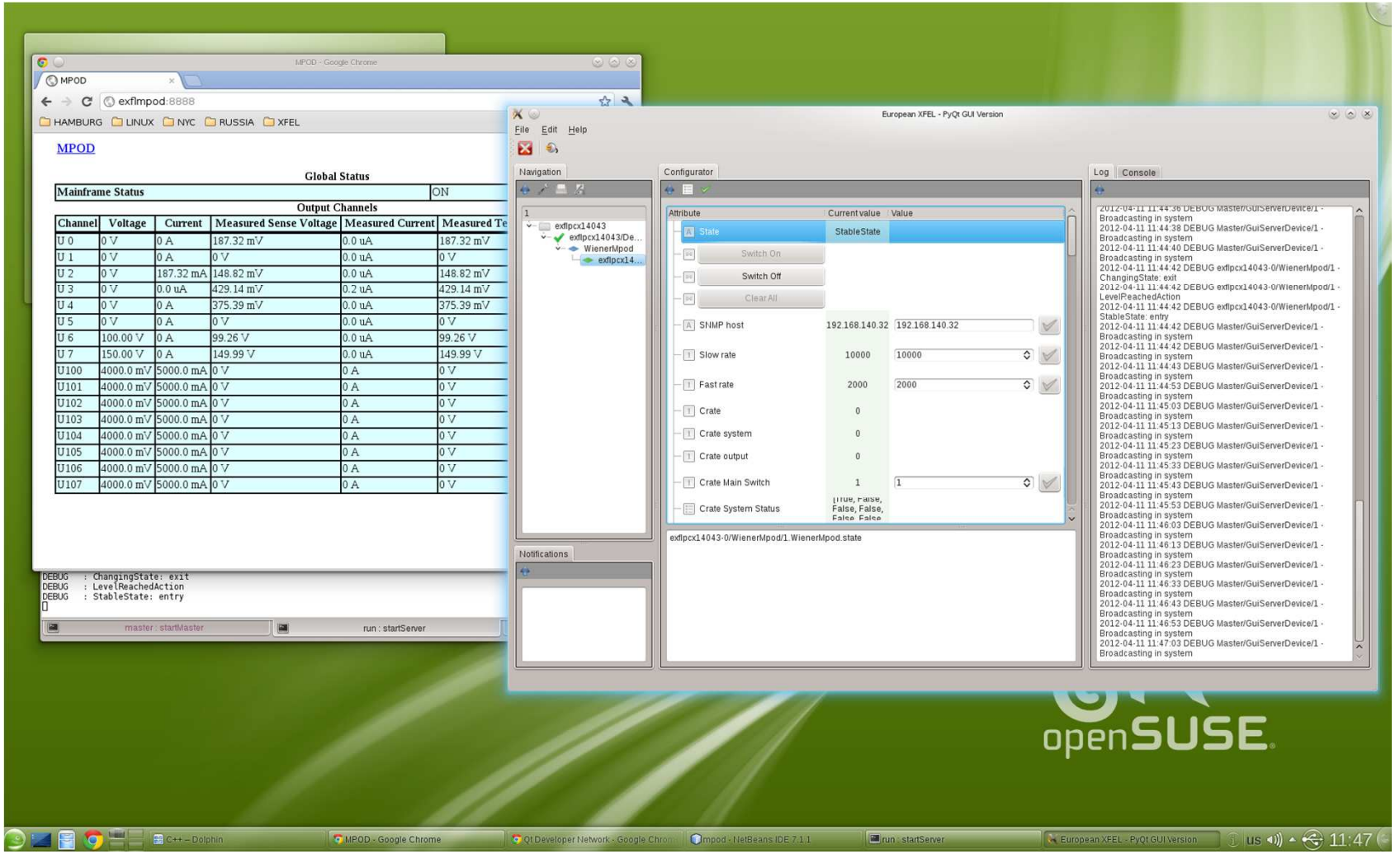
Generic GUI view of MPOD HV/LV device (1/2)

Full Implementation chain: s/w framework + GUI + Device + HV/LV h/w



European XFEL

Generic GUI view of MPOD HV/LV device (2/2)



PBS control and DAQ h/w solutions

Standards for DAQ and control

- MTCA.4 crate board: remote operation, RTM signal conditioning
- FPGA processing: data reduction/rejection and VETO generation/receiving (low latency SFP)
- 10Gbps data streaming; 1 Gbps low latency feedbak (VETO)
- DAQ and laser timing from e-machine solutions

DAQ “clock and control” MTCA.4 sequencing board development

- 16 modules = 1 Mpxl
- One fast signal sequencing link / module (or quadrant)

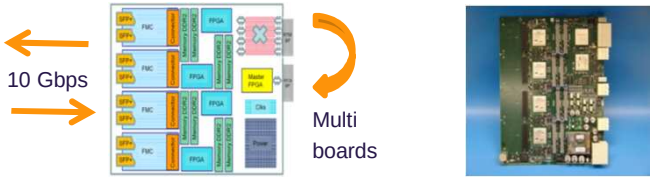
DAQ “train builder” ATCA readout board development

- collect image fragments from modules (10 Gbps links)
- reorganize into complete trains of pulse ordered images (cross-point)
- data processing in FPGA – remove empty, no ROI… frames
- send trains Round-Robin to PC layer (10 Gbps links)
- Multi board train builder installation should satisfy 4Mpxl camera demands in 2015

MTCA.4 Fast ADC and Digitizers

- Use SIS 8300 as standard – in use with e-machine groups
- Digitizer SP Devices AB family – MTCA.4 and DAQ update

Prototype sequencer MTCA.4 RTM (UCL)



Prototype train builder ATCA board (STFC)

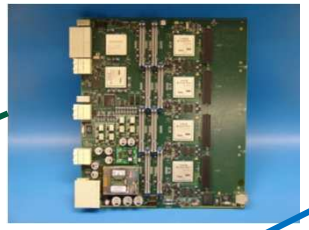
Standard XFEL Digitizer selected

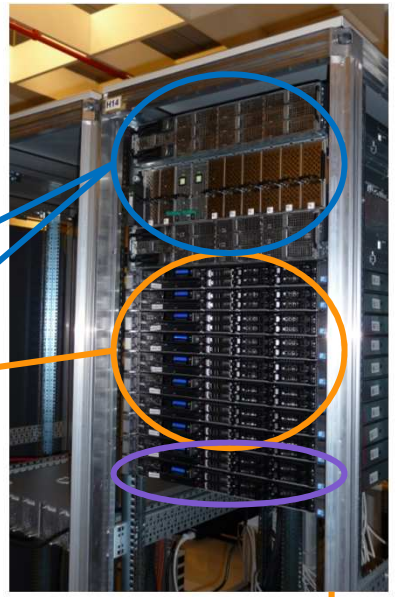
Device	Characteristics	Provider	Usage
Fast ADC	125 MHz, 16 bit	www.struck.de	4.5Mz shaped signals: APD, BSD...
Digitizer	1-7 GS/s, 14-8 bit	www.spdevices.com	eTOF, iTOF, VMI…

European XFEL

PBS Test slice – h/w setup in DESY-CC

TB prototype Q3/2012

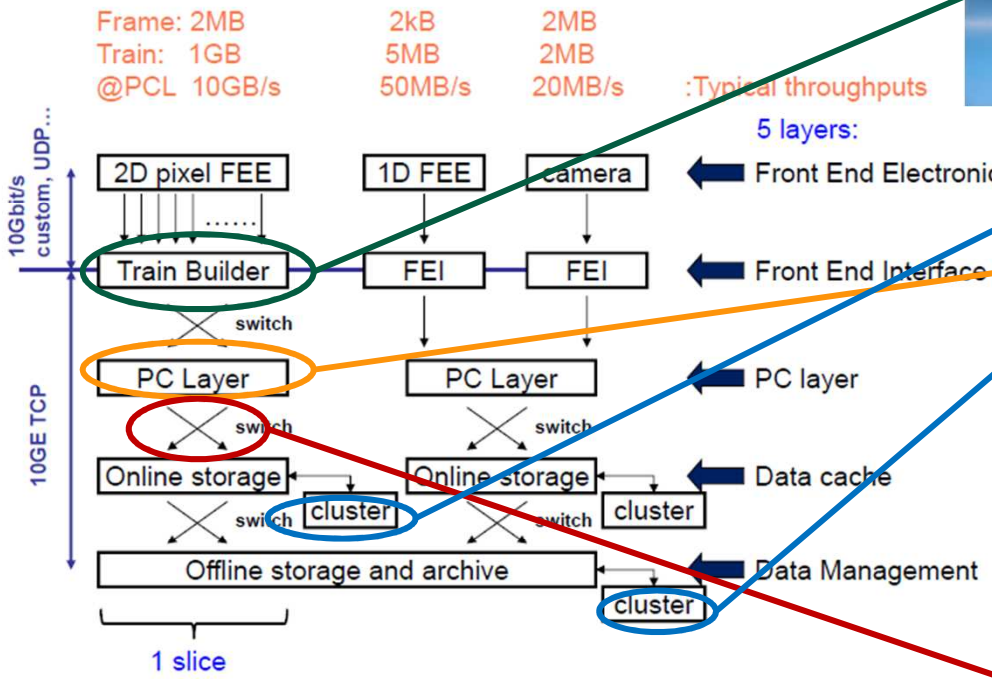


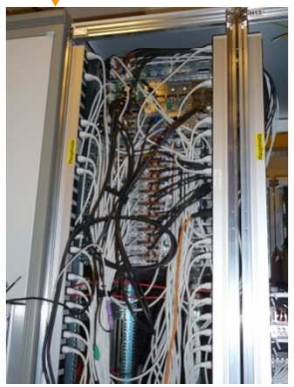


Compute + GPUs nodes

PC nodes

DB+MDS nodes





10 Gbps switch

Test of a vertical ½ to 1 Mpxl slice of architecture started
- Uses homogeneous s/w framework
- Test that data handling h/w behaviour is as expected
- Platform for testing s/w (control, DAQ, DM and SC)
- First results encouraging

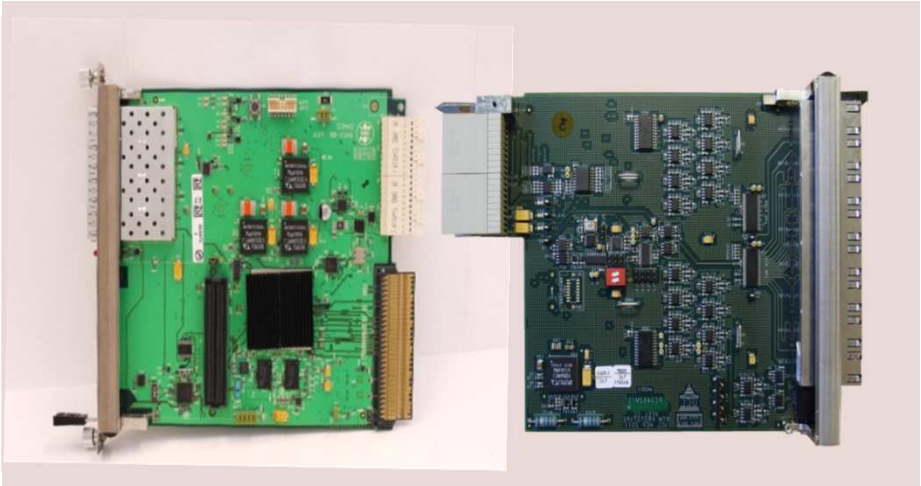
Comparison of forecasted and achieved progress: Jan. 12 → Mar. 12

- **PSP 50) Experiment DAQ and electronics development (on schedule)**
  - Selection of high performance digitizer completed, addition design features (10Gbps data streaming and SFP low latency links) for XFEL specified, contract approved.
  - Further development of Struck 8300 fast ADC MTCA.4 single crate DAQ system (FPGA f/w and s/w device integration) in preparation for WP81 beamline tests.
  - VETO system "final" specification completed, needs OK from camera and other sub-system developers
  - Establishing a collaboration with DataXpress collaboration to investigate VETO and DAQ performance using CFEL LCLS data.
  - Commercial and webcam work started with WP74 (by A.Parenti new to WP76)

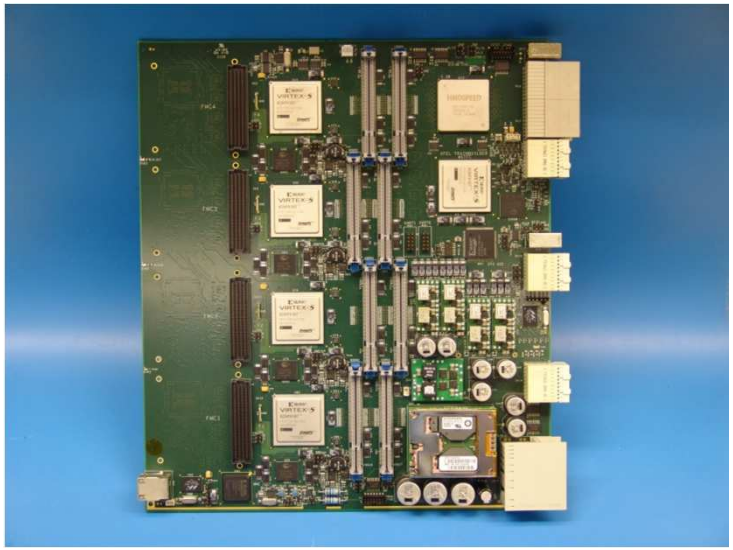
- **PSP 60) Pixel DAQ and electronics development**
  - Received the HV and LV specification from AGIPD (did not change)
  - Did not receive the interlock specification from AGIPD (not critical)

2D Synchronizer and train builder prototypes

DAMC2 MTCA.4 frontend



2D synchronizer MTCA.4 RTM



Bare Train builder ATCA without:

- 10Gbps FMCs
- Memory boards

Comparison of forecasted and achieved progress: Jan. 12 → Mar. 12

- **PSP 70) Pixel electronics development**
  - **2D camera synchronization board (UCL contract on schedule)**
    - → Prototype of 2D camera synchronizer (Clock and Control) delivered, test phase started, no unexpected issues.
  - **Train Builder readout board (STFC contract on new schedule)**
    - → Prototype of 2D camera DAQ board (Train Builder) delivered, smoke and power testing started.

- **PSP 80) Control system interfaces**
  - **DOOCS**
    - → Interfacing to machine control system discussion started
    - → Detail planning following ACC2012 control session
    - → See control workshop summary talk of Kay
  - **Undulator**
    - → Requires DOOCS gateway work.

Comparison of forecasted and achieved progress: Jan. 12 → Mar. 12

- **PSP 90) Infrastructure**
  - → Specification of Beckhoff and DAQ systems for use in SPB nearly complete, based on SPB + SFX implementation. Product are space, power, connectivity requirements required for hutch planning.
  - → Tunnel rack usage planning (WP73, WP74…)

- **PSP 99) Manpower**
  - Additional manpower hired:
    - → DB developer – database content and API,
    - → PLC and control developer – slow control,
    - → Detector s/w+h/w integrator – commercial and web cams,
    - → Installation and cable data base technician advertised

Reasons and Impact for schedule deviations Jan. 12 → Mar. 12

- s/w specification of laser API delayed
  - Reason: waited for first release of s/w
  - Impact: API delayed

Activities and milestones scheduled for the next half year

- Initial results from vertical slice test to prove DAQ and DM architecture, capability of handling maximum rates, etc.
- Field tests of first s/w release with h/w: AGIPD HV+LV tests system, APD single crate DAQ system...
- If 2D camera DAQ board arrives tests in slice tests and with the sequencer in preparation for first camera 2D camera sub-modules
- Preparation of Beckhoff control for pnCCD system being developed by WP75
- Tunnel rack assignment and input to specification
- Integration of additional h/w devices into s/w framework: LPD, TB, CC...
- Further development of s/w framework
- Organization of a data rejection/compression/VETO workshop in the fall
- …

WP schedule and critical path

- Review of installation schedule with other photon system WPs is needed.
- Update of the 2009 computing TDR needed was planned for 2011, but need to include experiment CDR input.

Open Issues

- Scheduling of installation and commissing