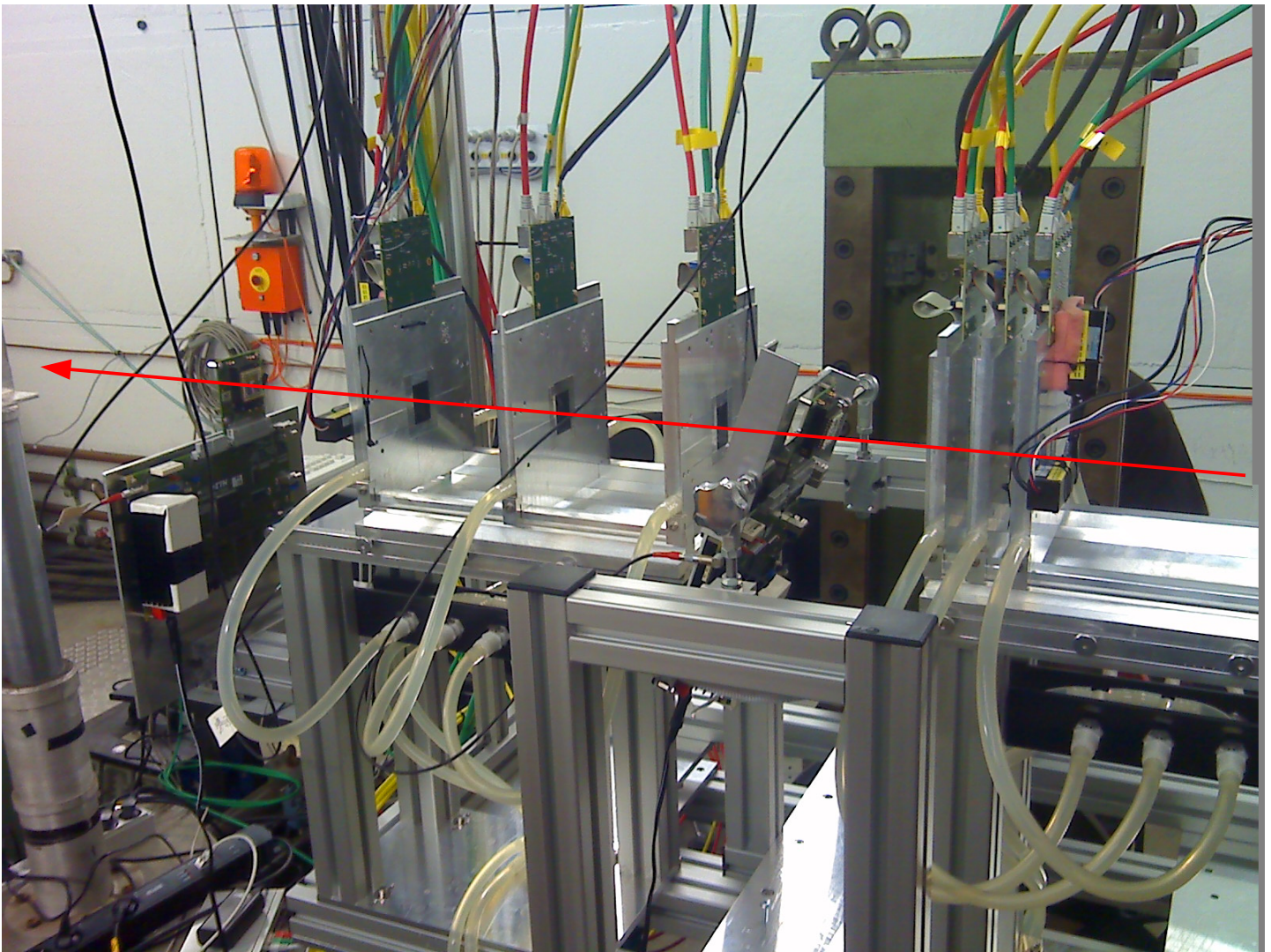
Pixel beam test April 2012

Daniel Pitzl
DESY CMS Pixel Upgrade, 11.4.2012

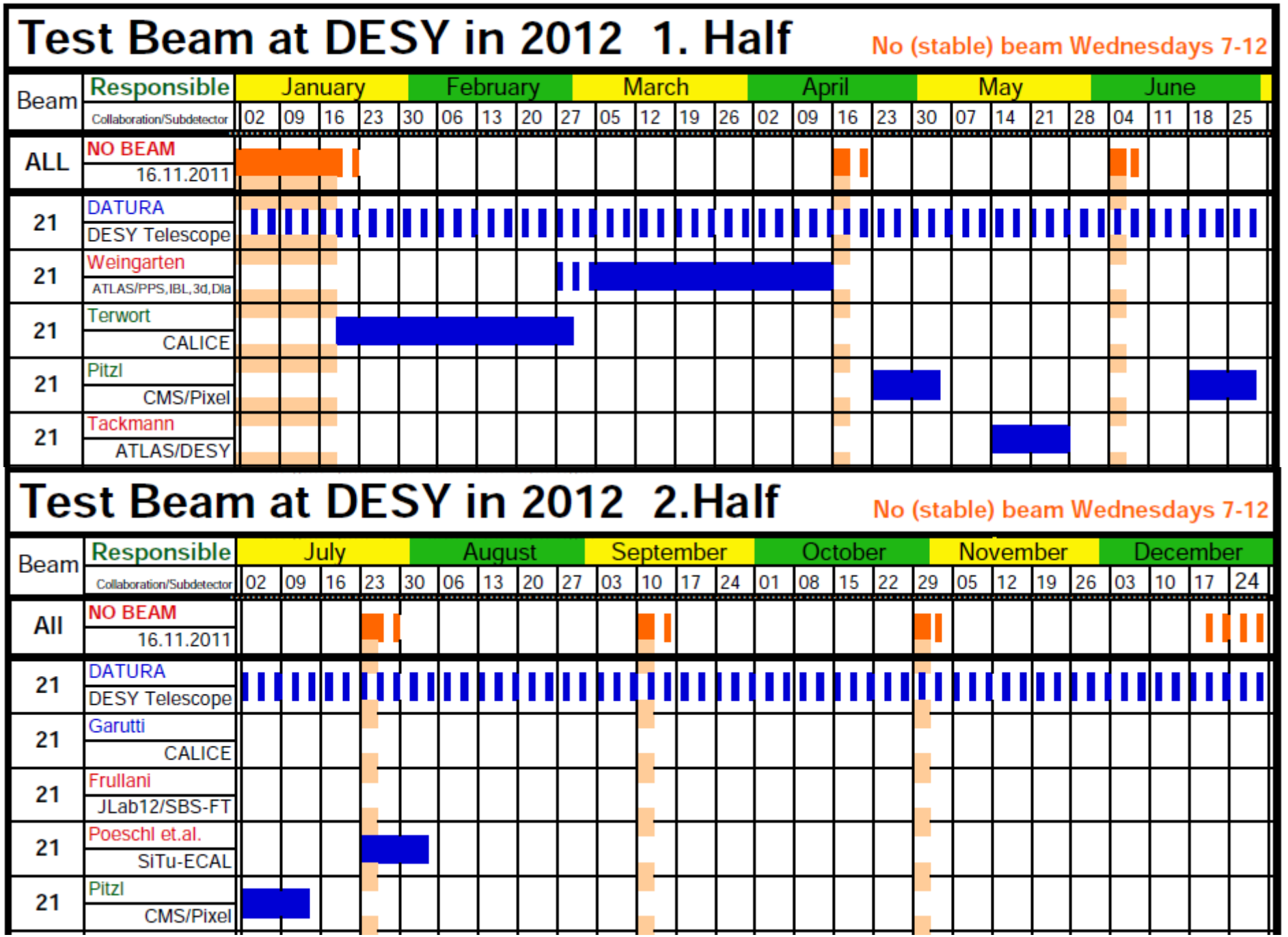


- goals: resolution and efficiency for present ROC
- scans
- runs
- monitoring

CMS Pixel in the DESY test beam

http://adweb.desy.de/~testbeam/

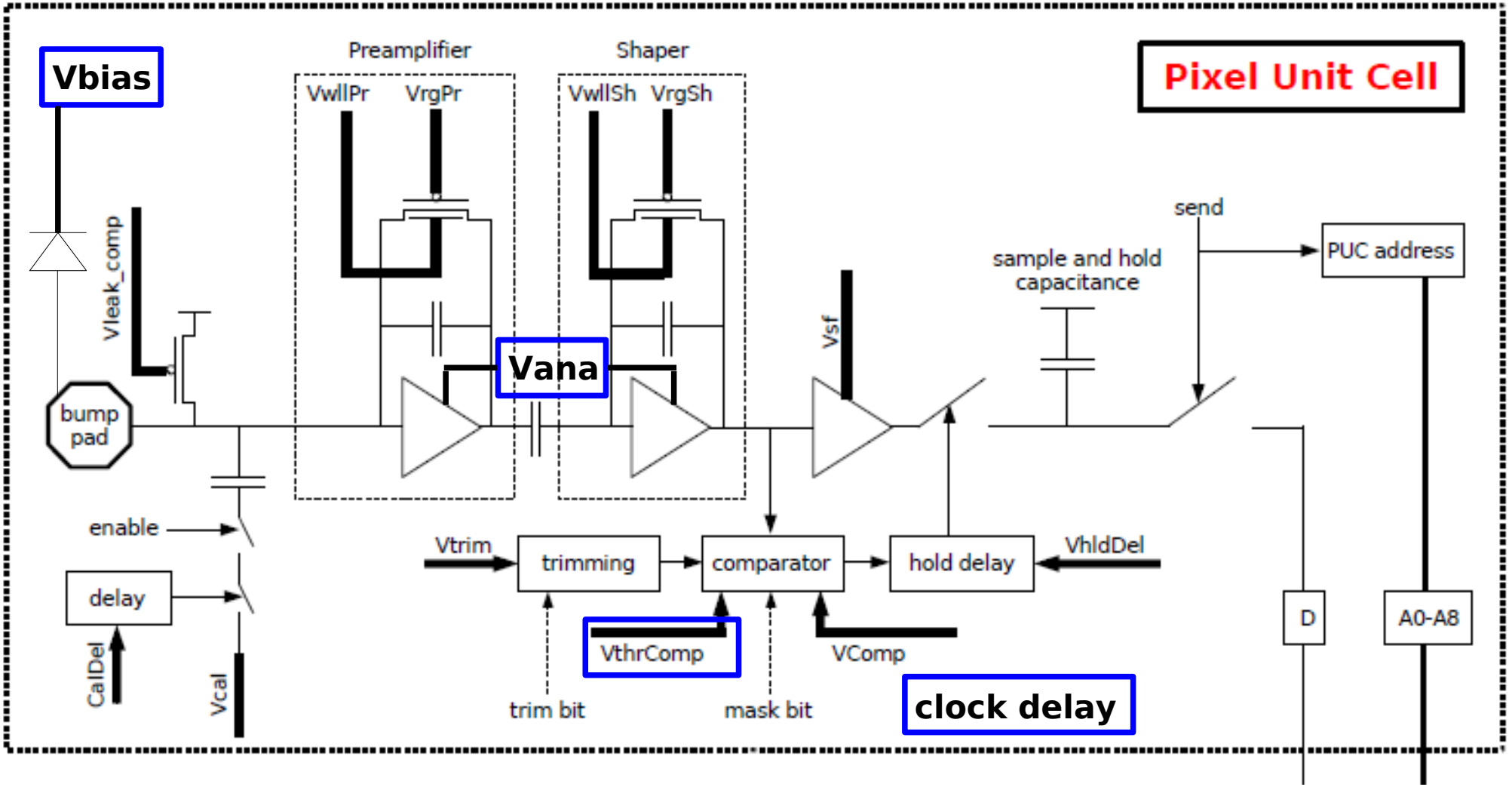
20.01.2012



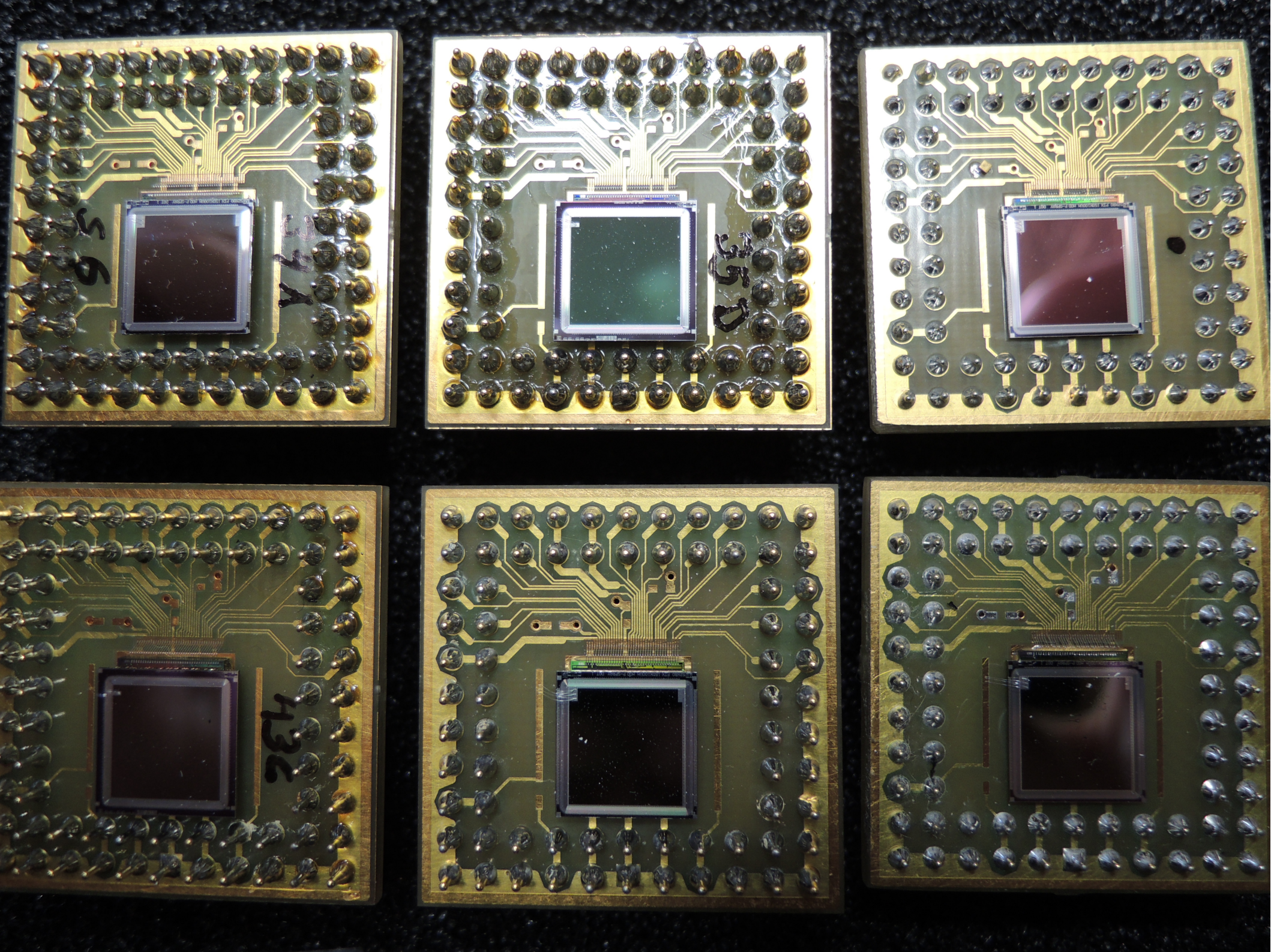
Goals for the April 2012 beam test

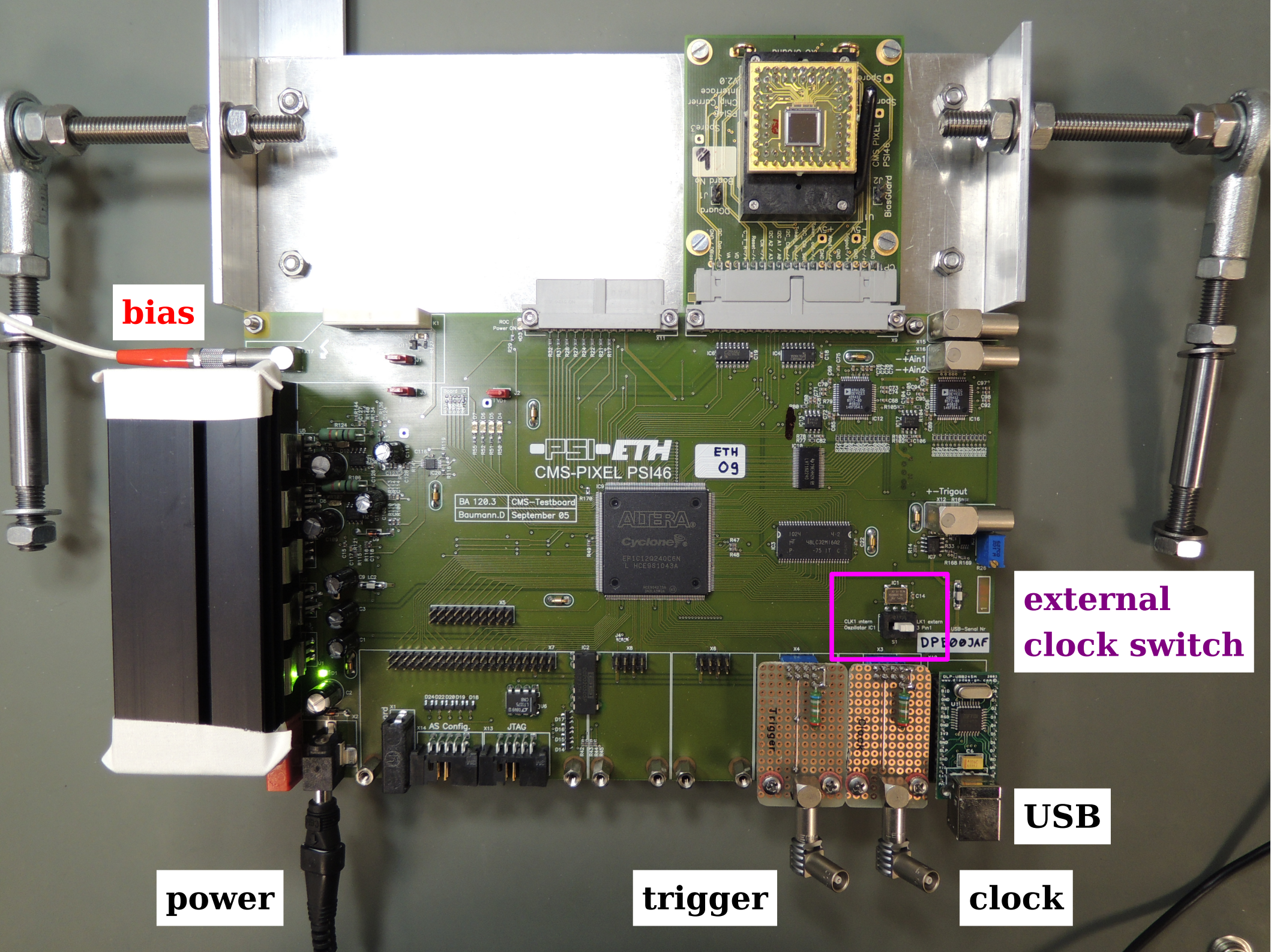
- Take reference data with the present Pixel ROC PSI46 v2.3
  - large statistics
- measure efficiency and resolution
  - vs clock delay (0..25 ns)
  - vs bias voltage (up to 150 V with new Keithley, need Triax adapter)
  - vs threshold (soft to hard, cutting small pulses)
  - vs tilt angle (0 to 30 deg, mimic Lorentz angle)
- Procedure established:
  - operate 2 single chip modules
  - clock synchronized with the DESY II beam
  - parallel DAQ with 2 PSI46 test boards and the EUDET telescope
  - analyze with modified/extended EUTelescope software
- 2nd beam test with new PSI46xdb mid June – mid July

PSI46 pixel ROC

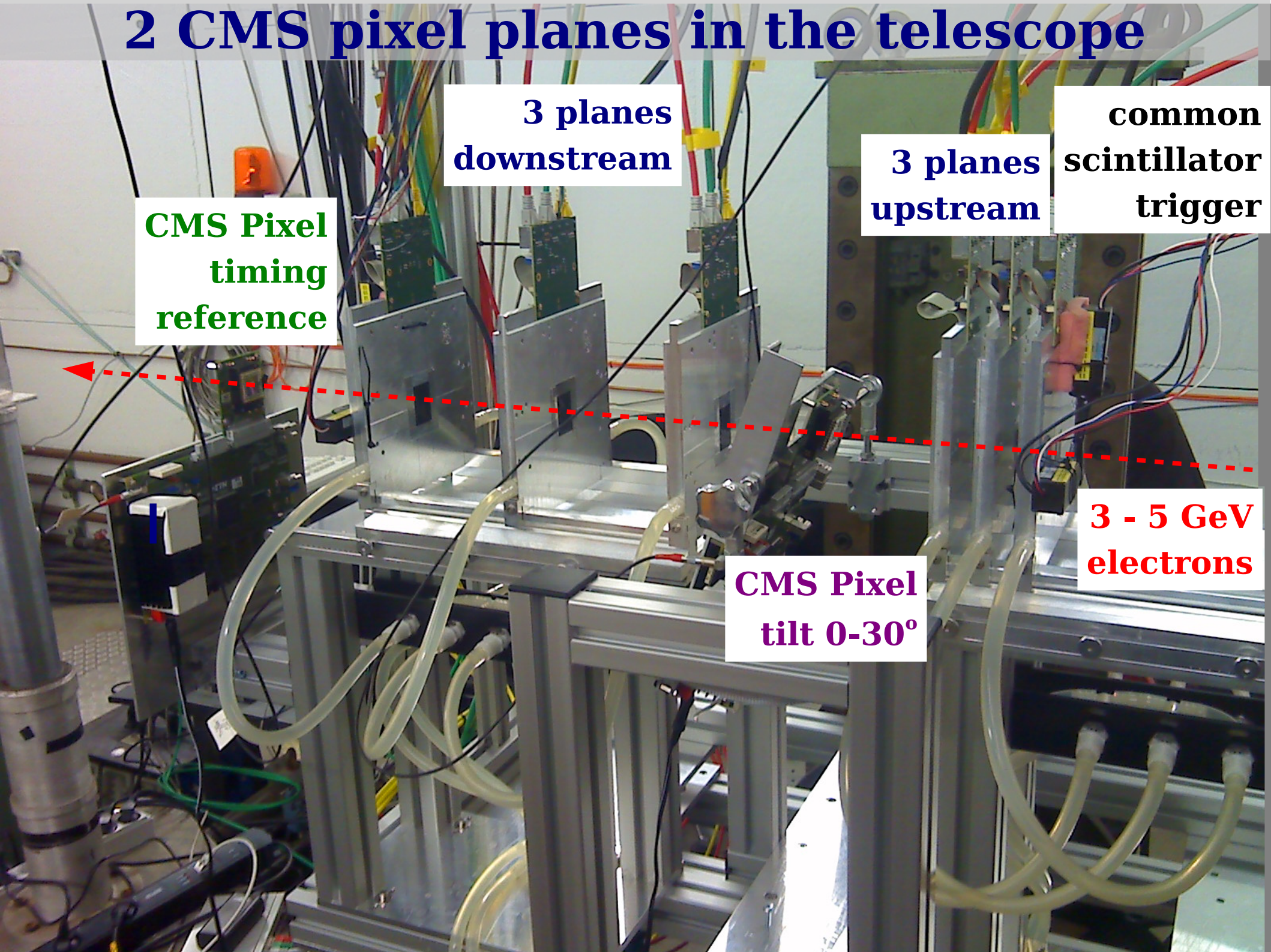


vary in beam test



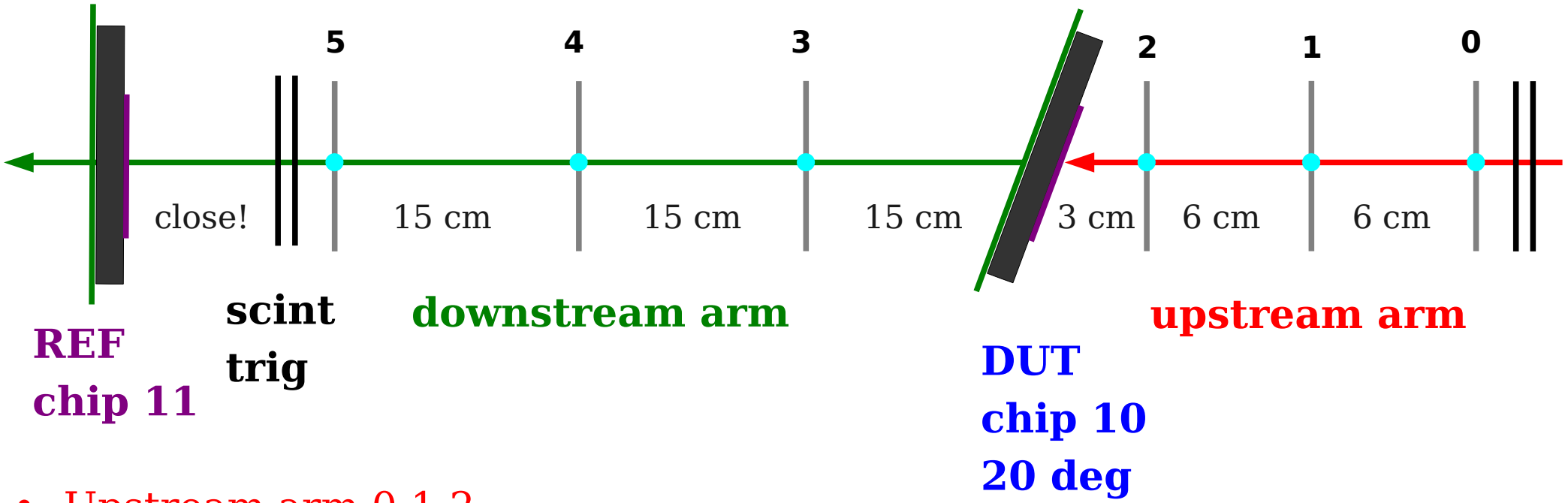

bias
external
clock switch
USB
power
trigger
clock

2 CMS pixel planes in the telescope



new telescope in TB 22

Default set up

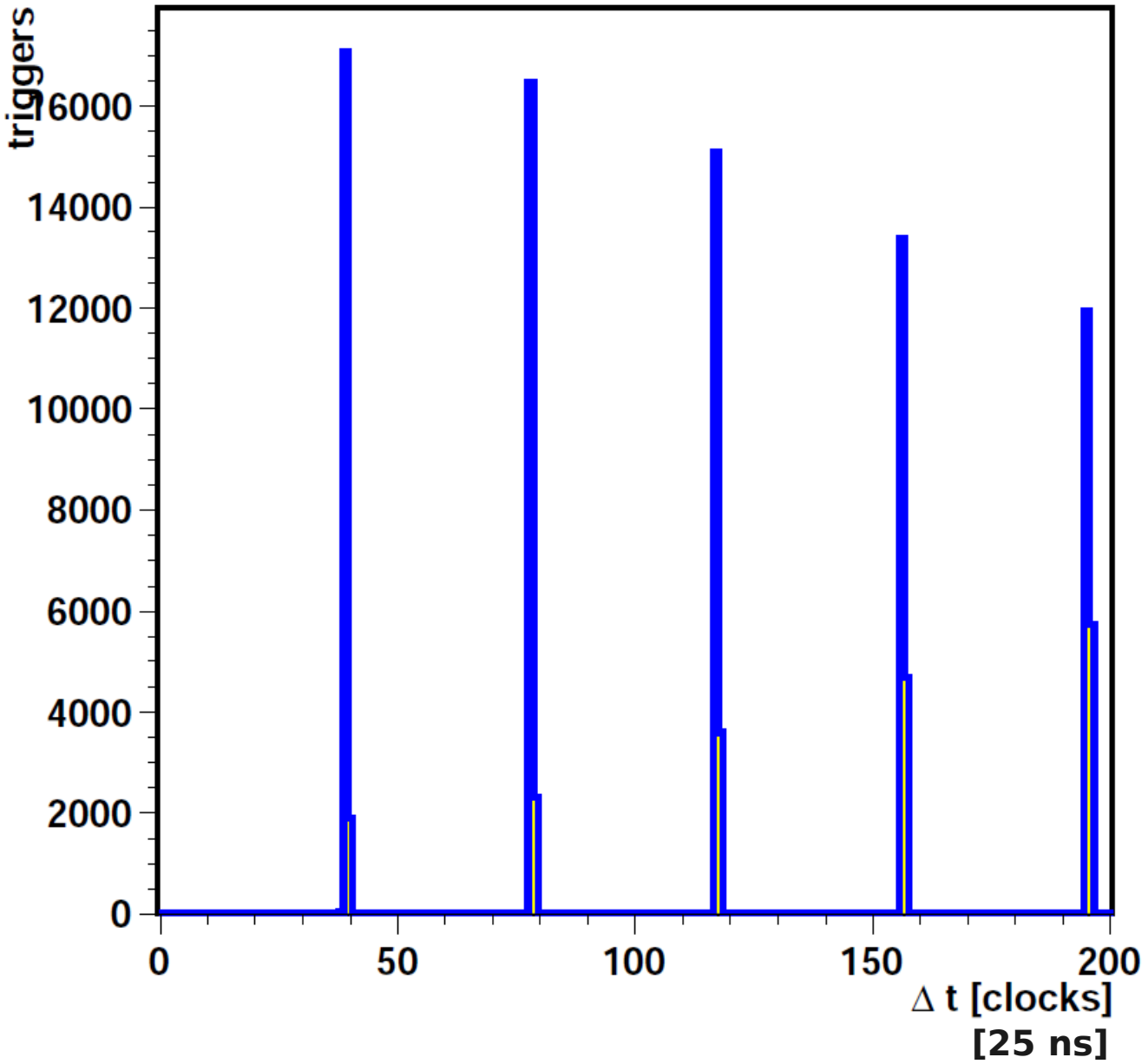


- Upstream arm 0-1-2:
  - as close as possible to DUT, but allow for insertion and tilting
- DUT = single chip module, tilted by up to 30°,
- Downstream arm 3-4-5:
  - equally spaced between DUT and REF, allow for DUT tilting
- REF = single chip module for timing, as close as possible behind scint
- trigger: 4-fold coincidence (config: TLU AndMask 15)

timing in DESY II

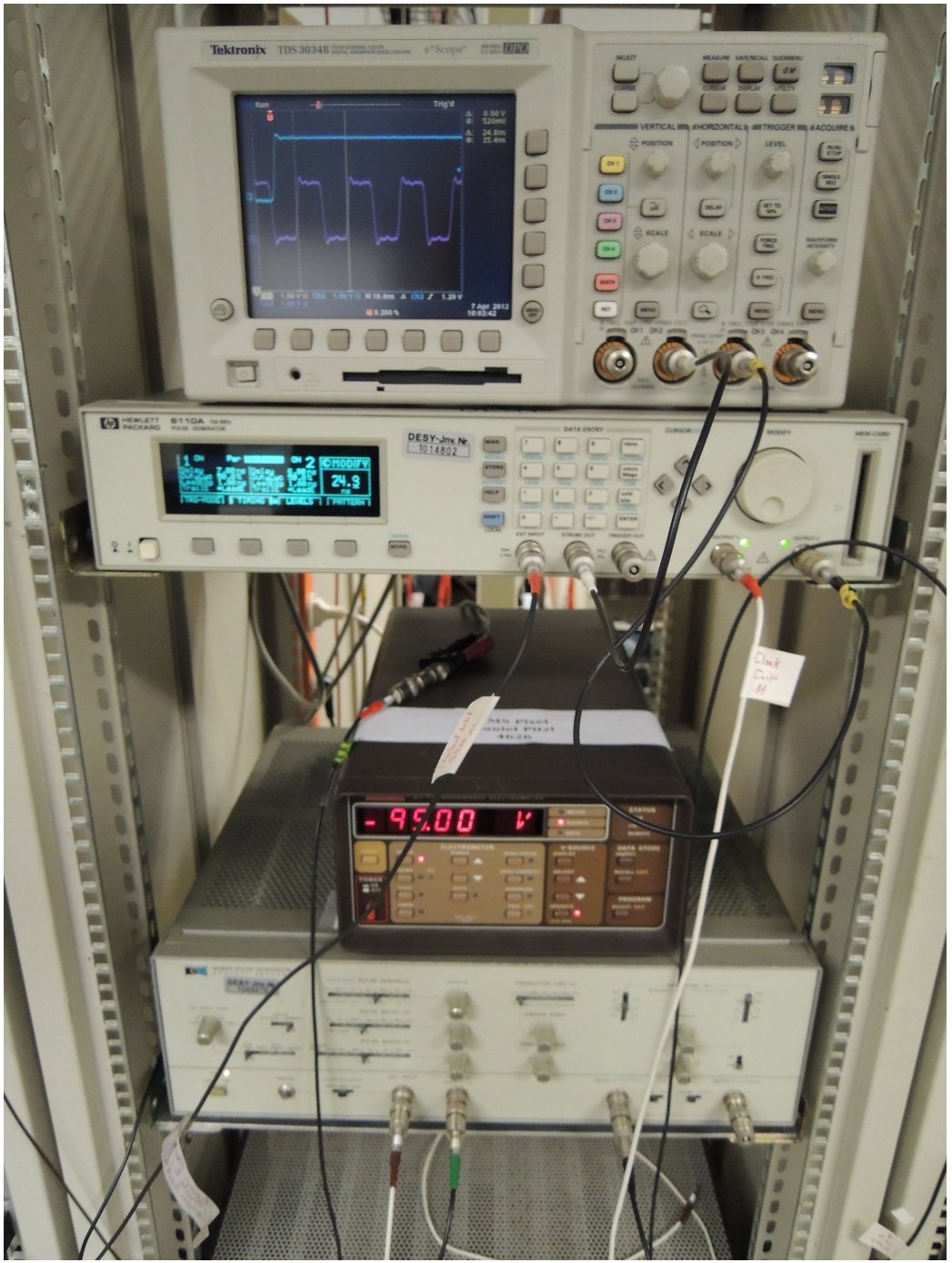
CMS pixel without telescope (fast)

time between events:



- DESY II circumference is 292.8 m
- DESY II has one bunch:
  - repeats every 0.976 µs (1.024 MHz)
  - = 39 × 25 ns
  - hardware signal
- CMS operates with 40 MHz clock
  - synchronous to the beam
  - need to generate!

clock, bias, and trigger

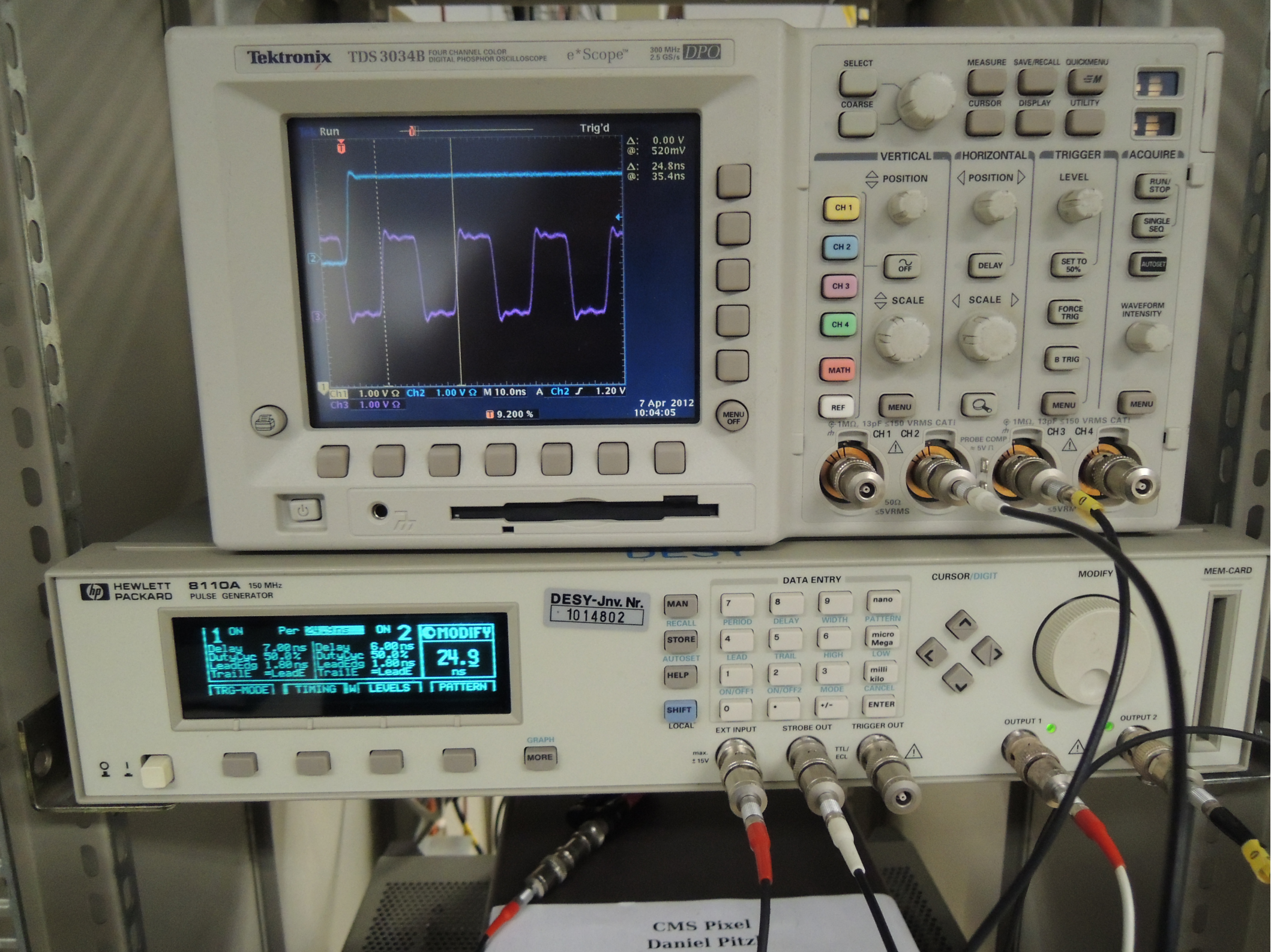


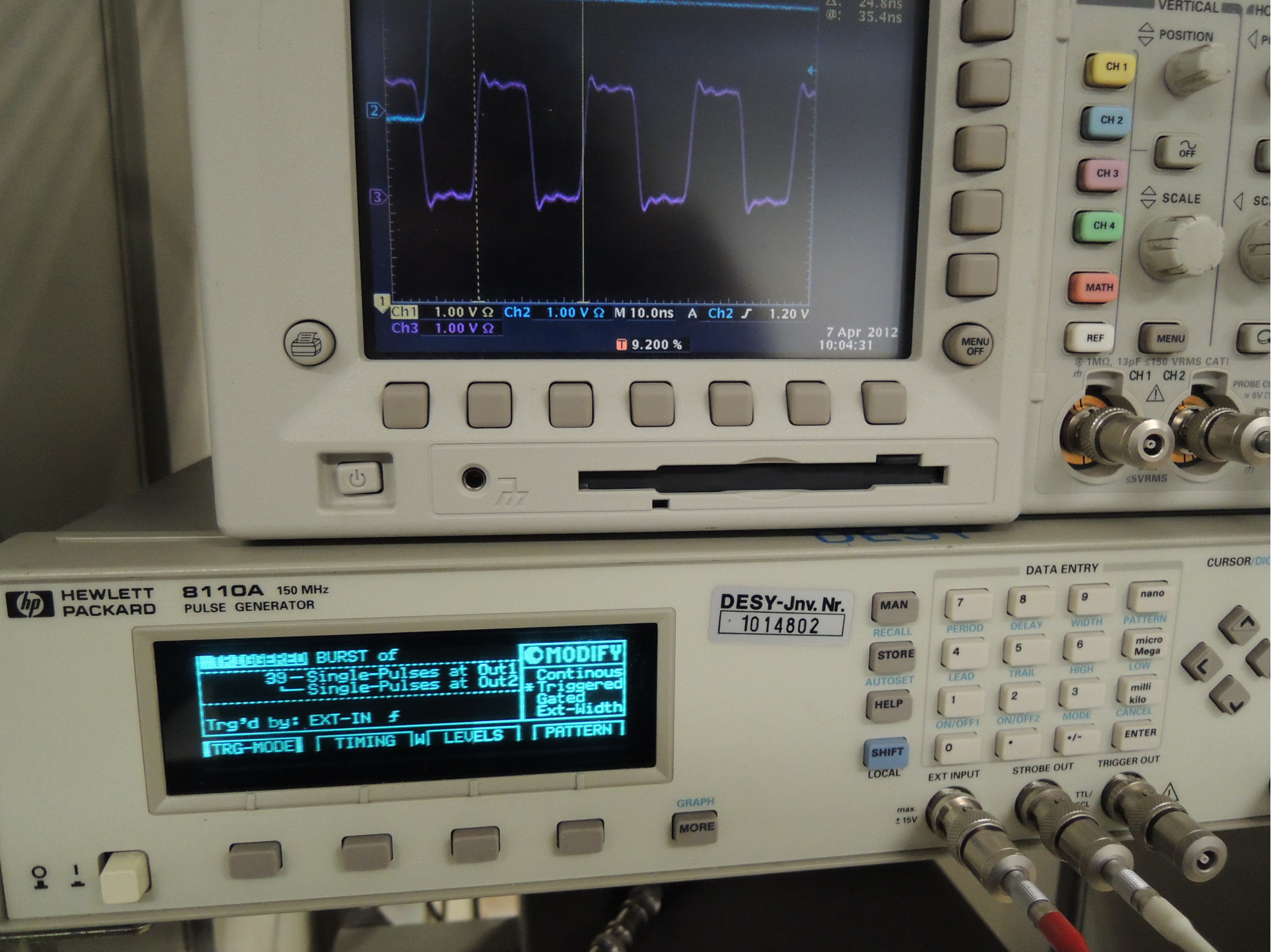
from U. Hurdelbrink (MHF):
generate 39 pulses of 25 ns
after every DESY bunch trigger

HP Agilent 8110A
pulse generator -> clock
(borrowed from U. Koetz)

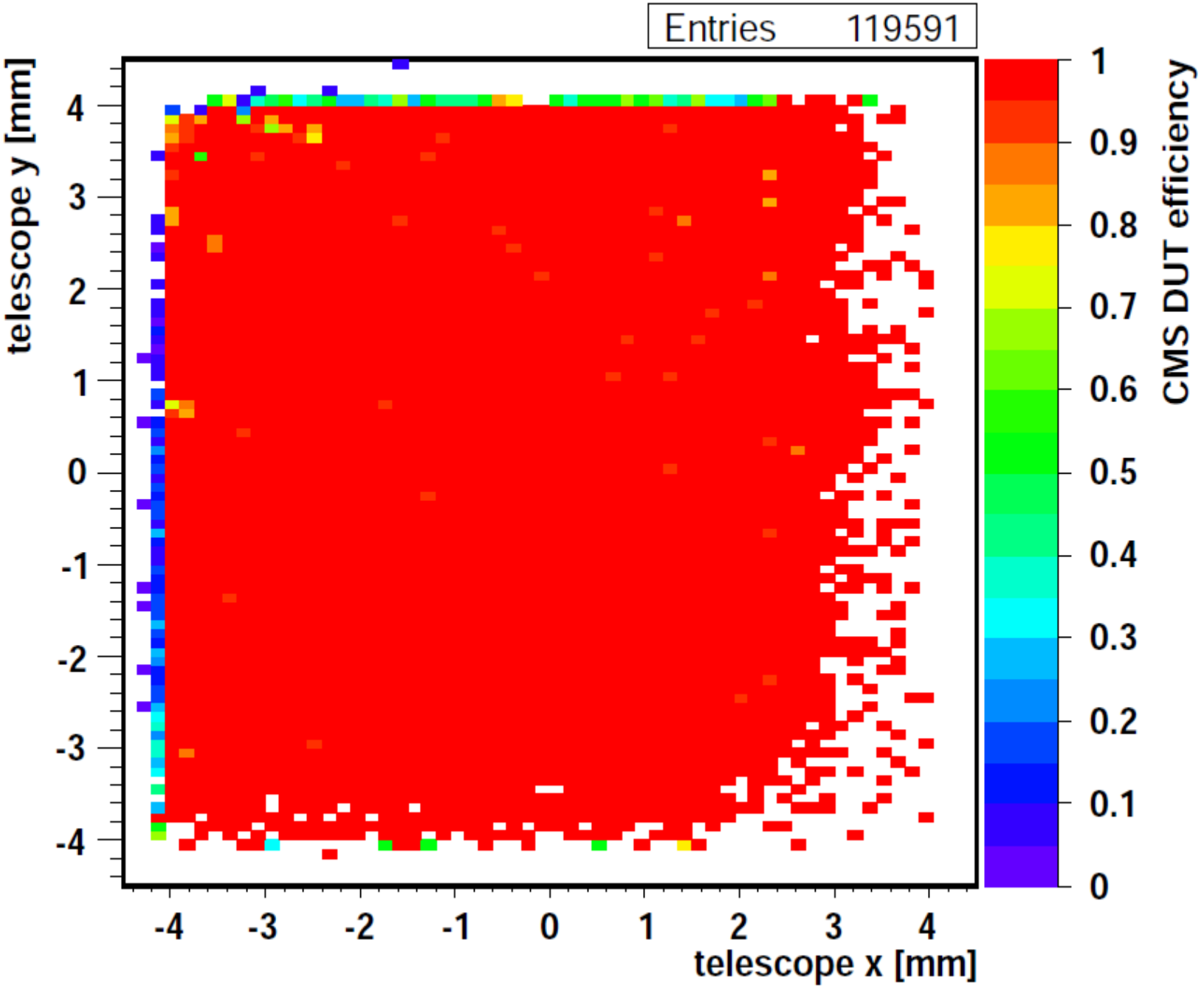
Keithley 617
bias voltage: -95V

HP pulse generator
-> trigger


Tektronix TDS 3034B FOUR CHANNEL COLOR DIGITAL PHOSPHOR OSCILLOSCOPE e*Scope 300 MHz 2.5 GS/s DPO
Run
Trig'd
Ch1 1.00 V Ω Ch2 1.00 V Ω M 10.0ns A Ch2 1.20 V
Ch3 1.00 V Ω
9.200 %
7 Apr 2012
10:04:05
SELECT
COARSE
MEASURE
CURSOR
SAVE/RECALL
DISPLAY
QUICKMENU
UTILITY
VERTICAL
HORIZONTAL
TRIGGER
ACQUIRE
POSITION
SCALE
LEVEL
CH 1
CH 2
CH 3
CH 4
MATH
REF
OFF
DELAY
SET TO 50%
FORCE TRIG
B TRIG
MENU
RUN/ STOP
SINGLE SEQ
AUTOSET
WAVEFORM INTENSITY
PROBE COMP ≈ 5V
CH1 CH2
CH3 CH4
50Ω ≤5VRMS
HEWLETT PACKARD 8110A 150 MHz PULSE GENERATOR
DESY-Jnv. Nr. 1014802
MODIFY
24.9 ns
TRG-MODE
TIMING
LEVELS
PATTERN
MAN
RECALL
STORE
AUTOSET
HELP
SHIFT
LOCAL
GRAPH
MORE
DATA ENTRY
CURSOR/DIGIT
MODIFY
MEM-CARD
PERIOD
DELAY
WIDTH
PATTERN
LEAD
TRAIL
HIGH
LOW
ON/OFF1
ON/OFF2
MODE
CANCEL
ENTER
EXT INPUT
STROBE OUT
TRIGGER OUT
TTL/ ECL
OUTPUT 1
OUTPUT 2
CMS Pixel
Daniel Pitz


Ch1 1.00 V Ω Ch2 1.00 V Ω M 10.0ns A Ch2 1.20 V
Ch3 1.00 V Ω
9.200 %
7 Apr 2012
10:04:31
VERTICAL
POSITION
CH 1
CH 2
CH 3
CH 4
OFF
SCALE
MATH
REF
MENU
MENU OFF
CH1 CH2
≤5VRMS
HEWLETT PACKARD
8110A 150 MHz
PULSE GENERATOR
DESY-Jnv. Nr.
1014802
BURST of
39 Single-Pulses at Out1
Single-Pulses at Out2
Trg'd by: EXT-IN
MODIFY
Continous
Triggered
Gated
Ext-Width
TRG-MODE
TIMING
LEVELS
PATTERN
GRAPH
MORE
MAN
RECALL
STORE
AUTOSET
HELP
SHIFT
LOCAL
DATA ENTRY
PERIOD
DELAY
WIDTH
PATTERN
LEAD
TRAIL
HIGH
LOW
ON/OFF1
ON/OFF2
MODE
CANCEL
ENTER
EXT INPUT
STROBE OUT
TRIGGER OUT
CURSOR

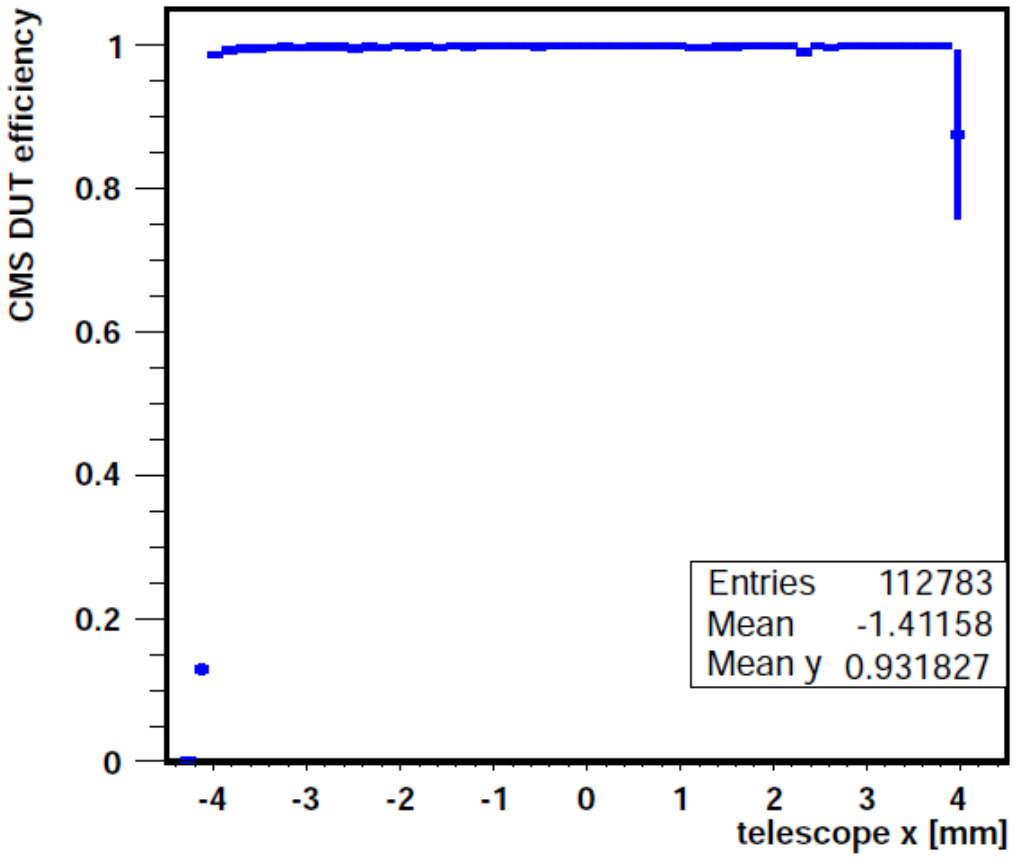
Efficiency map



- run 2880
  - 60 min
- 4.0 GeV
- chip 10
- tilt 20°
- clock delay 7 ns

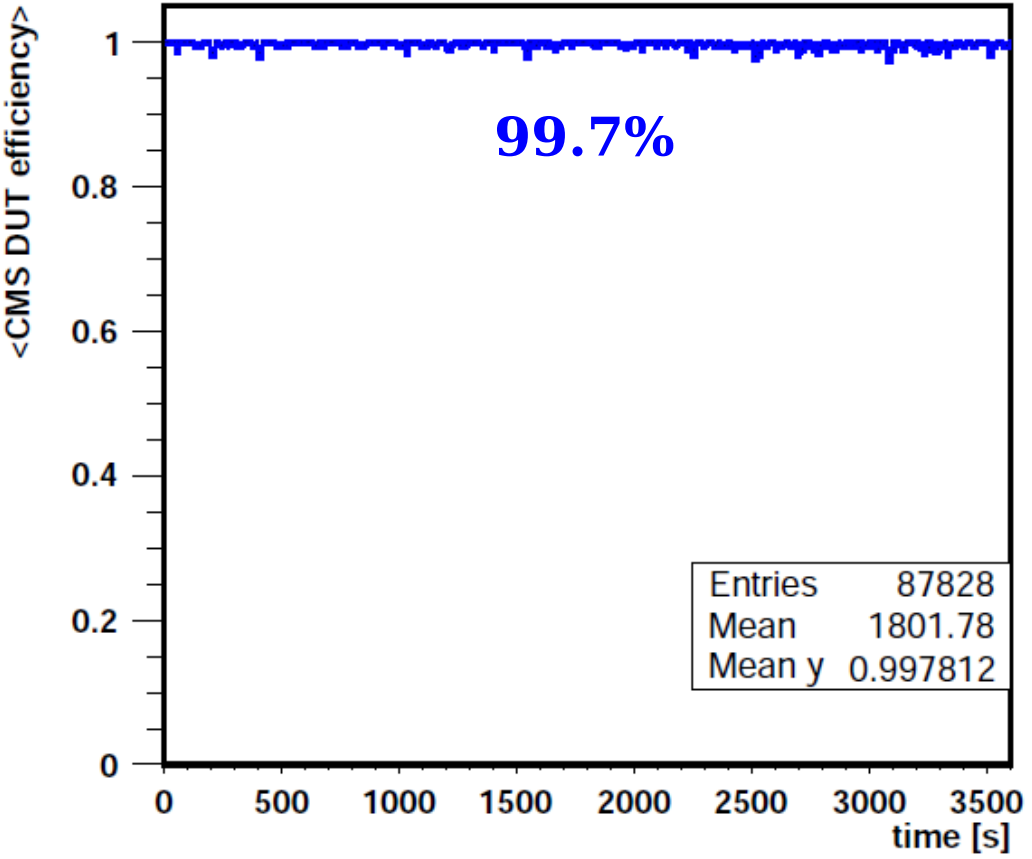
Efficiency profiles

fiducial cuts in *y*



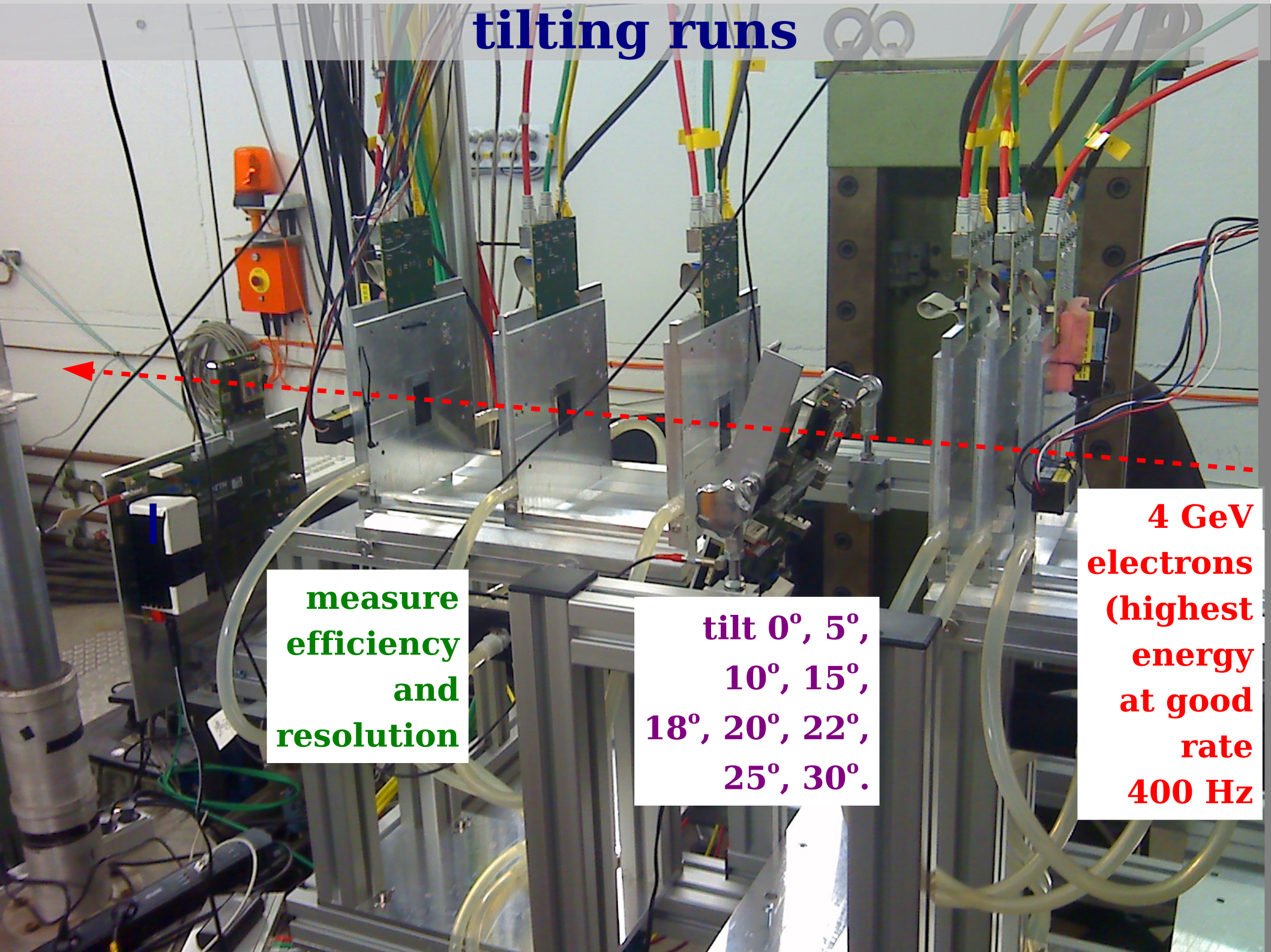
52 columns

fiducial cuts in *x* and *y*

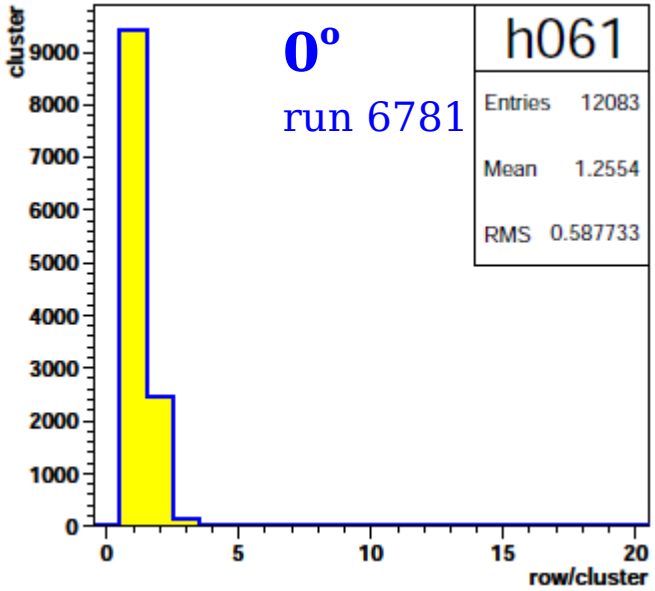


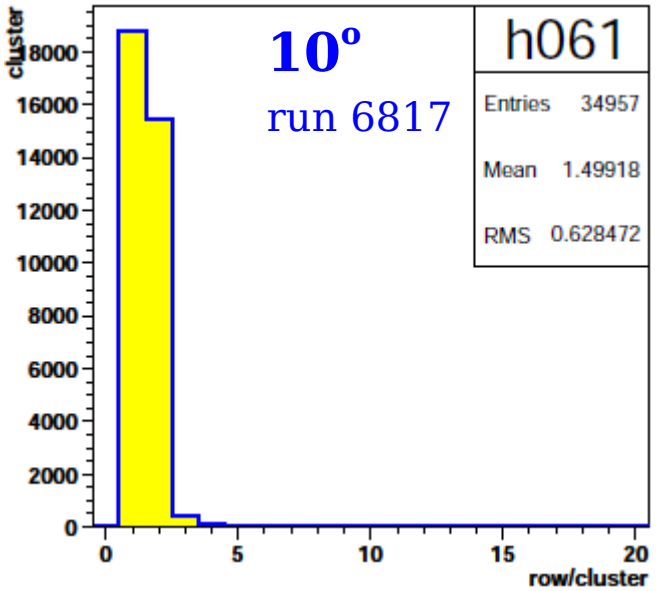
one hour

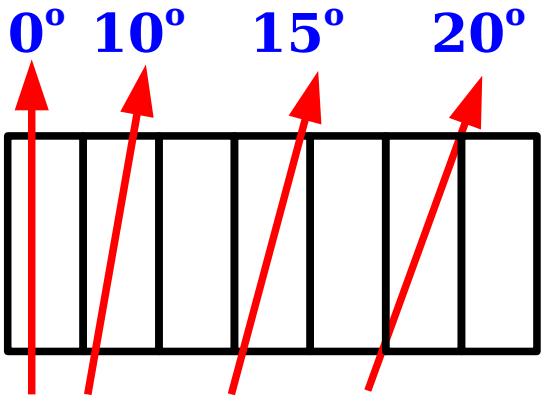
tilting runs



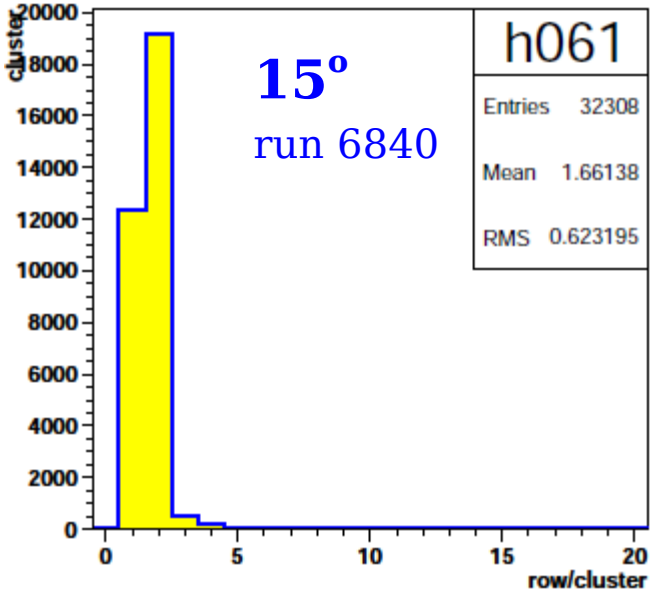
cluster size vs tilt angle

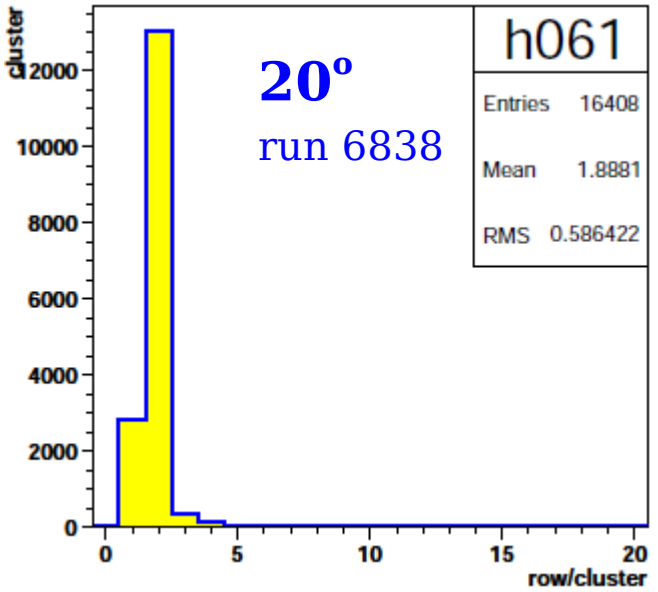


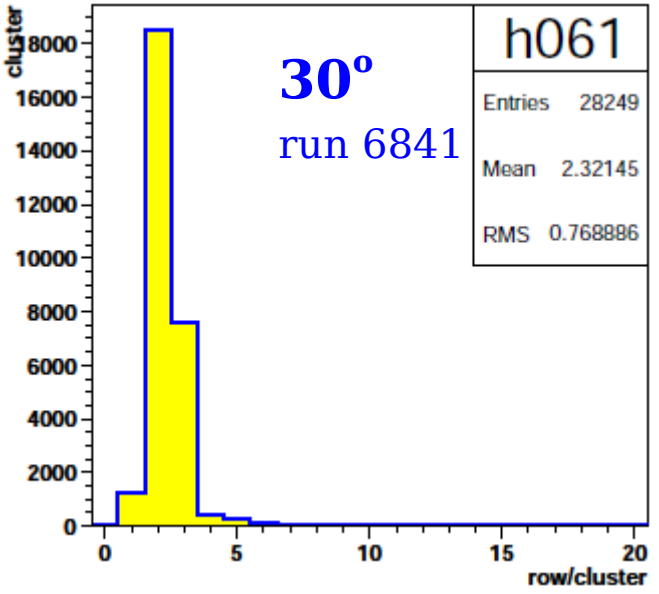




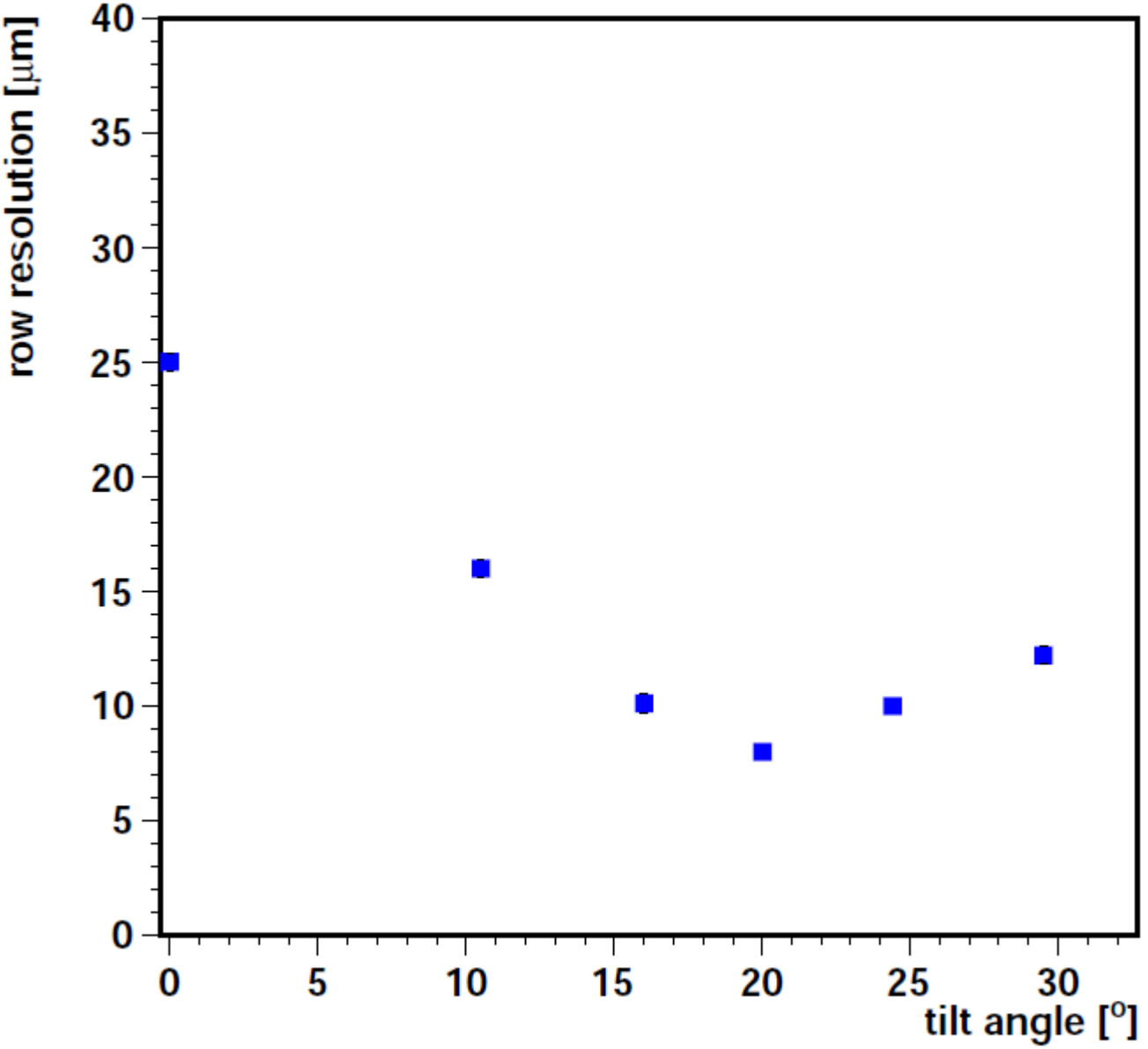
atan(100/285) = 19.3°

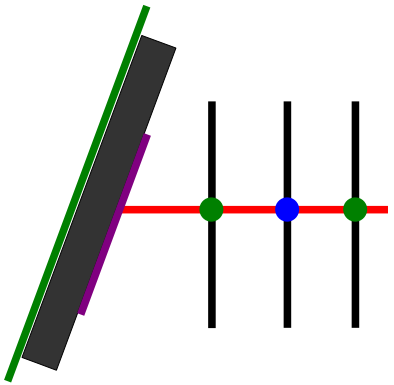






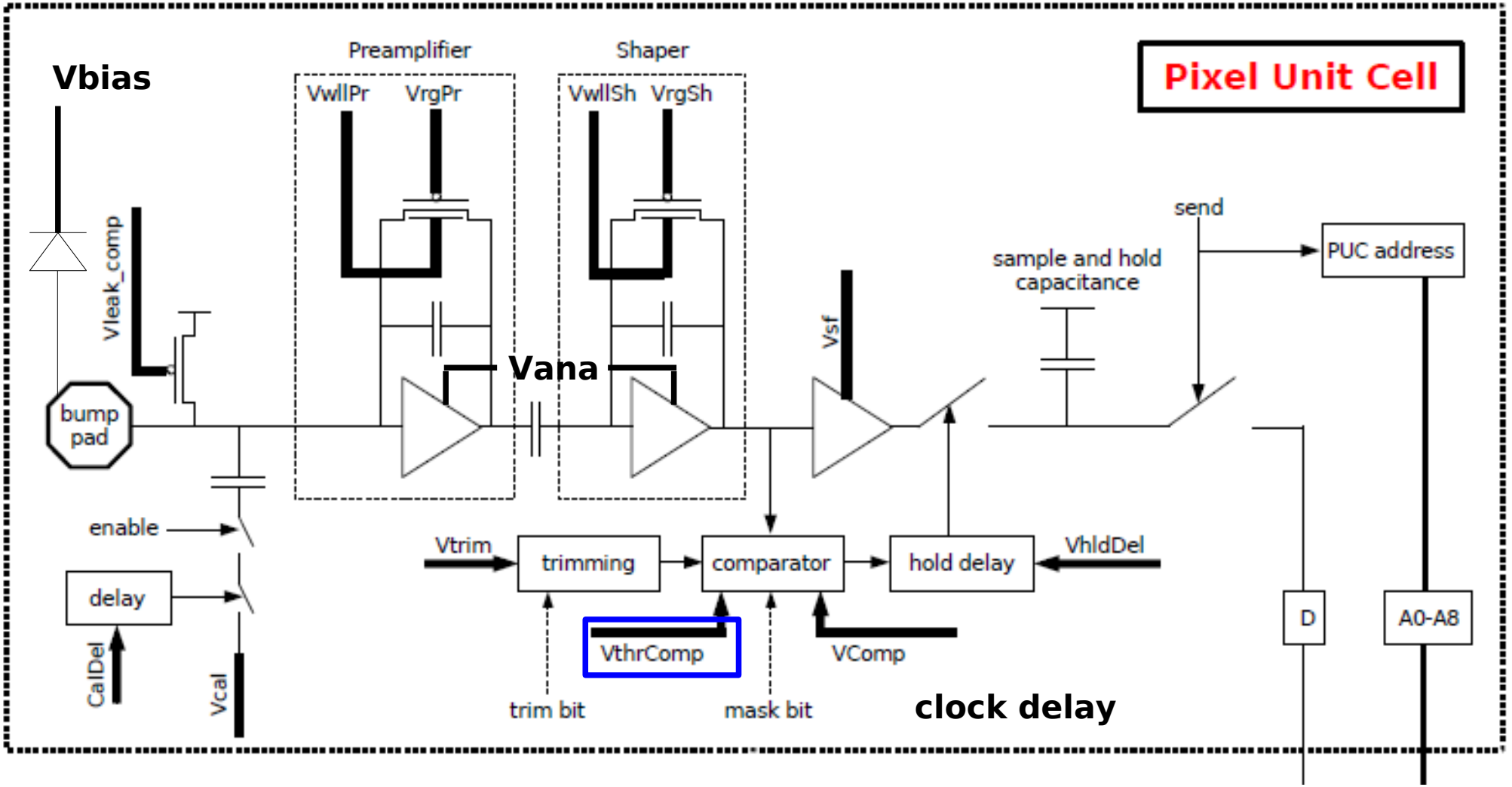
CMS pixel row resolution vs tilt angle





- 6 GeV, telescope extrapolation uncertainty subtracted.
- row pixels = 100 μm.
- Binary:
  - σ = 100 / √12 = 29 μm
- Optimal angle 19°:
  - σ = 8 μm.

threshold scan



threshold from soft to hard: loose small pulses

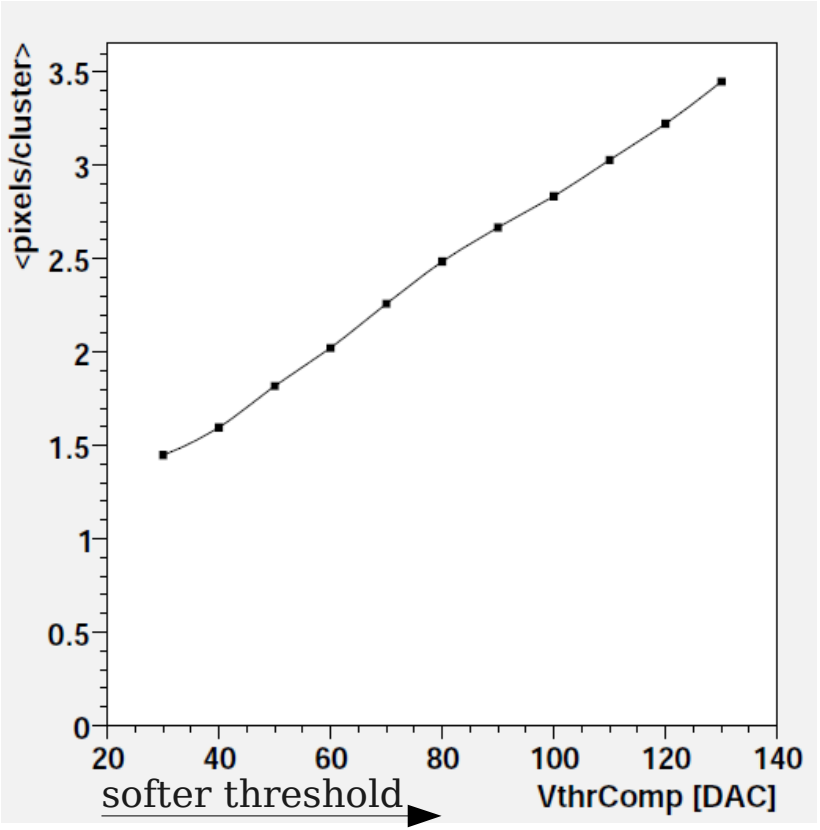
simulates reduced charge collection

study cluster size, resolution, efficiency

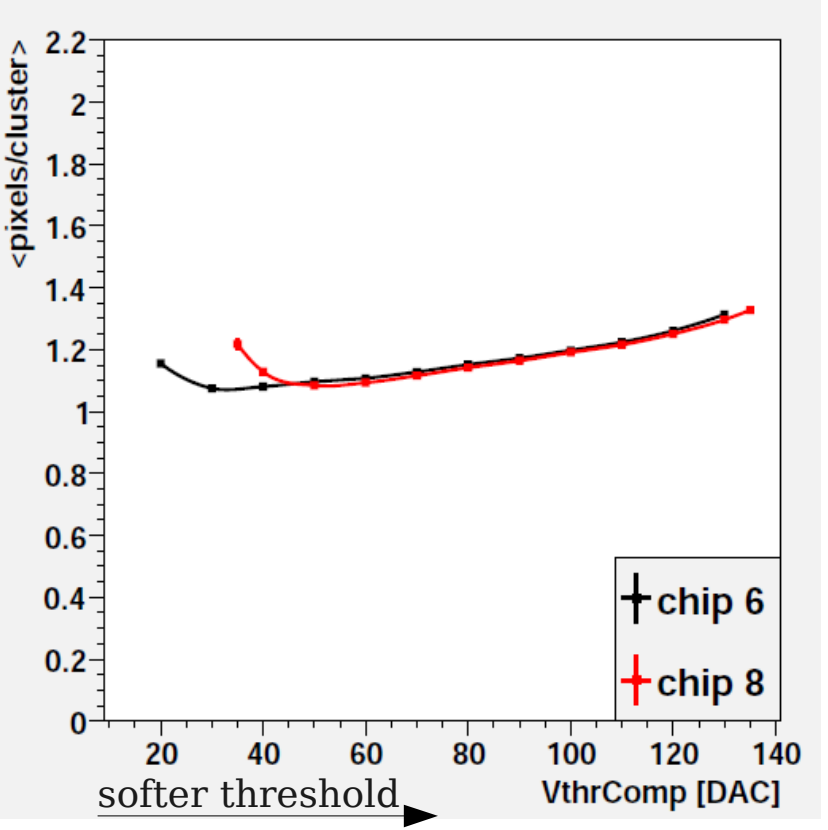
Cluster size vs. ROC threshold

A. Gajos, summer student, Sep 2011

Ru source: 3 MeV e



Test beam at 0º



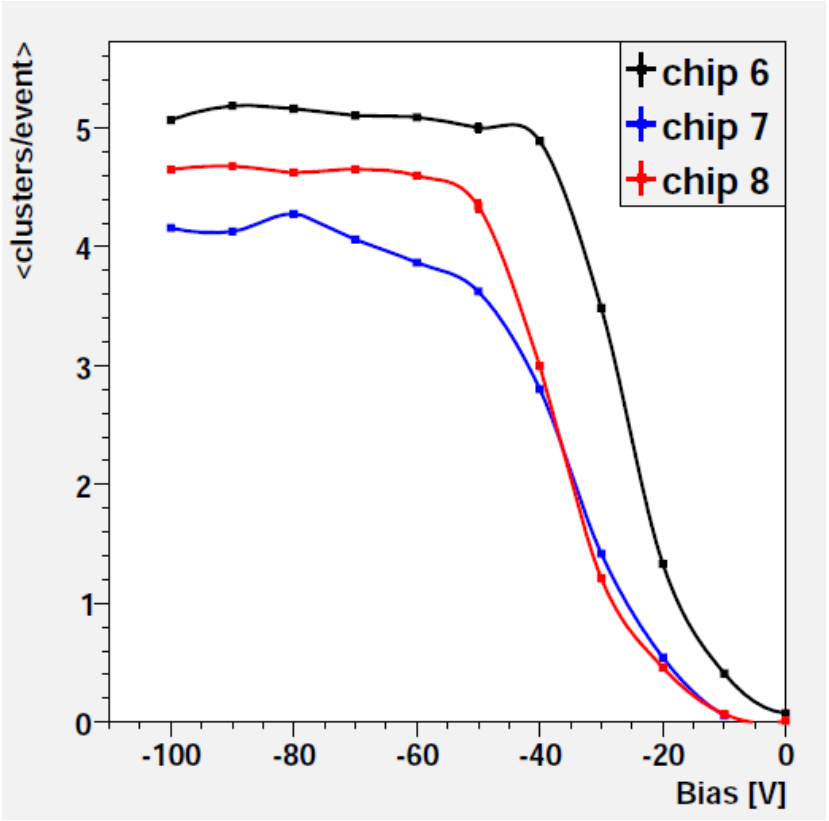
- strong effect:
  - all incident angles
  - lots of scsttering
  - makes large clusters

- weak effect:
  - mostly 1-pixel clusters at 0°
- repeat at 20°
  - expect larger effect

Cluster rate vs. sensor bias voltage

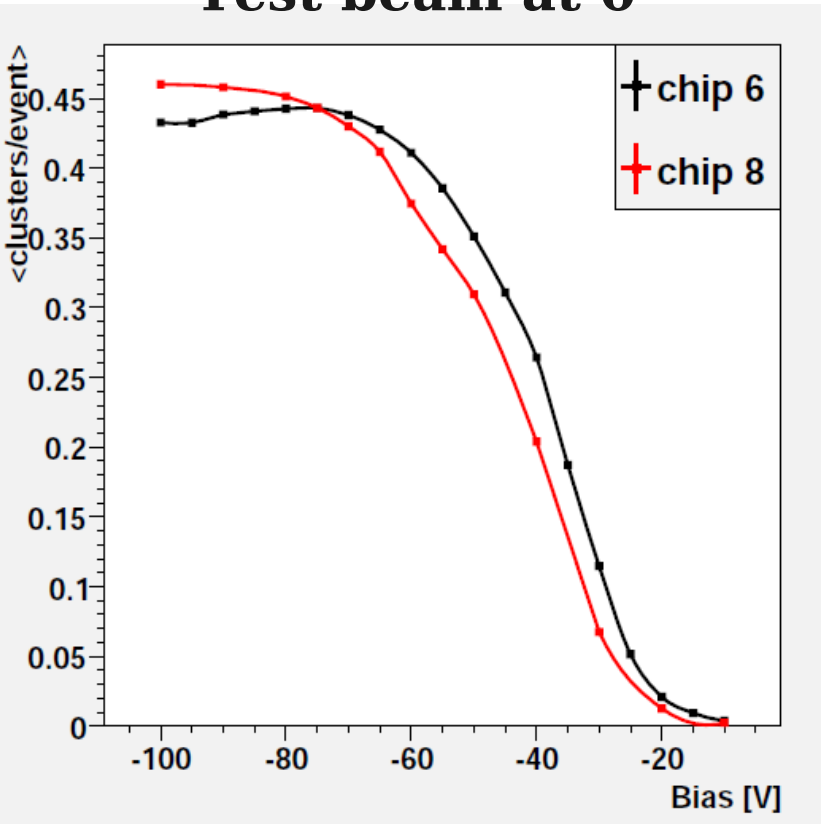
A. Gajos, summer student, Sep 2011

Ru source: 3 MeV e



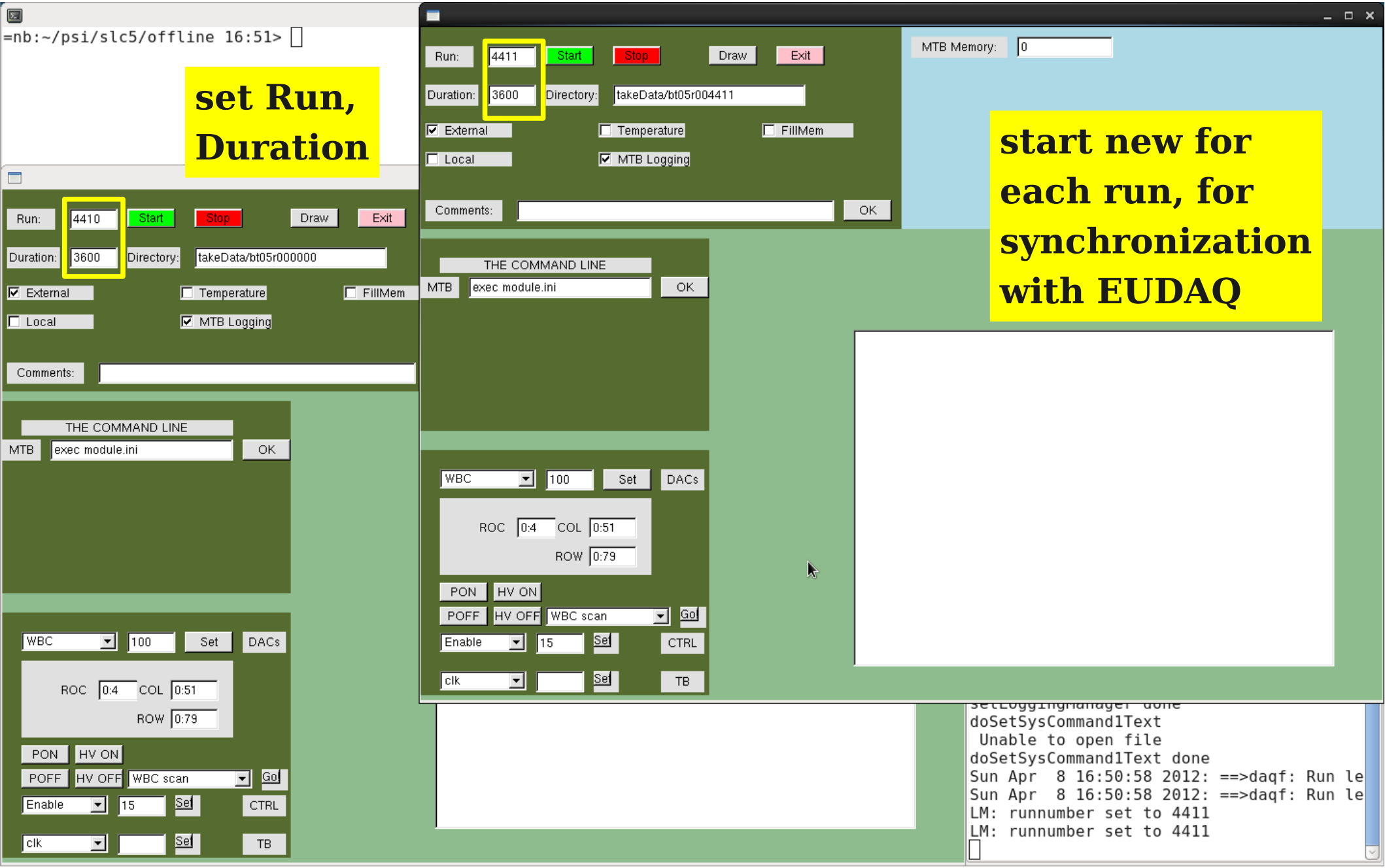
- large pulses → cluster rate reaches plateau at –50V
- Chip variation: source alignment and threshold differences

Test beam at 0º



- efficiency plateau at –80V when full charge is collected
- Chips similar: vertical incidence and optimized thresholds

CMS pixel DAQ



Data taking

- CMS pixel DAQ: from `psi46expert`
  - `../bin/takeData -dir chip10` (DUT), set run i, duration, start
  - `../bin/takeData -dir chip11` (REF), set run j, duration, start
- EUDAQ:
  - `./STARTRUN`
  - config
  - start
- check CMS pixel: from `takeData`
  - `../../offline/b2h -c 10 -r i | less`
  - `root -l data00i.root`
  - `root> .x data2ps.C`
  - `acroread data.pdf`
  - `repeat for chip 11 run j`

EuTelescope software in Marlin

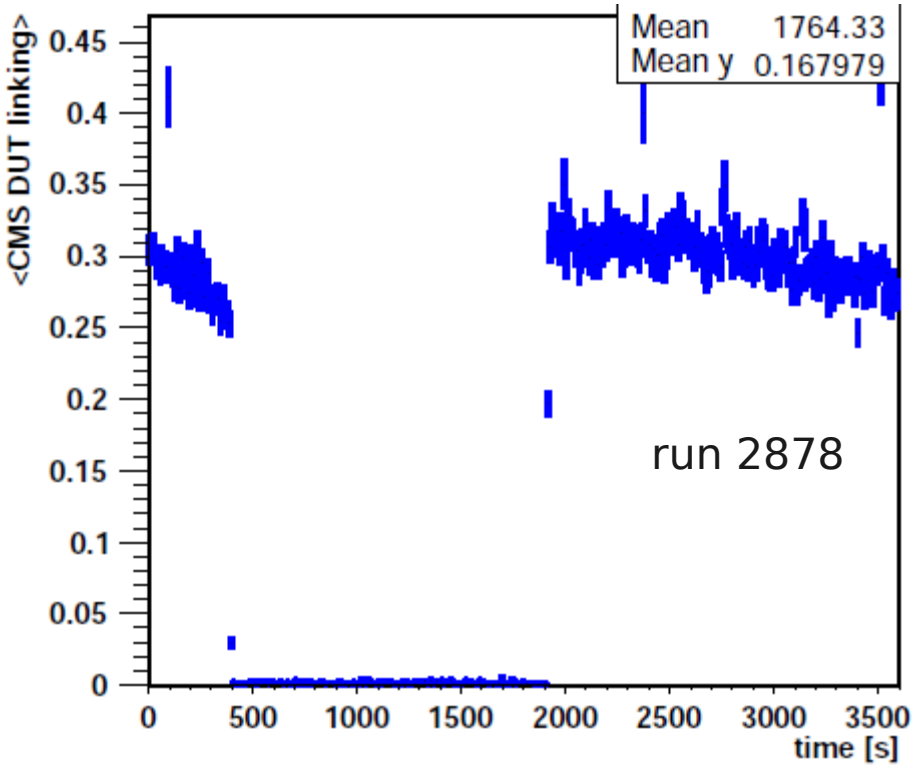
step	output.format	constants
0. EUDAQ data taking: 900s	**native.bin,** e.g. 200 MB 500k triggers	
1. convert, find hot pixels: 70s	**raw.lcio,** e.g. 200 MB	**hotpixel.db**
2. clustering: 240s	**clusters.lcio,** e.g. 400 MB	**offset.db**
3. hits, coarse align: 250s	**hits.lcio,** e.g. 600 MB	**pre-align.db**
4. Millepede alignment: 12s **GBL**	**pede.bin,** e.g. 120 MB	**align.db**
5. track fitting: 270s **GBL**	**tracks.lcio,** e.g. 25 MB	

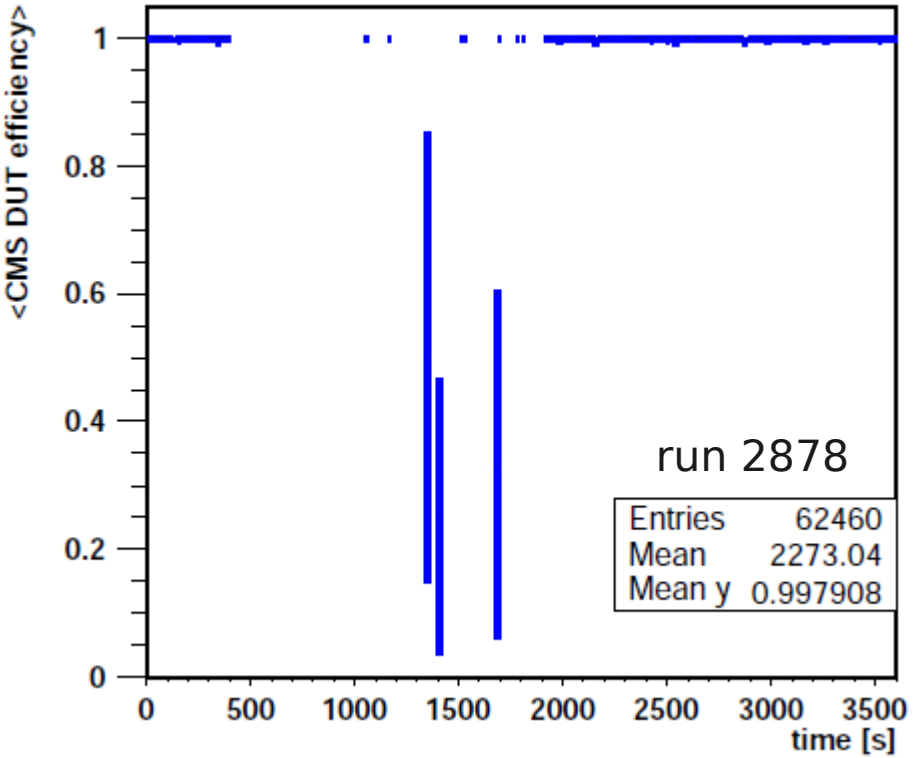
All steps produce ROOT histograms for monitoring

alignment of DUT and REF not yet fully automated

prompt offline feedback

- process EUTel runs on `desy-cms010` as soon as possible
  - convert, cluster, hits, align, fit
  - check histograms (macros available)
  - iterate TestFitter for CMS DUT and REF alignment
  - evaluate run quality: efficiency vs time stable?





documentation

- paper logbook and online logbook (text or web?):
  - record settings (bias, delay, trigger, beam energy, tilt, threshold)
  - record conditions (e.g. temperature)
  - record date, time, run numbers
  - record interruptions and adjustments, access to beam area
  - sign by name
  - make fotos

proposed programme

- Defaults: DUT at 20°, bias -150 V, softest threshold, optimal delays
- Optimize rate in test beam by adjusting position ½ day
- Clock delay scan: 0..24 ns, 4 ns steps, finer at edges (~10 runs) ½ day
- Bias voltage scan: -150 to -10 V, 20 V steps (8 runs) ½ day
- DUT tilt scan: 0°, 5°, 10°, 15°, 18°, 20°, 22°, 25°, 30° (9 long runs) 1.5 day
- Threshold scan: `VthrComp` 97 to 7 step 10 (10 long runs) 1.5 day
- gain calibrations each day
- scan Vana (less power), always re-optimize other DACs 2 days
  - possibly repeat delay and threshold scans
- another chip as DUT 1 day
- repeat problematic runs 1 day
- reserve 1 day + weekends + extension week

chip 10 DACs

1	Vdig	6
2	Vana	126
3	Vsf	170
4	Vcomp	10
5	Vleak_comp	0
6	VrgPr	0
7	VwllPr	35
8	VrgSh	0
9	VwllSh	35
10	VhldDel	150
11	Vtrim	113
12	VthrComp	97
253	CtrlReg	0
254	WBC	98

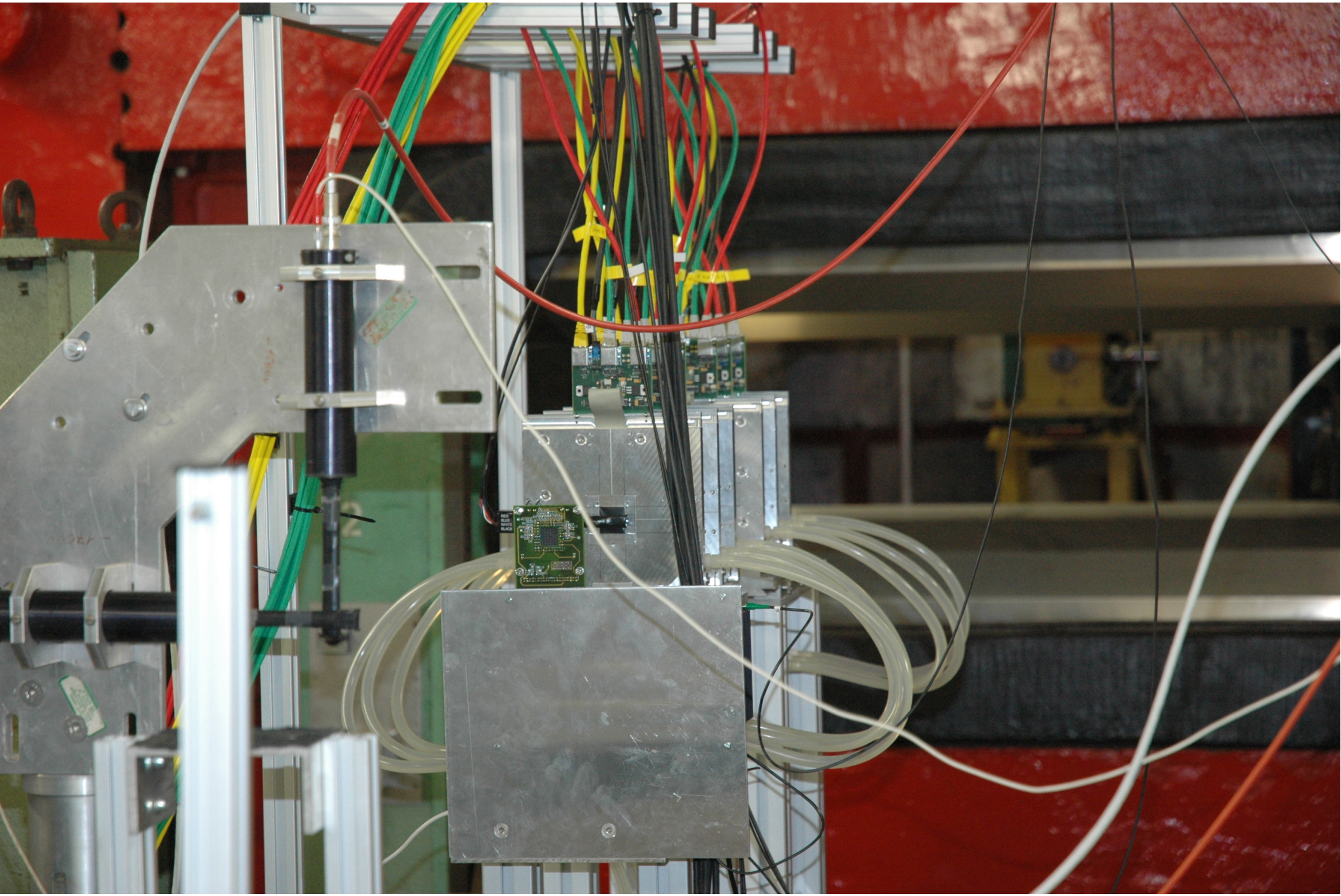
13	VIBias_Bus	30
14	Vbias_sf	10
15	VoffsetOp	27
16	VIbiasOp	115
17	VOffsetR0	120
18	VIon	130
19	VIbias_PH	130
20	Ibias_DAC	101
21	VIbias_roc	190
22	VIColOr	99
23	Vnpix	0
24	VSumCol	0
25	Vcal	200
26	CalDel	124
27	RangeTemp	0

Summary

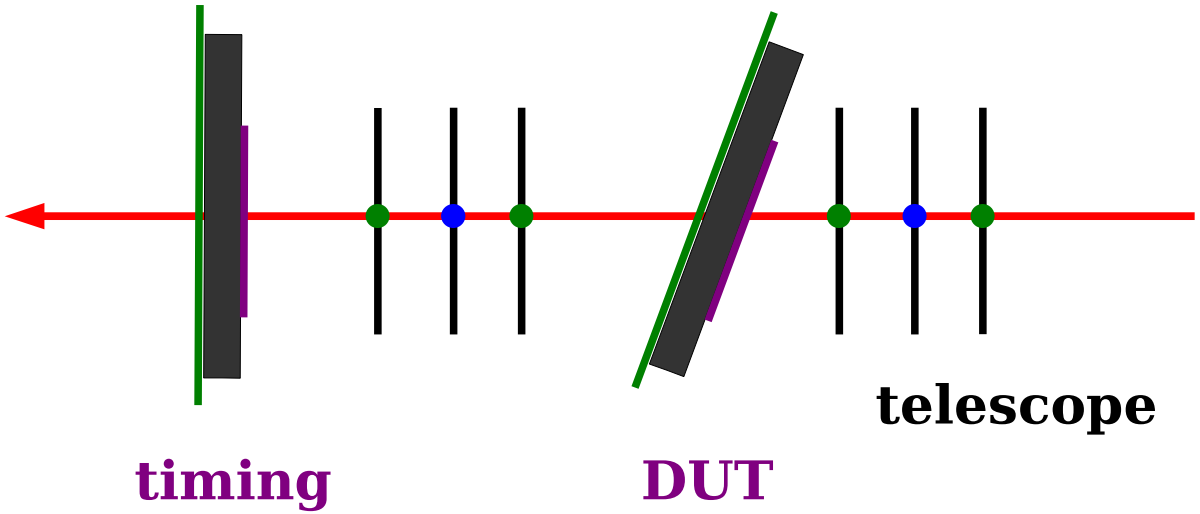
- Preparations for the April 2012 pixel beam test are well advanced:
  - hardware ready
  - offline software ready
  - measurement program defined
- to do:
  - improve online and prompt offline monitoring
  - prepare DAC parameters for lower Vana
  - prepare chip 13 as backup
  - temperature monitor with USB readout
  - shift assignments

Acknowledgements

- Ingrid Gregor, Artem Kravchenko, Igor Rubinskiy (all DESY ATLAS):
  - building the next telescope
- Adam Zuber, Holger Maser (DESY CMS):
  - tilting support frame for the test board
- Torsten Külper (FH electronics lab):
  - making the trigger and clock adapters for the test board
- Beat Meier (PSI):
  - new test board firmware with external trigger input
- Ulrich Hurdelbrink (machine group):
  - developing the clock generation setup
- Claus Kleinwort (DESY CMS):
  - General Broken Lines code, advice on alignment

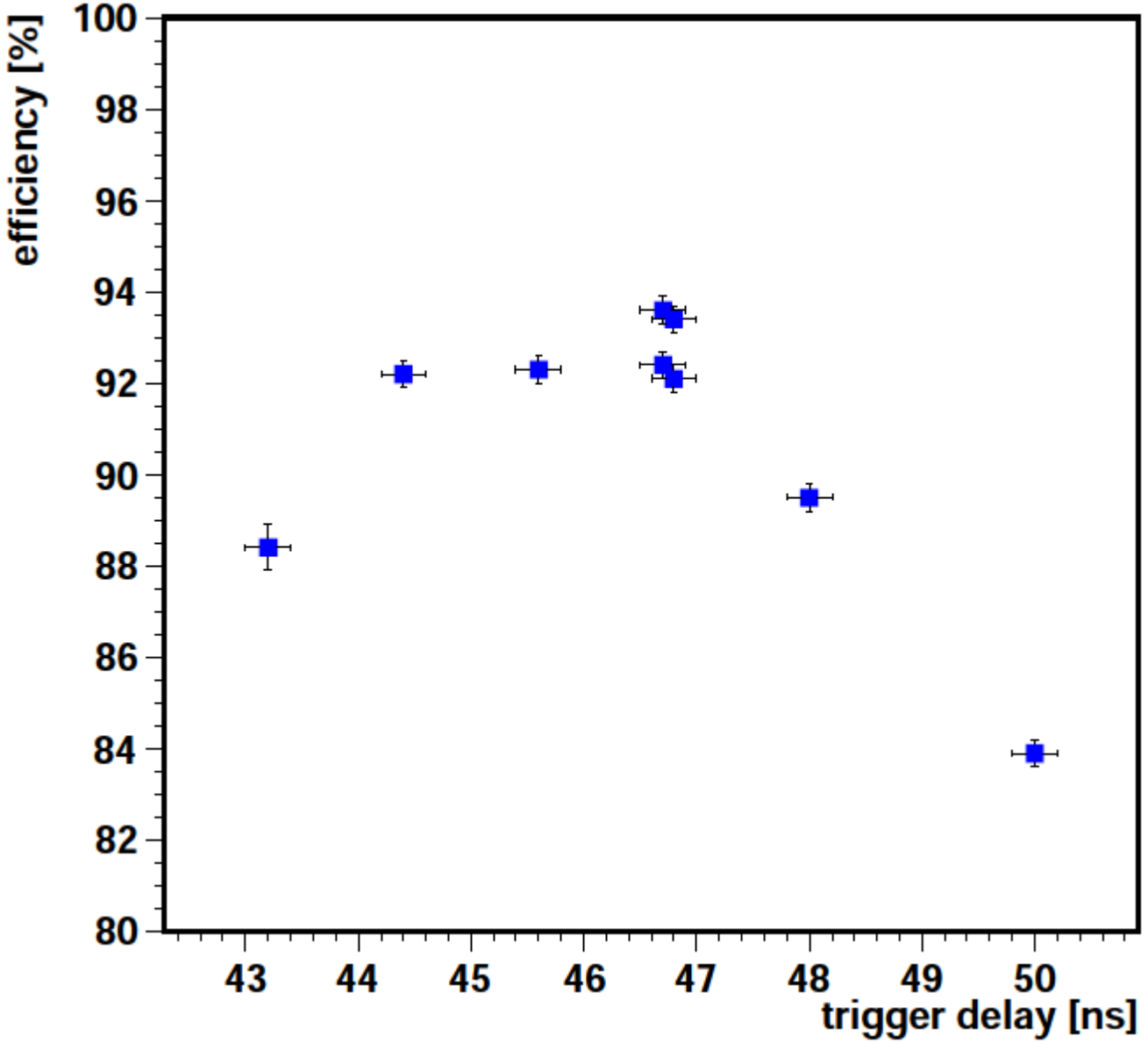


efficiency measurement



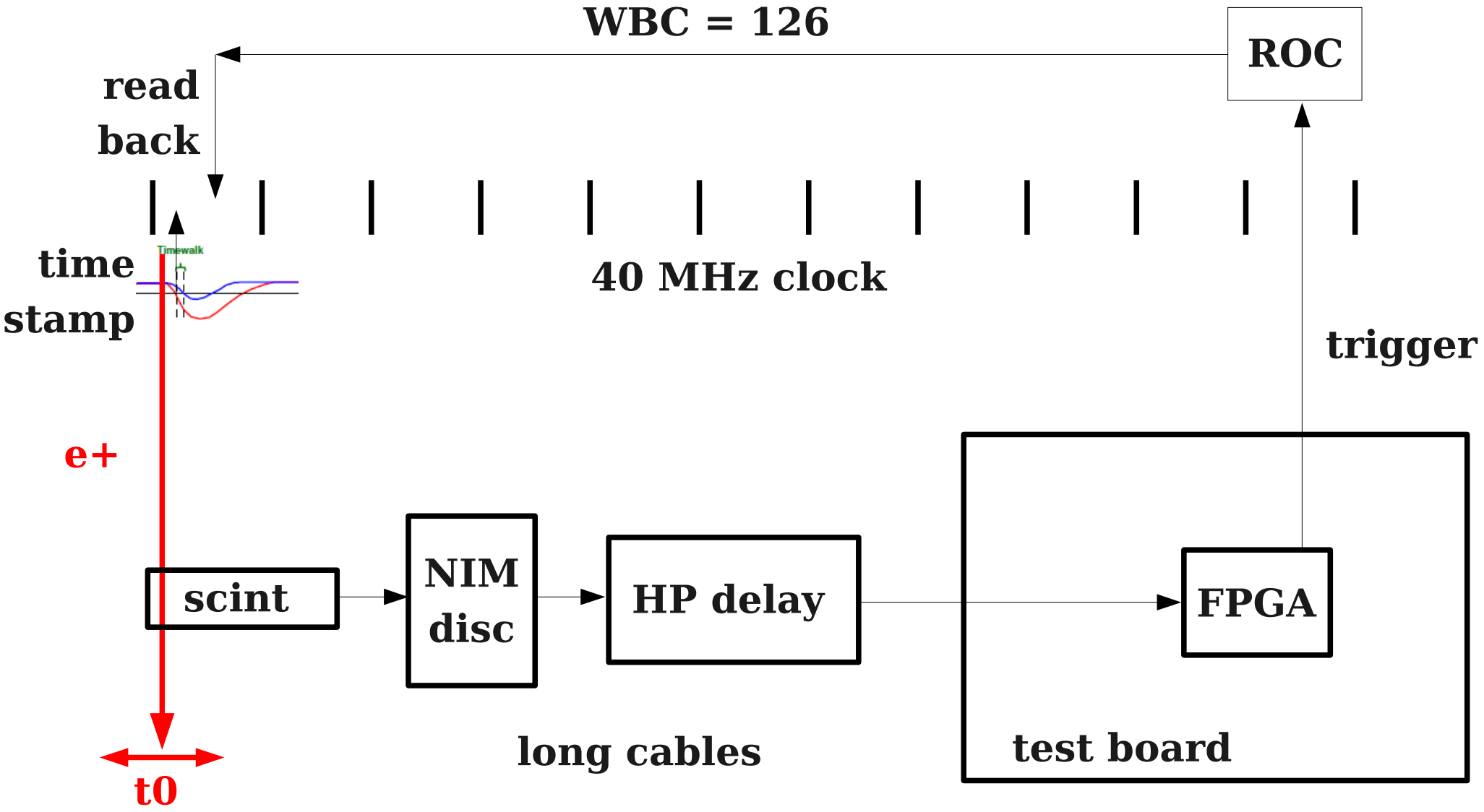
- Trigger and DAQ for 2 test boards and telescope established
- Software to be written:
  - link telescope track to hit in timing plane.
  - need General Broken Line fit, taking material into account,
  - with interface to MillePede II for common alignment.
- efficiency = DUT / (Telescope track && timing hit)
  - as function of position, angle, bias voltage, threshold, timing, ...

Efficiency vs timing delay



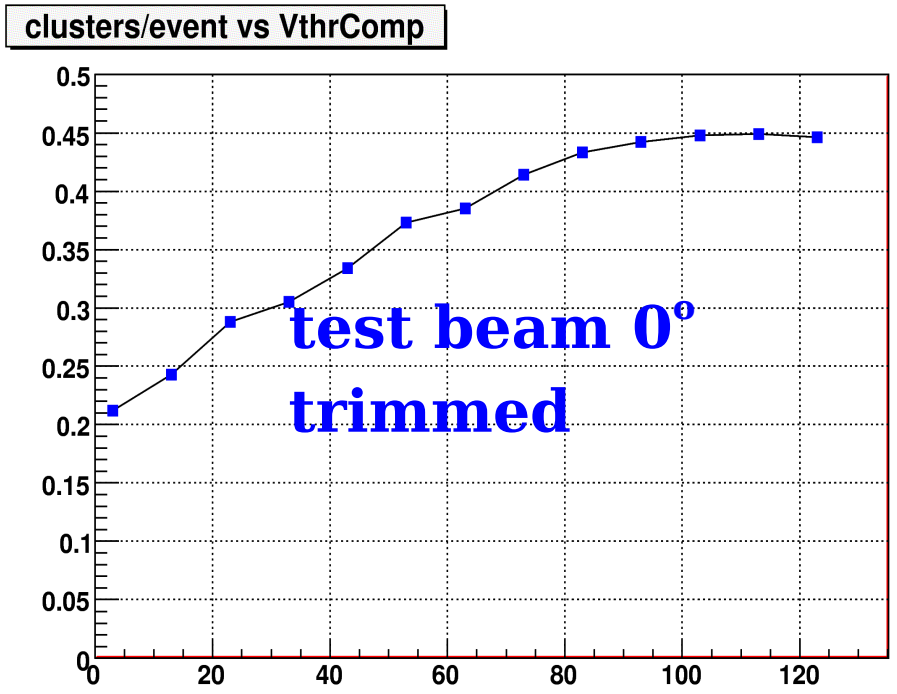
- old Runs 158 – 179
- efficiency plateau:
  - only ~3 ns wide
  - only 92 - 93%
- now much better: 99.7%
- scan clock delay (relative to beam)
  - 0..24 ns, step 4 ns, finer steps at edges of plateau

WBC timing needs scanning

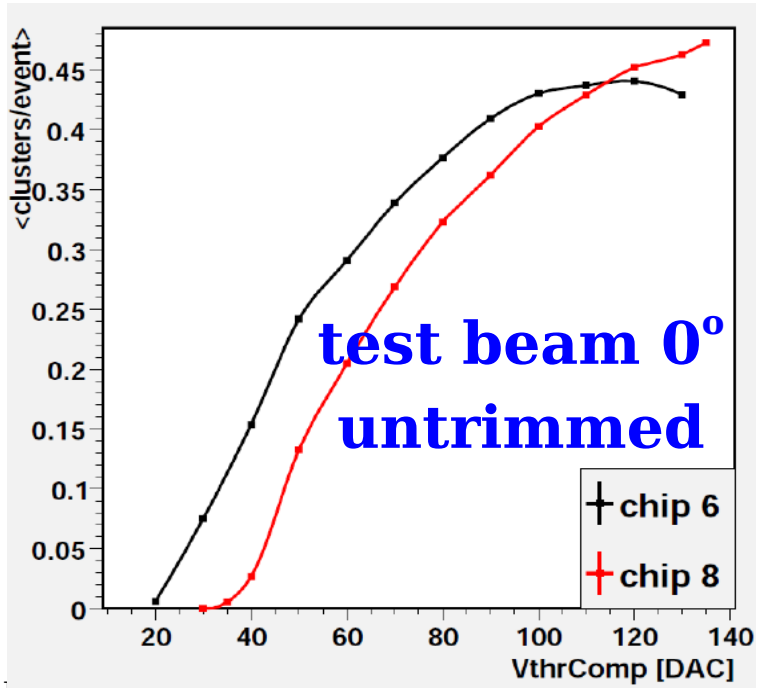


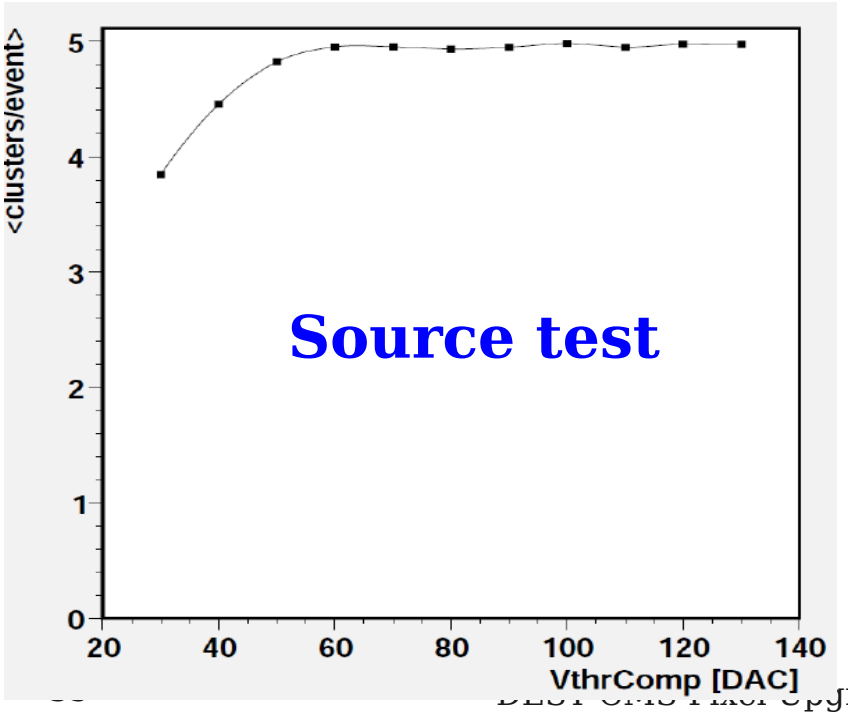
beam not synchronized to clock

Threshold Scan Results

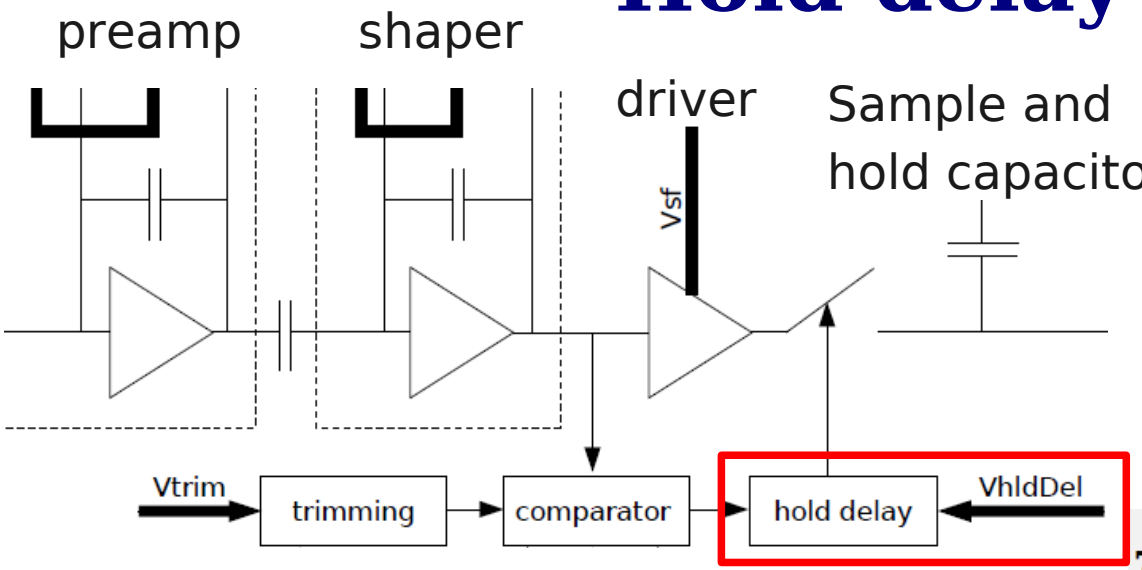


- Uniforming of pixel thresholds (trimming) makes an efficiency plateau visible
- More close to source test results now ?

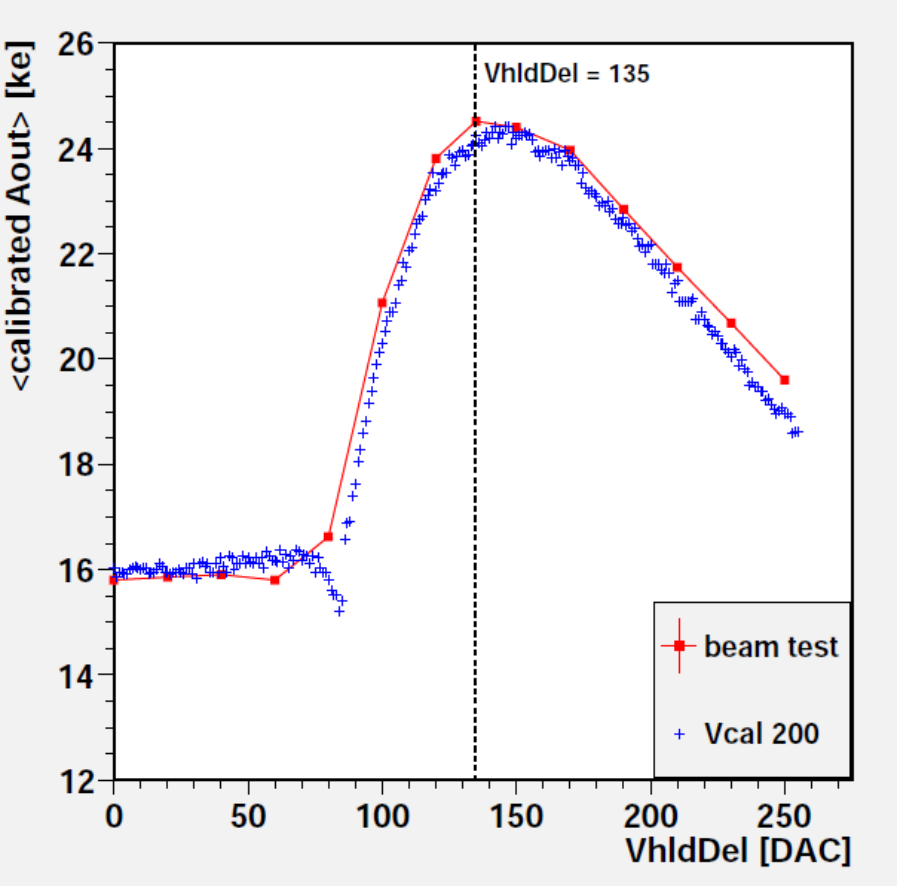




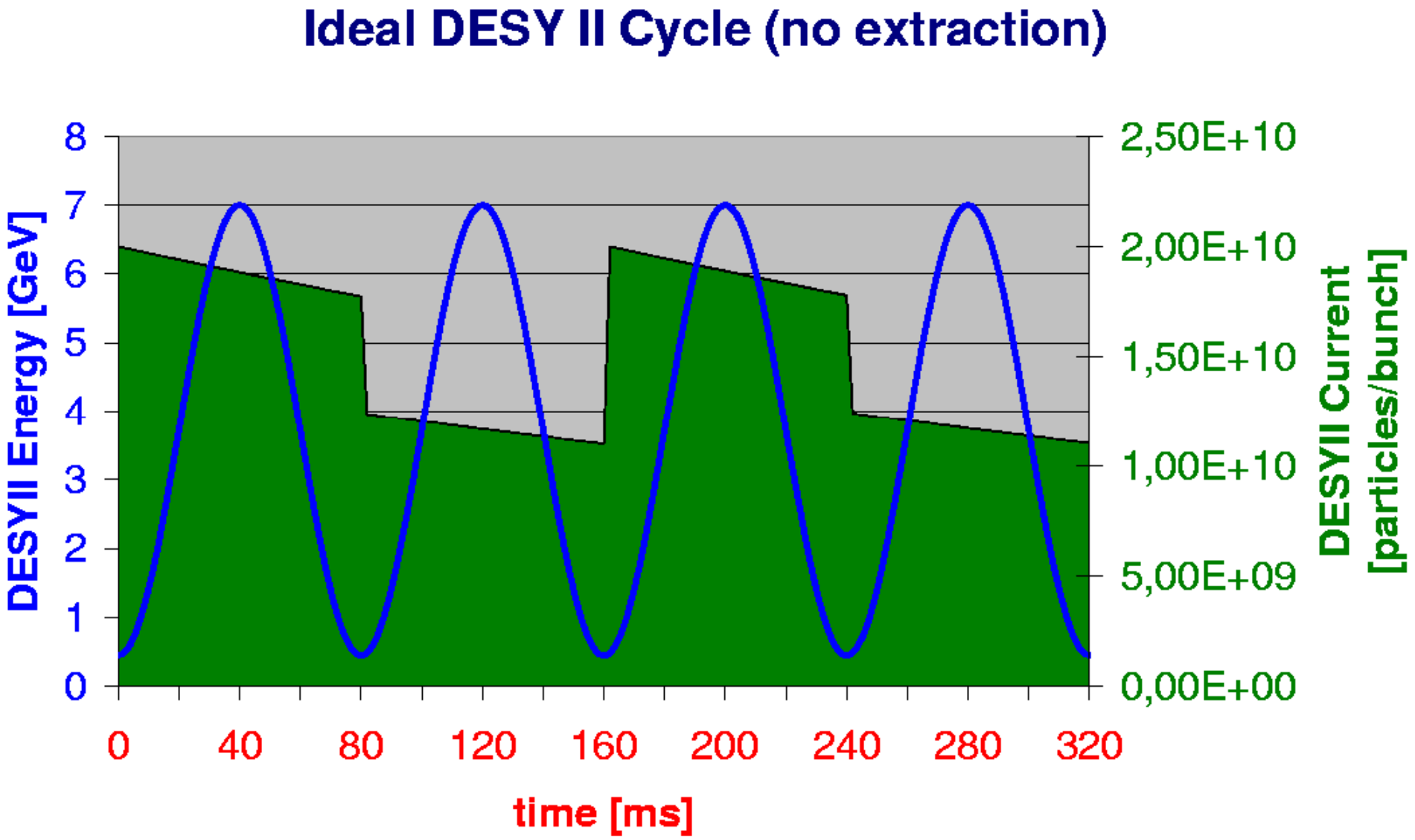
Hold delay scan

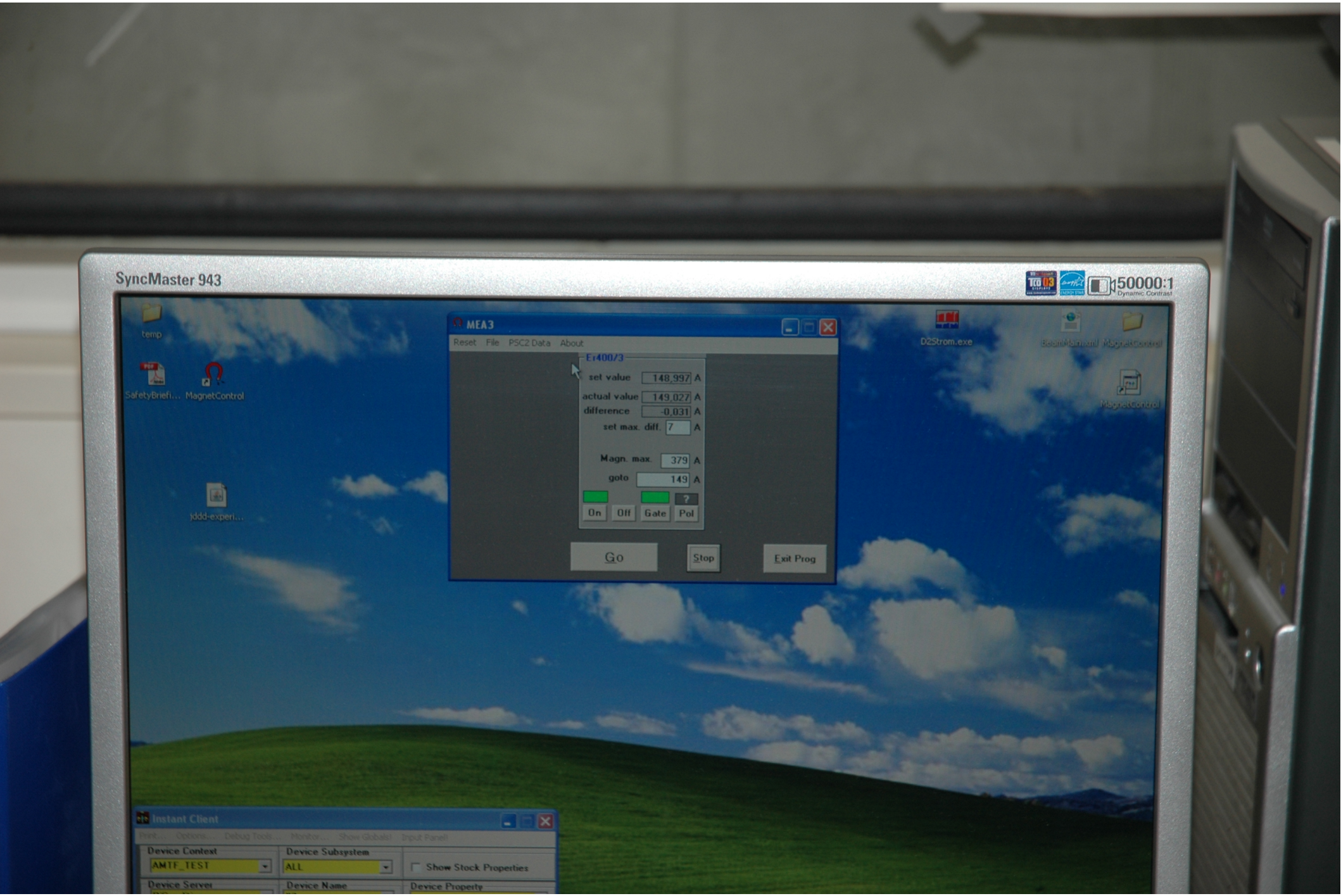


- VhldDel parameter was previously scanned with calibrate pulses generated by ROC
- Test beam results show very good conformity with Vcal scans
- VhldDel = 135 optimal for sampling maximal pulses



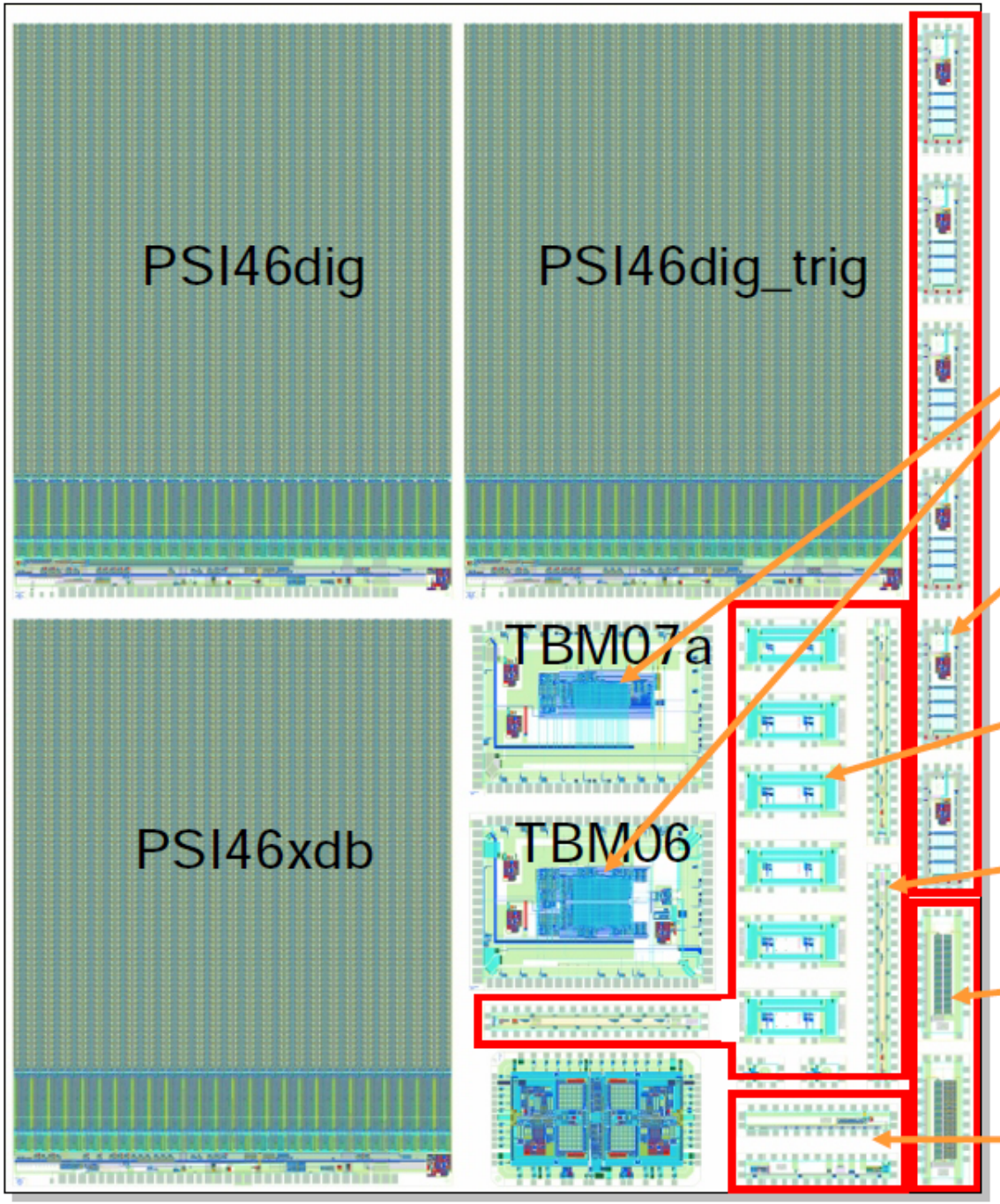
DESY II energy cycle




SyncMaster 943
50000:1
Dynamic Contrast
temp
SafetyBriefi...
MagnetControl
jddd-experi...
D2Strom.exe
MEA3
Reset File PSC2 Data About
Er400/3
set value 148,997 A
actual value 149,027 A
difference -0,031 A
set max. diff. 7 A
Magn. max. 379 A
goto 149 A
On Off Gate Pol
Go
Stop
Exit Prog
Instant Client
Device Context
AMTF_TEST
Device Subsystem
ALL
Show Stock Properties
Device Server
Device Name
Device Property


Gebiet bereit
1 DWL 2
Ein/Aus
Interlock 2 Hauptgebiet
DESY MEA
Erstfehler
Türen
Schlüsselkasten OK
Not-Aus OK
Gebiet OK
Σ BS ZU
LP
Schlüsselkasten
DESY MEA
Schlüssel vorhanden
1. System
2. System
verriegelt
verriegelt
Verriegelung
LP
Interlock 2 Teststrahl 21
DESY MEA
Erstfehler-speicher
HG
HG ok
HBS
HBS zu
LP
Experimente Interlock
DESY MEA
Beam Shutter
auf
läuft auf
läuft zu
zu
BEAM 21
STRAHL 21
Linac Freigabe
H-BS Netz
Interlock 2 gebrückt
DWL
Interlock 2 ok
Ansage
Baby Line
Interlock
Ein/Aus
LP

ROC submission 2012a



Size: 17.4 mm x 21.2 mm

60 recticles/wafer, 6 wafers

3 new ROC versions (PSI)

2 new TBM versions
Ed Bartz, Rudgers

LCDS cable drivers with bug fixed in read back (PSI)

Digital Level Translator DTL to replace the ALT chip (PSI)
Christoph Nägeli

LCDS/LVDS converter for test setups (PSI)

SEU resistent register test structures (PSI)

ADC, PLL and oscillator test structures (PSI)

Beat Meier (PSI): Pixel Upgrade plenary at CERN, 1.2.2012

ROC submission 2012a

- **PSI46xdb**: Enlarged data buffers, reduced crosstalk and better level distribution; - 3 DACs
- **PSI46dig_trig**: Digital readout added; - 4 DACs
- **PSI46dig**: Trigger mechanism removed; read back; - 7 DACs
- 2 **TBM** versions
- **DLT** Digital Level Translator for POH, replacing the ALT
- LCDS/LVDS level translator for test boards (LCDS not a standard)
- Other test structures (ADC, PLL)
- Tape out: January 2012 to IBM
- 6 wafers in May 2012 (not yet confirmed from IBM)

Beat Meier (PSI): Pixel Upgrade plenary at CERN, 1.2.2012

`https://indico.cern.ch/conferenceDisplay.py?confId=172930`

ROC submission 2012a

Data Rate, Efficiency:

- Extended data buffer 32 → 80 cells
- Extended time stamp buffer 16 → 24

Crosstalk, threshold uniformity:

- 6 metal layer (process option)
- Thick top metal (LM instead of MZ process option, +37%)
  → better power and ground distribution (lower resistance)
  → better threshold uniformity
- New routing for calibrate signal → less crosstalk of calibrate signal
- Better decoupling of comparator and digital voltage → less crosstalk
- Different other minor layout changes to reduce crosstalk

Beat Meier (PSI): Pixel Upgrade plenary at CERN, 1.2.2012

ROC submission 2012a

DAC:

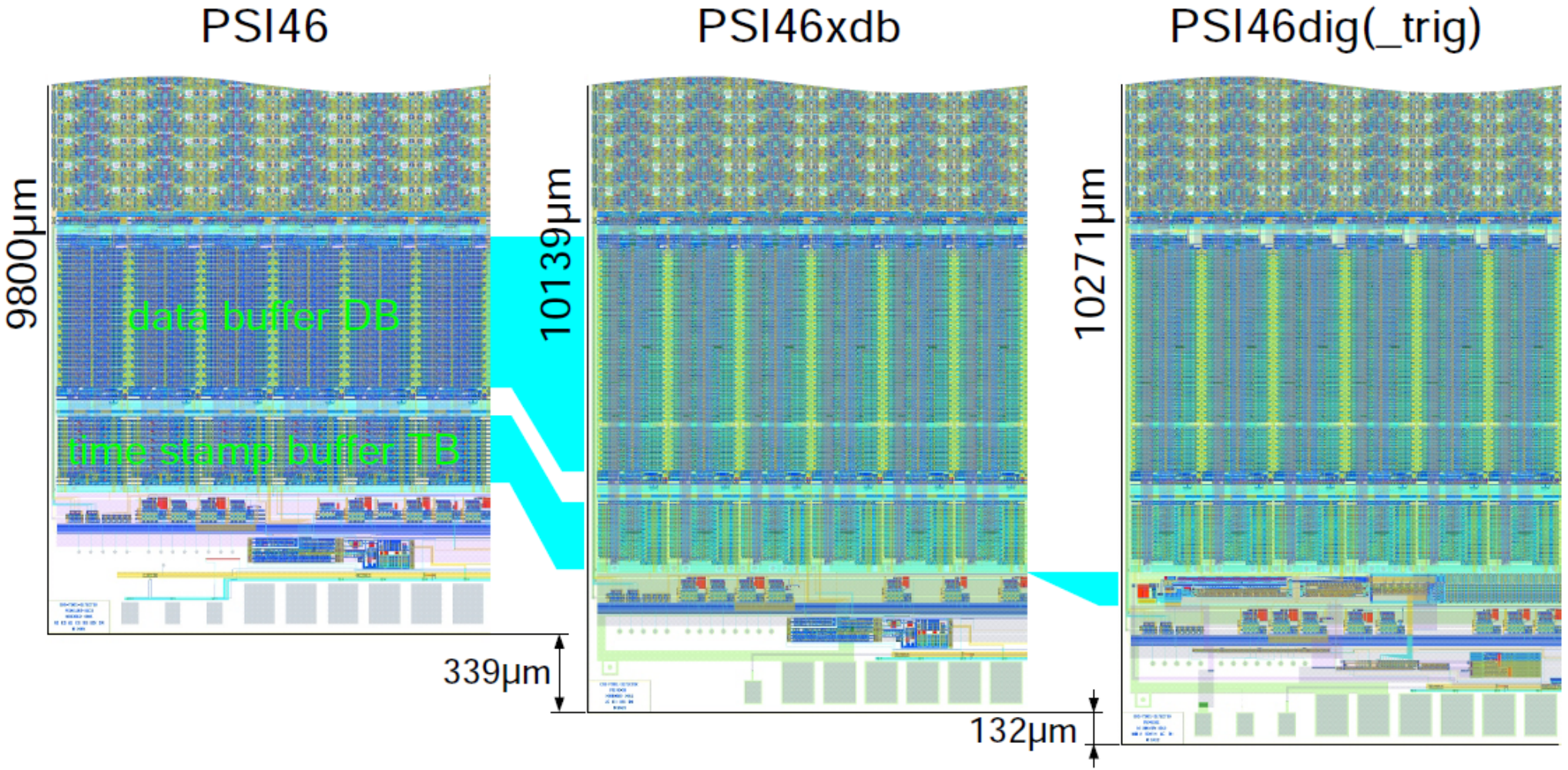
- 3 DACs removed: VRGPR, VRGSH and Vleakage
- All DAC's with power on reset for low power ROC configuration
- Current control instead of voltage control for S&H and analog power supply → easier and independent setup

Timing:

- Small performance optimization in column drain mechanism (timing)
- Modified comparator with reduced timewalk

- Same analog read out as PSI46 → same test board
- Comparison possible between PSI46 and PSI46xdb

ROC submission 2012a



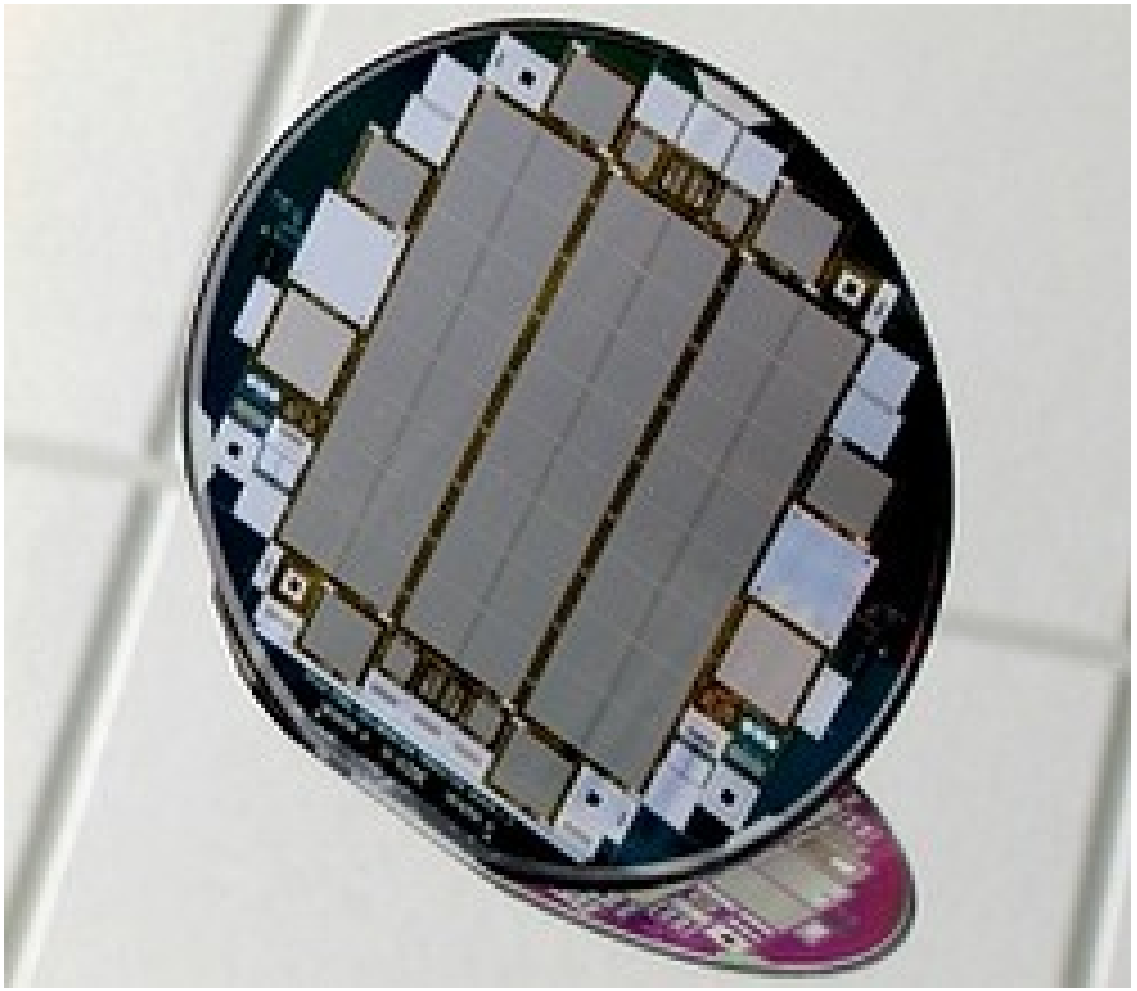
- DB 32
- TB 16

- DB 80
- TB 25

- DB 80
- TB 32

RB 64
8-bit ADC

CMS Pixel Sensors



design: Tilman Rohe, PSI

- 60 wafers under production at CIS (Erfurt)
  - standard CMS pixel sensor design (double sided, n-in-n, p-spray insulation).
  - for Karlsruhe, INFN, CERN/Taiwan, MRI, Purdue, DESY.
  - 5 wafers with increased bump pad passivation opening: 30 µm, for DESY.
  - Delivery in Mar 2012.
- Full sensors for first bump bondings.
- Single chip sensors for tests with new ROCs.