Architecture for the LLRF system based on the ATCA standard

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on behalf of LLRF Team

Outline

- Requirements (functional and technical) & goals
- Concept
- Modules – basic elements of the system
- Analog signals in ATCA:
    - Zone3,
    - Backplane,
    - AMC bay
- System architecture
- Tests
- Conclusion
- Discussion

Requirements (technical)

One RF Station

- 96 analog inputs 1.3 GHz, 0dBm
  - Isolation better then 50 dB
  - ADC 14 bits resolution, SF 40-100 MHz
  - Clock stability > 5 ps rms
- RF drive output 1.3 GHz, 0dBm
- Interface to the interlock system
- System latency < 500 ns
- Low latency links to other modules
- 6 different clocks must available (stability > 5ps rms)
- Partial redundancy

Requirements (functional)

- Scalable / Flexible (add new,not know during design,functionality)
- Available in the next 20 years (multi-vendor)
- Support modern control algorithms
- Limited number of different boards
- Modularity (partially upgradeable)
- Low-cost version available (monitoring)
- Provide SASE operation

- Reliability, operability and maintainability based on an average lifetime of 20 years with an average uptime in excess of 99%
- Easy (Possible) Maintenance NO front panel connections

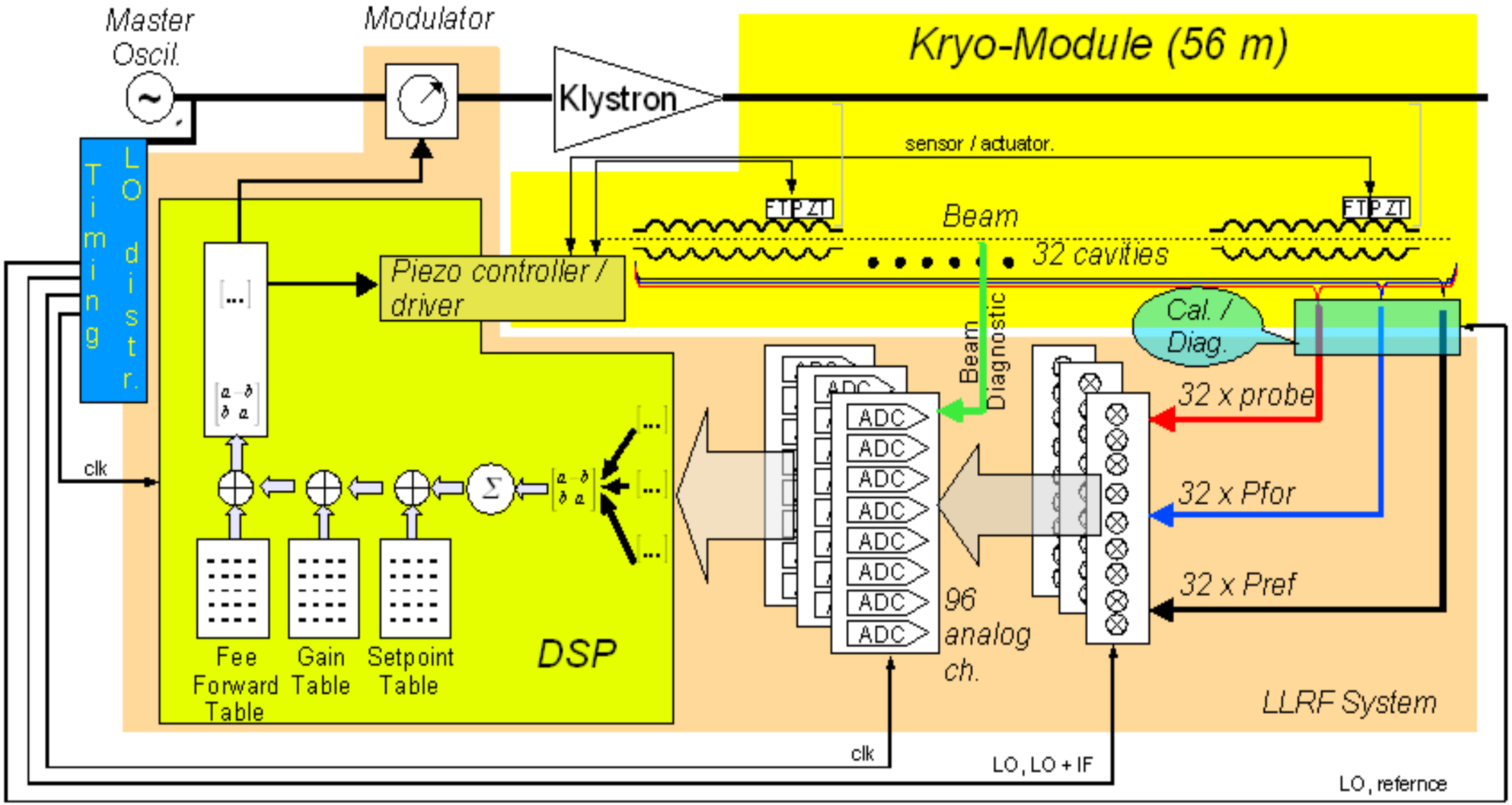
Goal of the project

Evaluate LLRF System based on ATCA

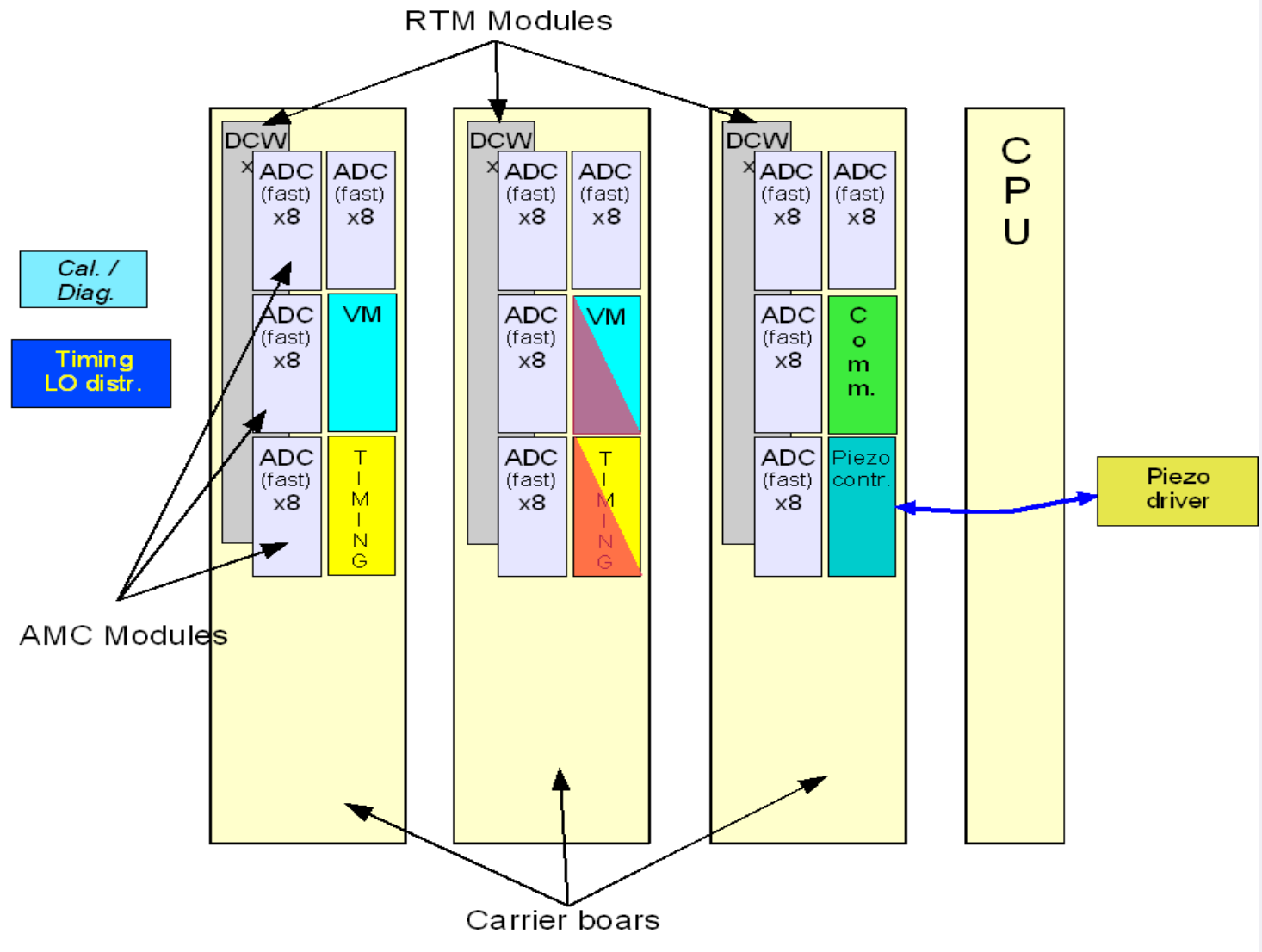
- advantages
- infrastructure (mainly usage of communication)
- documentation
- technology

Demonstrate beam stability in ACC1

Concept – main elements of LLRF system



Concept – modular system based on ATCA



Problems:

- analog signals in ATCA are not defined
- no analog IOs connected from rear

ATCA Boards

CPU – Adlink ATCA-6890

- Hot swap support, PICMG 3.1 Ethernet/Fibre Channel over PICMG 3.0
- Dual Intel Xeon
- Backplane interface: base interface with 2 GbE ports and fabric interface with 4 GbE ports (Intel 82571EB OPHIR)
- IPMI/IPMB management (ATMEGA128L/ATMEGA8L)

ATCA Carrier Board (more details in “ATCA carrier board”)

- 6 x AMC.1 bays with analog signals
- Low Latency Links
- 3 x DSP Processor (user)
- Virtex 5 FPGA (user)
- Power Quick II Processor (Board Management)
- Power management compatible with IPMI 1.5
- Flexible configuration of communication on Zone 2 (switches)

Advanced Mezzanine Card

Features: *(more details in "AMC Mezzanine Cards")*

- AMC - ADC - 8 channels, 14 bits, SF 105 MHz
- AMC – ADC – 2 channels, 10 bits, SF 2 GHz
- AMC - Timing module
- AMC - Piezo controller
- AMC - Vector modulator
- AMC - Communication module
- AMC – Radiation monitoring module

RTM and Boxex

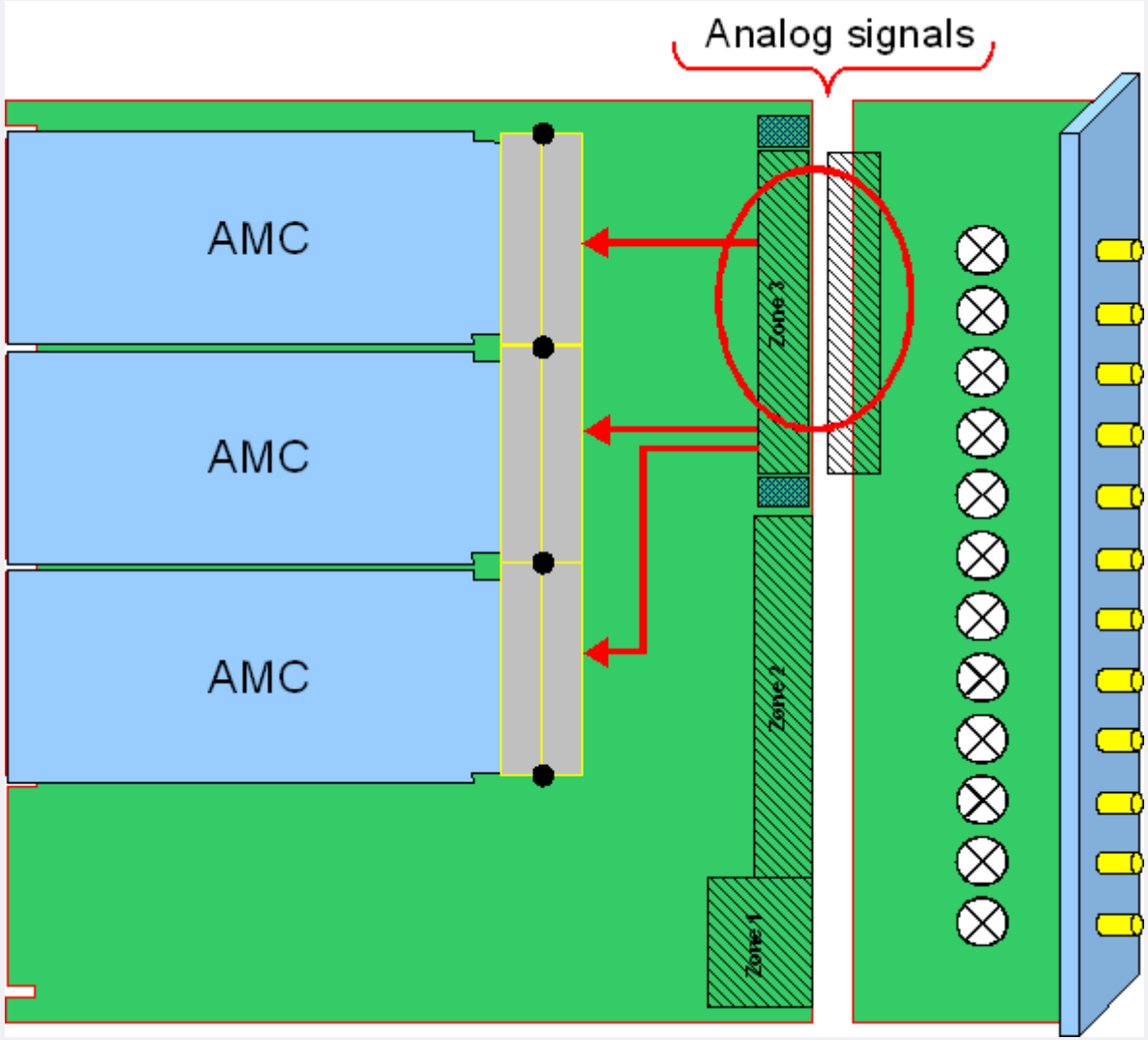
Rear Transition Module: *(more details in "Downconverter")*

- Rear connections to the ATCA Carrier Board
- Inputs
  - 32 channels inputs (from patch panel) - 32 channels down converter, 1.3 GHz input, IF 1-10 MHz
  - 8 digitals inputs (interlock system)
  - LO and timing inputs
- Power management

Boxes:

- Piezo driver and actuator
- Callibration module
- LO and Timing distribution

Analog signals in ATCA



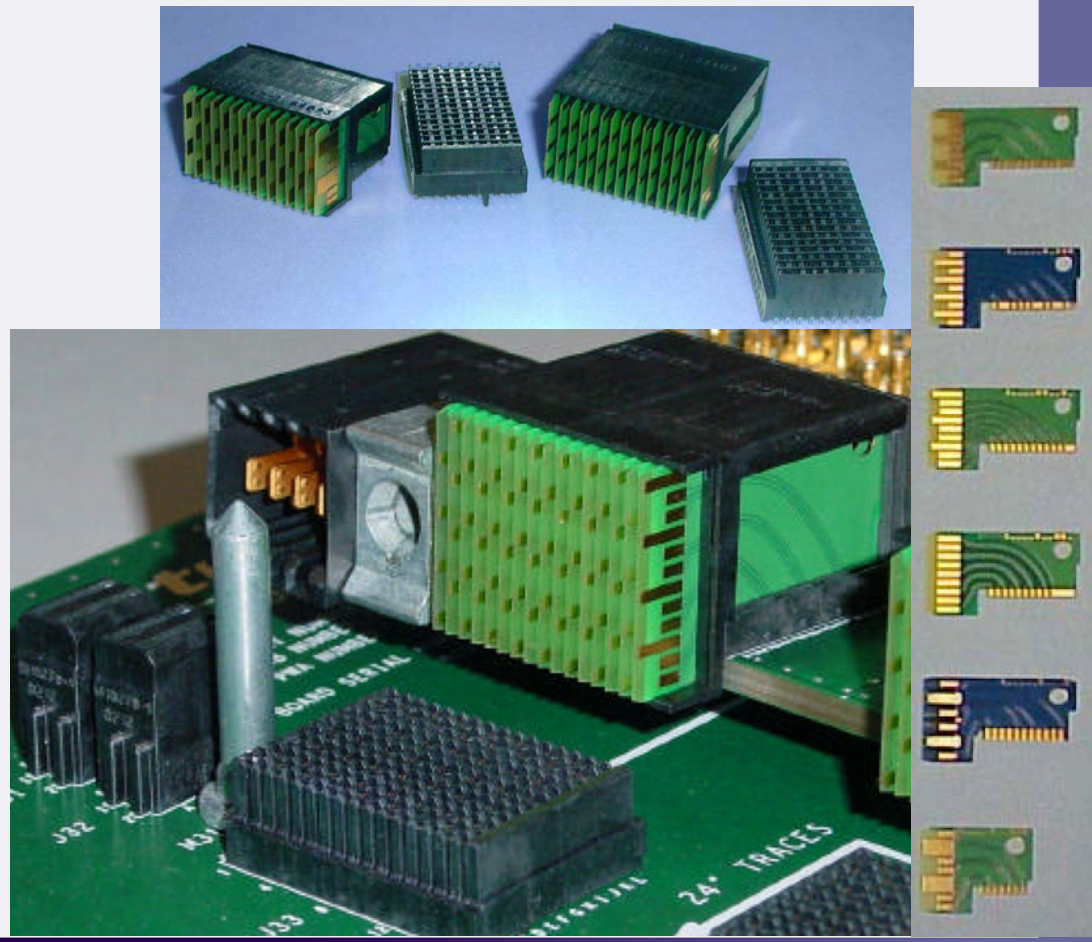
- Connections to the ATCA carrier board through RTM module
- Analog signals must be routed from Zone 3 to AMC modules

Signals on Zone 3

Signals on the beckplane:

- signals from cavities (down converted to IF 1-10 MHz)
- signals to VM
- LO and timing signals
- interlock signals
- power for RTM modules

Multigig RT-2 connector from tyco electronics
(113 signals / inch with 3.125 Gb/s)



Backplane (zone 3)

Functions:

- provide analog signals from RTM to carrier to and from the carrier board (IF, LO, reference clock)
- power supply
- distribute timing signals (bus, 3 x clock, 3 x trigger)
- distribute interlock signals (bus)
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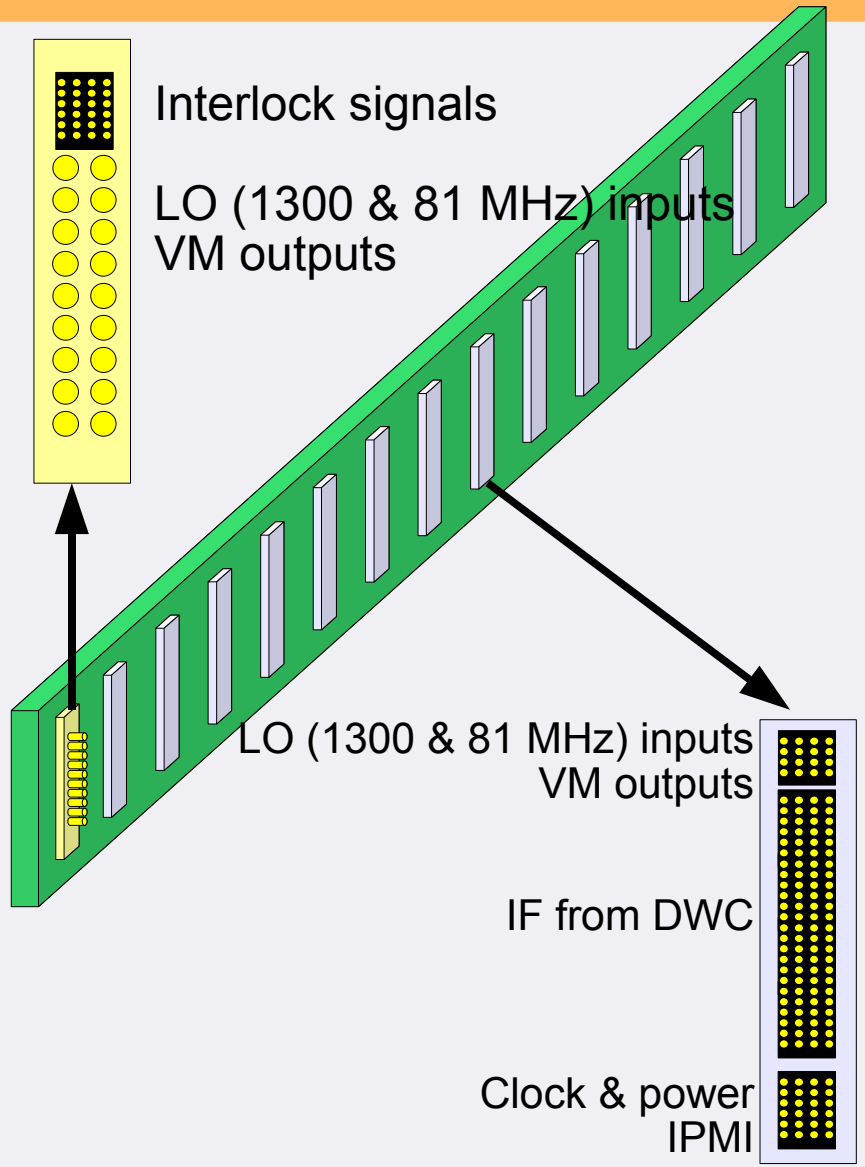
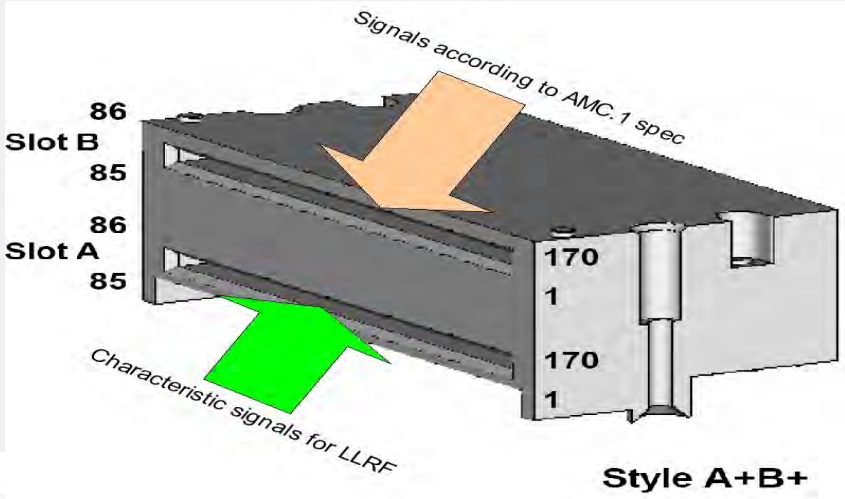
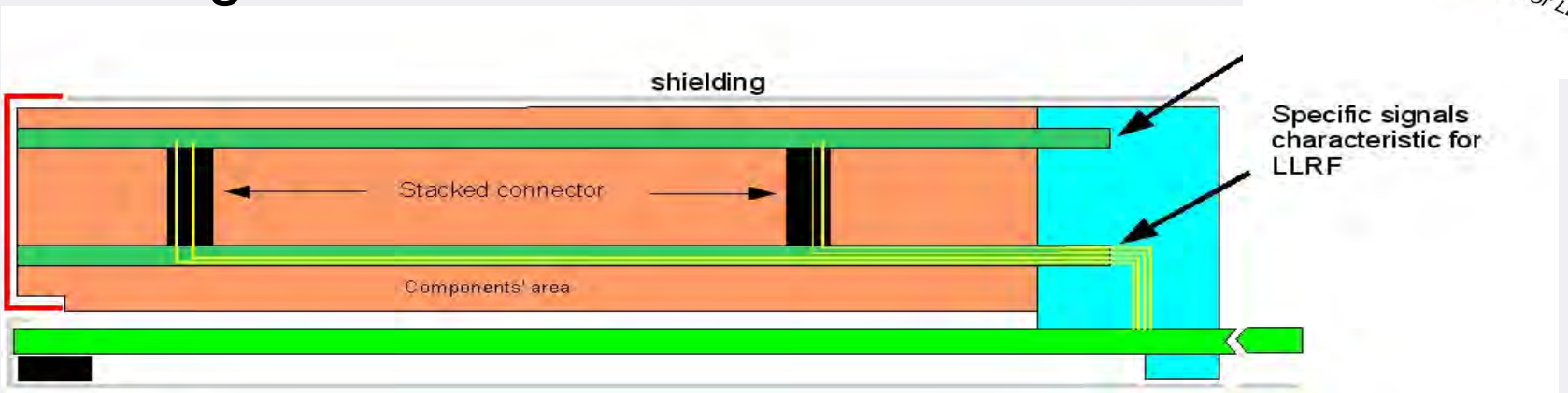
- Separated connectors for:
  - IF,
  - reference clocks & VM outputs,
  - Clock and trigger, power management & power supply

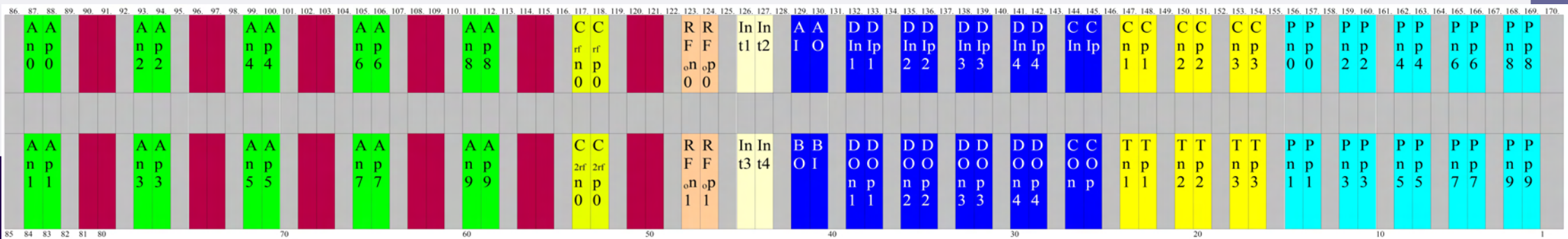


Signals in AMC bay

- AMC-DESY bay – compromise between AMC.1 specification and needs of the LLRF System
- Separation between analog and digital signals in the connector pin assignment



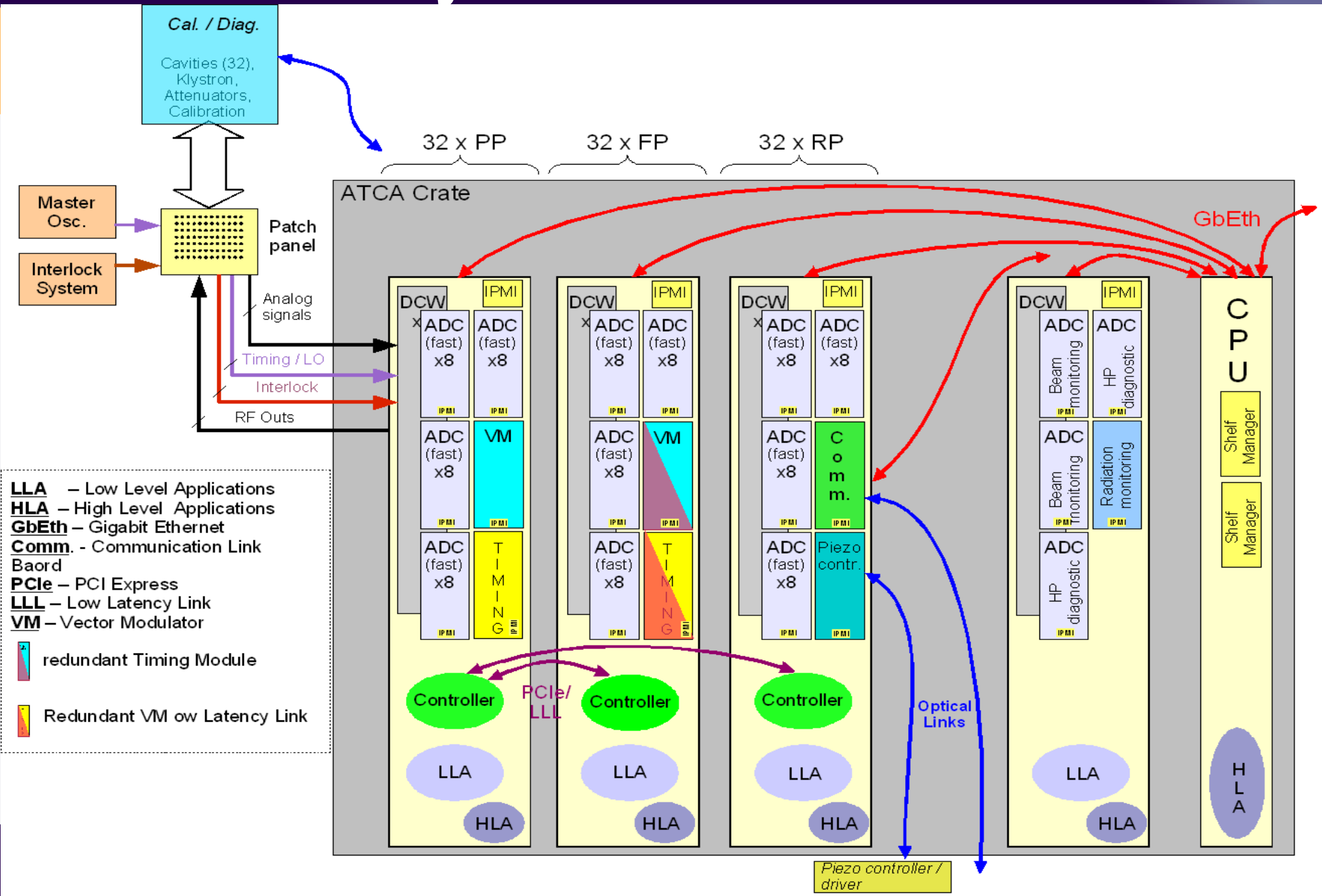




System Architecture

The European X-Ray Laser Project

XFEL
X-Ray Free-Electron Laser



Tests

Possible tests at FLASH

- ACC 1
  - no piezo,
  - only one module (8 cavities),
  - needed infrastructure exists
- ACC4 & ACC6 & ACC6 –
  - there are piezo in cavities
  - no cabling

Conclusions

Infrastructure offered by ATCA standard can be used efficiency used in LLRF system based on this standard
- communication over standard backplane (Zone 2)
- IPMI
- size of boards
- modular design

Custom design backplane ONLY in Zone 3
Compatibility with on market available AMC modules (CPUs, carrier boards, AMC modules)

Discussion

Thank you for attention