ATCA carrier board

Tomasz Jezynski
on behalf of LLRF Team

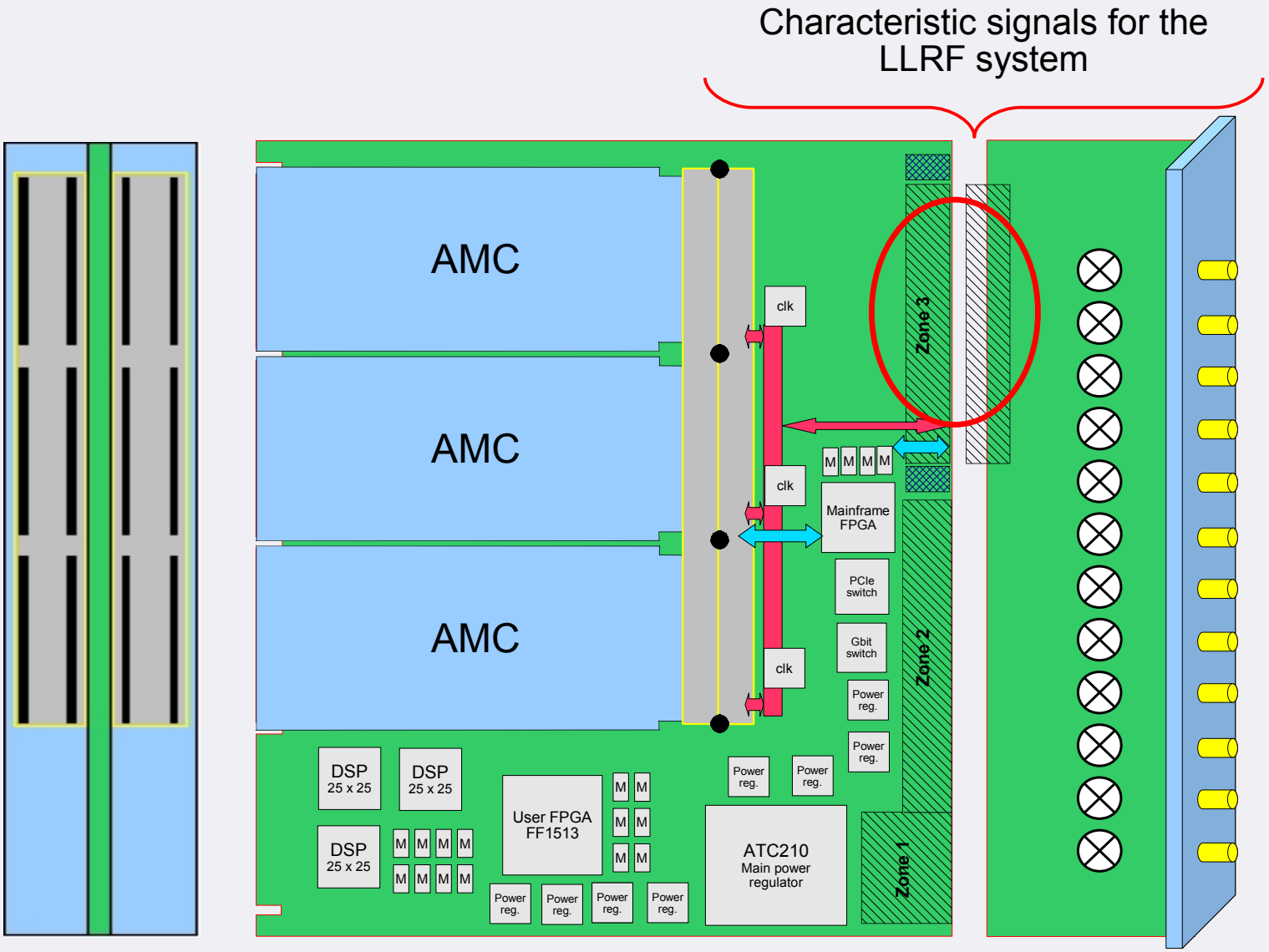
Outline

- Requirements
- Concept
- Block diagram
  - General overview
  - Communication interfaces – topology, connectors (details about protocols [“Communication links” (11:30 – 11:45)]
  - Power supply
  - Signals distribution
  - Timing distribution (clock and trigger distribution on the carrier board and on a backplane)
- Mechanics - front panel and mechanical construction
- Component placement - PCB layout

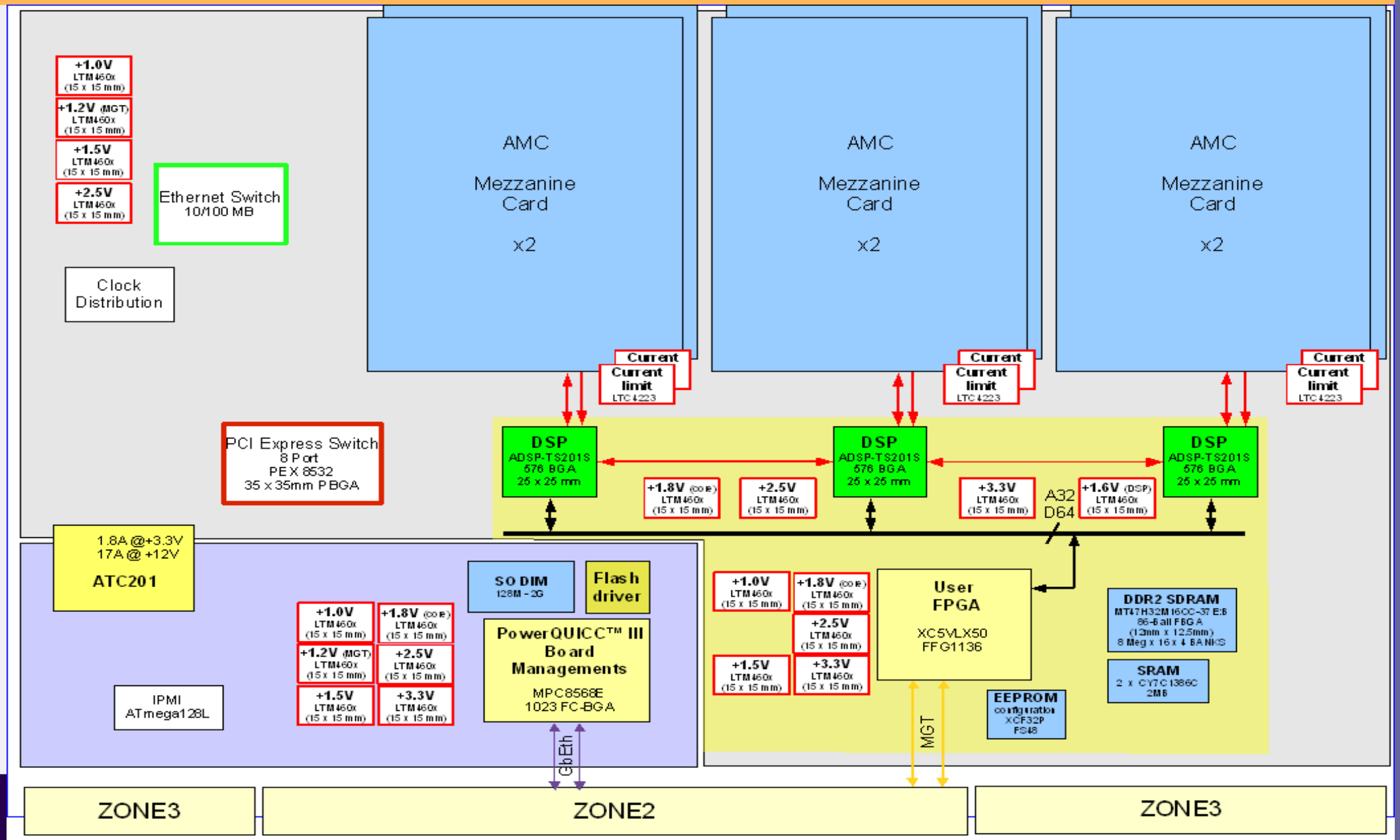
Requirements

- 6 x AMC bay compatible with AMC.1 and AMC-DESY specification
    - inputs:
        - sinusoidal signal IF (1-50 MHz) or RF 1.3 GHz, 0 dBm
        - sinusoidal signal RF 1.3 GHz, 0 dBm
        - sinusoidal signal RF 2.6 GHz, 0 dBm
        - 8 digital interlock signals
    - outputs
        - sinusoidal signal RF 1.3 GHz, 0 dBm
    - inputs/outputs:
        - 3 x clock B-LVDS (5 ps rms)
        - 3 x trigger B-LVDS (5 ps rms)
        - 10 differential lines for Low Latency Protocol (custom)
- Signals provided to AMC bays vi Zone 3 (RTM Module)
    - all signals mentioned above (for AMC bays)
- Clock signals distribution on board
- Floating Point Processor for Low Level Applications
- User FPGA for controller

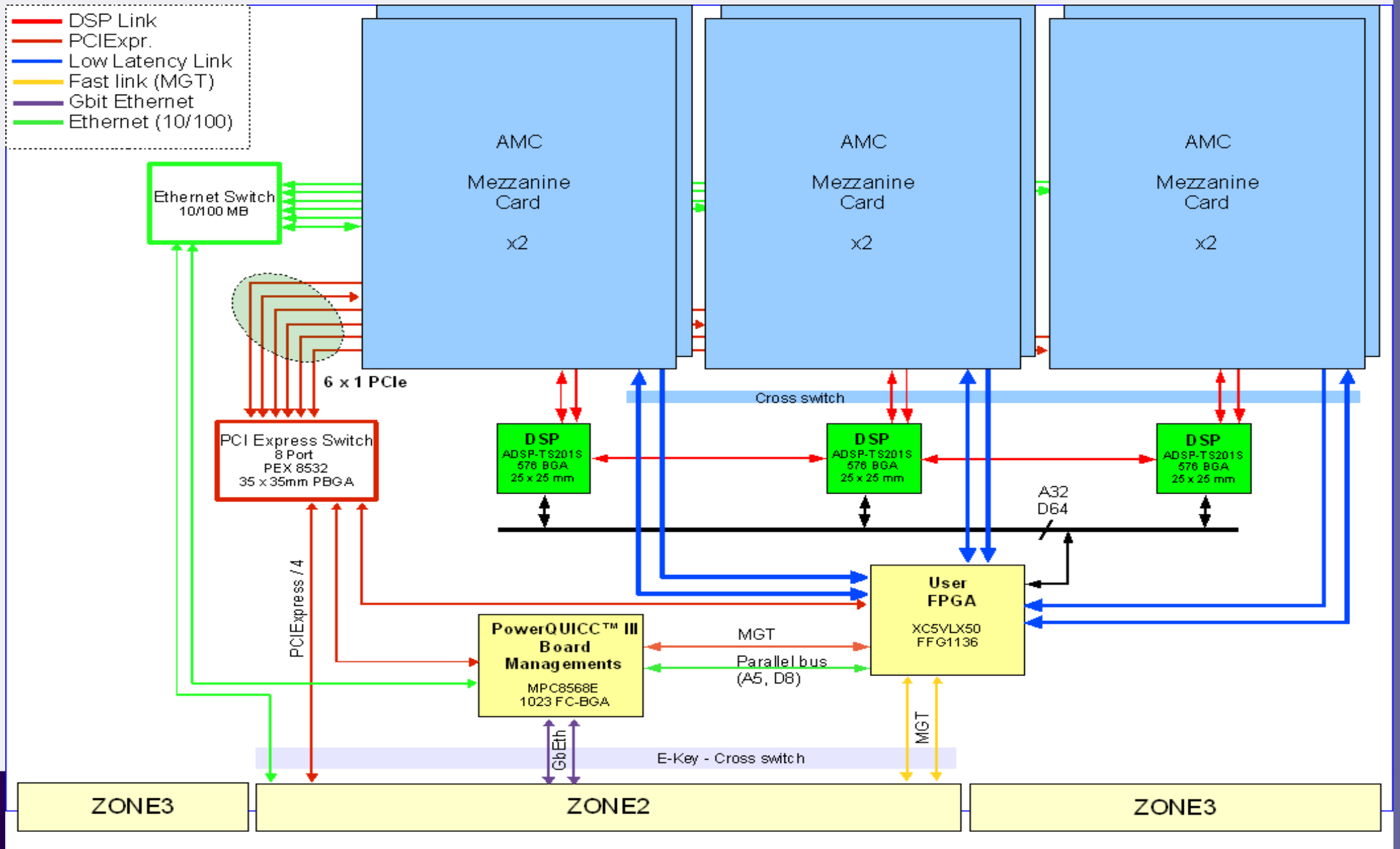
Carrier board - concept



Block diagram

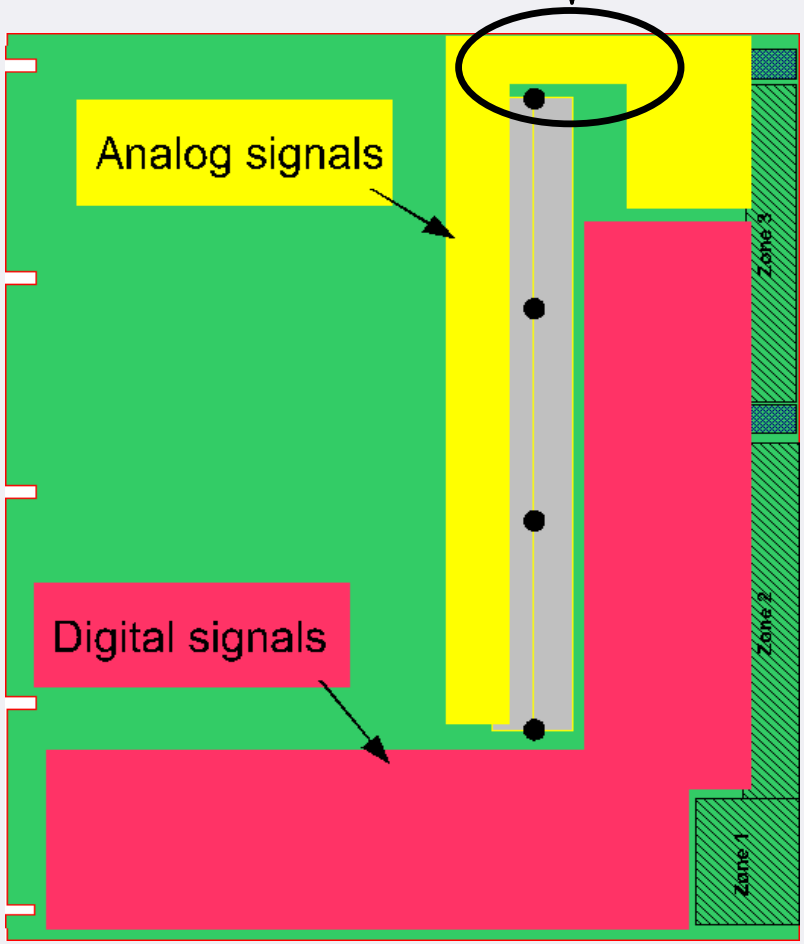


Block diagram - communication

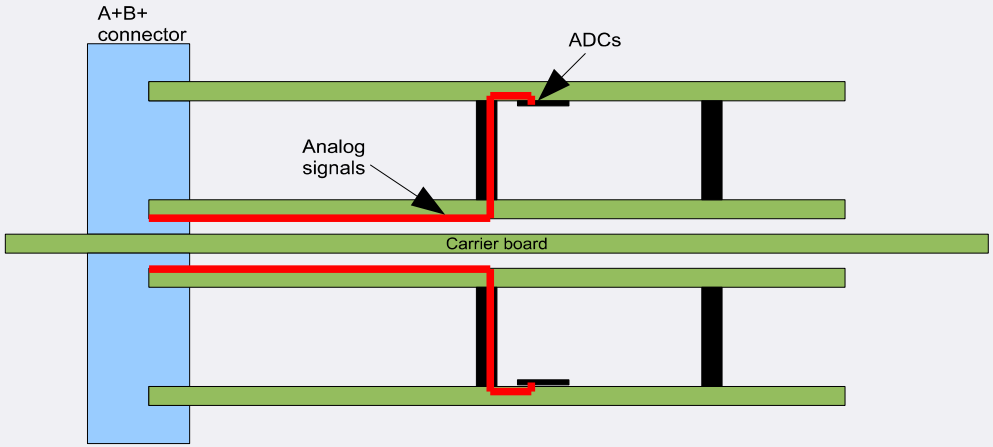


Analog signals

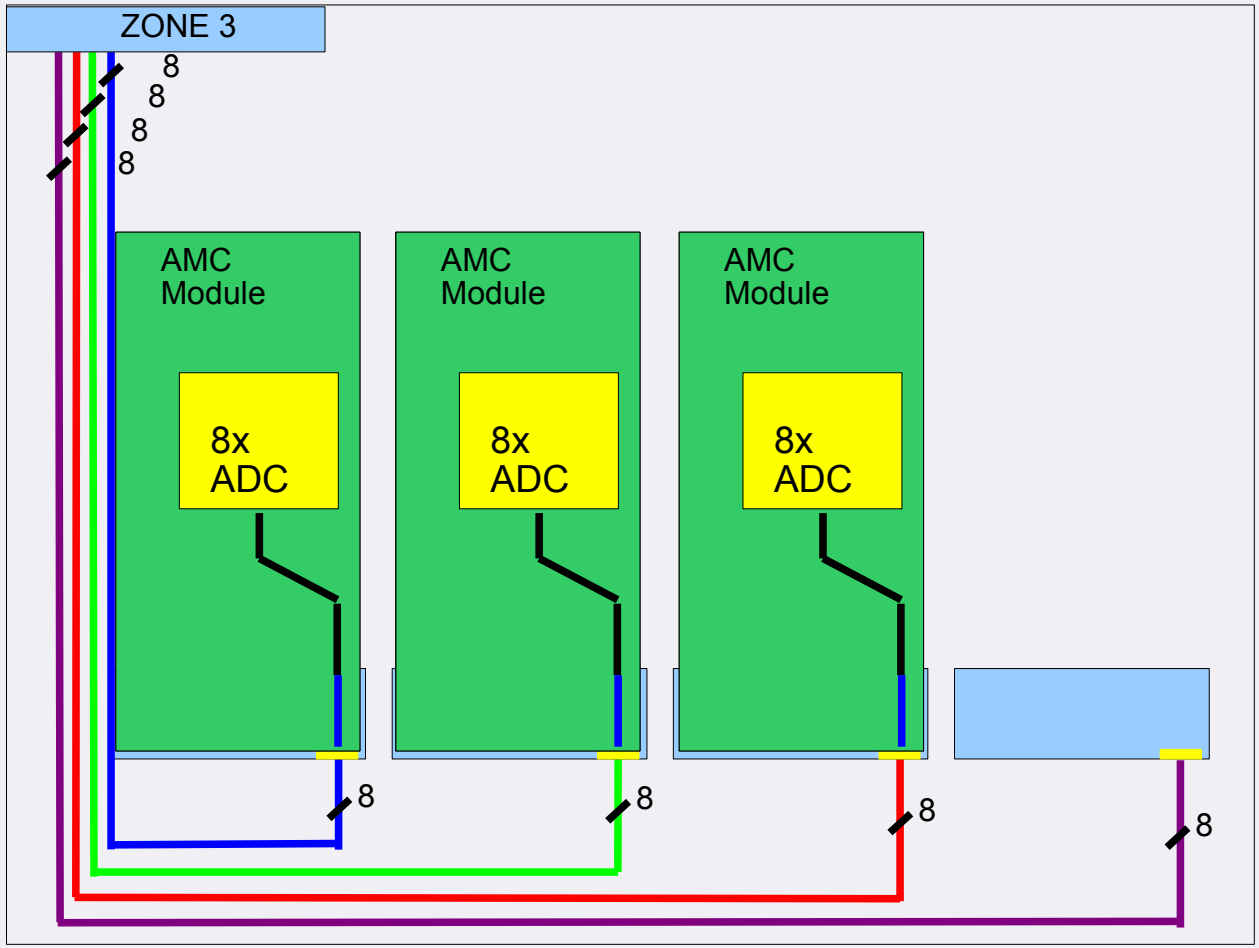
- 6 x 10 differential lines for IF (p-t-p)
- 6 RF output 1.3 GHz for VM
- reference clock – 1.3 GHz (multi drop)
- coded clock – 2.6 GHz (multi drop)



- Analog and digital lines are separated
- For analog signals and fast digital lines strip-lines are designed

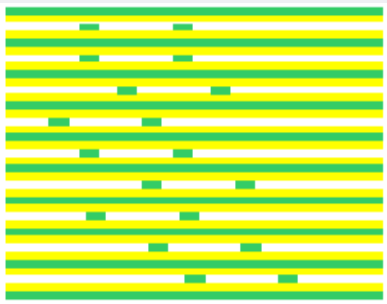


Analog signals



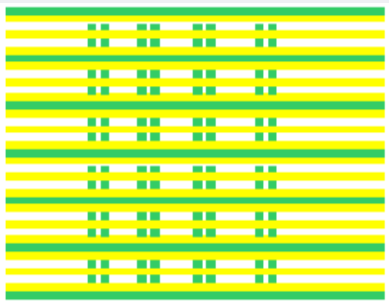
PCB stack

Analog



striplines

Digital

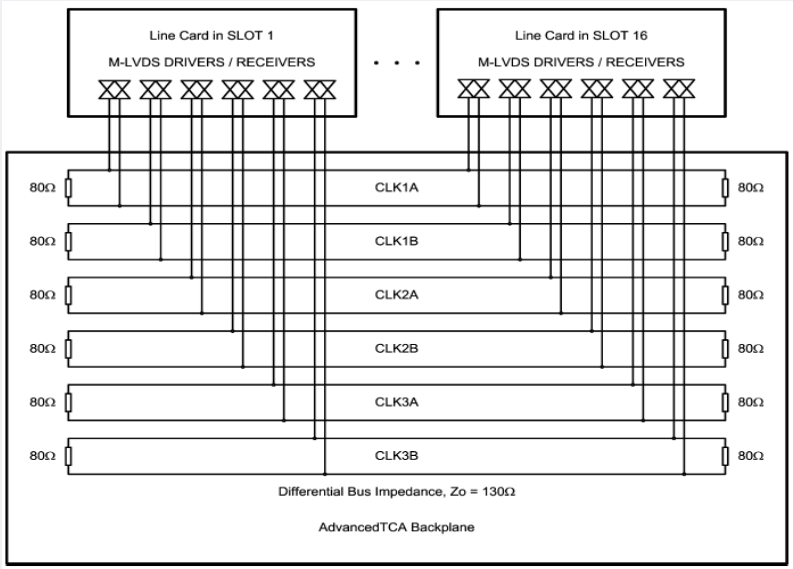


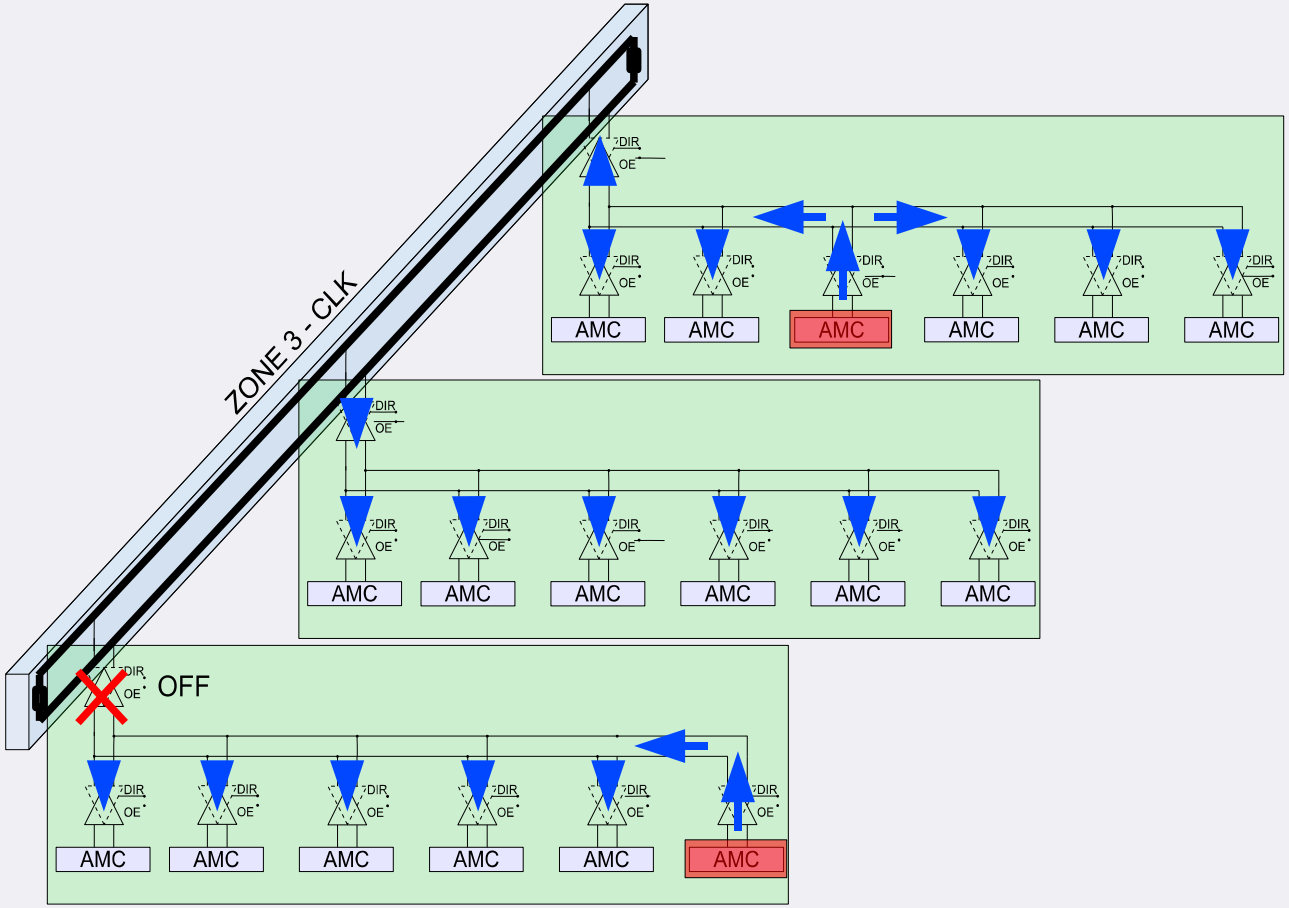
Broadside-coupled
differential striplines

Clock and trigger distribution

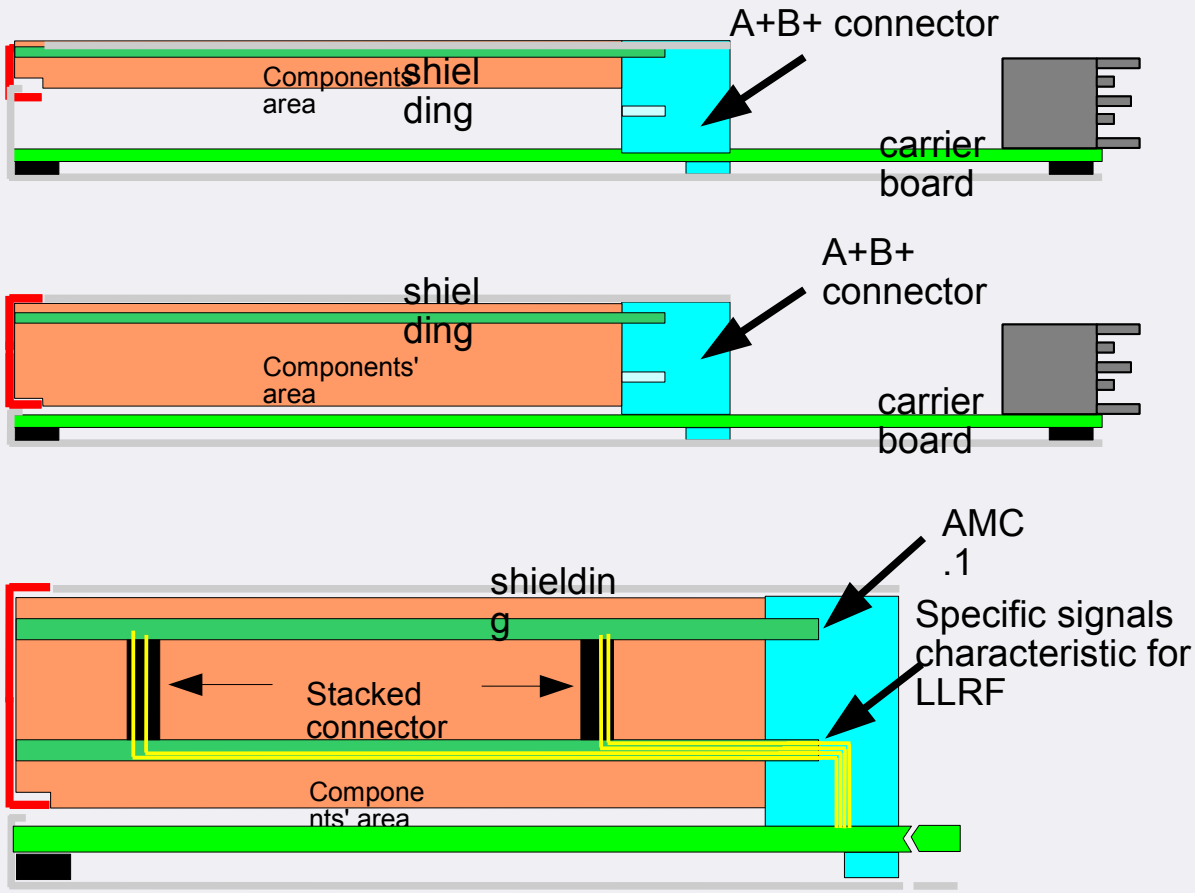
3 x clock & 3 x trigger signals generated at any AMC slot must be distributed to each AMC slot and others carrier boards

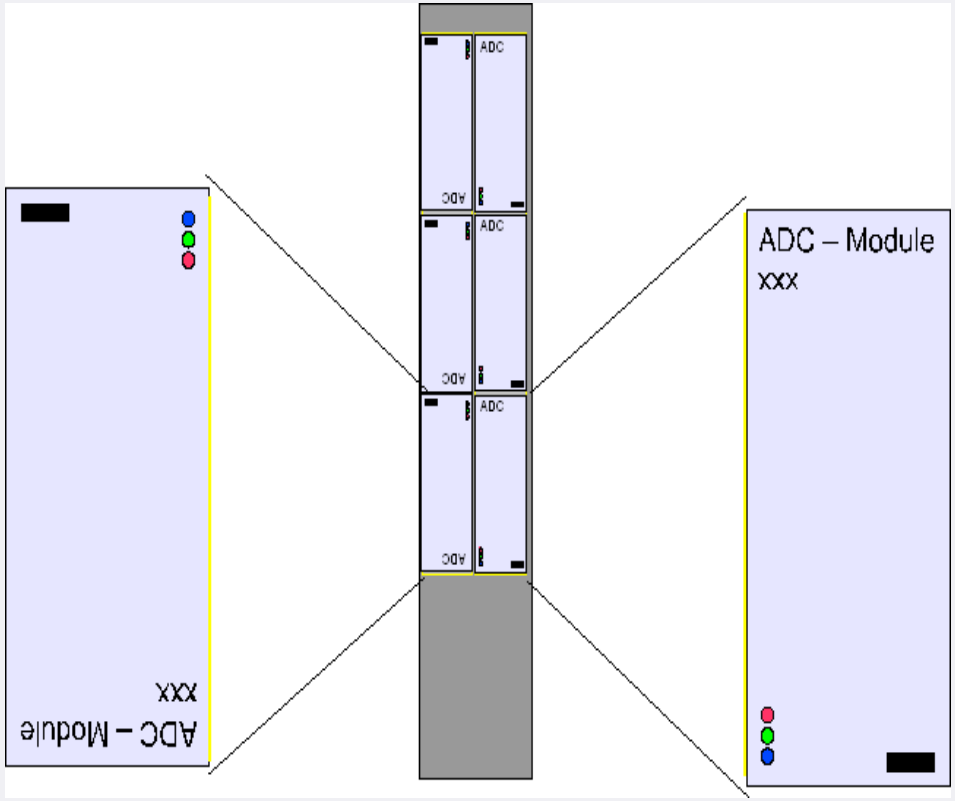
- LVDS bus
  - bidirectional buffers
    - OE
    - DIR





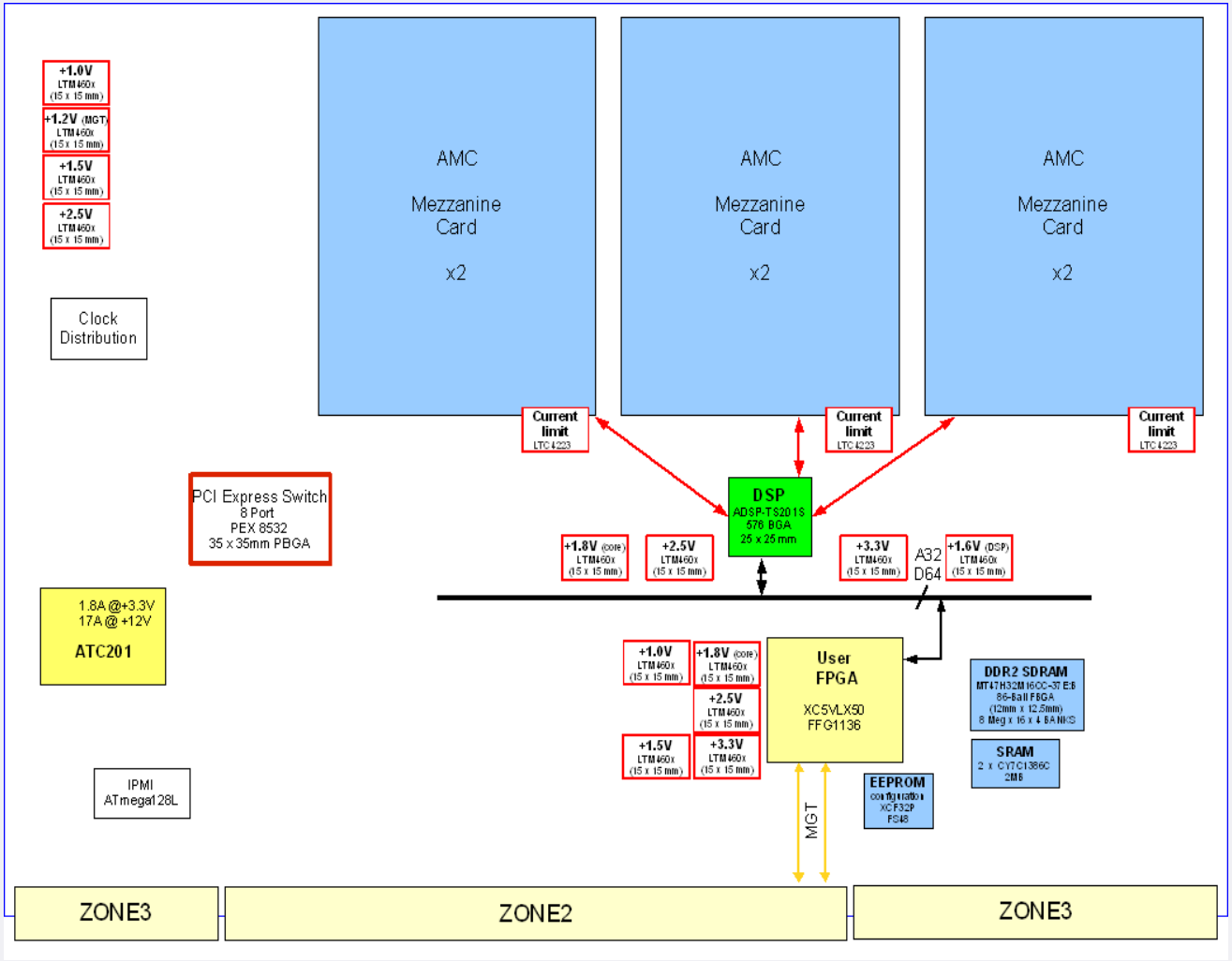
Mechanics


A+B+ connector
Components area
shiel
ding
carrier
board
A+B+
connector
shiel
ding
Components'
area
carrier
board
AMC
.1
shieldin
g
Specific signals
characteristic for
LLRF
Stacked
connector
Compone
nts' area


ADC – Module
xxx
ADC
ADC
ADC
ADC
ADC
ADC
ADC – Module
xxx

Status and plans

Test carrier board – reduced functionality of the final board



Purpose – evaluate:

- PCI Express
- analog signals distribution
- clock signals distribution

platform for software development:

- IPMI
- communication (PCIEx)

Status and plans

Test carrier board

schematics

Power regulators	– 80% 10.12
IPMI	- 100%
DSP	- 100%
User FPGA	- 80%, 10.12
Analog signals	- 0%, 10.12
Clock distribution	– 50% 10.12
Configuration	- 100%
PCIExpress	- 100%
E-Key	- 10% 17.12

PCB layout	15.01.2008
Assembled board	07.02.2008

Final board

schematics

Power regulators	- 01.02.2008
IPMI (new)	- 01.02.2008
DSP (3x)	- 01.02.2008
User FPGA	
Analog signals (x6)	- 01.02.2008
Clock distribution	
Configuration	
PCIExpress	
E-Key (extended)	- 01.02.2008
Local Processor Management	- 28.03.2008
Gbit Ethernet	- 28.03.2008

PCB layout	end of 03.2008
Assembled board	end of 04.2008

Discussion

Thank you for attention