

Advanced Mezzanine Card Modules and LLRF System

Agenda

1. AMC specification
2. Modular architecture of LLRF system
3. A typical LLRF AMC module
4. AMC modules for Low Level RF system

AMC specification

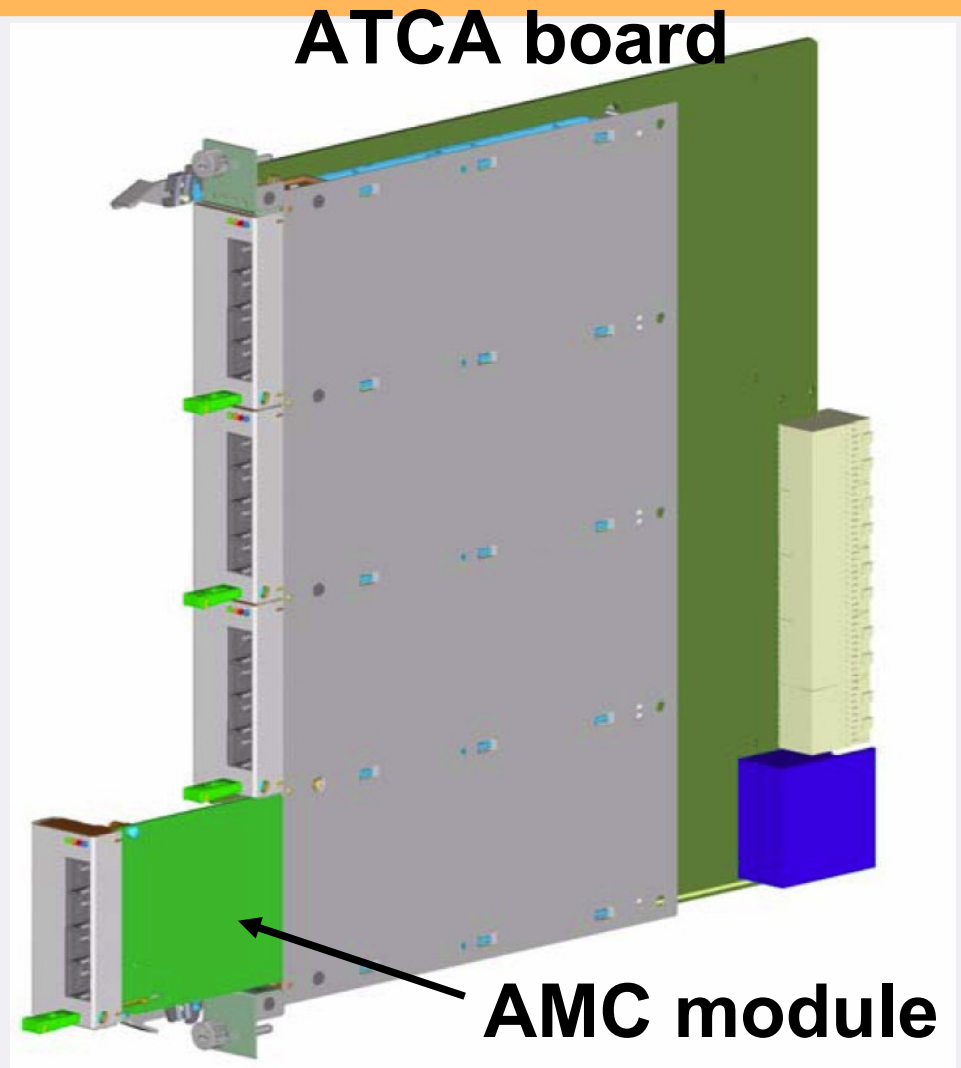
Advanced Mezzanine Cards are printed circuit boards (PCBs) that follow a specification of the PCI Industrial Computers Manufacturers Group (PICMG).

Features of AMC modules:

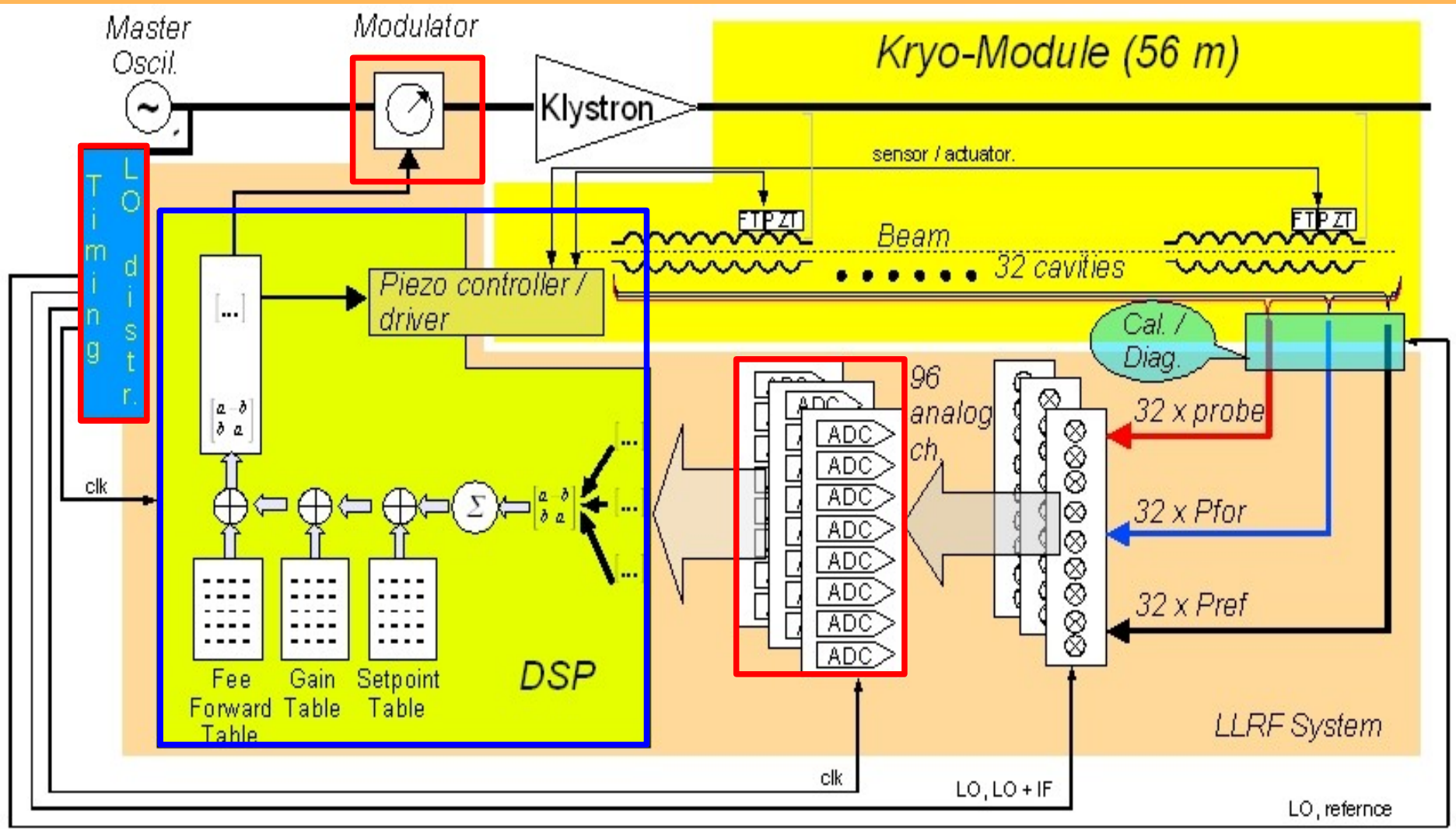
- ★ Edge connector (max. 340 pins),
- ★ Build-in IPMI controller,
- ★ Two power supplies +3V3/+12V,
- ★ Maximum power 60 W per module
- ★ Module dimensions:
180mm x 73mm x 28mm

Communication interfaces:

- ★ Fabric interface:
 - ◆ PCI Express (PCI Express Advanced Switching)
 - ◆ Gigabit Ethernet and XAUI
 - ◆ Serial RapidIO
- ★ System Management Interface
- ★ Synchronisation Clock interface
- ★ JTAG Test Interface
- ★ Power (+3V3, +12V)



Modular architecture of LLRF system (1)

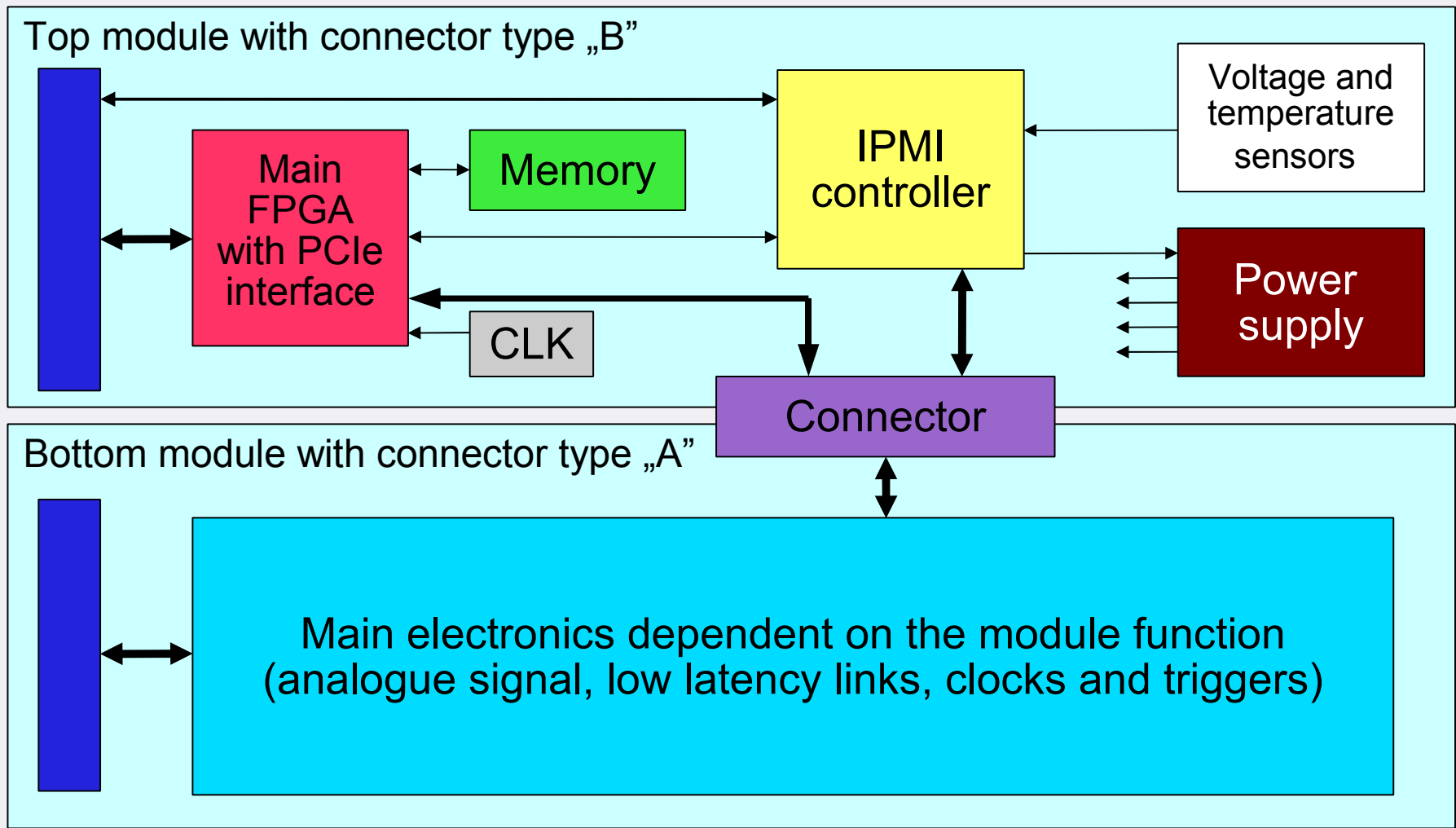


Modular architecture of LLRF system (2)

Main LLRF controller will be built on ATCA carrier board, while auxiliary submodules will be build on AMC modules:

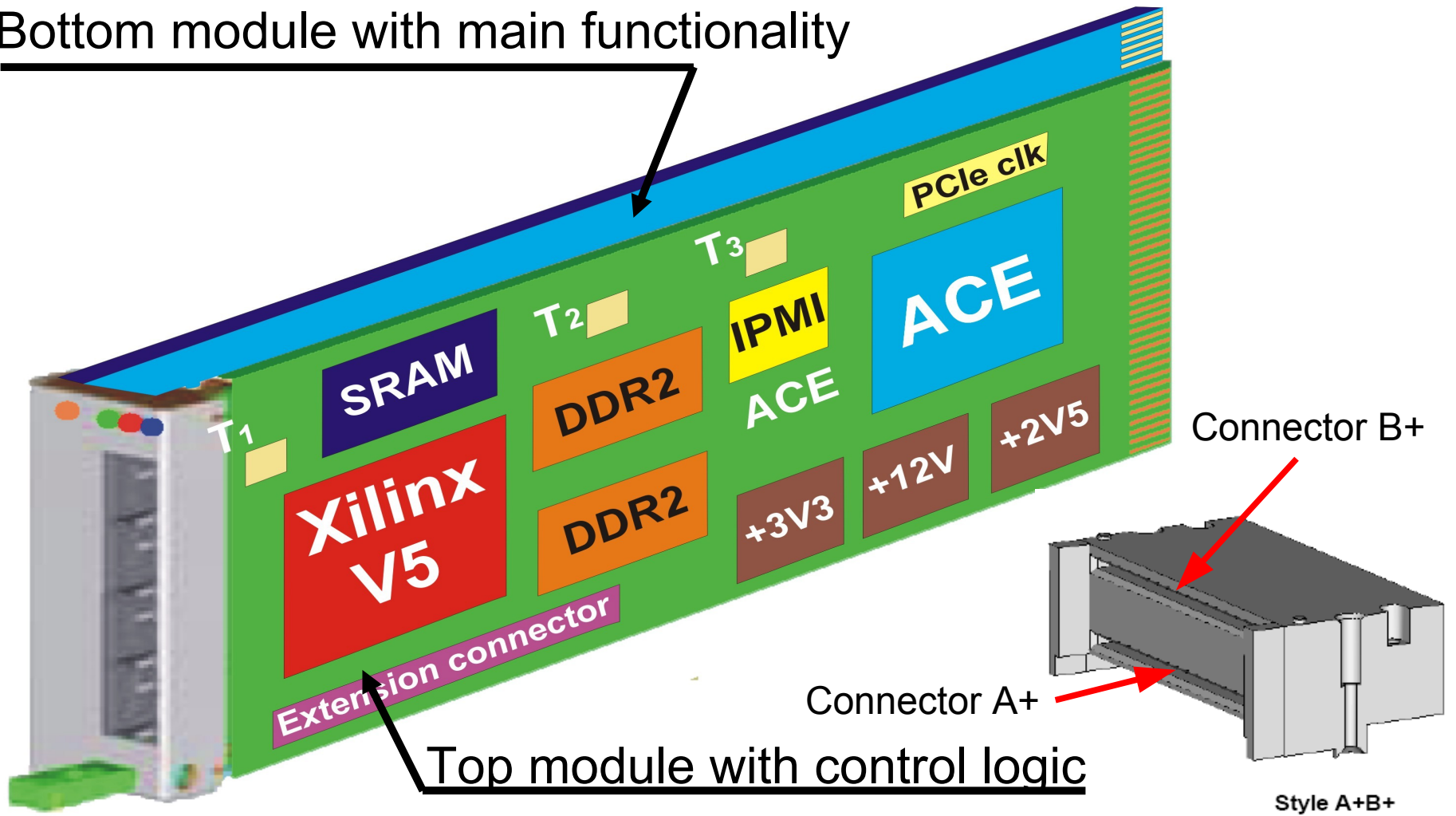
- ★ 8 x ADC (100 MHz) + FPGA (front panel and rear connection)
 - industrial module available,
 - our design in progress,
- ★ Vector modulator + 2 x DACs (800 MHz) + FPGA + memory,
- ★ Transient detector, 1 x ADC (2 GHz) + fast static memory,
- ★ Clock Synthesizer and Timing Module,
- ★ Piezo controller,
- ★ Radiation monitoring module (detection of neutron and gamma radiation).

Block diagram of the typical LLRF AMC module (1)



Block diagram of the typical LLRF AMC module (2)

Bottom module with main functionality



Top module with control logic

AMC modules for Low Level RF system

Octuple Analog-to-Digital module

Requirements:

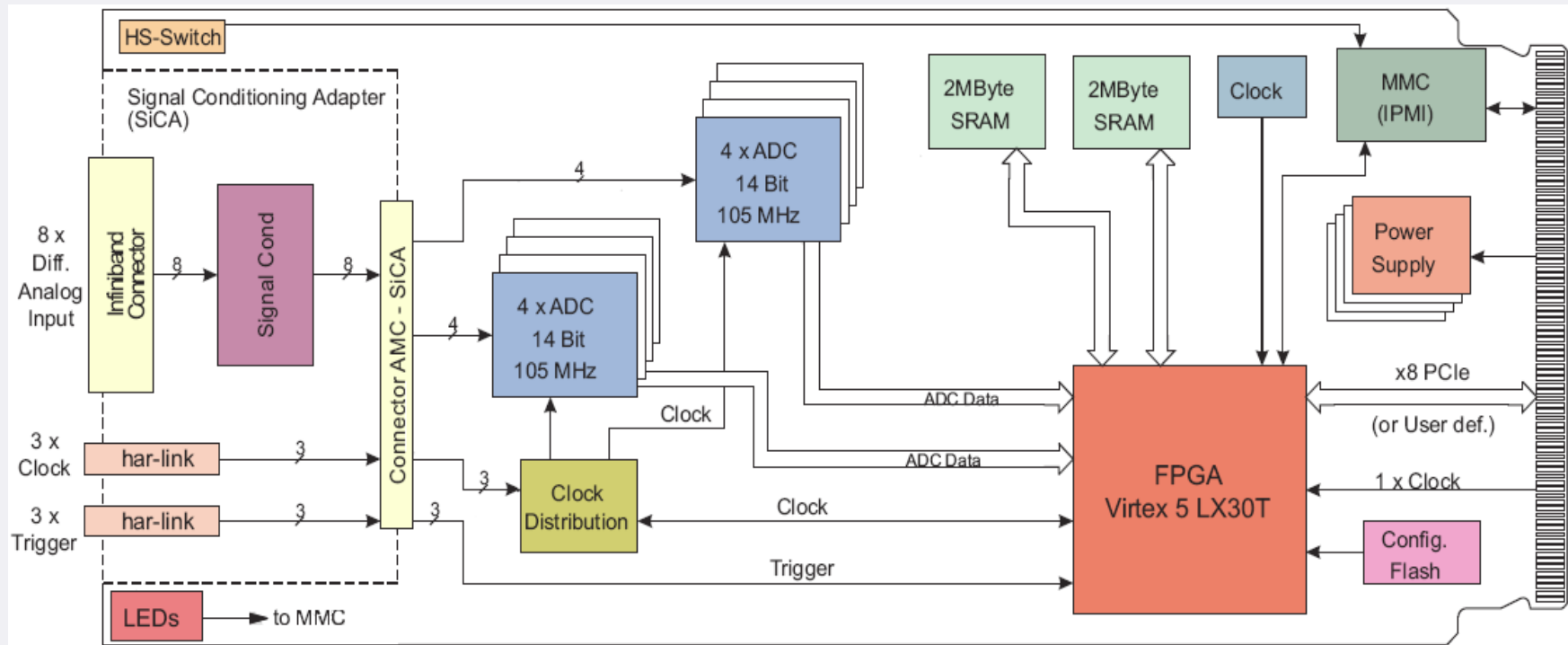
Octuple ADC: 14-16 bit, 100 MHz sample rate, conversion time up to 7 clocks
Configuration interface: AMC.1 PCI Express x1

- ◆ FPGA: Virtex 5 with external static memory (2-4 MB, 250 MHz)
- ◆ Two different configurable clocks for ADC 1-4 and ADC 5-8
- ◆ Clock distribution stability better than 5 ps
- ◆ Full support for IPMI standard

Additional signals from rear connector:

- ◆ 8 analog conditioned input signals (± 1 V, 10-100 MHz)
- ◆ 6 clock inputs up to 100 MHz (LVDS with jitter less than 5 ps)
 - 2 clocks connected to FPGA and ADC
 - 4 clocks connected to FPGA

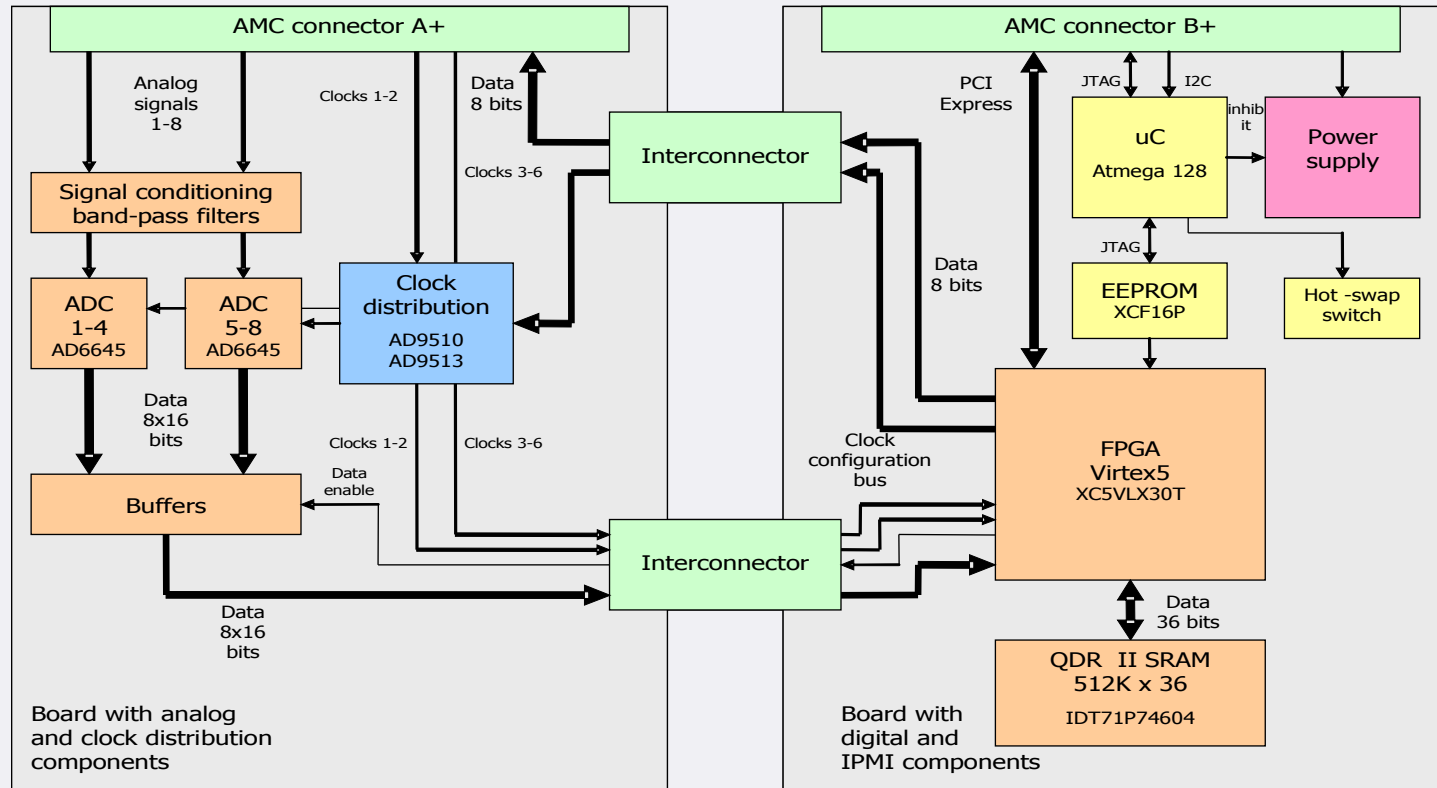
Octuple Analog-to-Digital module - TAMC900



Features:

- ★ 8 x LTC2254, 14-bit, 105 Msp/s ADC converter
- ★ 4 MB of QDR II memory (data buffer for maximum 2 ms)
- ★ 3 external clock and 3 trigger inputs

Octuple Analog-to-Digital module



Features:

- ★ 8 x AD6645, 14-bit, 105 Msp/s ADC converter
- ★ 4 MB (512 kB x36) of QDR II memory
- ★ 6 external clock/trigger inputs

Designed by: Tomasz Klonowski

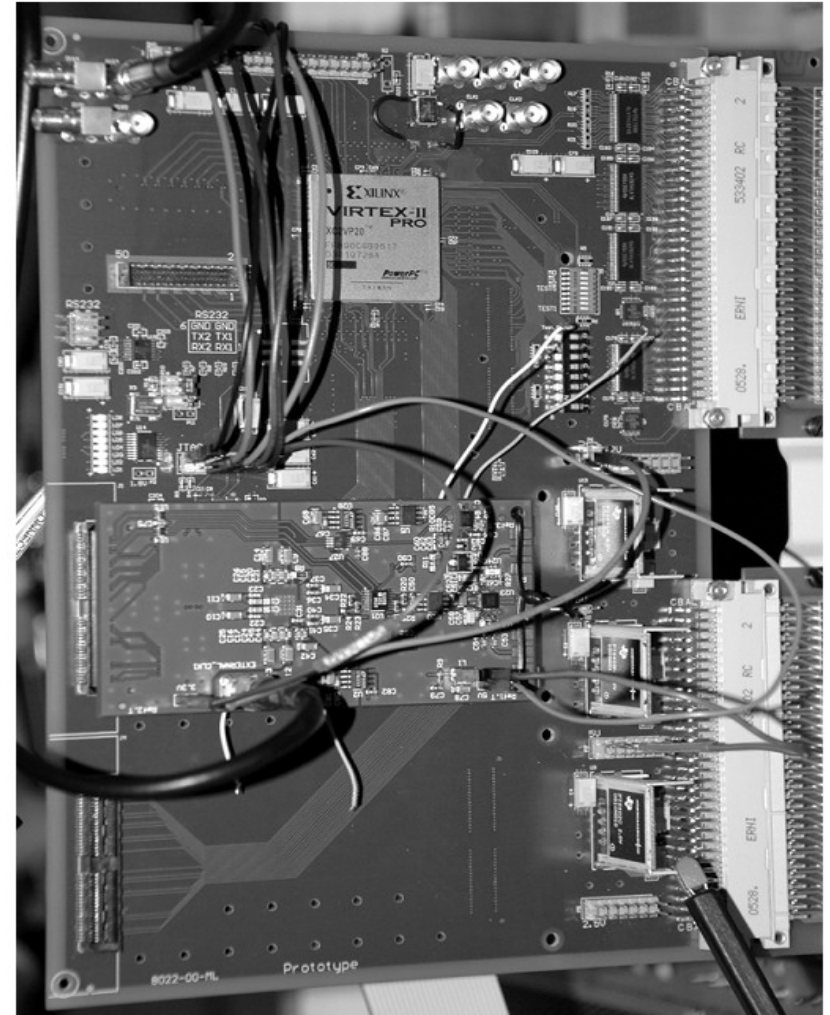
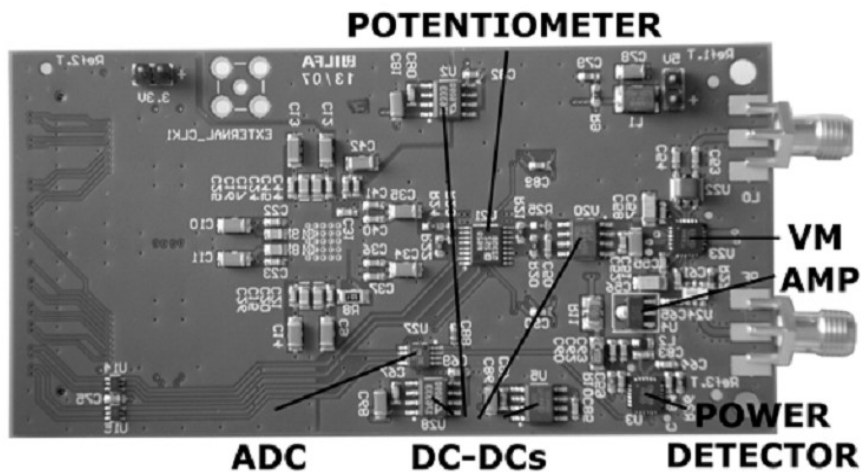
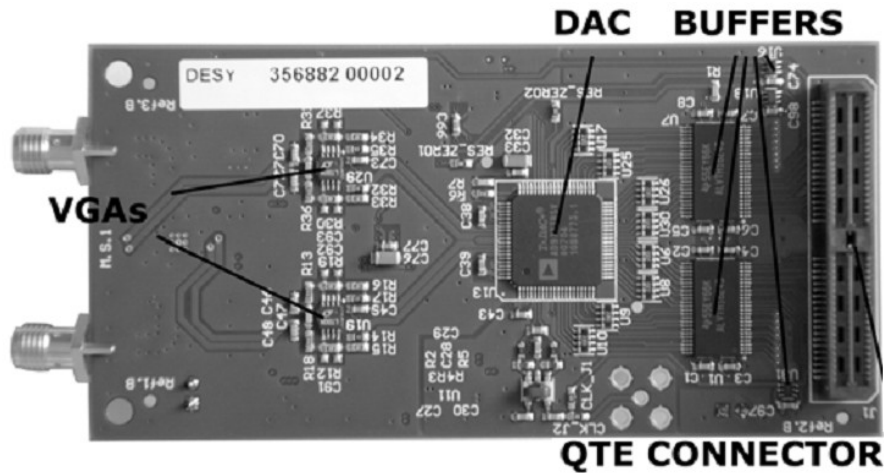
Vector modulator (1)

Requirements:

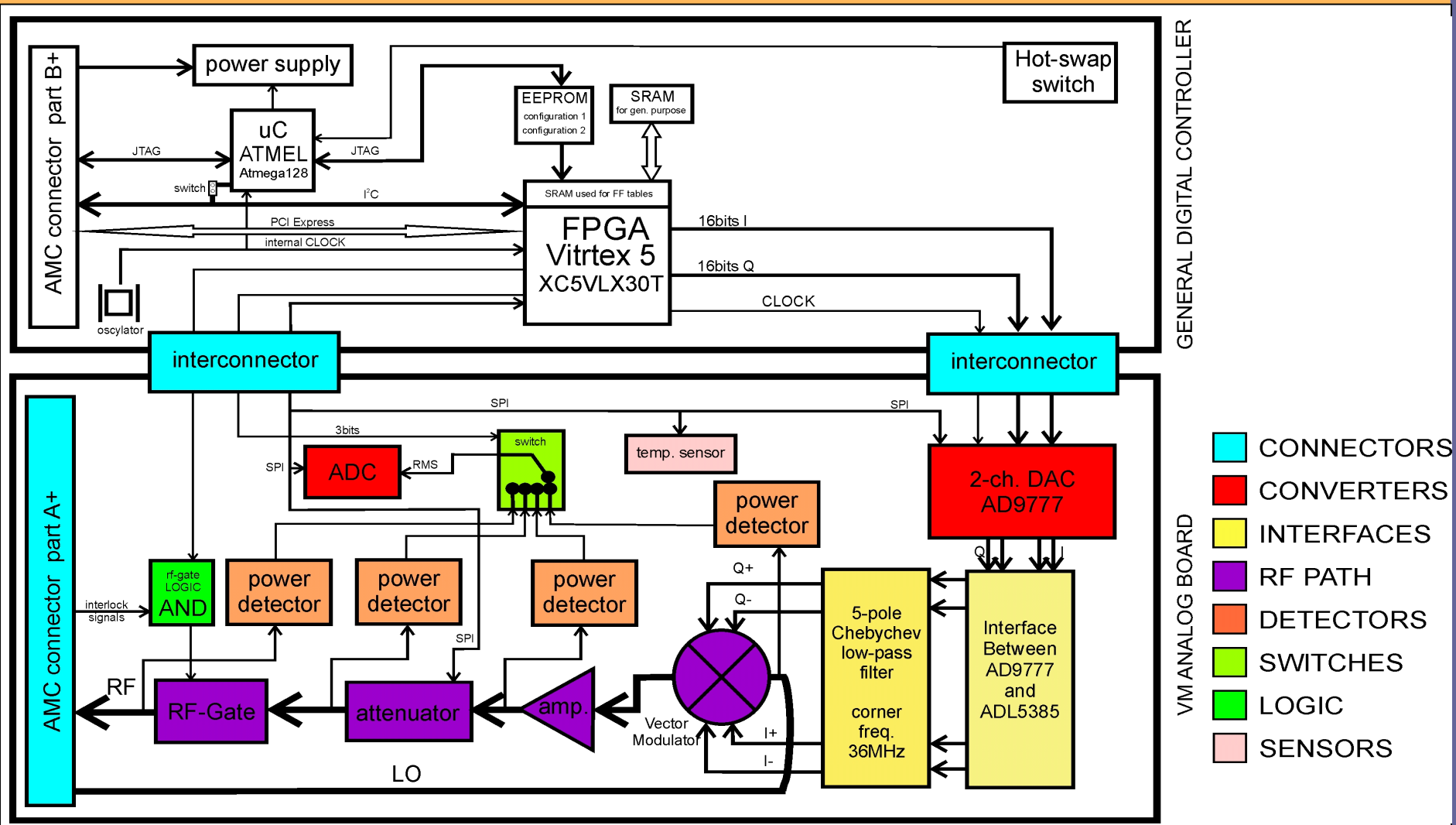
- ★ LO input frequency : 1.3 GHz
- ★ Nominal Input level: $\pm 1 V_{pp}$
- ★ Nominal Input power range: ± 6 dBm
- ★ Input impedance: 100 Ohm nom.
- ★ Input VSWR : max. 1.5:1
(input return loss = 14 dB for VSWR = 1.5)
- ★ Output frequency: 1.3 GHz
- ★ Output level: 0 dBm nom.
- ★ Output impedance: 100 Ohm nom.
- ★ Operating temperature range: -10 deg. C to +70 deg.C
- ★ Humidity: max. 95 % non-condensing

Designed by: Marcin Smelkowski

Prototype of vector modulator



Vector modulator (2)



Clock Synthesizer and Timing Module (1)

★ Clock synthesizer requirements:

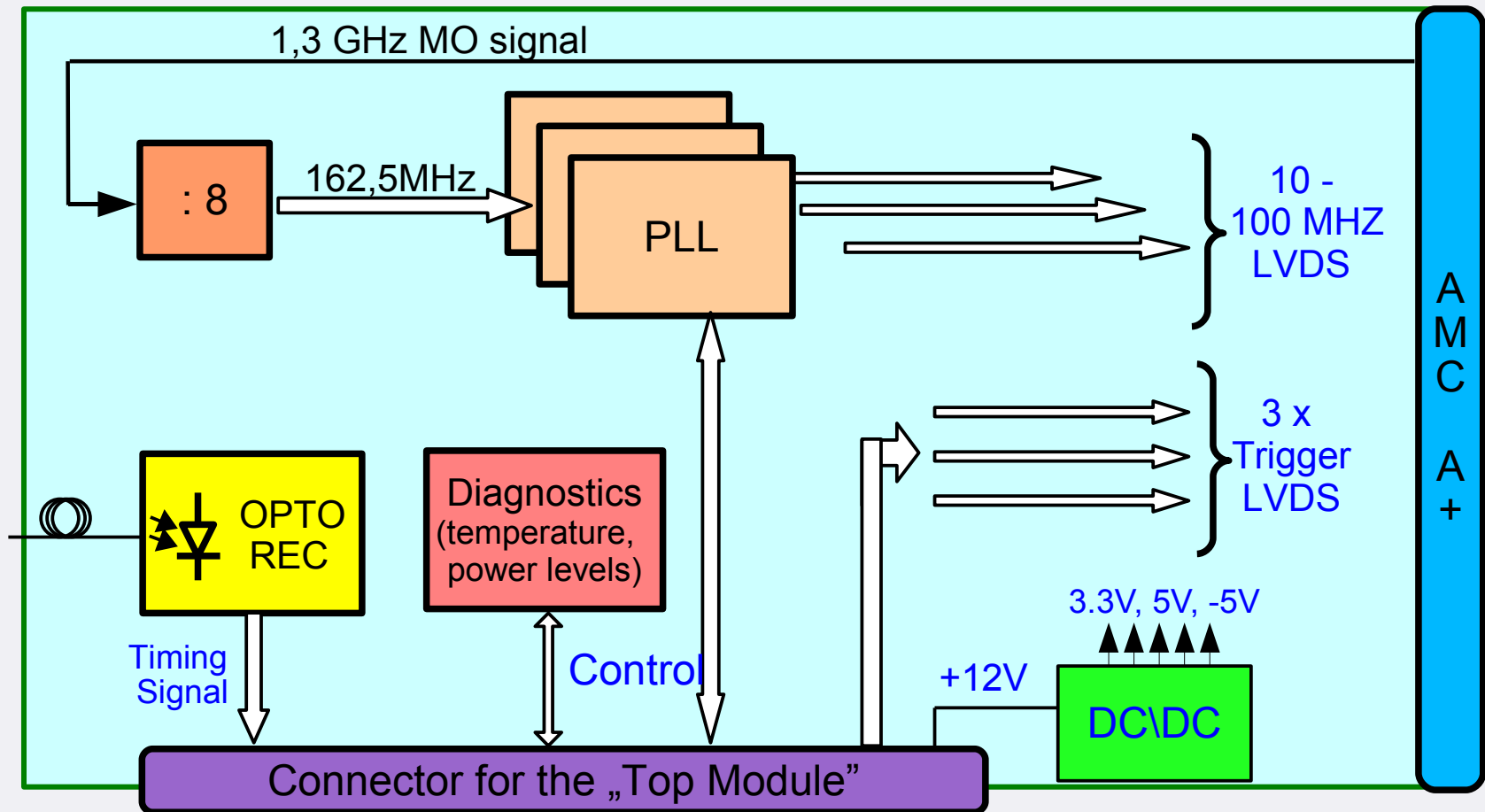
- ▶ Synthesize clock from the MO 1.3 GHz reference signal
- ▶ Clock frequencies: 10 MHz – 100 MHz with 1 MHz step
- ▶ Clock stability better than 5 ps, (desirable < 2 ps)
- ▶ 3 independent clock outputs (LVDS levels)

★ Timing Receiver requirements:

- ▶ Receive and decode timing signals from the existing FLASH timing
- ▶ Optical fibre input
- ▶ 3 independent trigger outputs (LVDS levels)
- ▶ Internal trigger generation mode (trigger frequency 0.1 – 33 Hz)

Designed by: Michał Ładno, Krzysztof Czuba

Clock Synthesizer and Timing Module (2)



Requirements for Radiation Monitoring (RAMC)

Requirements:

- ★ Detection ability: neutron fluence, gamma dose
- ★ Lowest detectable level of fluence: $10^4 - 10^5 \text{ n}\cdot\text{cm}^{-2}$
- ★ Lowest detectable level gamma: $10^{-3} - 10^{-2} \text{ Gy(Si)}$
- ★ Level of neutron fluence tolerance: in range of $10^{12} \text{ n}\cdot\text{cm}^{-2}$
- ★ Level of gamma rad. tolerance: in range of 10^3 Gy(Si)
- ★ Dynamic range for neutron fluence: 6 orders of magnitude
- ★ Dynamic range for gamma: 3 orders of magnitude

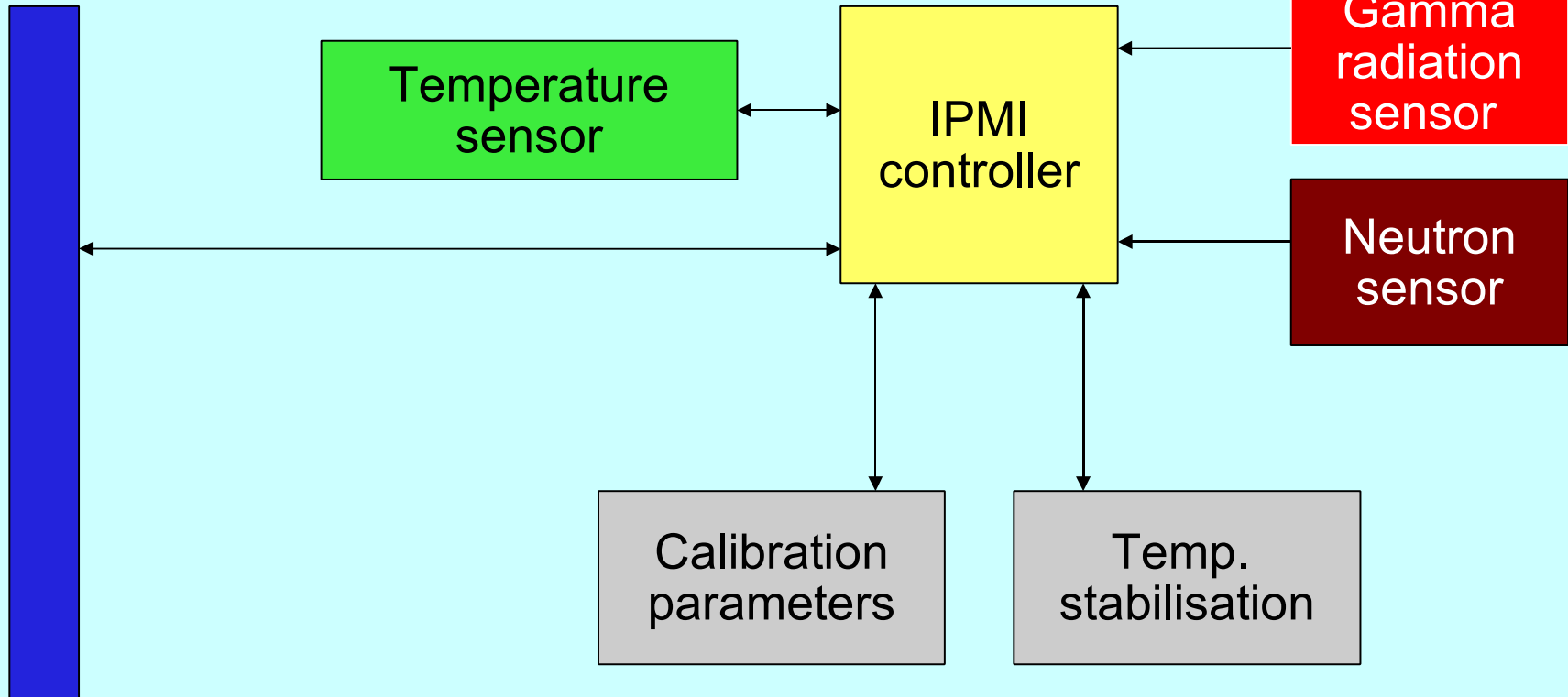
Gamma and neutron radiation should be monitoring in real-time in each ATCA crate and in various places where other electronics is installed.

When allowed dose or fluence is violated alarm should be triggered (IPMI message).

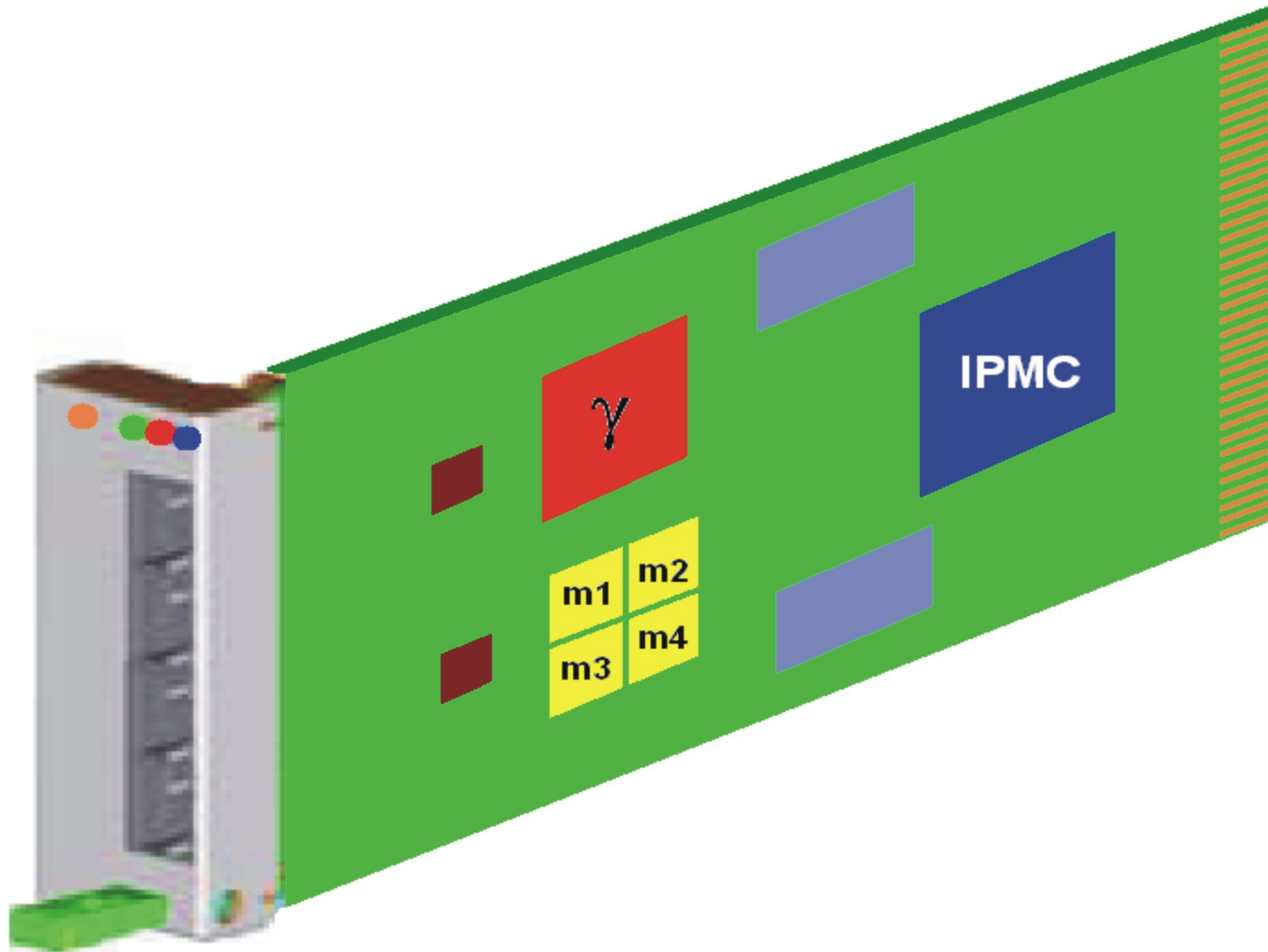
All measured data should be stored in main data base for further analysis

Radiation monitoring RAMC

Top module with connector type „B”



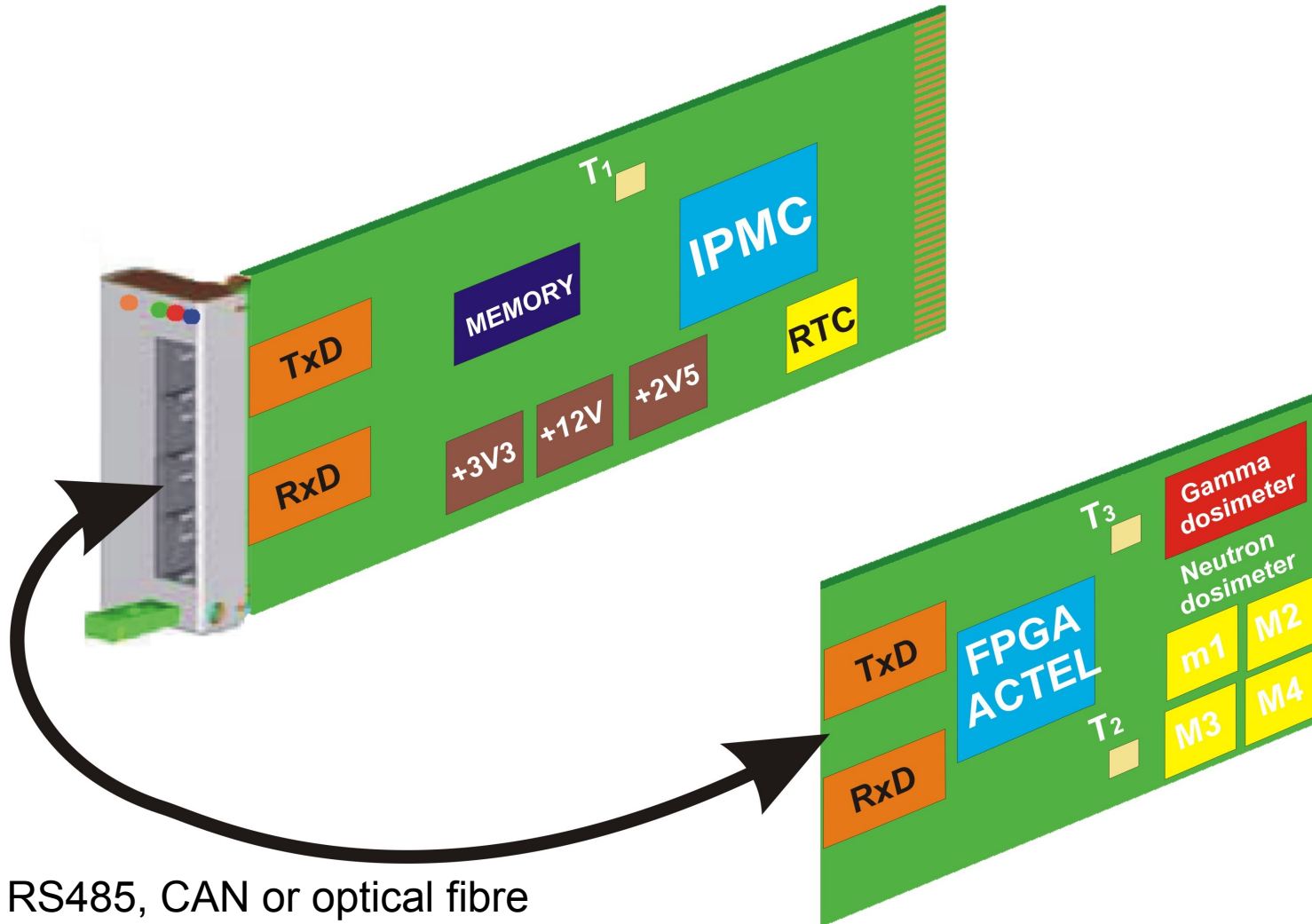
Radiation monitoring RAMC



Thank you for your attention

Spare slides

Radiation monitoring with extension board



EIA RS485, CAN or optical fibre