Piezodriver and Piezo Control

Work Package 1.4

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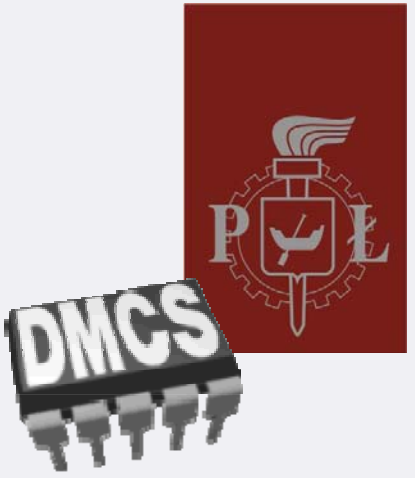


The agenda

The main aim of the piezocontrol system

General requirements and assumptions of piezocontrol system

Overview of the piezocontrol system in regard of LLRF system

Piezocontroller architecture

Piezodriver scheme

Piezo read-out architecture

The main aim of Piezo Control system

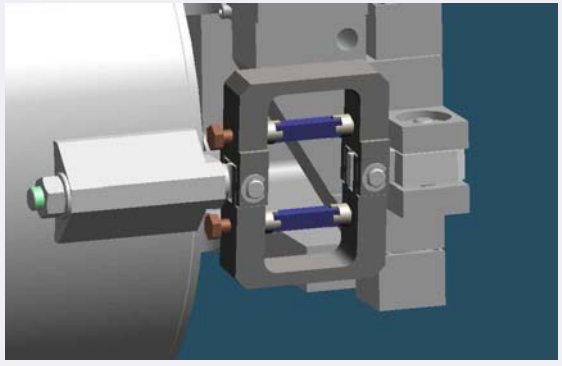
Drive the piezoelements assembled in fast tuners frames to minimize the Lorentz force and microphonics effects

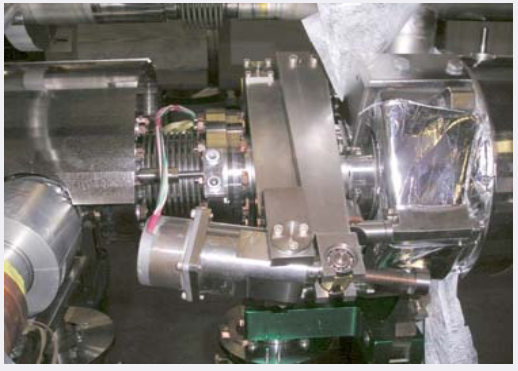
Dimensions: **10x10x30mm**
Manufacturer: **NOLIAC**

On-line frequency detuning calculation

Microphonics measurement (i.e. diagnostics of cryogenic system)

Dimensions: **10x10x36mm**
Manufacturer: **PI**





General requirements of PiezoControl system

Lorentz force detuning (LFD) during flat-top $\Delta\omega_{flat\ top}$ < 20 Hz for field up to 30 MV/m
(compensation up to 600 Hz – possible resonance compensation up to 1kHz)

Commercial available piezoelements (PI and NOLIAC)
C_{2K}= 3÷5 µF, V_{max}= 100 V, oper. freq. for LFD/microphonics up to 1 kHz (full voltage scale), → I_{load} ~ 300mA

Maximal repetition rate of RF (LFD compensation) pulse under 10 Hz
(20 Hz optional if better klystron will be available – piezo driver need to be checked)

Scalable system: 101 modules, 808 cavities, 1616 Piezos

Piezo must be protected and monitored – 2 piezo for each cavity (higher reliability)
(piezo is fragile to over current and over voltage (>150÷200), piezo lifetime must by over 10^{10} pulses, resonance in the cables, piezo might fall out when stepper motor is wrongly tuned)

Piezo function exchange possibility (in case of breakdown) – manual or automatic

System must adjust pulse generated to piezo in regards to RF pulse
(different accelerating field gradient, flat-top and rising time duration demands different settings – feed-forward tables)

Possible microphonics compensation between the RF pulses (sensor/actuator mode)
(microphonics has smaller impact than LFD, constant offset of Δω during flat top, feedback loop)

General assumptions for PiezoControl system

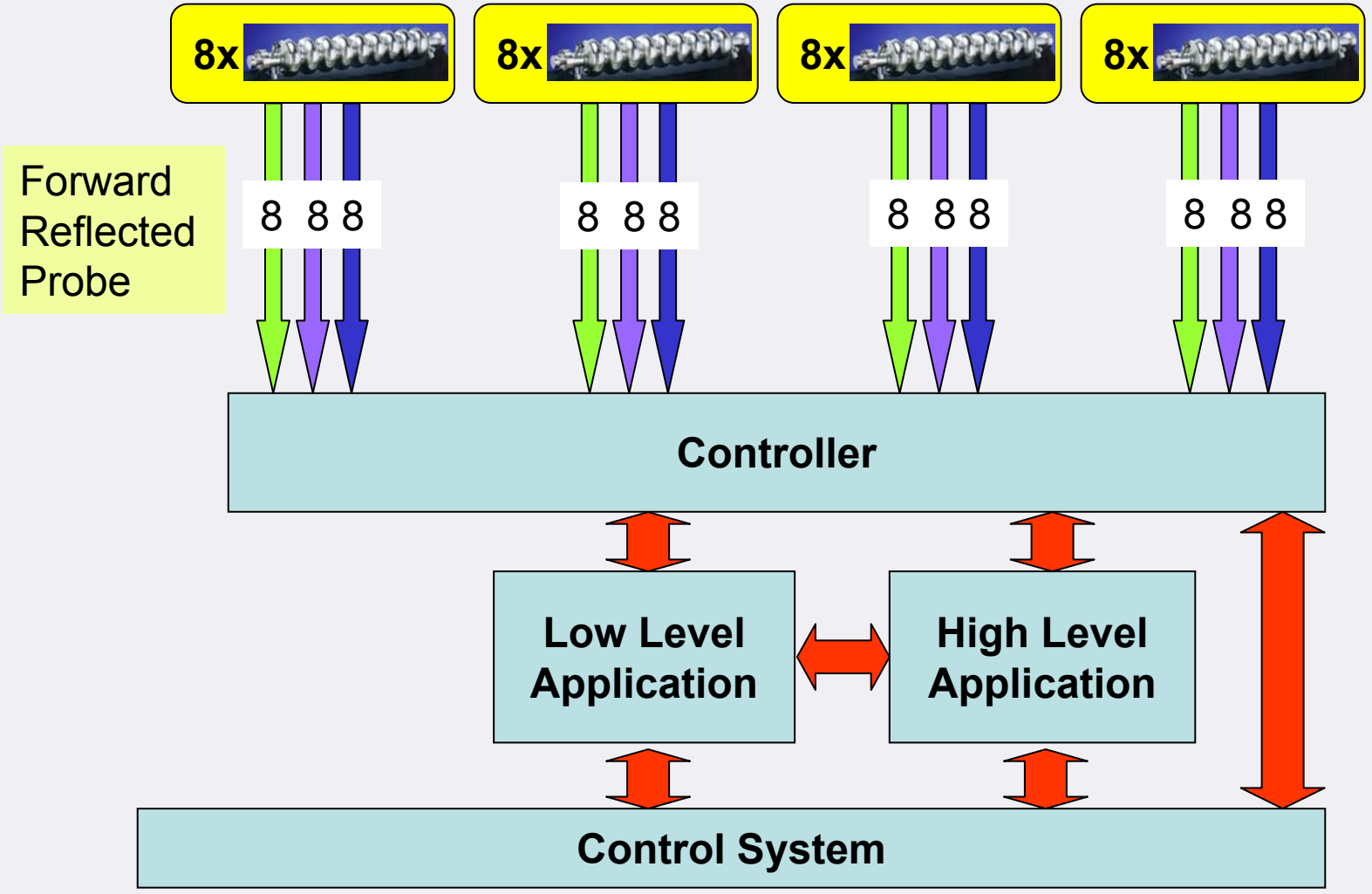
Standalone box for piezodriver, DACs and ADCs cards
(no-ATCA standard due to power supply) → EuroCrate 6U
ATCA integrated switched driver is under investigation (optional)

Piezocontroller close to LLRF controller
(DSP or FPGA based – calc. power needed for feedback and feed-forward loops)

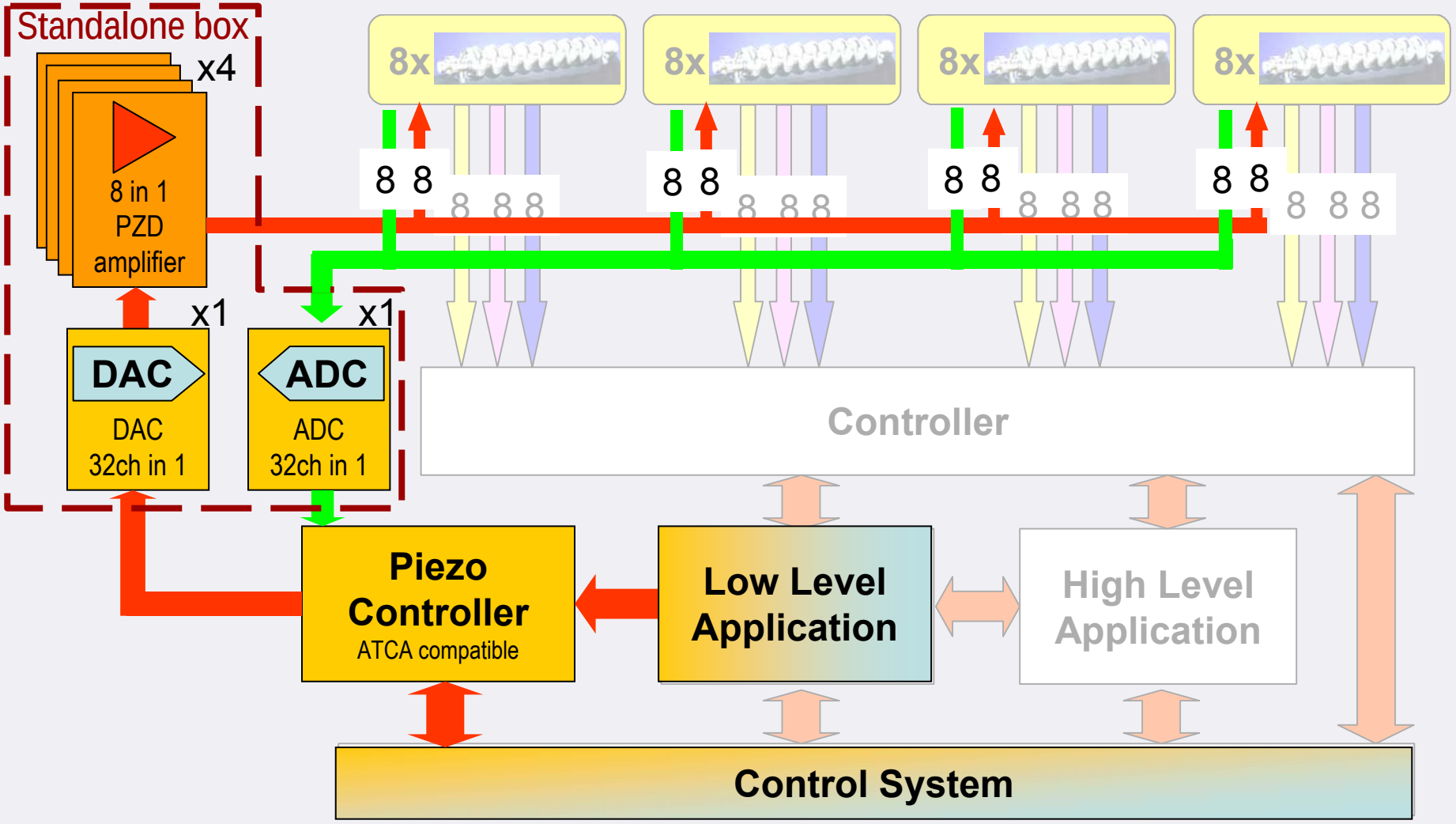
Optical link between PiezoController and DACs and ADCs cards (cable reduction)

System suitable for 64 PI's and/or NOLIAC's piezoelements (32 pairs actuator/sensor)
(4 modules x 8 cavities x 2 piezoelements each) → 25 (+1) PiezoControl systems

Overview of the piezocontrol system



Overview of the piezocontrol system



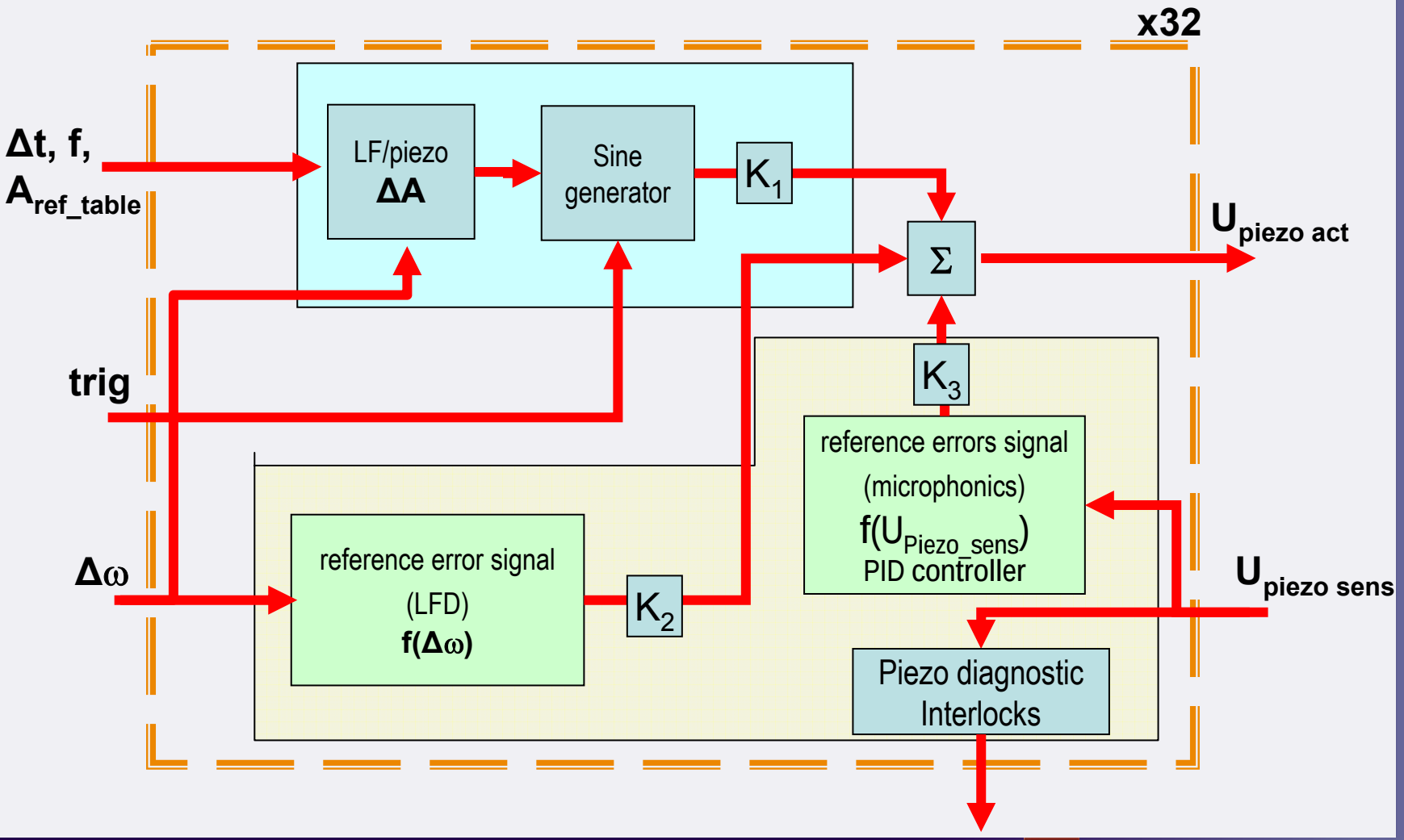
Requirements for PiezoController

Hardware requirements:

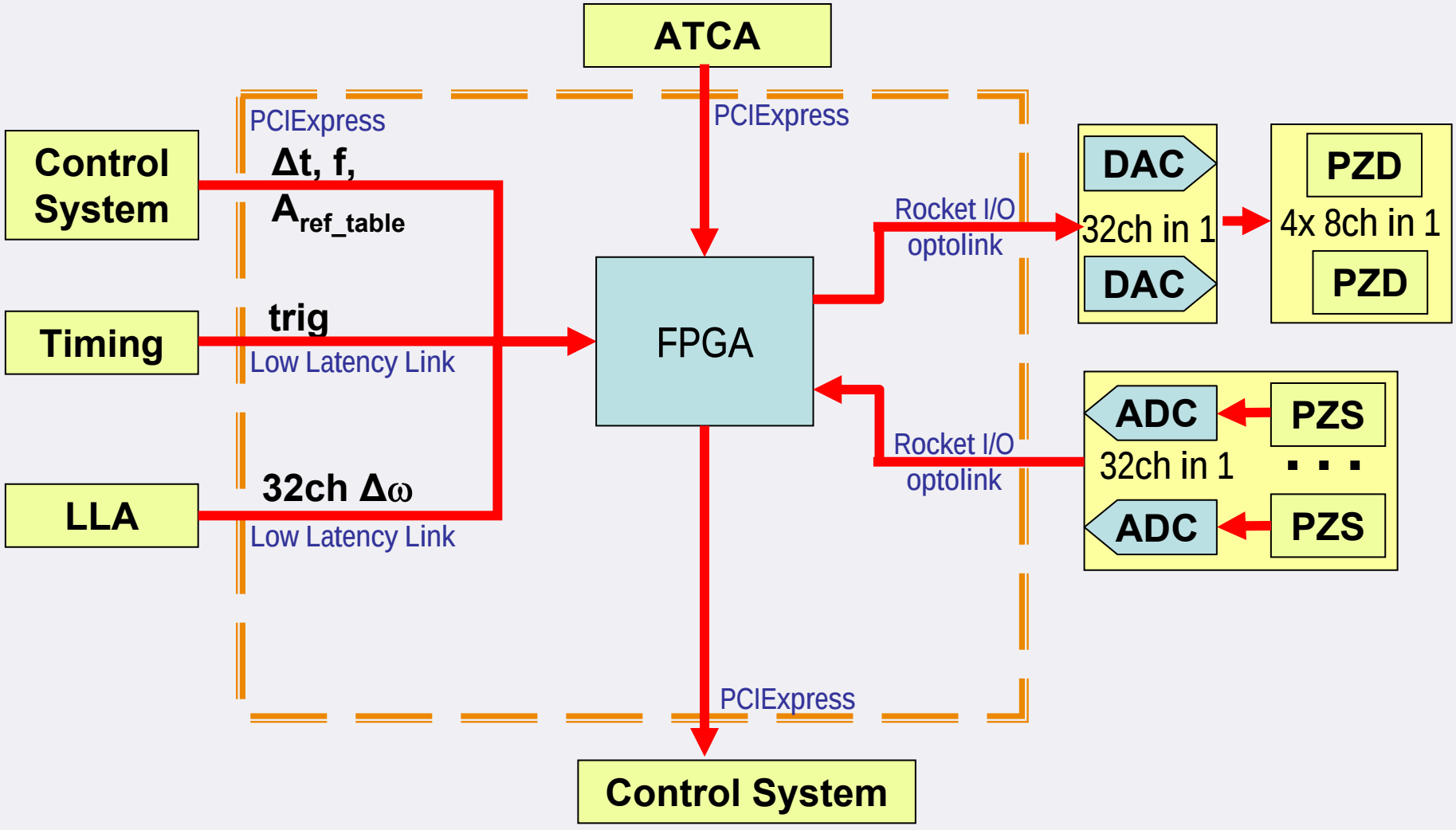
- Lorentz Force:
  - Processing power (possible parallel calculation for different piezo)
    ~ 0,2 MIPS/channel needed
- Microphonics:
  - Processing power (possible parallel calculation for different piezo)
    ~1 MIPS/channel needed
- ATCA Carrier Board compatible (PCI Express) t_{dealy}<50 µs
  (for LF and microphonics settings and data exchange with control system, diagnostic)
- Link to LLA (Low Latency Link for $\Delta\omega$) t_{dealy}<1 µs
- Rocket I/O to back-plane -> OptoLink to DACs and ADCs cards (> 15 Mb/s)
- SRAM 2x 16MB Cypress (data storage)

AMC card with FPGA

Piezocontroller – inside FPGA



Piezocontroller architecture for 32 cavities



Low Level Application

FPGA implementation (as LLA) of detuning algorithm for 8 cavities

$$\Delta\omega = -\frac{1}{2\pi}\left(\frac{d\phi_{probe}}{dt} - 2\omega_{1/2}\frac{|U_{for}|}{|U_{probe}|}\sin\left(\phi_{for} - \phi_{probe}\right)\right)$$

Successfully tested with SimCon [ACC3, 4, 6]

U_{for}	is a magnitude of forward signal,
ϕ_{for}	is a phase of forward signal,
U_{probe}	is a magnitude of probe signal,
ϕ_{probe}	is a phase of probe signal,
$\omega_{1/2}$	cavity half-bandwidth

Forward signal and reflected signal must be decoupled (signal calibration)

Piezo Read-out (ADC card)

Main objective:

- read and adjust the impedance of piezoelements, which work as sensors in fast tuners,
- convert signal to digital representation

General overview:

- Standalone box (no ATCA, EuroCrate),
- close to PZD for exchanging piezostack functionality
- 32 analog input channels (for 4 cryomodules),
- 32 channel ADC (sampling higher than 10 kHz/channel)
- Opitcal Link to PiezoController for data exchange and board monitoring
- Piezo diagnostic (i.e. capacitance measurement)

DAC board

Optolink to PiezoController for data exchange and board monitoring

DAC 32 channels (14 bits)

Output voltage **± 1 V**

Mounted in EuroCrate 6U close to PZD

Piezodriver main parameters

Suitable for both types of piezostacks **up to 5µF**:

Physik Instrumente (P-888.90 PIC255); C_{2K}≈4,4 µF

NOLIAC (SCMAS/S1/A/10/10/20 /200/42/6000); C_{2K}≈ 2,4 µF

Maximal supply voltage up to **± 150 V (nominal operating voltage ±80V)**

Input voltage **± 1 V**

Amplifier gain **G_u= 100V/V**,

Operational temperature **T_c < 75°C (T_j <125 °C)**

Pass-band frequency up to **5 kHz** (for load 5µF)

Need **dedicated Power Supply**

Output voltage and current might be **monitored**

Each channel of PiezoDriver is equipped with **Power Booster PB51**

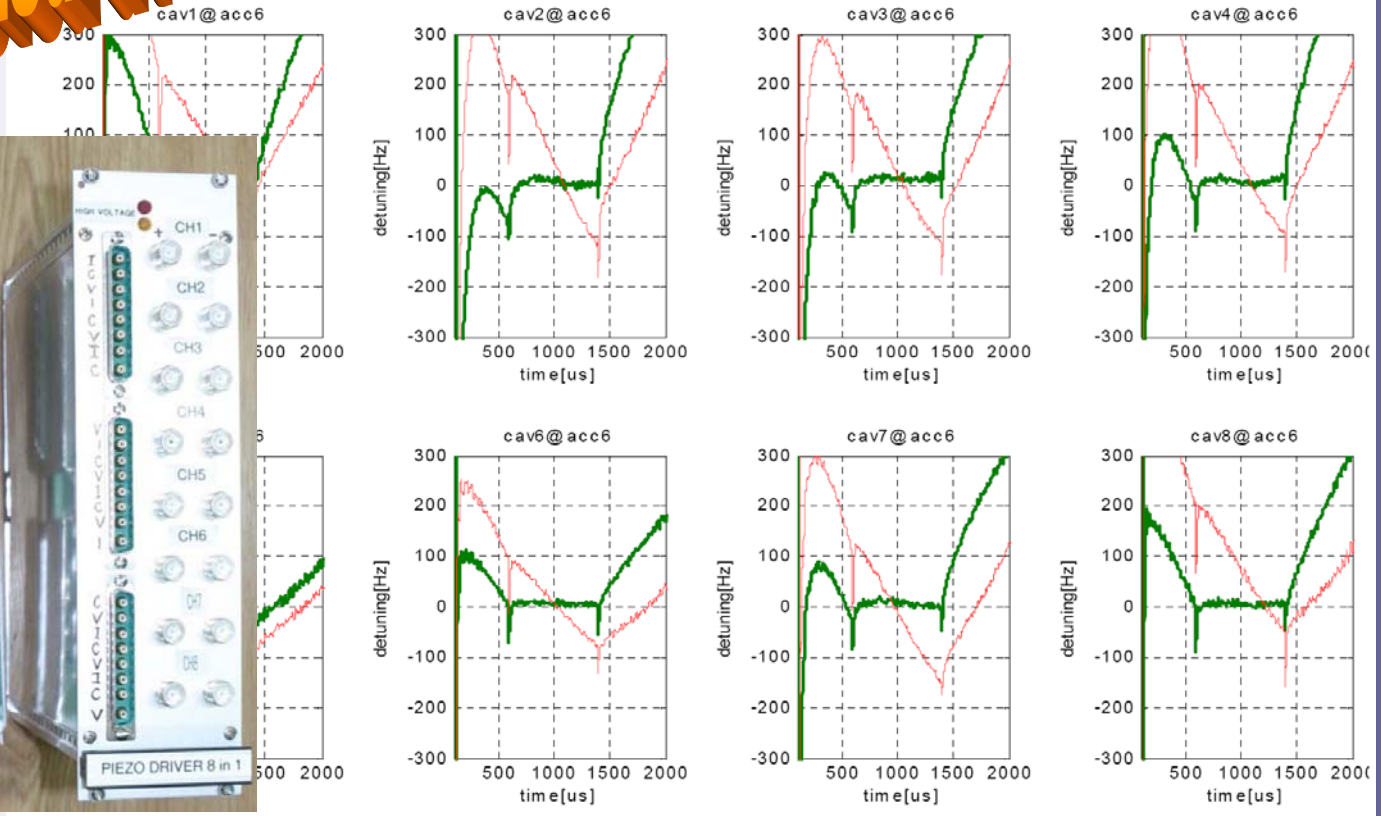
8 channels PZD on single board

Up to 4 periods of sinus wave input signal 200 Hz, 10 Hz repetition rate,

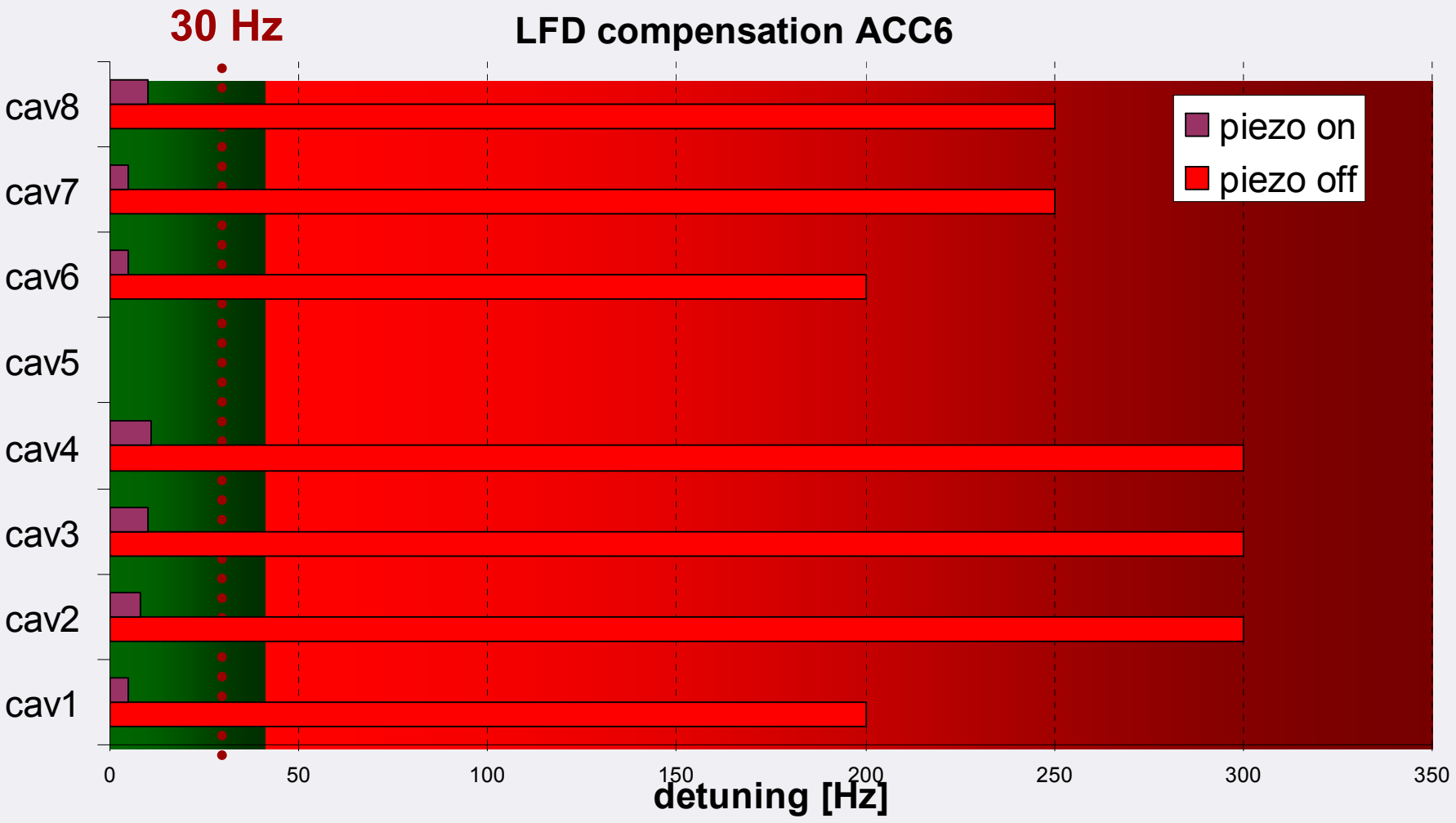
Results

Successfully tested at FLASH

FLASH, ACC6
Acc. Grad = 22 MV/m, Rep. Rate = 5 Hz



Results from ACC6



Summary

PiezoDriver 8 in 1 ver.1 ***is ready*** and was tested with in-situ at FLASH

Some minor modification need to be done – cross-talk reduction, additional thermal protection

DAC cards (32 in 1) with optolink suitable for EuroCrate will be ready in ***beginning of 2008*** (test in-situ scheduled for Jan 2008)

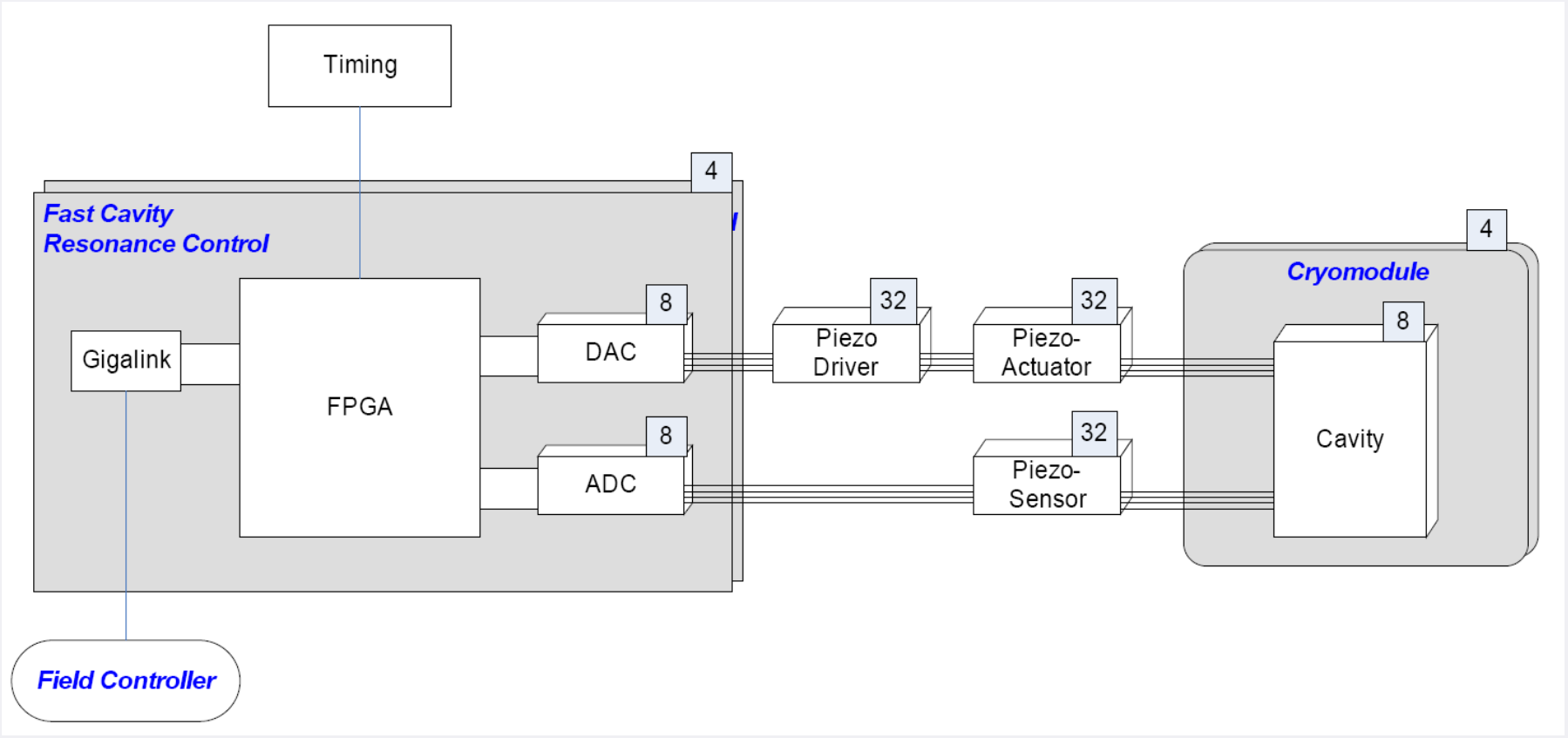
ADC cards (32 in 1) with optolink will be ready in ***I quarter of 2008***

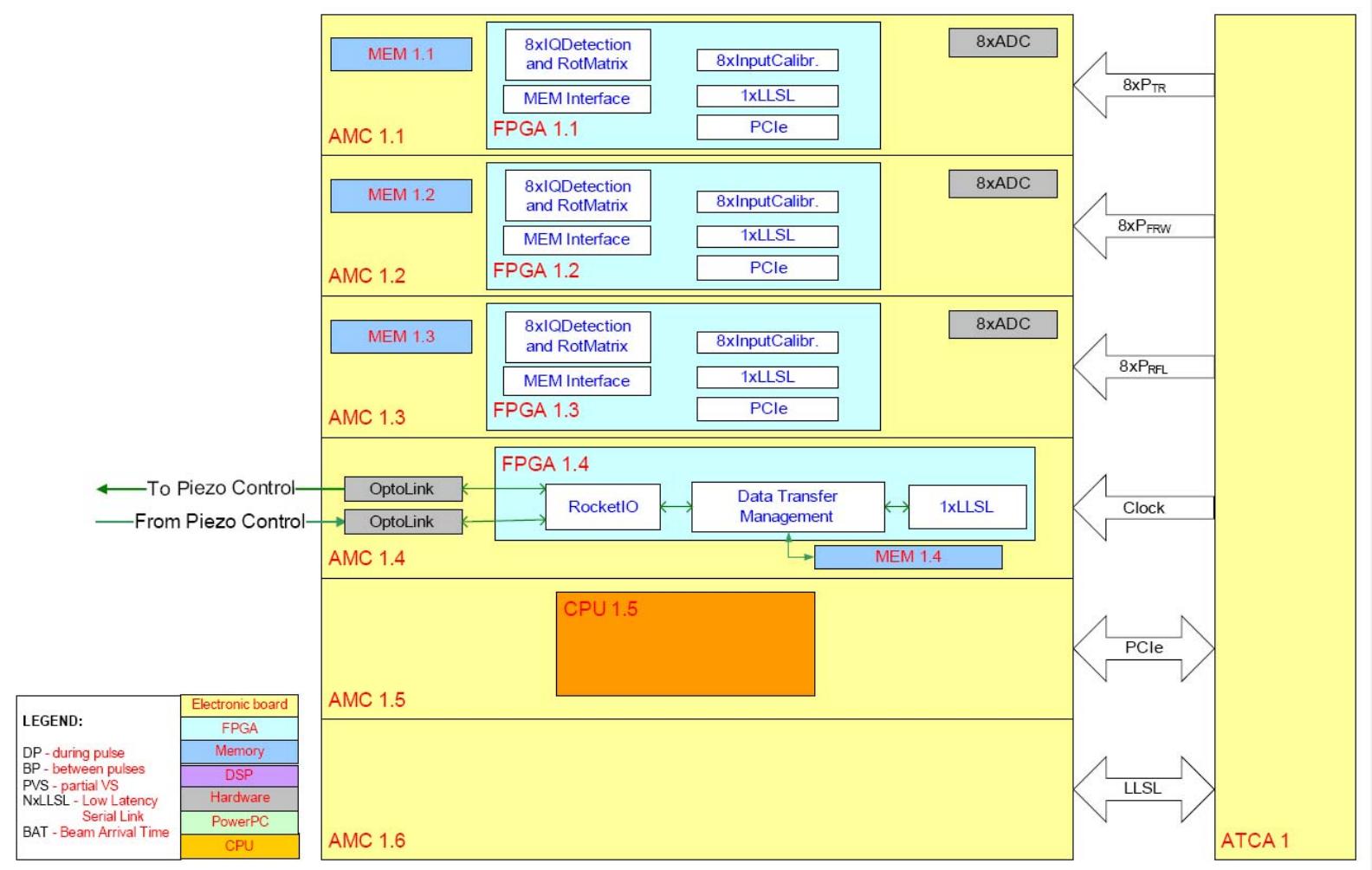
1st version of **AMC PiezoController** will be ready in ***June 2008***. Control algorithm are validated with SimCon (i.e. LFD).

People involved in design - 3 PhDs, 2 PhD students, 4 students

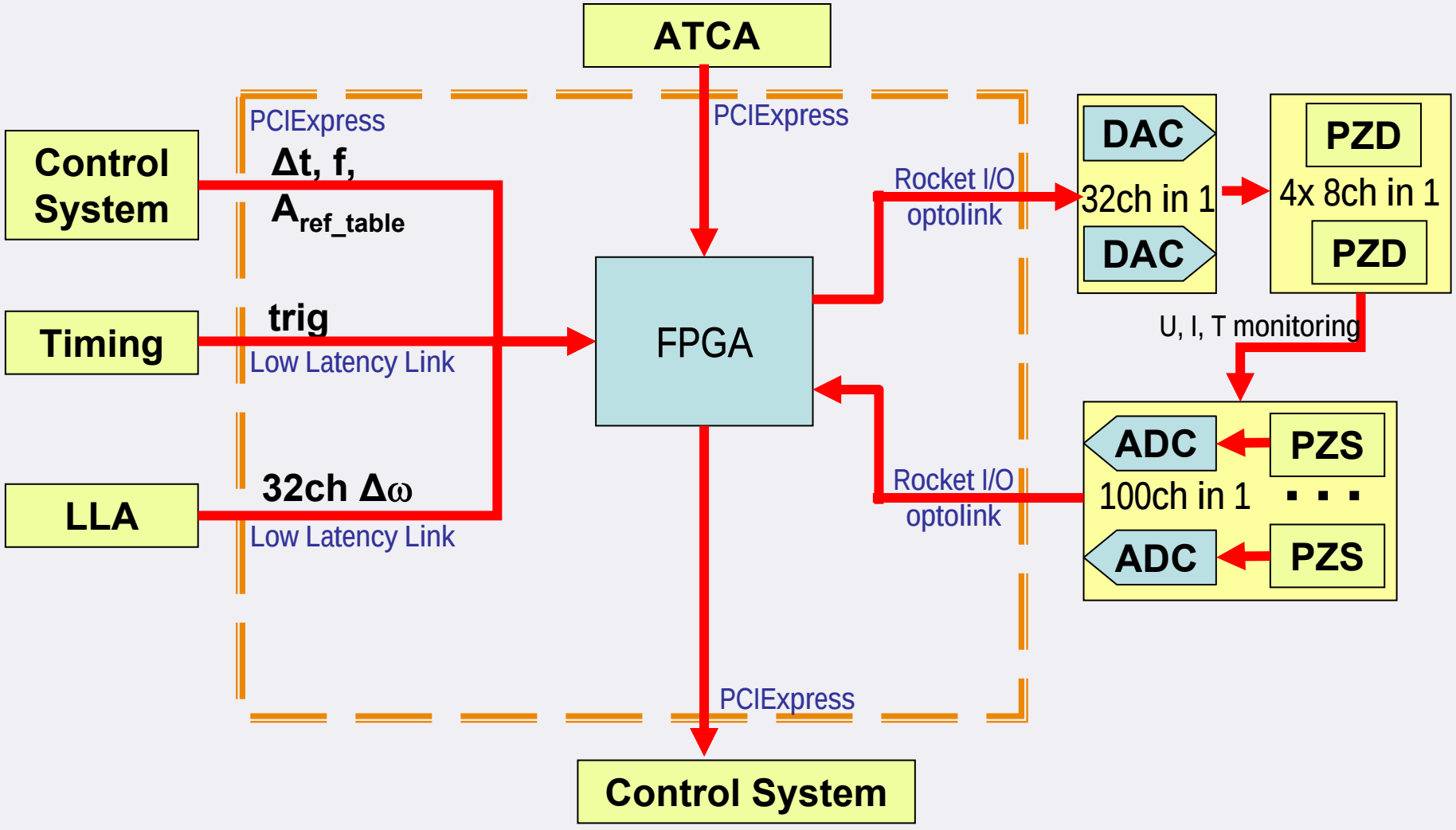
Further experiments needed at BESSY (Berlin) and FLASH (or MTS) (especially microphonics investigation)

Thank you for your attention

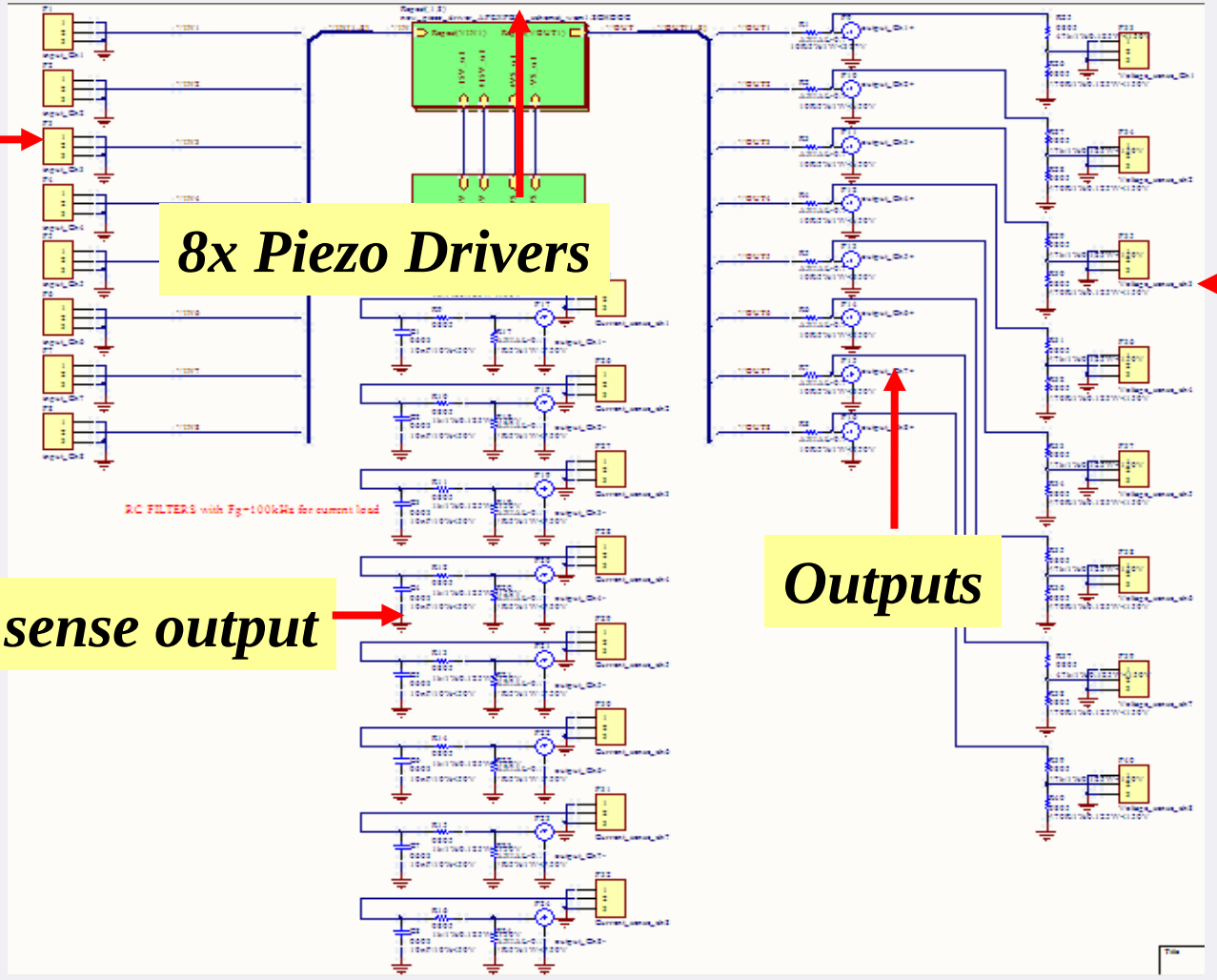

Timing
4
Fast Cavity
Resonance Control
Gigalink
FPGA
8
DAC
8
ADC
32
Piezo
Driver
32
Piezo-
Actuator
32
Piezo-
Sensor
4
Cryomodule
8
Cavity
Field Controller


MEM 1.1
8xIQDetection and RotMatrix
MEM Interface
8xInputCalibr.
1xLLSL
PCIe
FPGA 1.1
AMC 1.1
8xADC
MEM 1.2
FPGA 1.2
AMC 1.2
MEM 1.3
FPGA 1.3
AMC 1.3
8xPTR
8xPFRW
8xPRFL
To Piezo Control
From Piezo Control
OptoLink
FPGA 1.4
RocketIO
Data Transfer Management
1xLLSL
MEM 1.4
AMC 1.4
Clock
CPU 1.5
AMC 1.5
PCIe
AMC 1.6
LLSL
ATCA 1
LEGEND:
DP - during pulse
BP - between pulses
PVS - partial VS
NxLLSL - Low Latency Serial Link
BAT - Beam Arrival Time
Electronic board
FPGA
Memory
DSP
Hardware
PowerPC
CPU

Piezocontroller architecture for 32 cavities



Piezodriver scheme



PiezoController architecture

The feedback loop's latencies (including calculation)< 0.5 ms

The piezo-to-piezo feedback loop based on PID controller
(vibration cancellation between the pulses – BESSY experiments)

The detuning-to-piezo loop based on adaptive feed-forward
(short RF pulse in comparison to mechanical action of cavity)
BESSY experiments

OptoLink to DAC board and ADC cards

Piezo diagnostic (i.e. capacitance measurement)

Interlocks (i.e. protection (cut-off) when module is warm)