Master Oscillator and Distribution

Phase Reference Signals for the ATCA System

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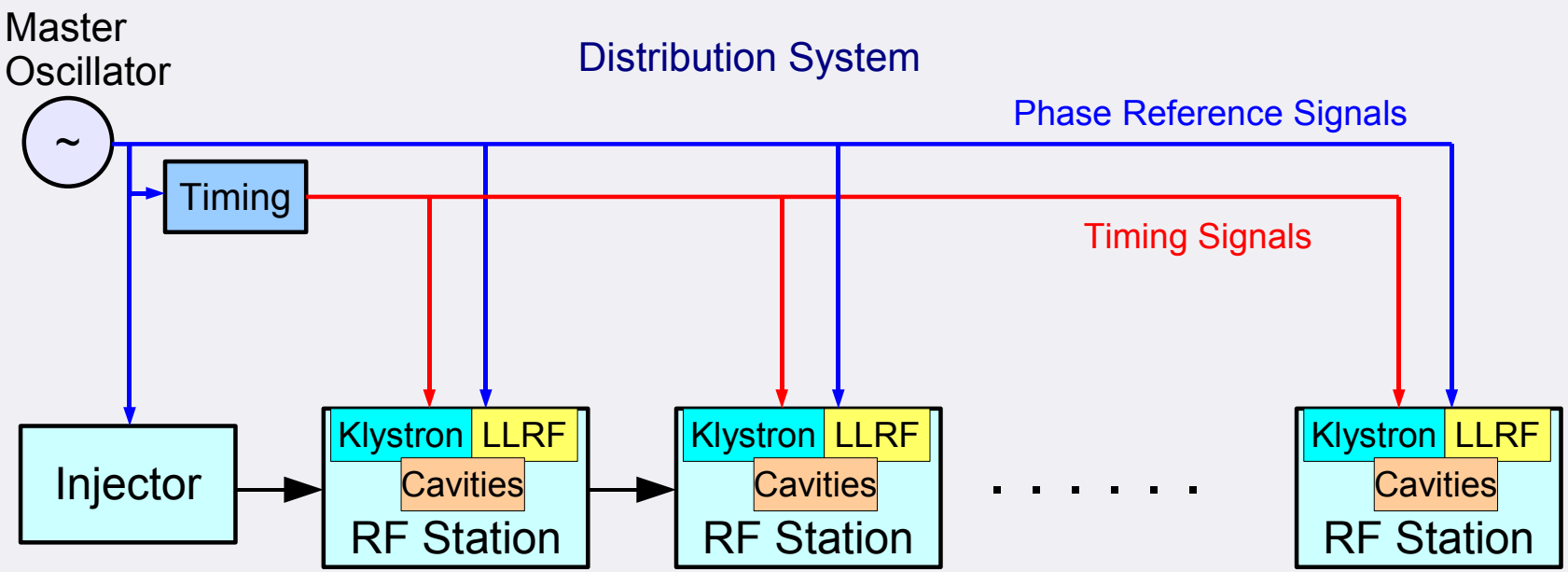
Outline

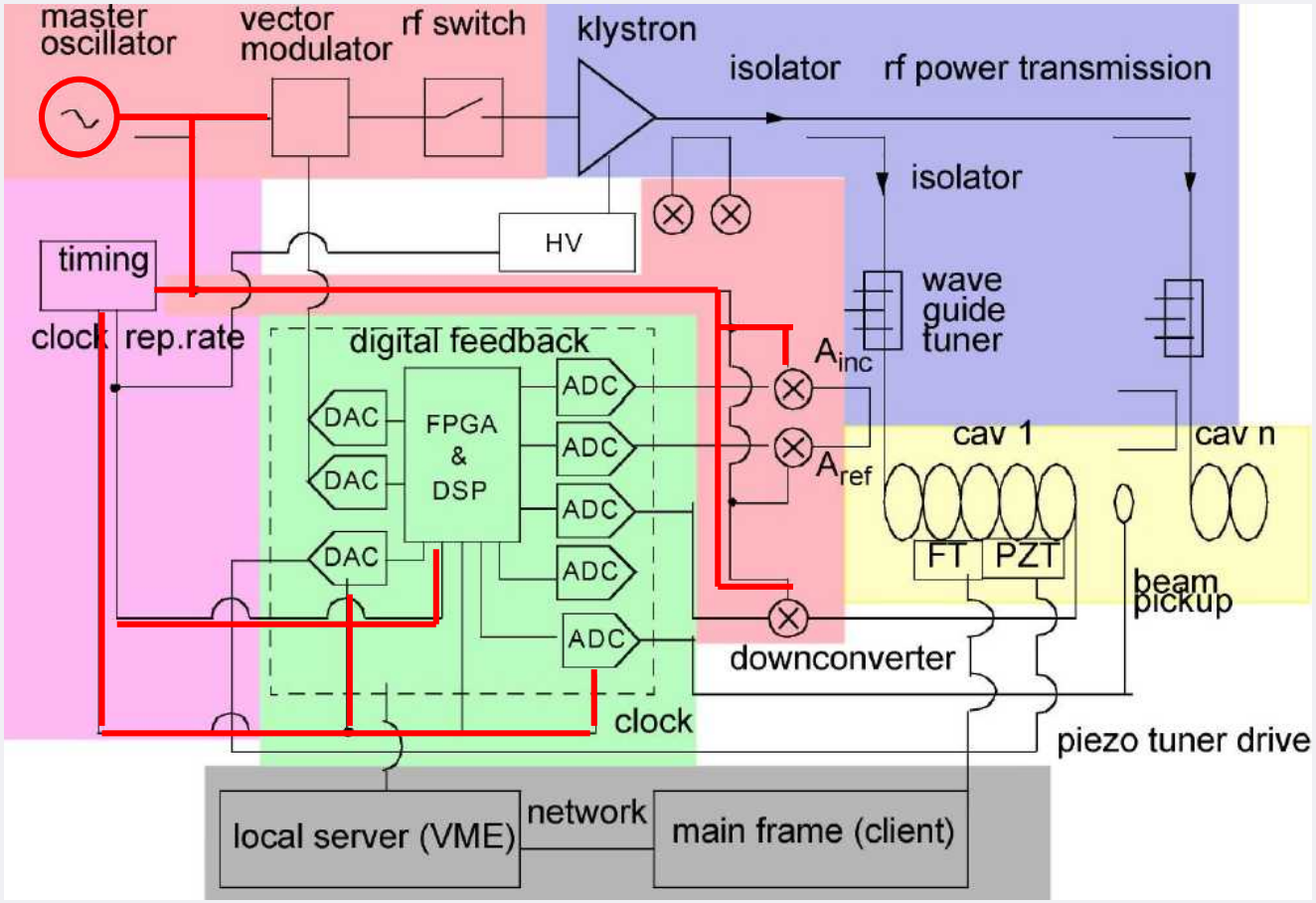
- Need for precise synchronization
- Phase reference and timing signals for LLRF
- MO and timing signals for ATCA (global and local distribution)
- Most important problems
- AMC clock synthesizer and timing receiver
- Project status and plans

Need for Precise Synchronization



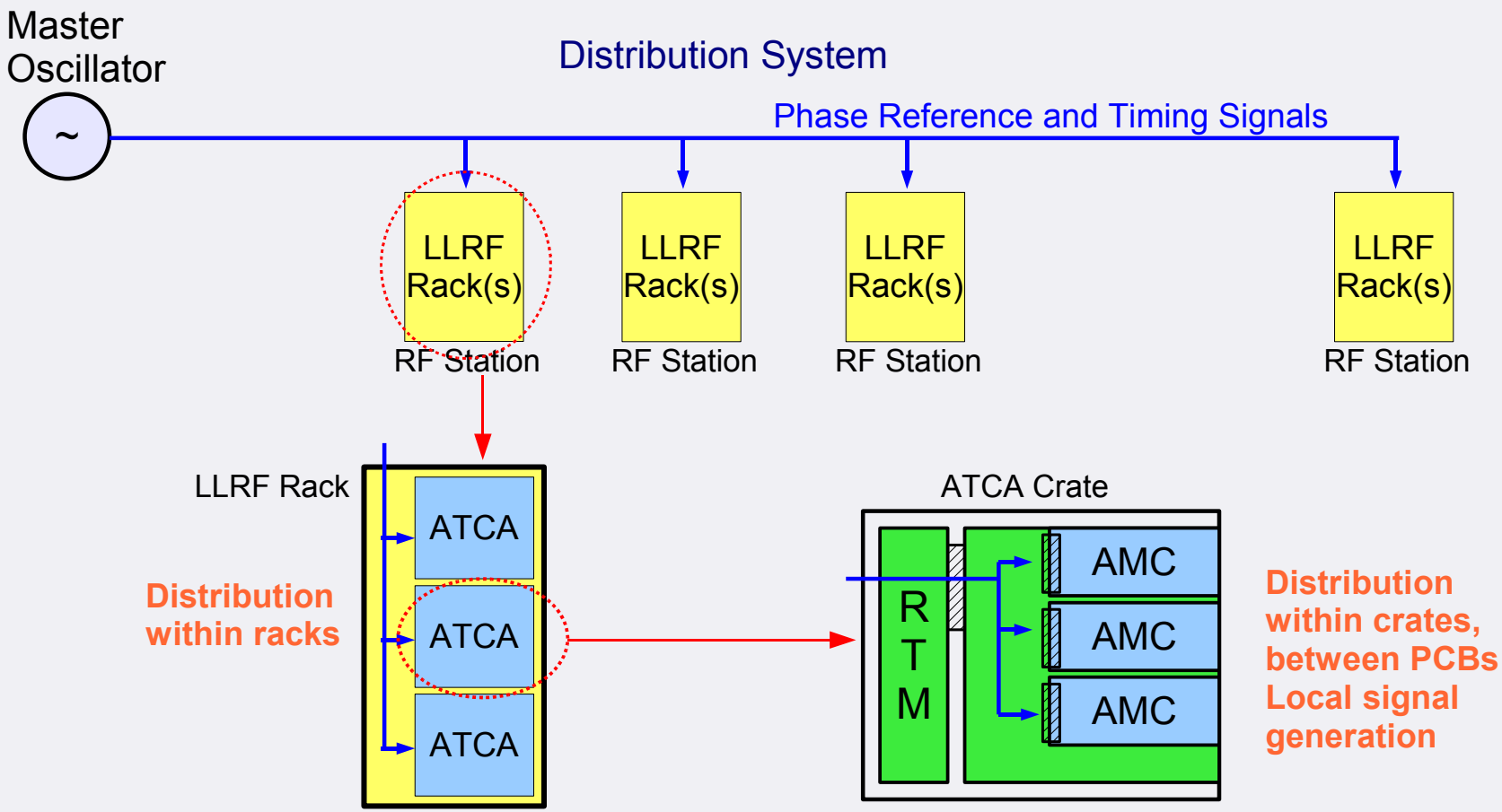
- Electronic devices should be synchronized with high accuracy
- Required jitter for phase reference signals:
  - 0.1 ps short term (10 fs at some locations in XFEL)
  - 1 ps long term

Phase Reference and Timing Signals for LLRF

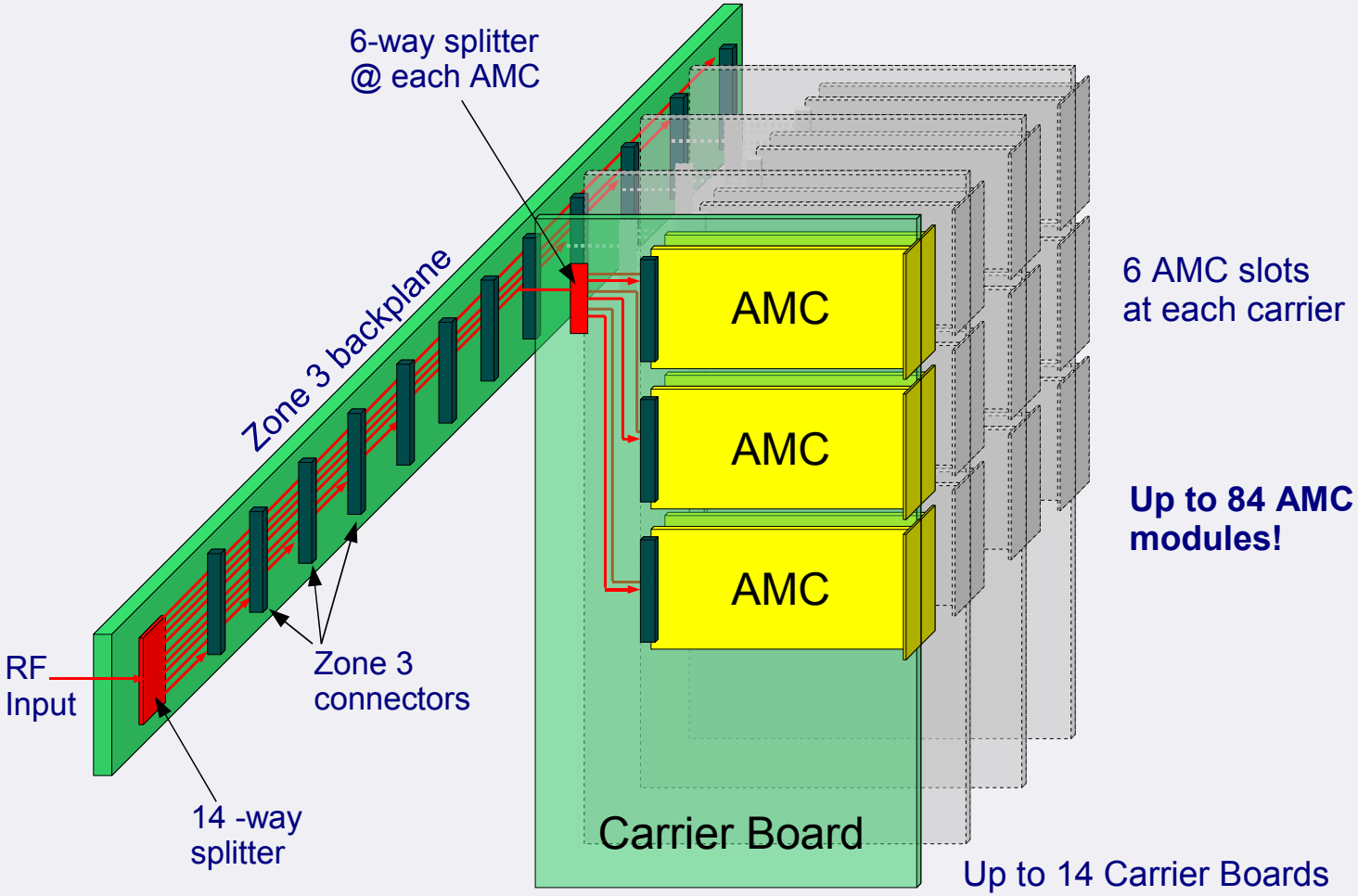


- VM input (1.3 GHz)
- LO for DWC (~1.3GHz)
- ADC and DAC clocks (tens of MHz)
- Triggers for FPGA

Global and Local MO Signal Distribution



MO Signal Distribution Within ATCA Crate

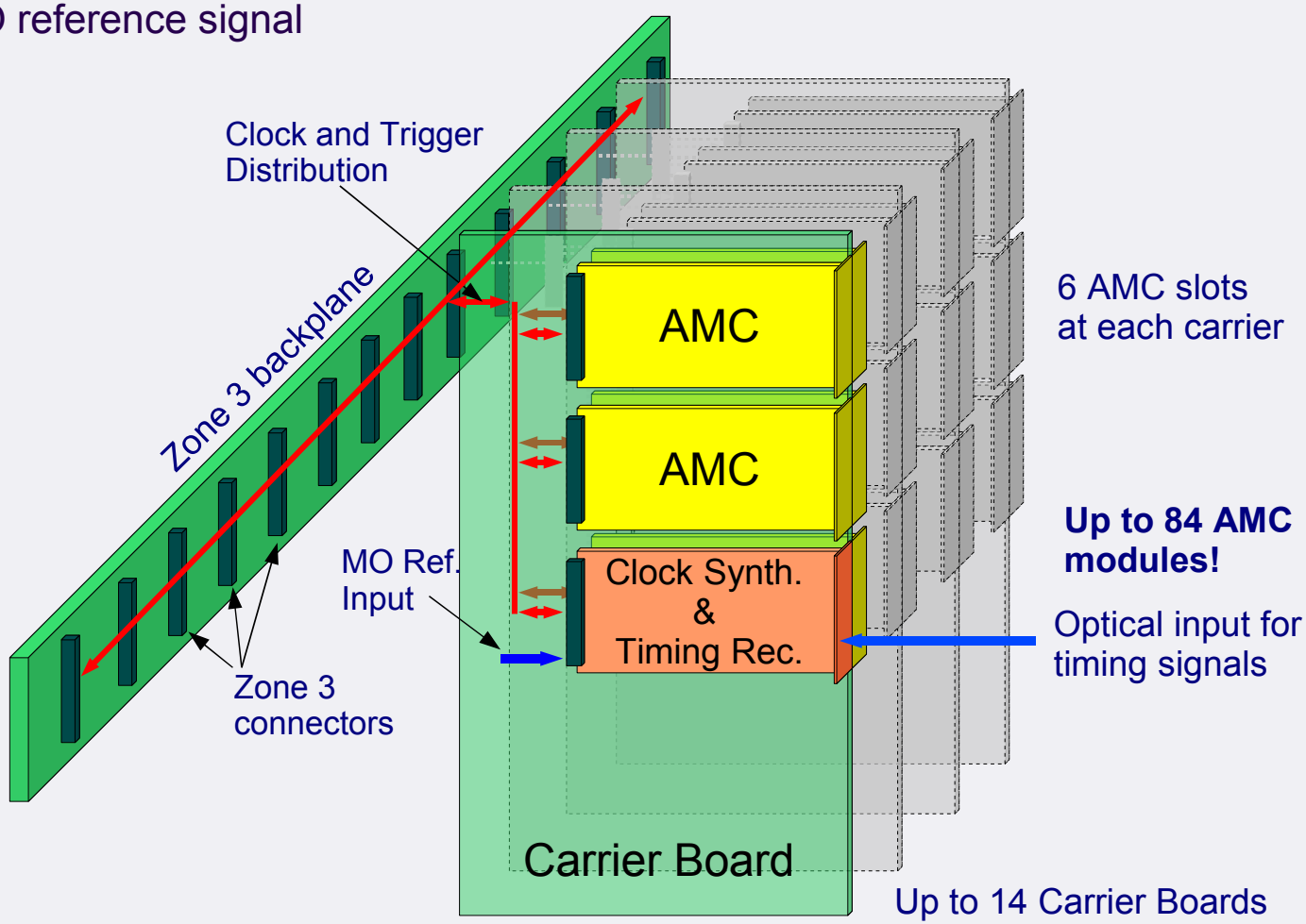


Tasks and problems

- Global: choice of distribution frequency
- Distribution within racks: choice of cables and connectors
- Distribution within crates:
  - Stable distribution in multilayer PCBs and dense **differential** connectors
  - Distribution between PCBs, problems with terminations when PCB removed
  - Interference from high-speed digital circuits
- Local signal generation
  - Building a circuit generating required signals (LO, Clocks, ...) from the distribution frequency with satisfying accuracy

Trigger and ADC Clock Generation and Distribution

Triggers will be extracted of timing signals (optical receiver). ADC clocks will be generated from the MO reference signal



AMC Clock Synthesizer and Timing Receiver Module

Objectives:

- Synthesize ADC clock signals from the MO signal
- Receive signals from the FLASH timing system and provide trigger signals for FPGAs

Module will consist of two PCBs:

1. “Analogue” part (bottom): receiver and synthesizer.
2. Digital part (top): control and interface for the analog part

Requirements for the AMC Timing Module

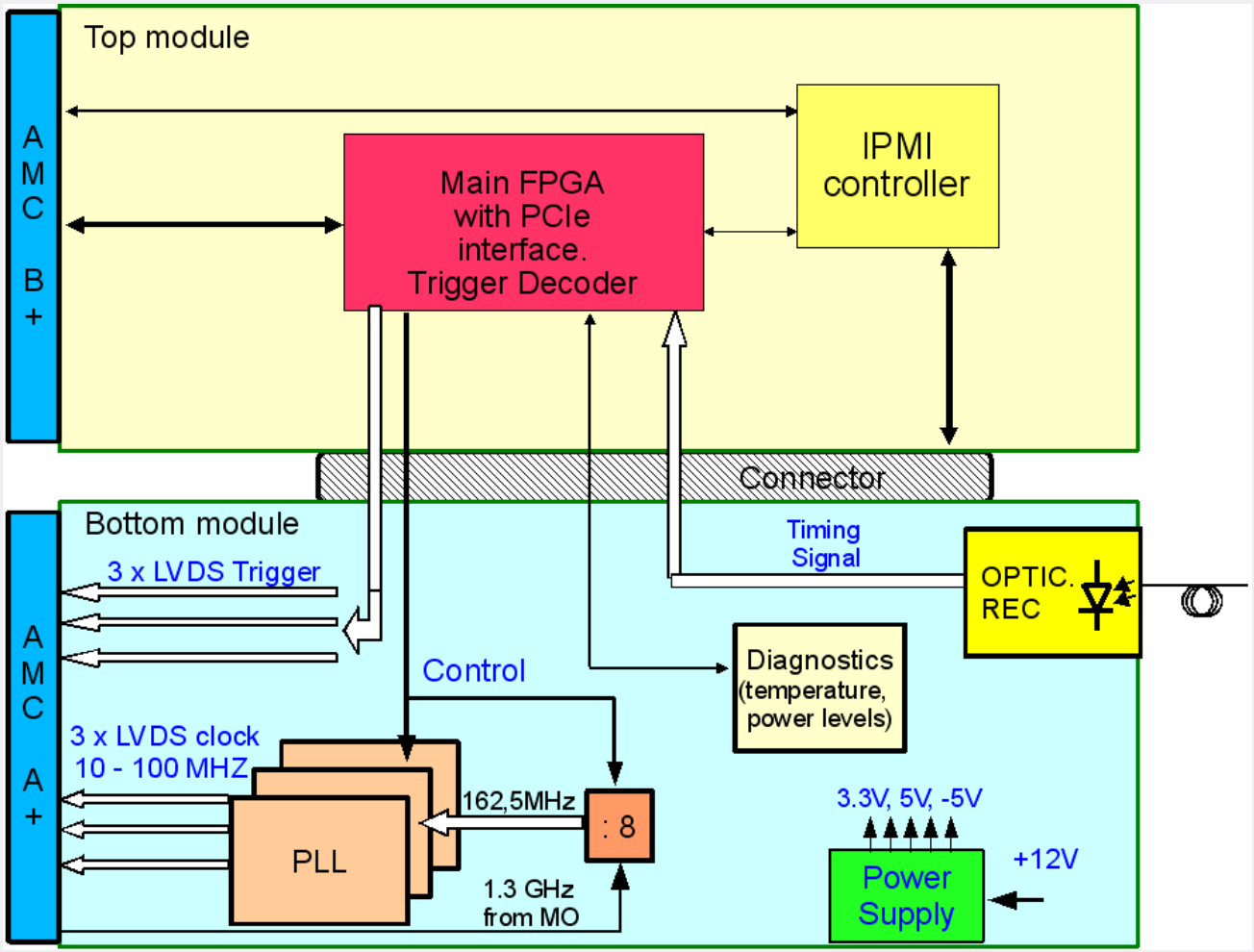
Clock synthesizer requirements:

- Input signal: 1.3 GHz from MO
- Output clock frequencies: 10 MHz – 100 MHz, 0.1MHz step
- Clock stability <5 ps, (desirable < 2ps)
- 3 independent clock outputs (LVDS bus)

Timing Receiver requirements:

- Receive and decode timing signals from the existing FLASH timing
- Optical input (at front panel)
- 3 independent trigger outputs (LVDS)
- Mode with self trigger generation (trig freq. 0.1 – 33 Hz)

Block Diagram



Board Status and Plans

- System conception (finished, spring 07)
- Schematics (finished, Nov. 07)
- PCB layout (in progress). Planned for Dec. 07 / Jan. 08
- PCB manufacturing and electrical tests: Feb. / March 08
- Software for the control module: March/May 08
- Functional tests: June 08

Work and Acceptance Test Procedure

- **After the PCB is manufactured:**
- Electrical tests (connections, shorts, ...)
- Write software for the main functionality of the module (synthesizer control, decoding timing signals, communications)
- Test performance of the main features: clock frequencies, jitter, trigger signals
- Write software for the auxiliary features: diagnostics: temperature sensors, signal presence monitors; self trigger generation

Thank You for Attention