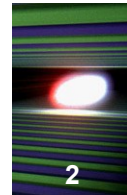


10GbE for data streaming in European XFEL DAQ System

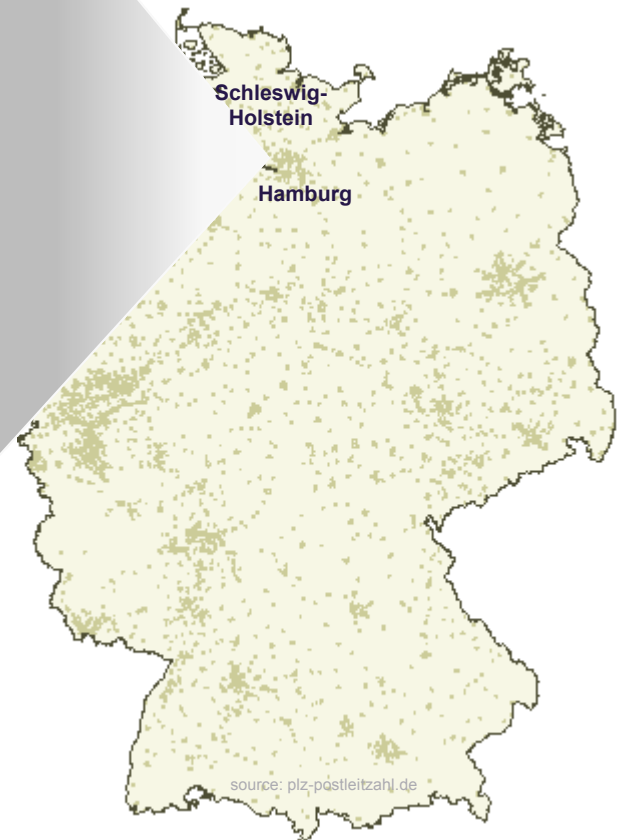
Patrick Gessler (XFEL)



- The European XFEL Project
- Detectors and photon diagnostics providing data
- Beam time structure drive DAQ and control
- Architecture concept
- Hardware overview
- Processing and streaming
- The big picture
- Conclusion

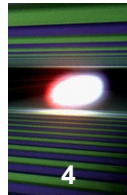
Der European X-Ray Free Electron Laser

3

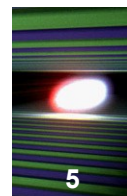


Length	3.4km
Depth of tunnels	6m bis 38m
Costs (Construction, Commission)	> 1 Mrd. Euro
Wave length Photons	0.05nm – 6nm
Users' operation	2016

Der European X-Ray Free Electron Laser



Detectors and photon diagnostics providing data



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Optics (WP73)

- KB mirrors for focusing
- Refractive lens focusing
- Monochromator
- Collimator
- Slits
- Attenuators

Vacuum systems (WP73)

- Turbo pumps
- Ion pumps

Beam diagnostics (WP74)

- Intensity monitors
- Beam positioning monitor
- Photon-electron spectrometers
- K-monochromator and cameras
- Screens and camera

Tunnels contain components listed above

Laser systems (WP78)

- Pump laser and diagnostics

Sample environment (WP79)

- Particle injector
- Cryostat
- Precision stages

Experiment detectors (WP8x)

- e- and ion TOF
- Point detectors (diodes)
- Spectrometers

Experiment 2D detectors (WP75)

- AGIPD
- LPD
- DSSC
- pnCCD

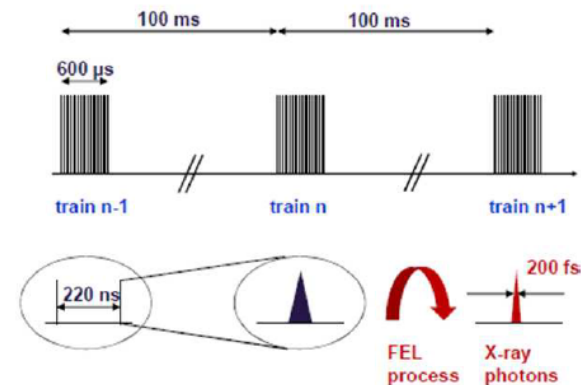
DAQ
significant

Experiment hutches contain components above +
many of the tunnel instruments

Beam time structure drive DAQ and control

6

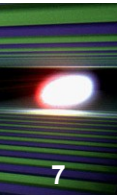
- Readout rate driven by bunch structure
 - 10 Hz train of pulses
 - 4.51 MHz pulses in train
- Data volume driven by detector type and use of data



Detector type	Sampling	Data/pulse	Data/train	XFEL/sec
1 Mpxl 2D camera	4.5 MHz	~ 2 MB	~ 1 GB	~ 10 GB
1 channel digitizer	5 GS/s	~ 2 kB	~ 6 MB	~ 60 MB
Low latency feedback	5 GS/s	~ 2 B	~ 4 KB	~ 40 KB
Screen camera	10 Hz	~ 2 MB	~ 2 MB	~ 20 MB

- **Experiment detectors** are characterized by large data sizes (PBS)
 - Need to acquire, long term storage required, offline analysis, multi-user full AAA s/w framework
- **Feedback systems** are characterized by low data rates and low send latency (machine+PBS)
 - Use on-the-fly, no need to store, trigger level with limited analysis, single user
- **Diagnostic devices** are characterized by low data sizes (machine+PBS)
 - Use on-the-fly, possibly short term storage, on-the-fly analysis, single user

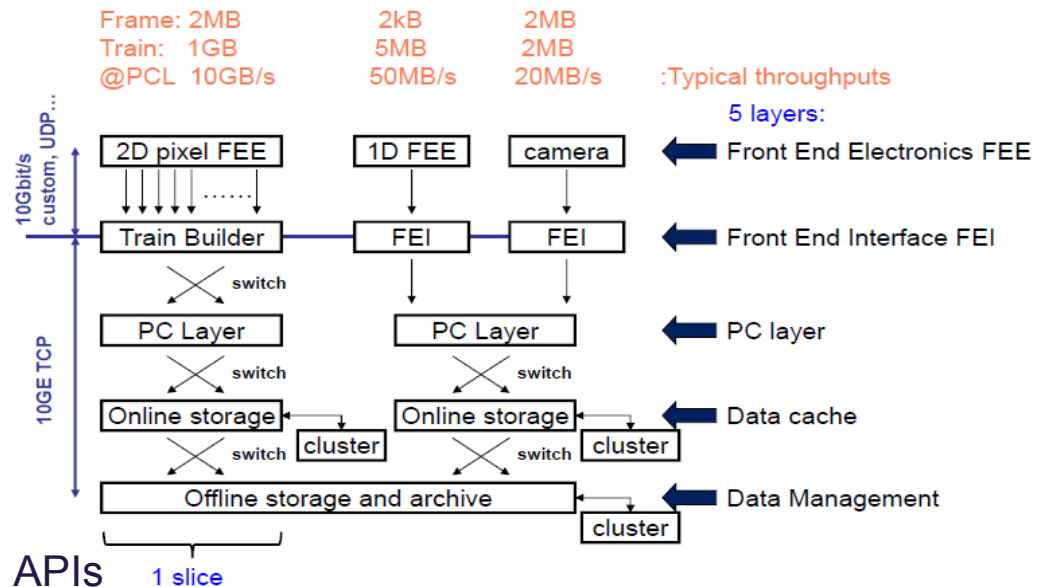
Architecture concept



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Large data volumes, their acquisition, storage and analysis and changing experiment configurations are issues the PBS system architecture is trying to solve

Architecture chosen

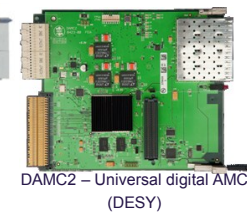


- Multiple layers with well defined APIs
 - to allow insertion of new technology layers
- Multiple slices for partitioning and scaling
 - camera sizes will increase and slice replication will be one solution
- Allow full speed write through to online storage, but discourage usage
 - sometimes this capability is needed to understand measurement
- Enforce data reduction and rejection in all layers
 - early data size reductions and data rejection are needed to reduce storage resources

MicroTCA.4 as main platform

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- MicroTCA.4 allows
 - High-bandwidth communication between
 - Boards and CPU via PCIe
 - Boards via point-to-point connections
 - Synchronization via Timing Receiver
 - Trigger
 - Clocks
 - Machine parameters
 - Bunch structure
 - Remote control and monitoring
 - Module changes during operation (Hotplug)
 - Functional extension via RTMs



MTCA.4 High-Speed Digitizer developments

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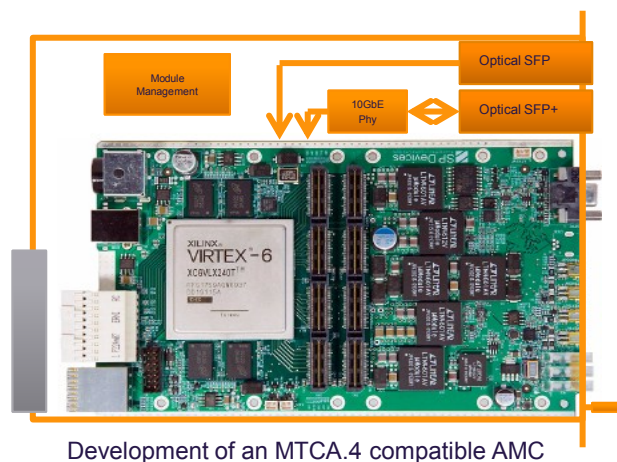
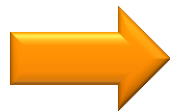
- A development with SP Devices Sweden AB just started

Product	Resolution	Maximum Sample Rate	Analog Bandwidth	Channels	On-Board Memory Size	Interface
SDR14	14bit in 14bit out	800 MSPS in 1600 MHz out	500 MHz	2 in 2 out	2 x 500 Mbyte	USB, cPCIe/PXIe, PCIe
ADQ108	8 bit	7 GSPS	2 GHz	1	1024 MS	USB, cPCIe/PXIe, PCIe
ADQ412	12 bit	1.8/3.6 GSPS	2/1.3 GHz	4/2	700 MS	USB, cPCIe/PXIe, PCIe
ADQ1600	14 bit	1.6 GSPS	800 MHz	1	500 MS	USB, cPCIe/PXIe, PCIe
ADQ DSP	-	-	-	-	1 GByte	USB, cPCIe/PXIe, PCIe

- They will design an AMC version of their digitizer family
 - Additional interfaces and MTCA.4 connectivity added
 - Final products expected end of Q4 2012



Existing Products
(PXIe/cPCIe, PCIe, USB)



Development of an MTCA.4 compatible AMC

Applications

- Photon Diagnostics
 - XGMD
 - XBPM
 - PES
- Detectors
 - 0D (e.g. APD)
 - 2D (e.g. pnCCD)
- Experiments
 - eTOF, iTOF

XFEL detectors

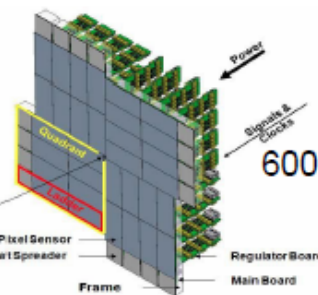
10

AGIPD Adaptive Gain Integrating Pixel Detector (AGIPD)



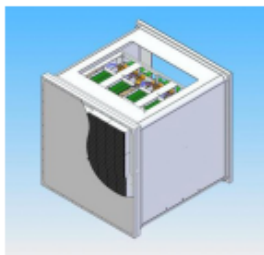
Energy range
3 - 13 keV
Dynamic range
 10^4 @12 keV
Single Photon Sens.
Storage Cells ≈ 300

DEPFET Sensor with Signal Compression (DSSC)



Energy range
0.5 - 6 keV (25 keV)
Dynamic range
6000 ph/pix/pulse@1 keV
Single Photon Sens.
Storage Cells ≈ 640

Large Pixel Detector (LPD)



Energy range
5 (1) - 20 keV (25 keV)
Dynamic range
 10^5 @12 keV
Single Photon Sens.
Storage Cells ≈ 512

Other Detectors

- 0D/1D detectors for high repetition rate applications (e.g. veto, dispersive spectrometers)
- Small areas, low rep. rate, low energy 2D imaging detectors
- Particle detectors (eTOF, iTOF)

Control and DAQ features

- 2D: custom systems (ASICs, capacitive and digital pipelines), acquire limited number of pulses per train; modular design = 16 modules per Mpxl
- 1D: strip detectors
- 0D (diodes...) and Particle detectors: use Fast ADCs or Digitizers

2D detector control, processing and streaming

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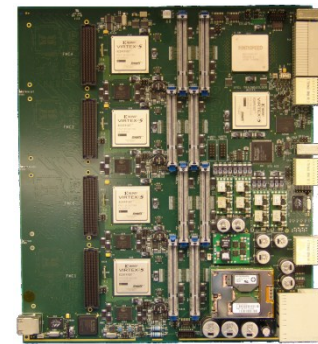
- Control and synchronization
 - Clock and Control RTM
 - Synchronized with Timing Receiver
 - One RTM controls a 1 Mpixel Detector
- Data reorganization and processing in Train Builder
 - Partial frames will be reassembled
 - A complete train put into memory
 - Transmitted via 10GbE to PC Layer
 - Dual 10GbE FMCs from DESY/FEA



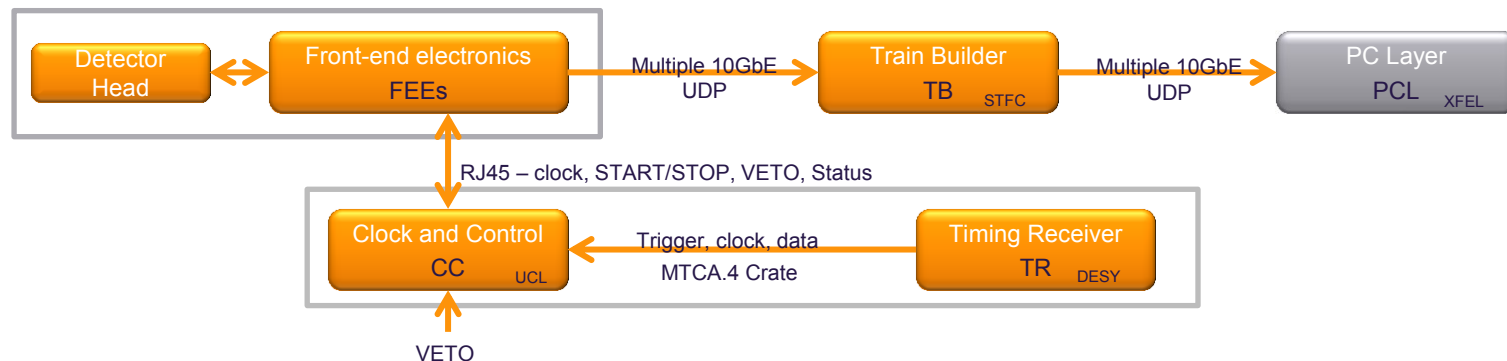
Clock and Control RTM (UCL)



DAMC2 (DESY/FEA)

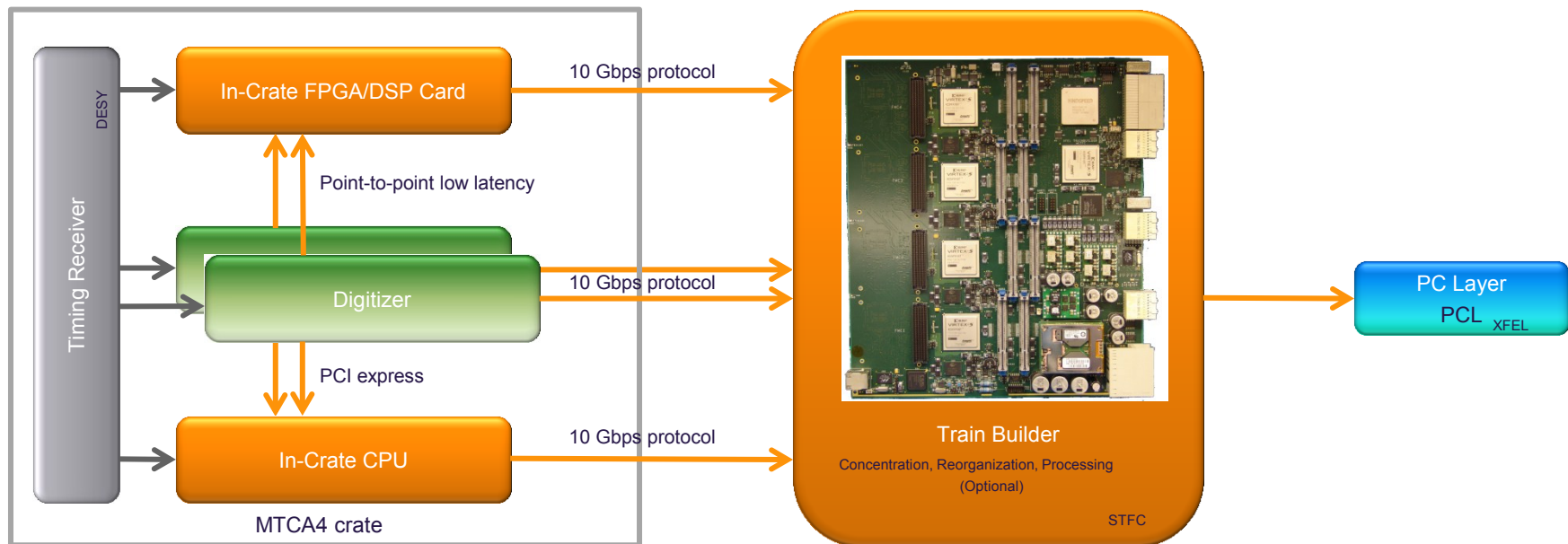


Train Builder ATCA Board (STFC)



Data processing and transmission concept

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In-crate processing

- In FPGAs of Digitizer
- In local CPU
- In a DSP/FPGA Board

Processing of multiple sources

- Processing in FPGAs
- Multiple Boards
- Communication between all FPGAs
- DDR and QDR Memory

PC Layer

- Software
- CPUs
- GPUs

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The big picture – DAQ and control part 2

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Experiment diagnostics

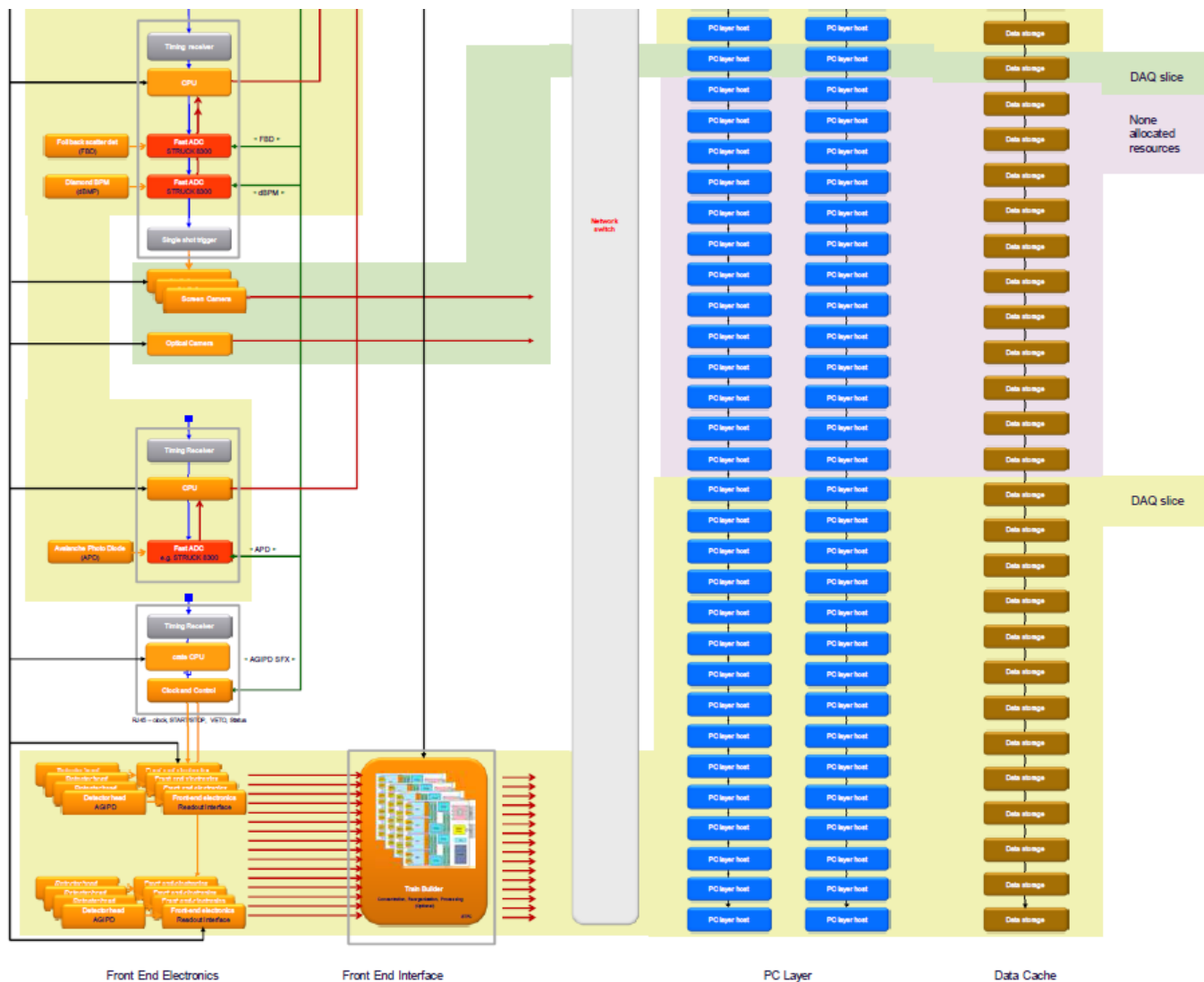
- BPM position monitors
- FBD foil back-scatter det.
- screen cameras
- optical microscope

Experiment VETO

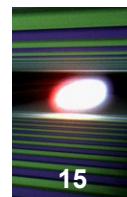
- fluorescence monitor
- ...

SFX large area camera

- AGIPD



DAQ layer:



- 10GbE interface rare on standard modules (PC, Digitizer)
 - Manufacturers thinking about adding it
 - Has to be requested in most cases
 - Add-on boards might be needed
- 10GbE provides a standard to stream data to FPGAs and PC
 - FPGA stages could be replaced with PCs for testing
 - COTS hardware available
- Bandwidth is sufficient for current sources but at limit
 - Future detector generations will require more
- Currently only UDP/IP implemented
 - Fine for FPGA → FPGA with no switch
 - TCP/IP via switch and to PC layer required/desired

Thank you for your attention!

Questions?