Industrial Participation in LLRF Control for the European X-FEL

S. Simrock, DESY

Overview

- Description of LLRF System
- Workbreakdown and Schedule
- Desired Contributions by Industry

Collaboration

DESY WUT-ISE TUL-DMCS PSI

also worldwide participation by
FNAL, KEK, IHEP, ORNL, JLAB ...

RF Control Requirements

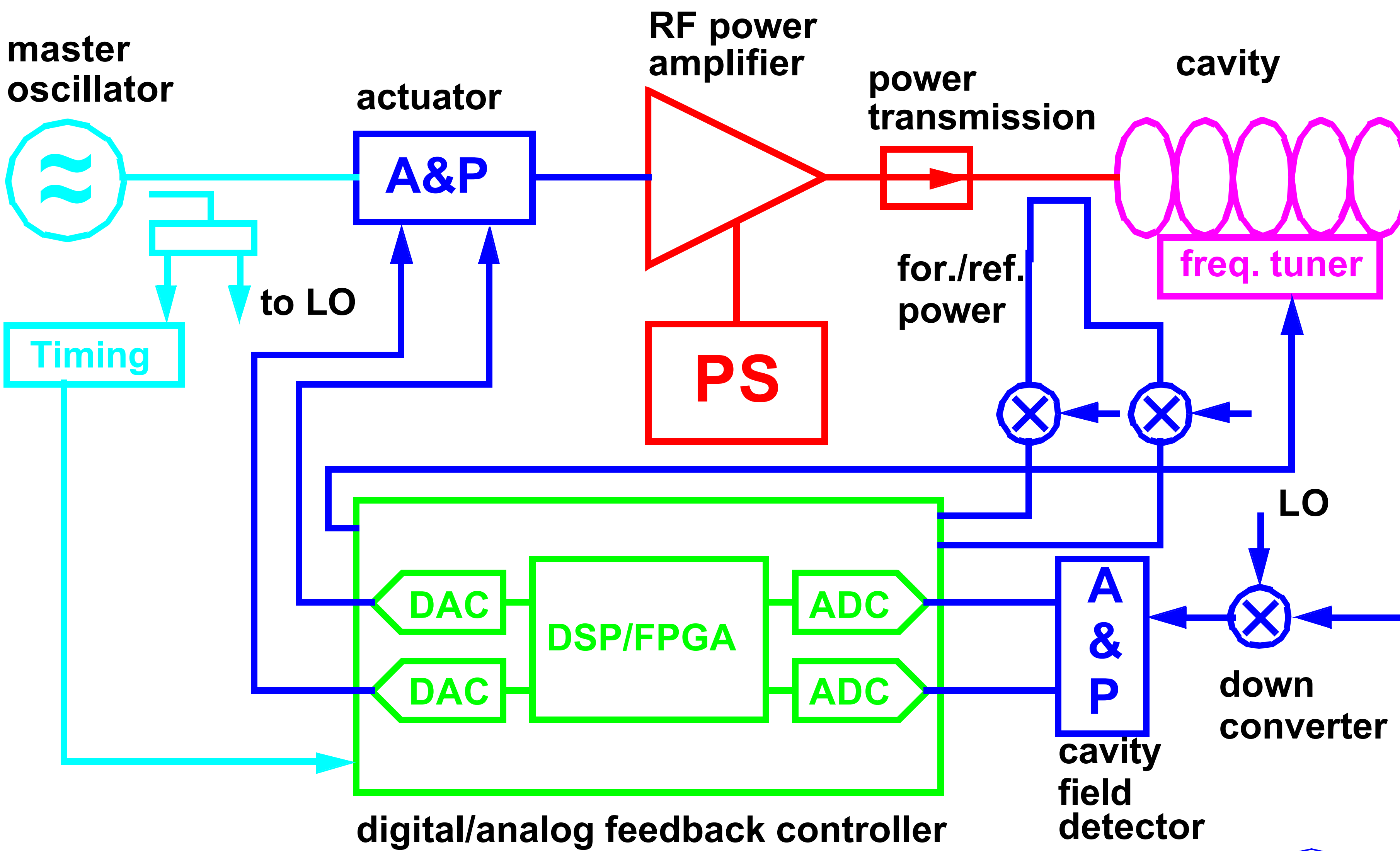
- Maintain Phase and Amplitude of the accelerating field within given tolerances to accelerate a charged particle beam

- Minimimize Power needed for control

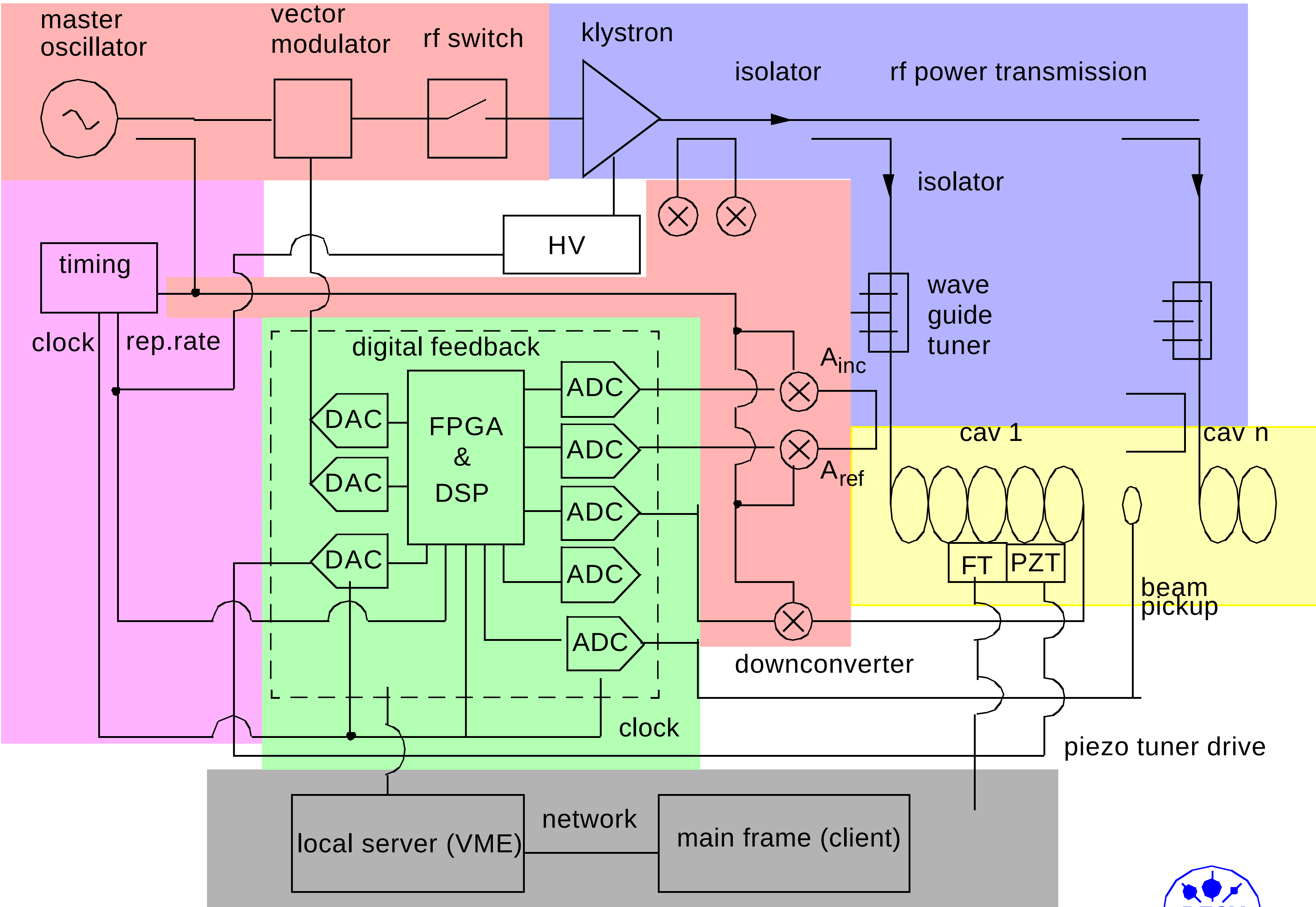
- RF system must be reproducible, reliable, operable, and well understood.

- Other performance goals
  - build-in diagnostics for calibration of gradient and phase, cavity detuning, etc.
  - provide exception handling capabilities
  - meet performance goals over wide range of operating parameters

RF System Architecture (1)



RF System Architecture (2)



LLRF Subsystem Hardware

- RF and Microwave components
  - M.O. and Frequency distribution
  - LO generation and ADC clock
  - Vectormodulator, rf switch
  - Down- and upconverter with level adjustment
  - Transient detection
- Timing (trigger and clocks)
  - Machine trigger
  - ADC clocks

LLRF Subsystem Hardware (C’ntd)

- Digital Feedback Hardware
  - Digital Signal Processing (FPGA,DSP)
  - Fast Analog IO (~100 in, ~50 out)
  - Digital in/output
  - Communication interfaces
- Piezo Driver
- Waveguide tuner control
- Crates, Racks, Cabling, Power supplies

LLRF Software

- Digital Feedback Code (VHDL, Assembler)
  - Gradient and phas calibration (rot. matrix)
  - state estimator
  - feedback algorithm / feedforward algorithm
  - exception detection and handling
  - loop phase and gain
  - klystron linearization
- Servers
  - DSP/FPGA (feedback/feedforward) server
  - LLRF monitor/calibration/ M.O./LO/rf distr., clock server,
  - Automation server
  - Other (WGT generation server, Piezo tuner, Motor tuner)

LLRF Software (C’ntd)

- Application Software
  - Adaptive Feedforward (synch. with beam)
  - System Identification
  - Detuning and loaded Q
  - Gradient and phase calibration
  - Beam phase measurement
  - Automated frequency tuning (motor tuner)
  - Piezo tuner control
  - Fundamental coupler Qext controlException handling

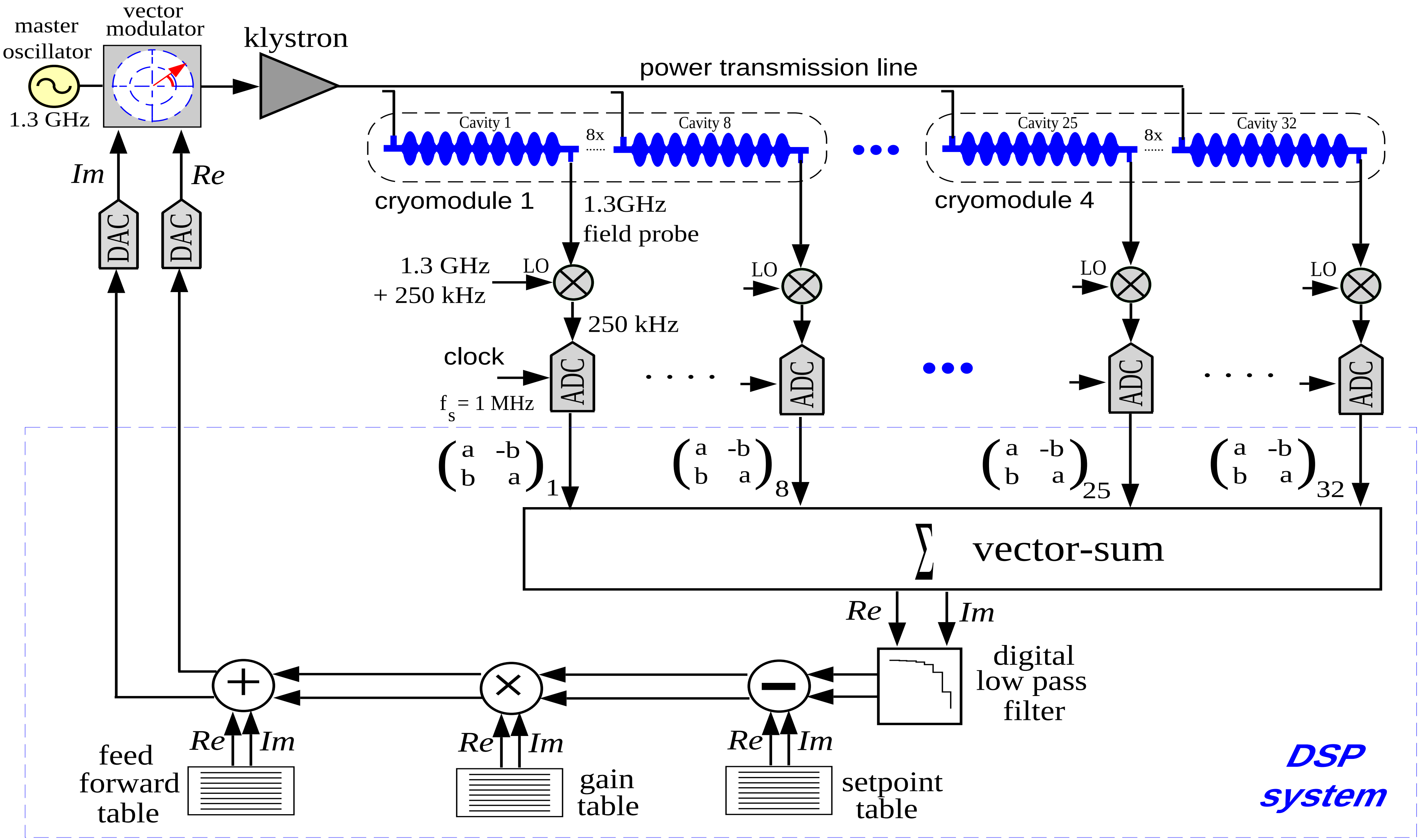
Other Issues

- EMC and EMI
- Radiation immunity
- Crates and Racks
- Packaging and Connectors
- Cabling
- Reliability
- Maintainability
- Cost vs performance optimisation
- RF System Modelling

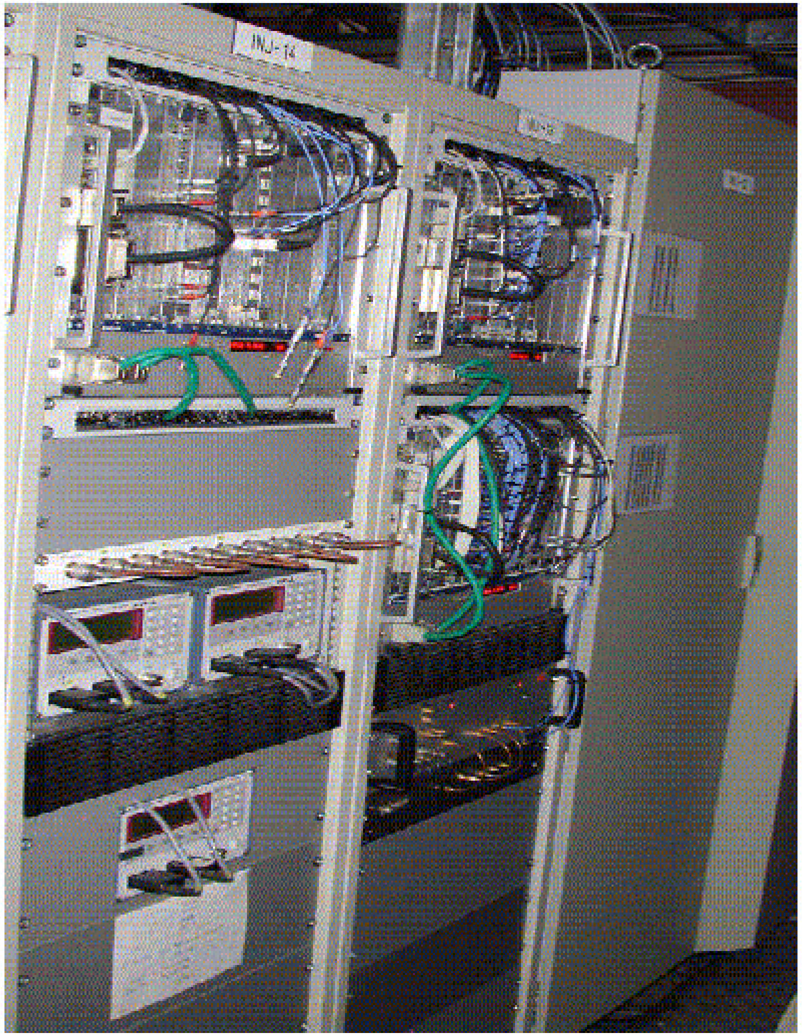
LLRF Tasks

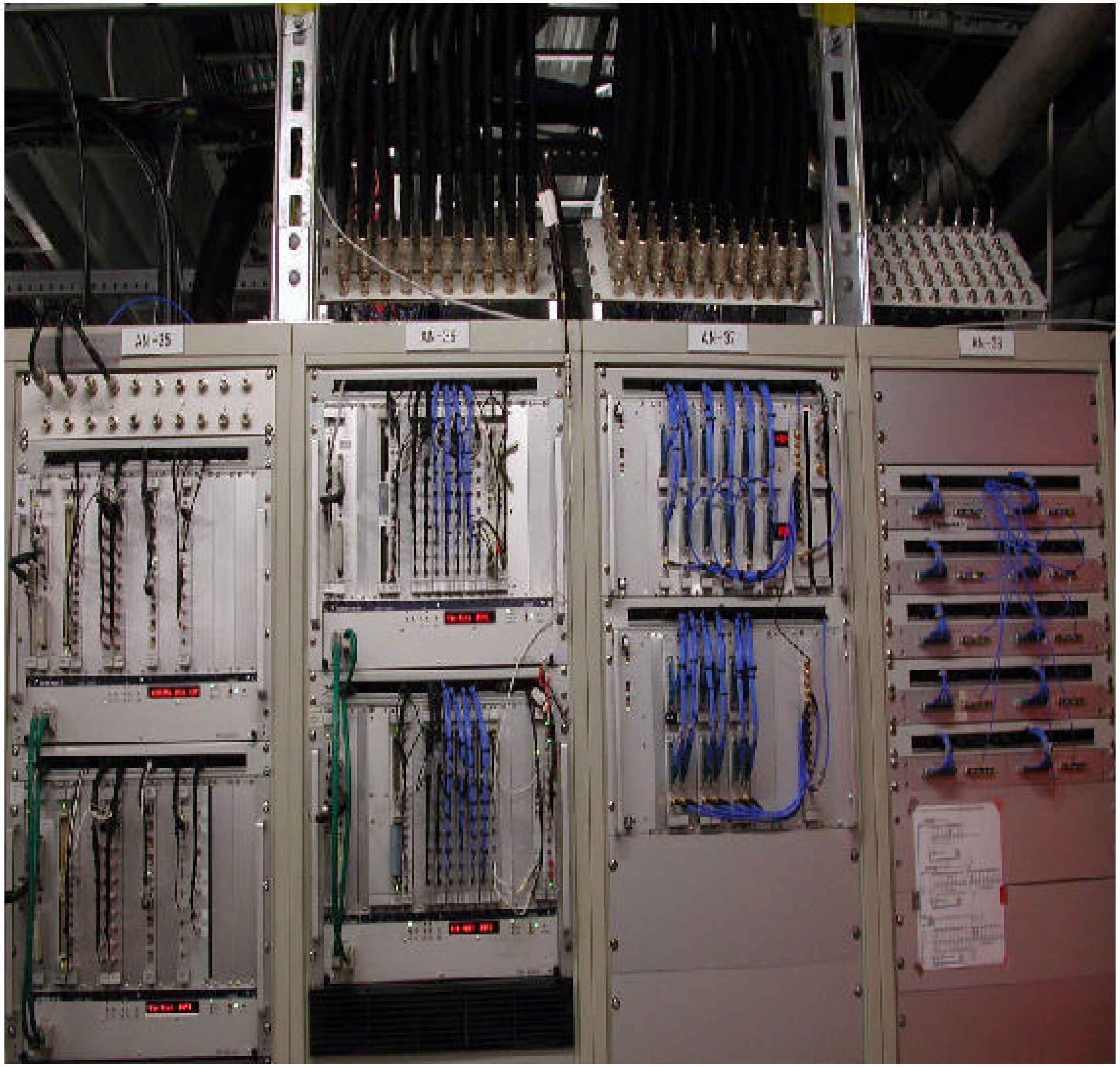
- Requirements
- Conceptual Design
- R&D Critical Items
- Detailed Design
- Prototype (Build, debug, prototype)
- Finalize Design
- Production
  - Procure Components
  - Production of boards
  - Assemble boards
- QA and QC boards
- Crates (ass., PS)
  - Inst. Boards, cabling, inst. Software, QA&QC)
  - Evaluate in Teststands, Burn-in
- Install in accelerator
- Commissioning
  - without rf power
  - With rf power
  - With beam
- Maint. (&upgrades)
- Documentation

Digital Control at the TTF

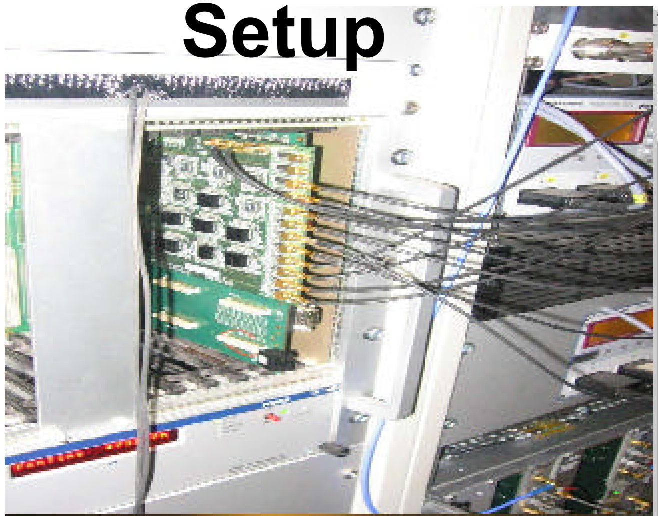


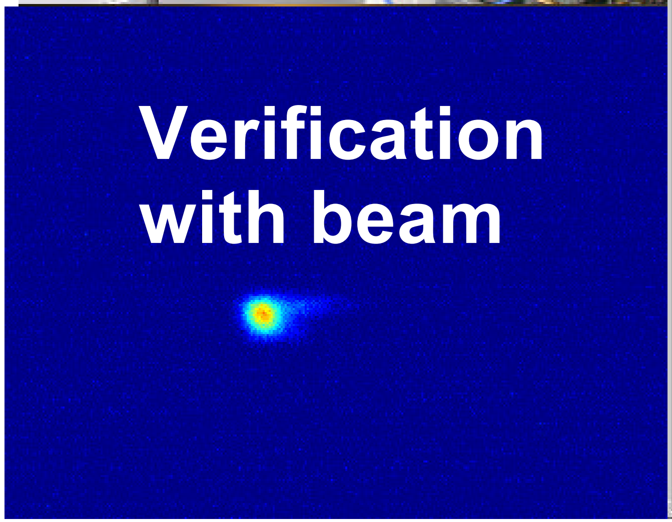
LLRF at the VUV-FEL

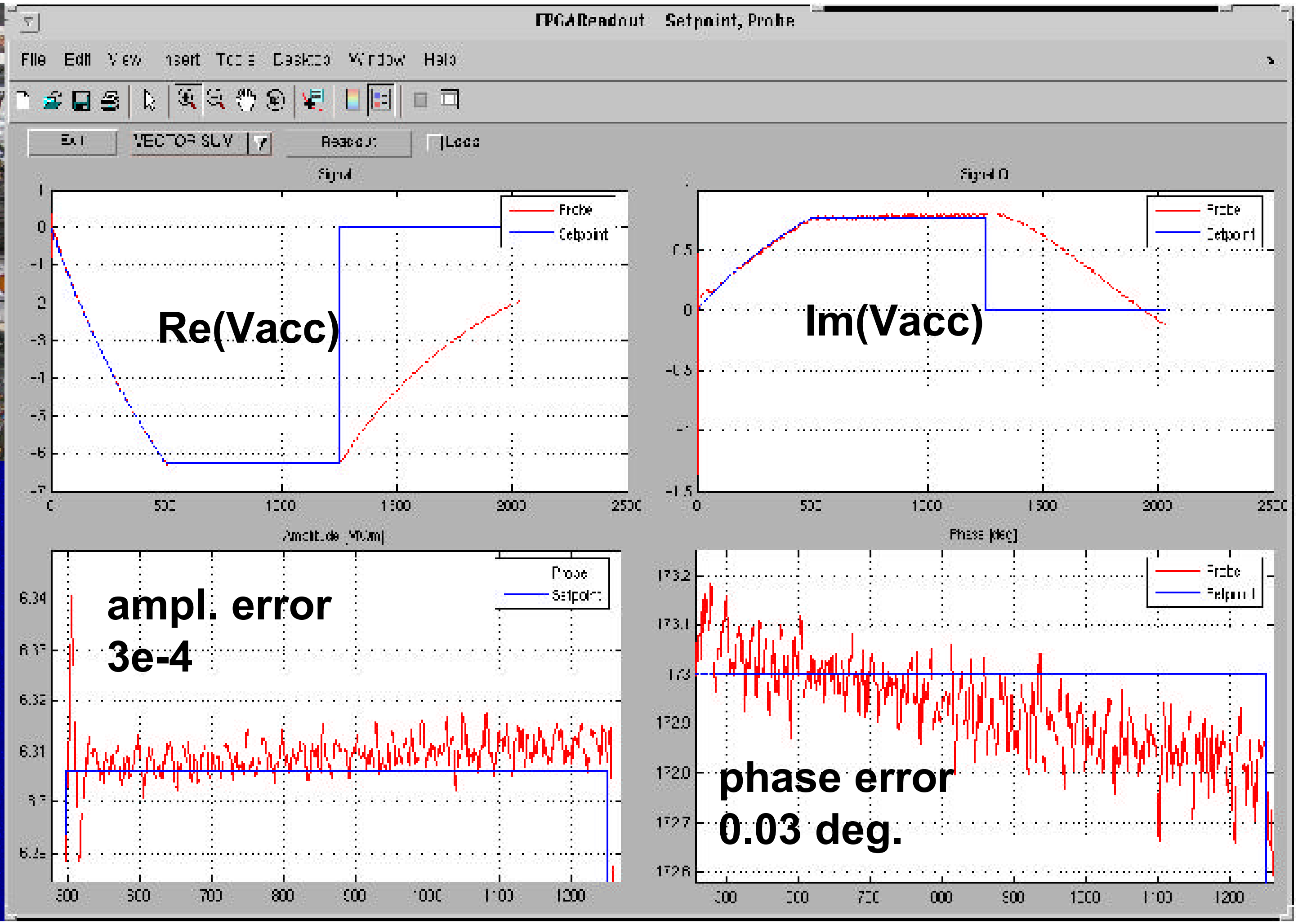




Performance of LLRF Verified at VUV-FEL with Beam







LLRF Work Topics for X-FEL

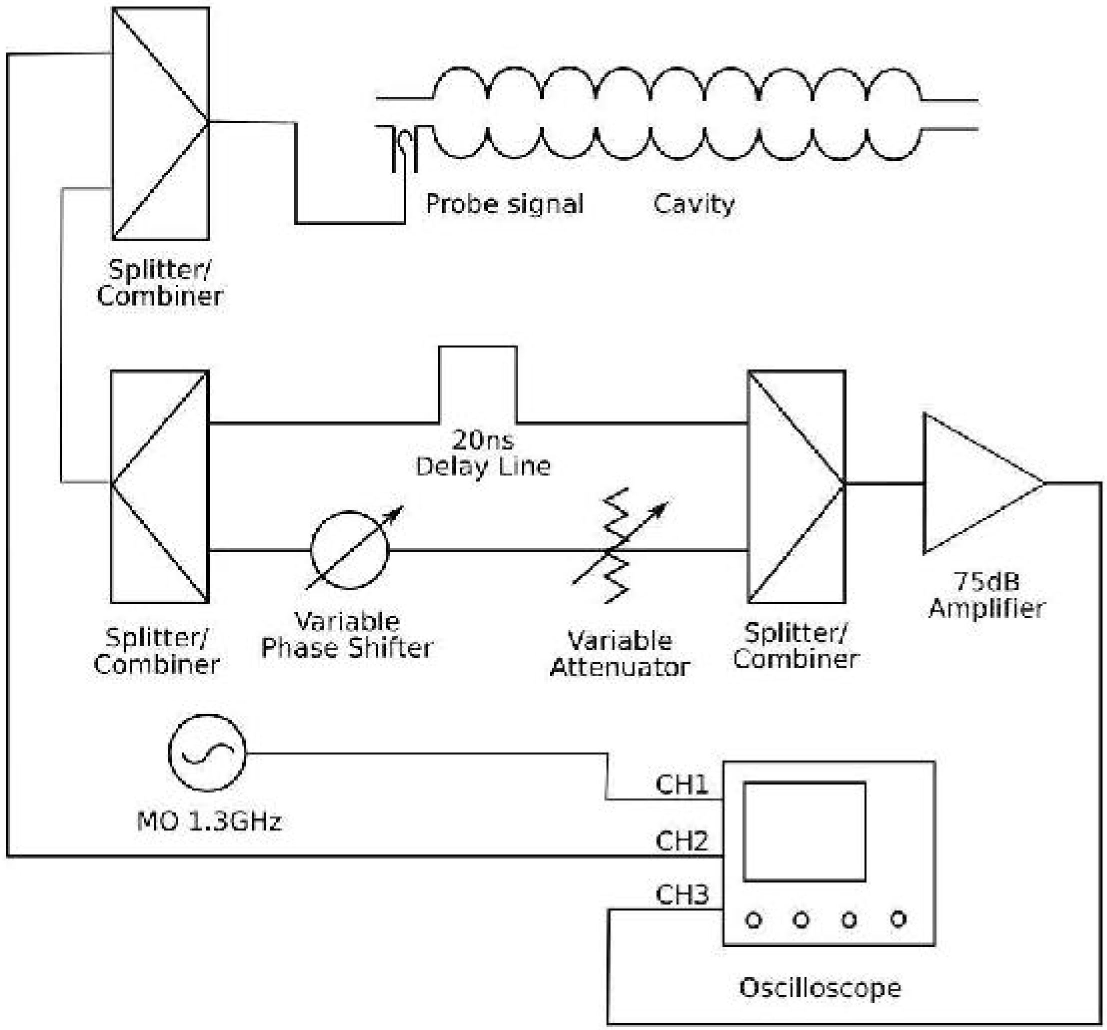
- Third Generation RF Control (WUT-ISE ...)
- Single Bunch Transient Detection (TUL-DMCS ...)
- Multichannel Downconverter (WUT-ISE ...)
- Stable M.O. and Frequency Distribution (WUT-ISE ...)
- RF Gun Control (PSI ...)

- Automation of LLRF Control (TUL-DMCS ...)
- Exception handling (DESY ...)
- Data Management Development (TUL-DMCS ...)
- Control Optimization (DESY ...)

- Cost and Reliability (DESY ...)
- Radiation Effects on Electronics (ALL)

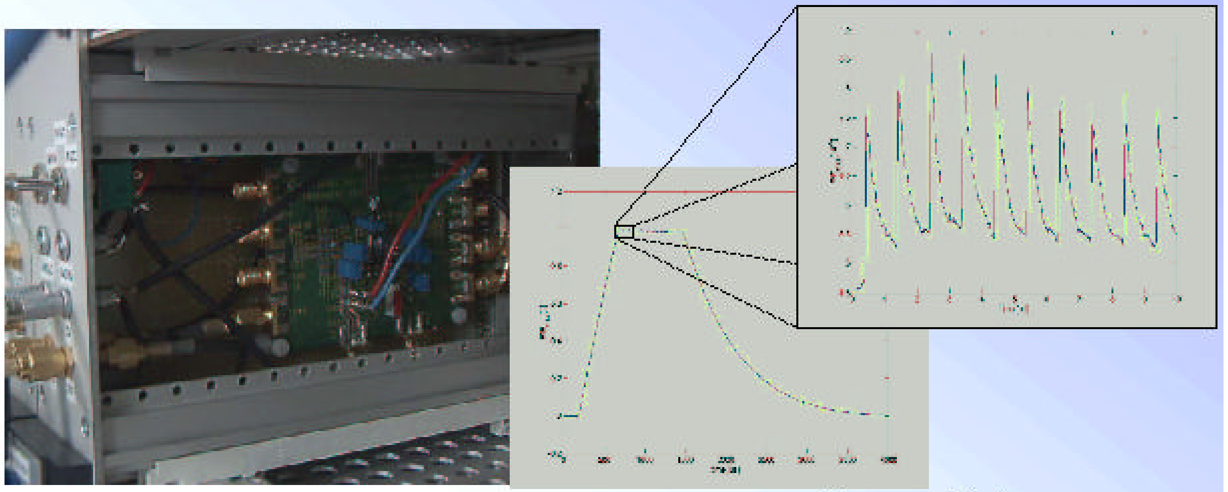
Single Bunch Transient Detection (1)

- Detection of transient of single bunch (1 nC)
  - with magnitude of about 2e-4
  - with a resolution of a few percent in amplitude and few degrees in phase.
- Conceptual idea: subtract delayed probe signal from original probe signal and amplify error
  - Transient vector is detected by fast sampling scope



Single Bunch Transient Detection (2)

- This requires development of new hardware (microwave, analog, digital)
  - with high bandwidth and low noise



Picture of the hardware

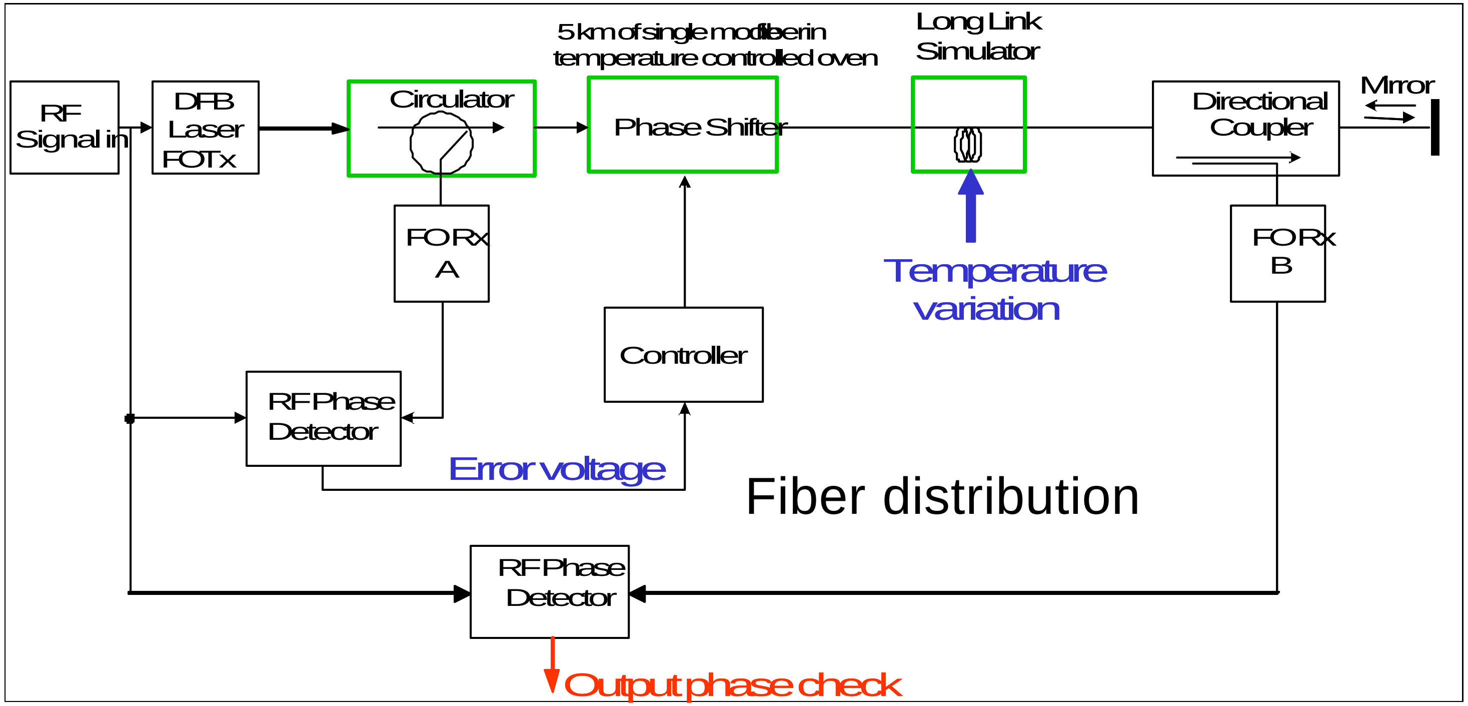
Measured data

- Demonstrated required performance close to thermal noise limit.

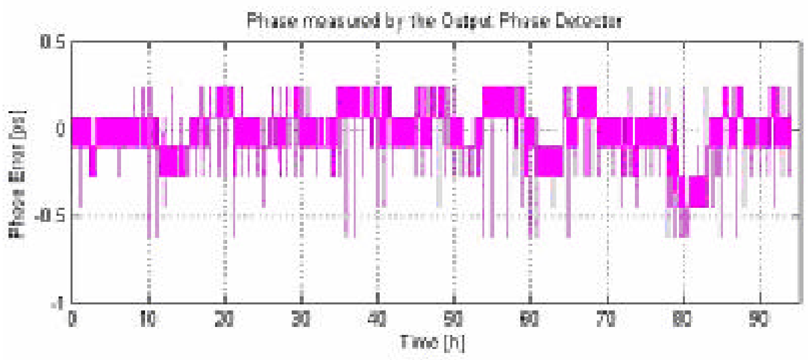
Beam Phase Set Point	Measured Phase	Measured Magnitude	Measured Beam Phase Error
-90,0	-90,9	4,19E-04	0,9
-45,0	-48,2	4,37E-04	3,2
0,0	1,7	3,95E-04	-1,7
45,0	41,6	4,09E-04	3,4
90,0	44,9	1,19E-04	45,1
180,0	35,6	8,92E-05	144,4

Highly stable frequency distribution (1)

- VUV-FEL, XFEL and ILC require a highly phase stable reference to
  - ensure that rf signals of laser, rf gun, and accelerating cavities are synchronized to better than 100 fs (short term) and 1 ps (long term)
- The proposed approach combines
  - a coaxial distribution system
  - with a fiber optic monitoring system.

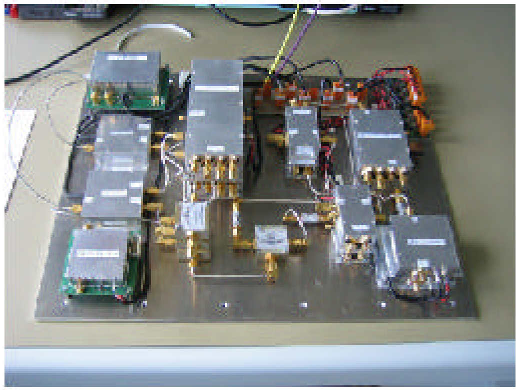


Highly stable frequency distribution (2)

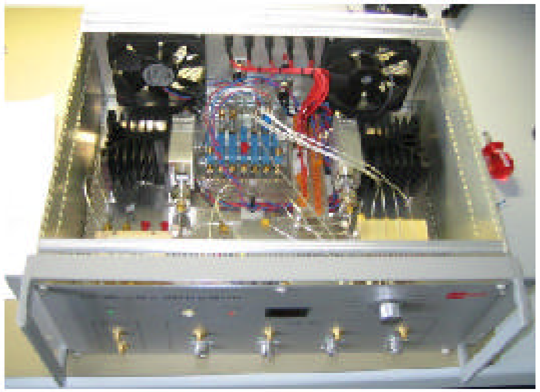


- Climate chamber for evaluation of temperature sensitivity of subsystems
- Short and long term error suppression

LOW POWER PART

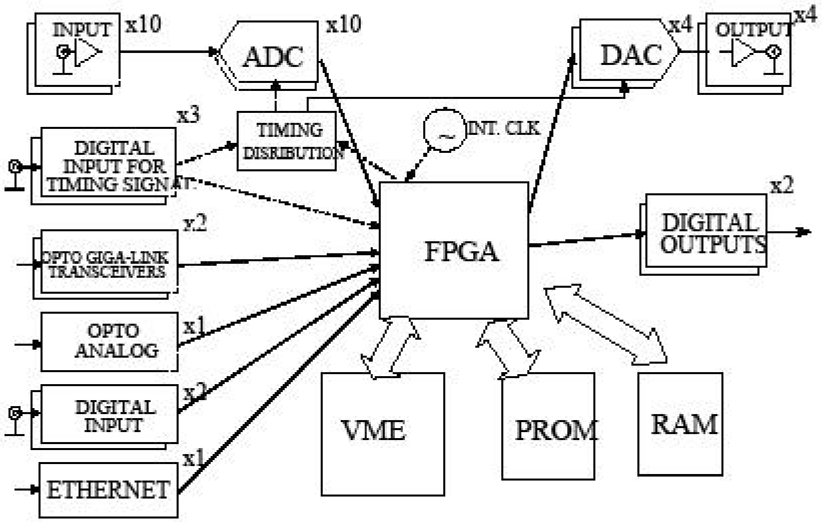


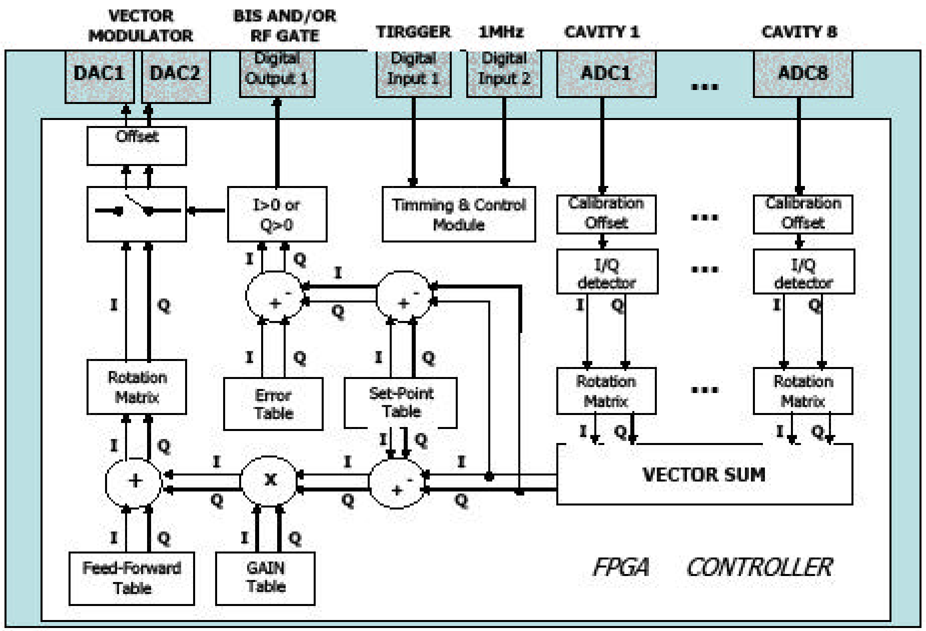
81 MHz POWER PART



- Master Oszillator with output for many frequencies

3rd Generation FPGA based RF Control (1)



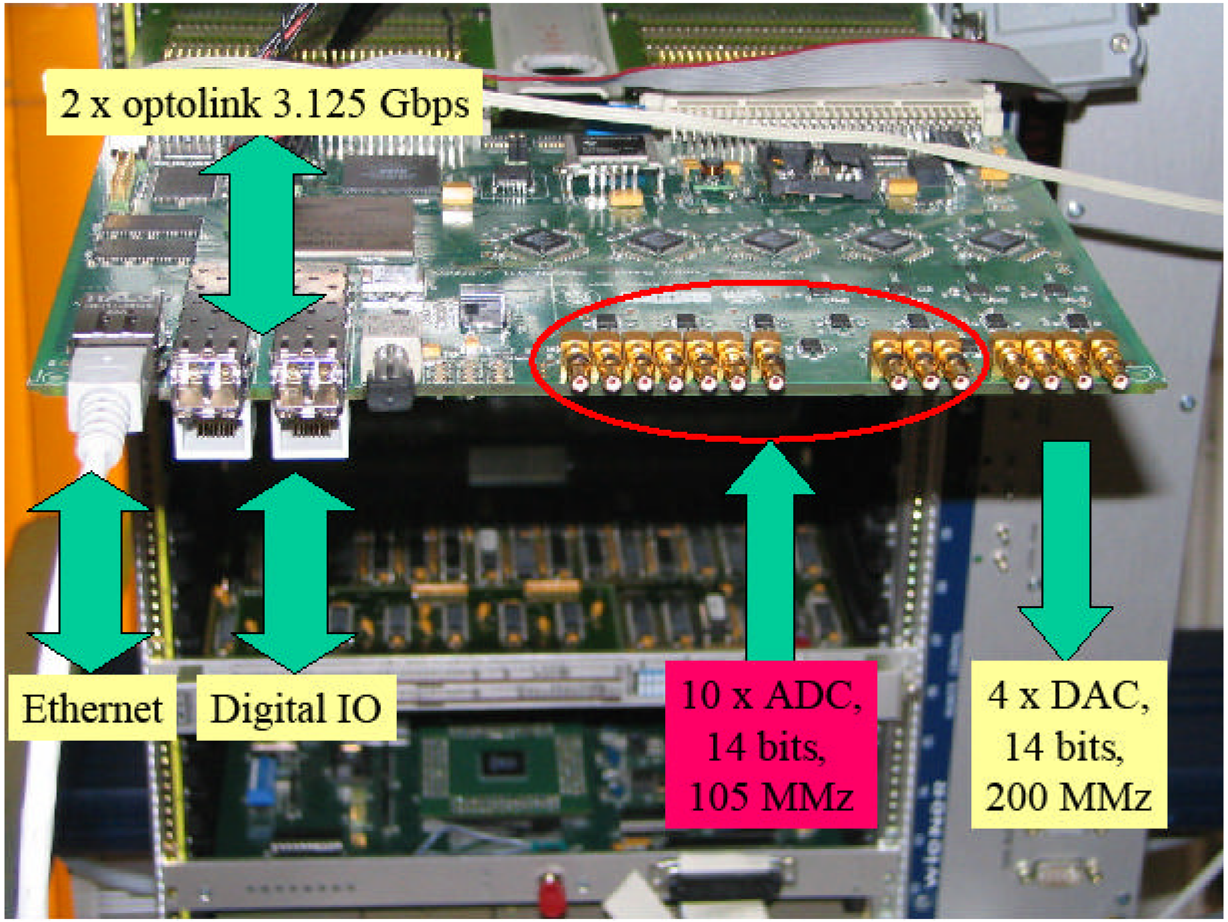


- Digital rf feedback systems for superconductind real time data processing
  - from a large number (up to 128) of ADC input channels and a smaller number (up to 64) DAC output channels.
- The latency from ADC clock to DAC output including all nec-essary data processing
  - should not exceed a few hun-dred nanoseconds.

3rd Generation FPGA based RF Control (2)

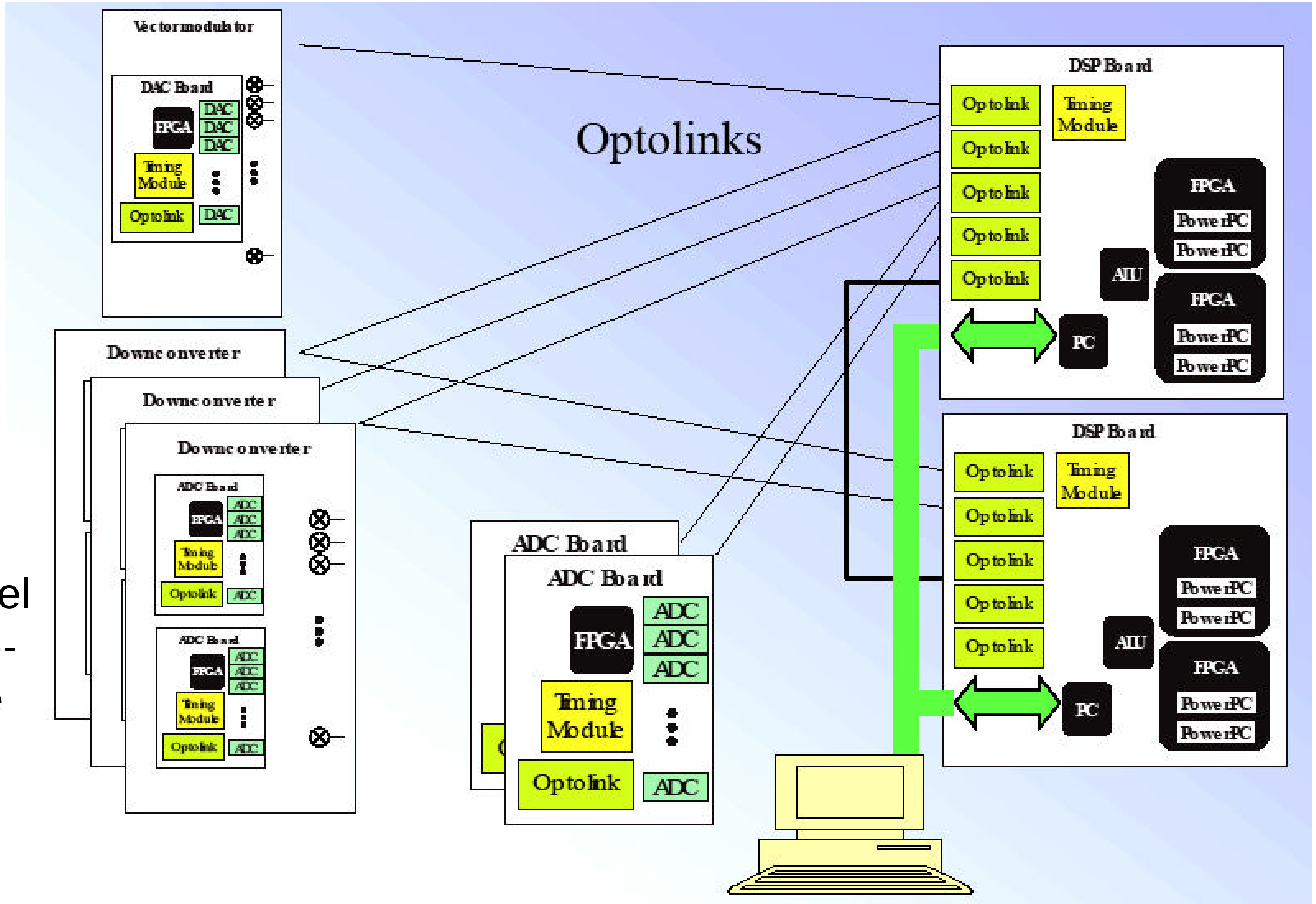
- FPGAs are well suited for this type of hardware due to their the large number of I/O pins, large number of logic cells, and large number of multi-plier cores which allow par-allel processing of data.

- Goal is to explore the feasi-bility of realization of digital feedback and feedforward algorithms, complex appli-cation algorithms, exception handling and built-in diag-nostics



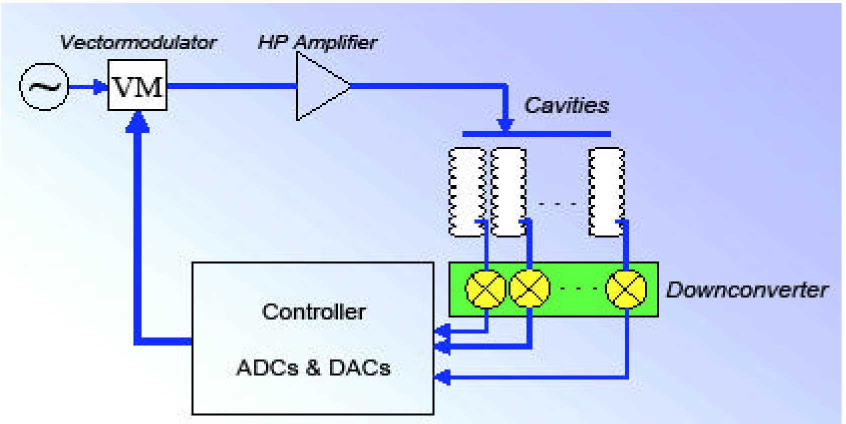
3rd Generation FPGA based RF Control (3)

- In future more distribution of subsystems connected by optical Gigalinks
- Example: Downconverters with analog I/O and preprocessing
- Issues for single tunnel operation are maintenance and moderate radiation levels



Multichannel downconverter (1)

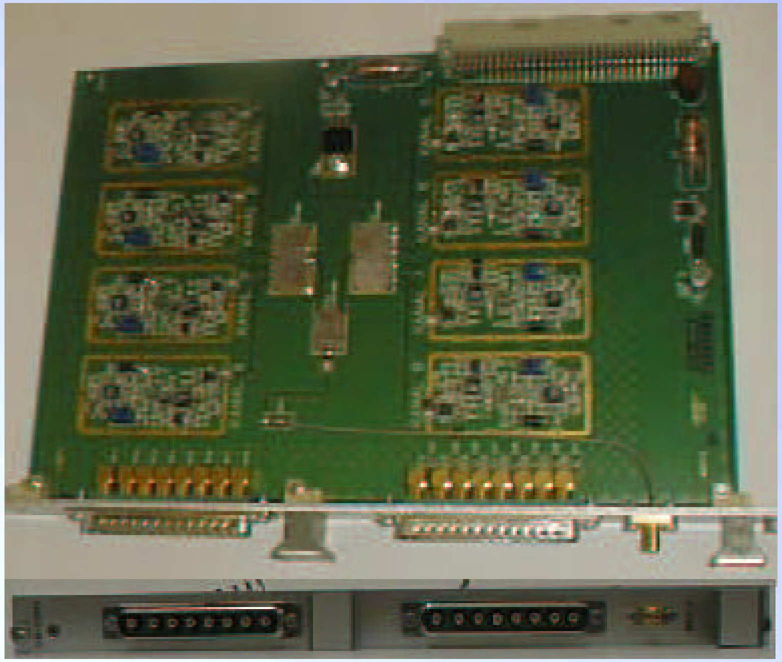
- Develop low cost and compact high-performance multichannel downconverter



Picture of 3rd generation downconverter.

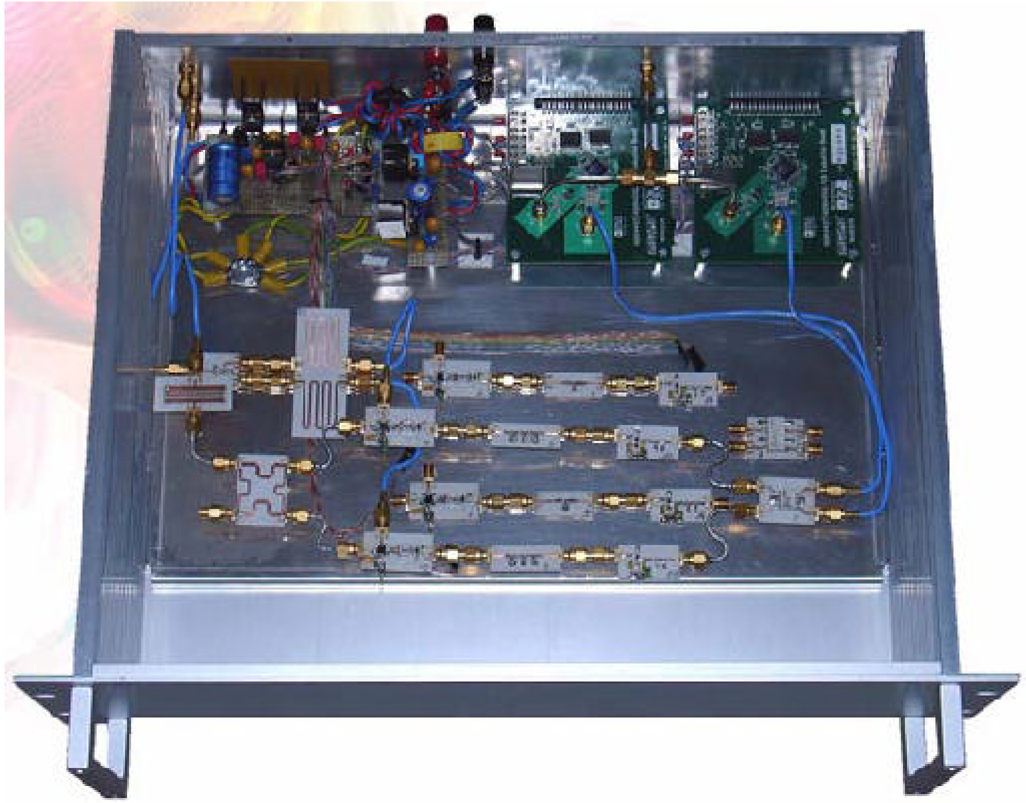
- 8 in/output channels, 1 LO input
- Linearity <-50dB
- Crosstalk between channels <-50dB
- LO leakage <-50dB @ 1.3GHz
- LO stability –15dB - –5dB

Design and assembly at DESY, layouting by external company



Multichannel downconverter (2)

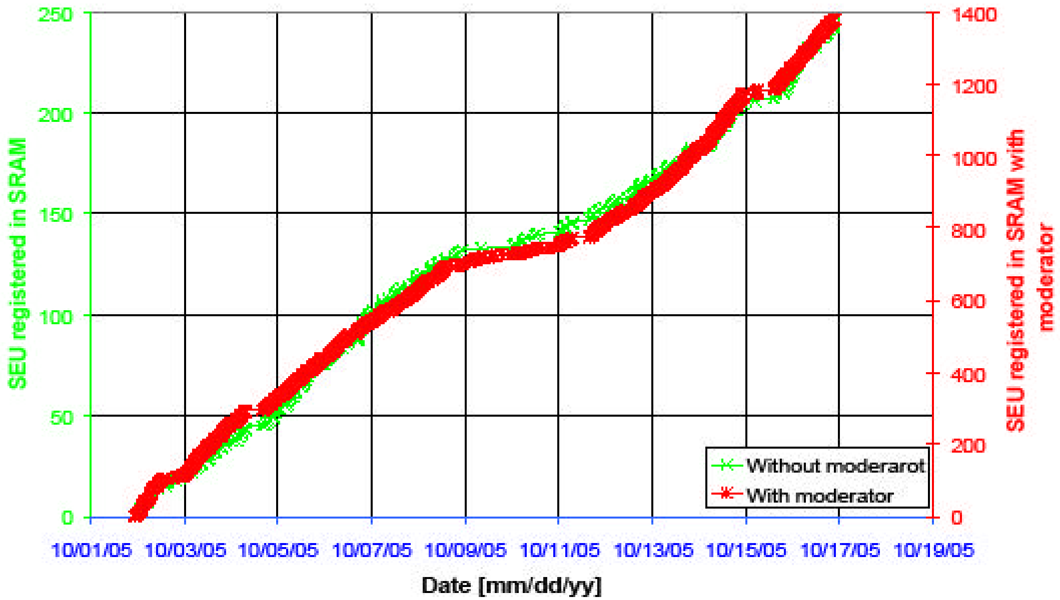
- Should include
  - remote controlled attenuators at rf inputs
  - RF outputs for transient detection
  - input for rf calibration signals
- Optional:
  - ADCs and FPGA for preprocessing on board and optical Gigalink to connect to main processor for control



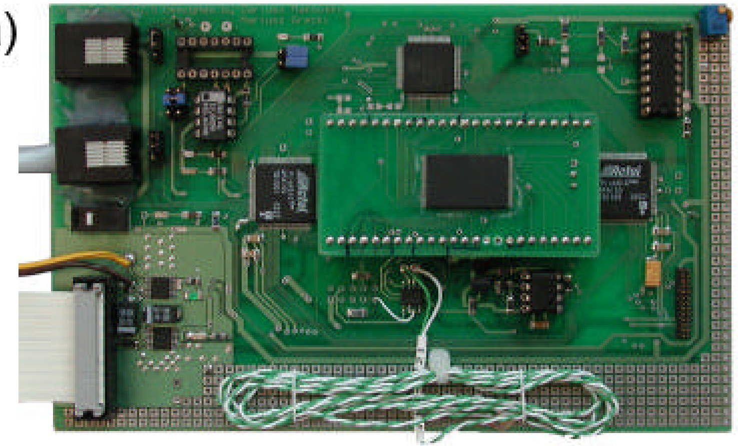
Study rad. effect on electronics (1)

- On-line, calibrated neutron and γ Dosimetry
- Dosimetry based on SEU in semi-conductors. Calibration with TLDs and Bubble Dosimeters

SEU registered in VUV-FEL



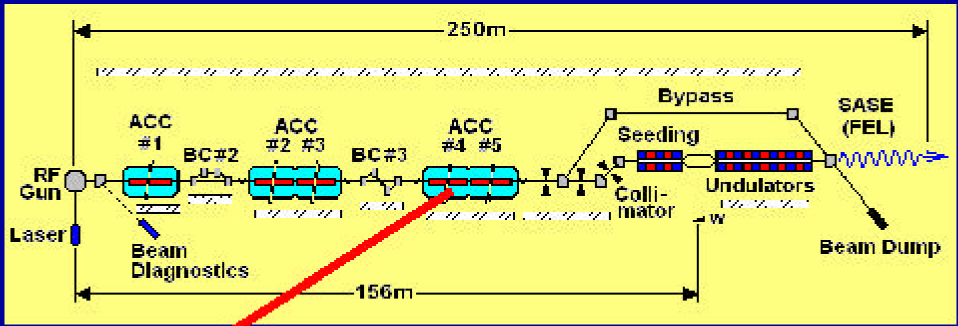
a)

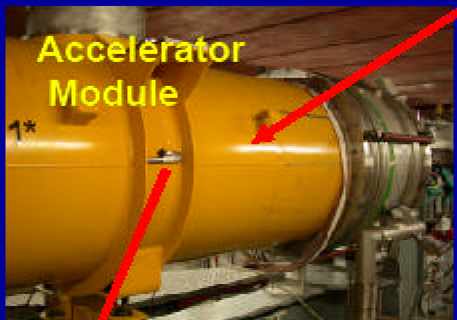


b)

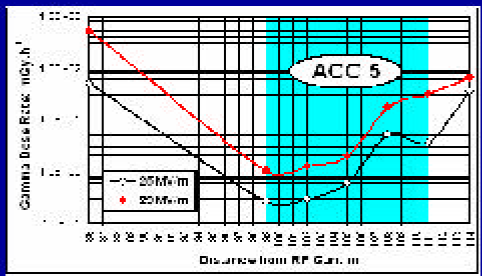
Study rad. effect on electronics (2)

- Radiation impact studies include performance degradation in analog circuits, single event effects in digital electronics, total ionizing dose effects leading to complete failure, and displacement damage.

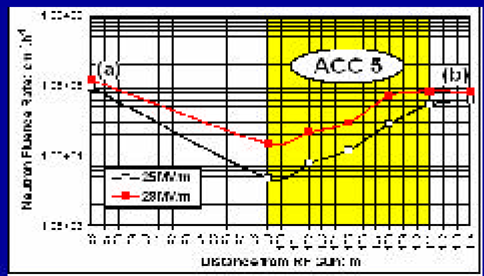




Neutron/Gamma
Dosimeter pairs



Gamma Dose Rate along the module tank, 0.5m from the module axis evaluated with PorTL (Al_2O_3) TLDs.

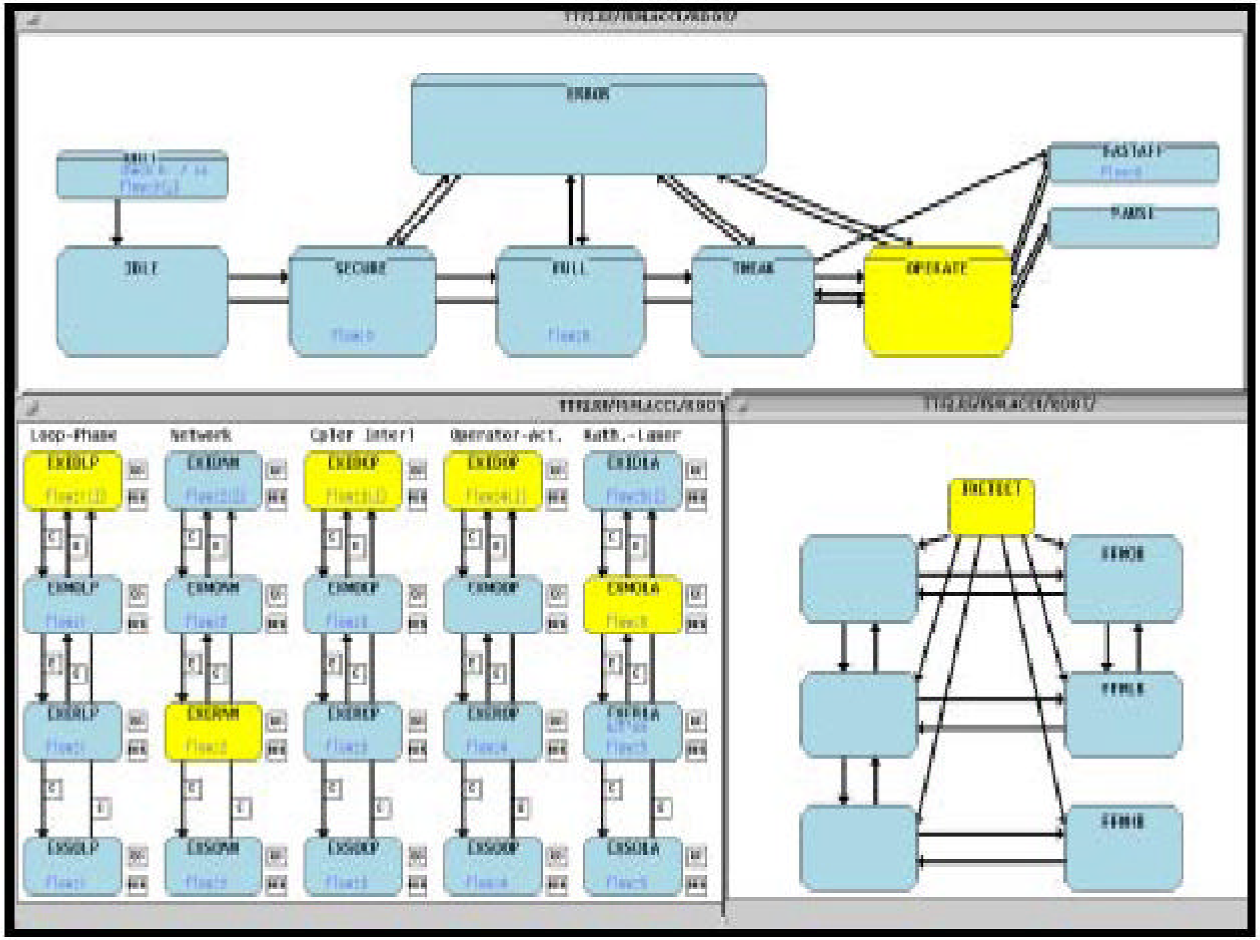


Neutron Fluence Rate along the module tank, 0.5m from the module axis evaluated with BDPND Superheated Emulsion (Bubble) dosimeters.

Finite State Machine (1)

- The automation of the LLRF system will be implemented in the framework of a finite state machine (FSM) which is a well established industrial standard.

- The first step will be the definition of the superstates, substates, flows, entry-, during-, and exit-procedures, entry conditions, timer and event triggered procedures etc..



Finite State Machine (2)

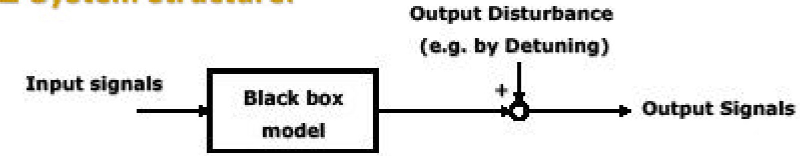
1. Offset Calibration
2. Loop Phase Determination
3. System Gain Determination
4. Predetuning of Vectorsum Estimation
5. Tuning of the Cavities
6. Adapt Feedforward
7. Synchronize ADCs of one RF Station
8. Calibrate DSP Matrices
9. Monitor Data Quality
10. Consistency Check
11. Interlock Reset
12. Calculate Detuning and Bandwidth
13. Adjustment of Waveguide Tuner
14. Momentum Management
15. Exeption Handling
16. Save and Restore Settings
17. History
18. Calibration of Forward and Reflected Power
19. Beam Phase Measurement
20. LO-Generator-Optimization
21. Track Frequency of RF Gun during Warm-Up
22. Klystron Linearization
23. Kryo Heatload Calculation
24. Hardware Diagnostics
25. Database with Calibrations
26. Database with Operational Limits
27. Adjustment of Amplitude and Phase
28. Close the Loop and increase Feedback Gain

- The next step is the description of the applications to be used by the FSM.
- Then the above functionality will be implemented as FSM server in DOOCS and the required application programs will be developed.

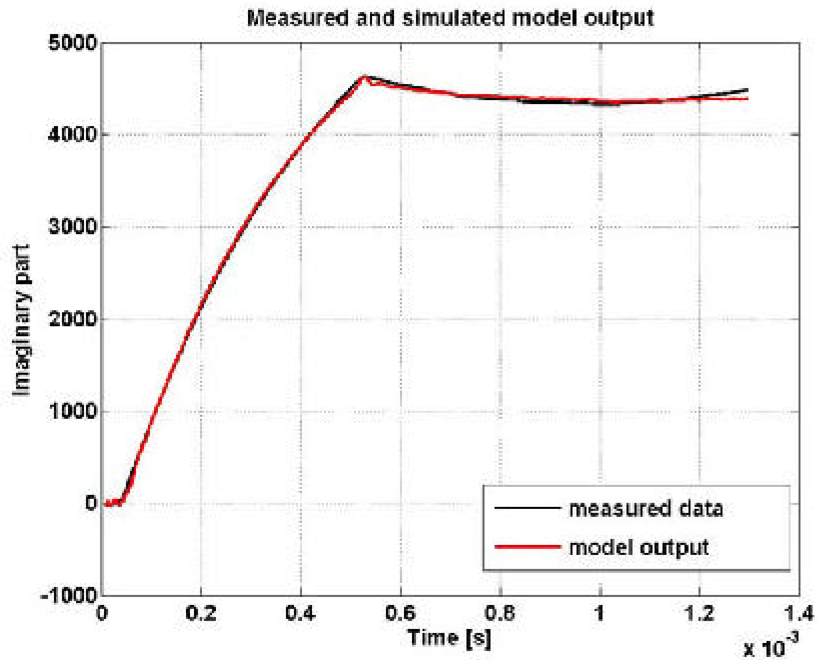
Development of optimal controller

- Modern control theory has developed established methods for the design of optimal controllers.
- The optimal controller should guarantee best performance and robustness in presence
  - of beamloading,
  - Lorentz force detuning
  - and microphonics
  - while operating close to saturation of the klystron and the performance limit of cavities and couplers.

- System identification:
  - Experimental based modelling
  - Excite system and record input & output data (open-loop)
  - Data analysis to infer a model with a choosen structure
- *Black box* model: Not physically interpretable
- System structure:

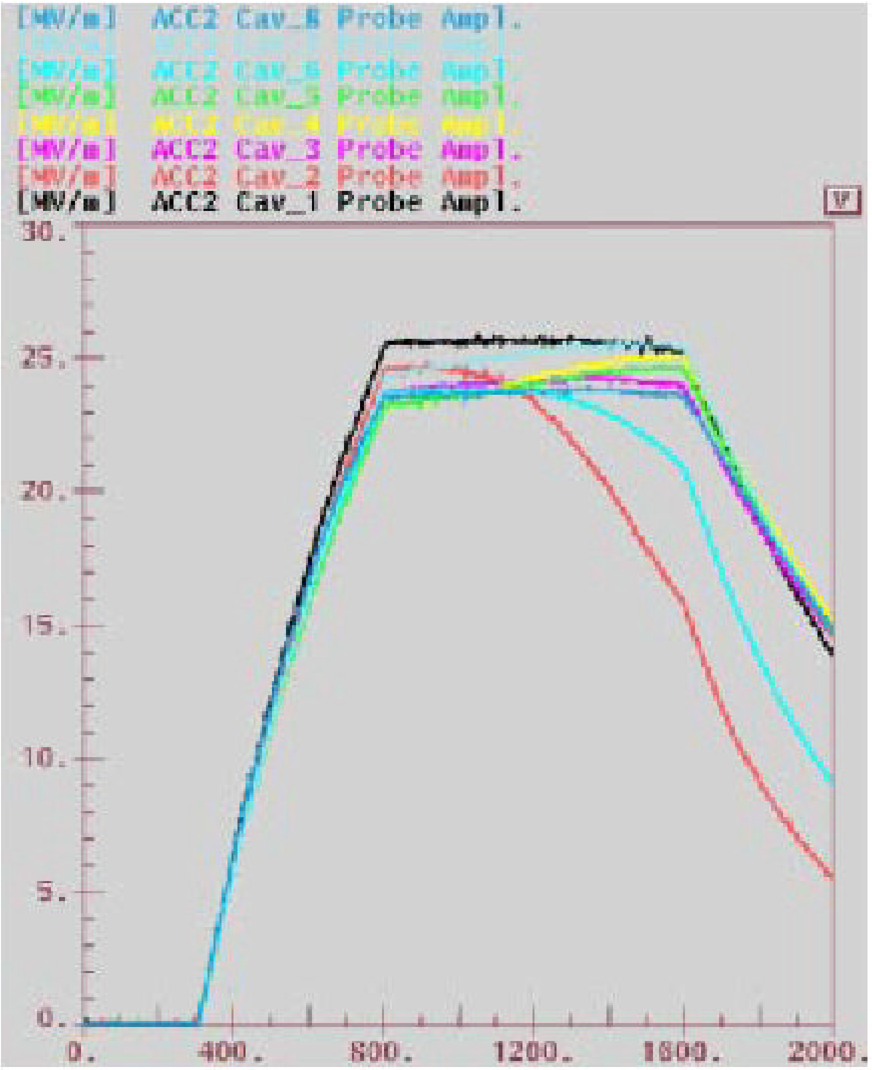


- Advantage: Model structure can be chosen appropriately for controller design



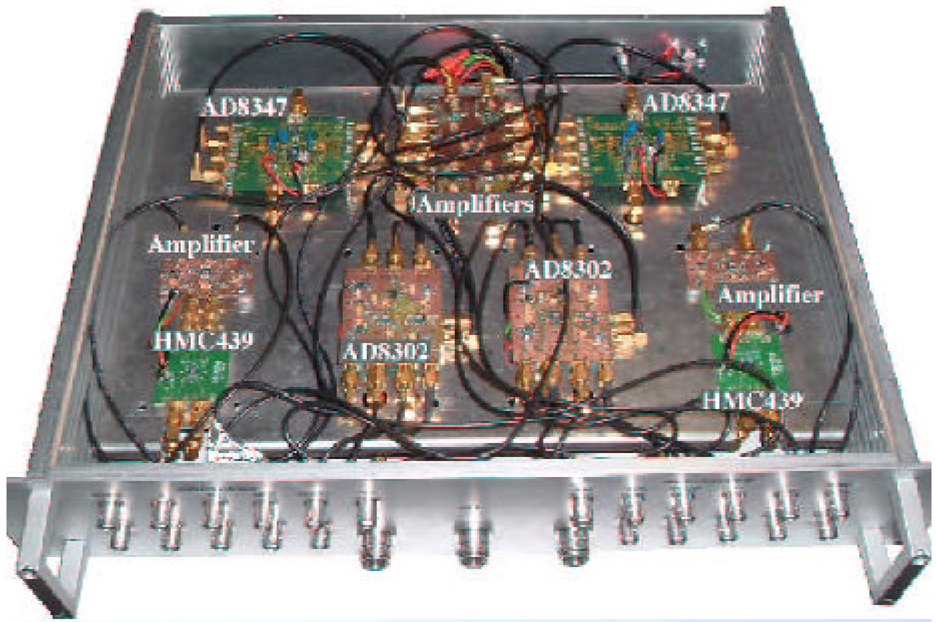
Exception handling

- Operation of superconducting cavities close to the performance limit will increase the trip rate due to the machine protection system.
- Typical trips include couplers sparcs, cavity quench, klystron sparcs or other faults caused by operation with high power.
- Prototype system evaluated successfully at the VUV-FEL with long pulse operation



Robust RF Gun RF Control

- The normalconducting RF gun requires special control considerations such as
  - low latency in the feedback loop
  - control for temperature of the of the rf gun resonator
  - and interlock scheme.
- Due to the lack of a field probe, the cavity field must be determined by a precision measurement of incident and reflected wave.
- Detuning measured during field decay



Design Optimization, Cost and Reliability

- High performance design using digital processing (FPGAs) and telecommunication components.
- Reduce cost of LLRF system by application of COTS.
- Redundant design where necessary
- Reliability studies on prototypes include EMI, thermal, and radiation effects.
- Software design using modularity, standardization, good specifications and documentation
- Built-in diagnostics for hardware and software

Performance ↑

Reliability ↑

Operability ↑

Maintainability ↑

AND

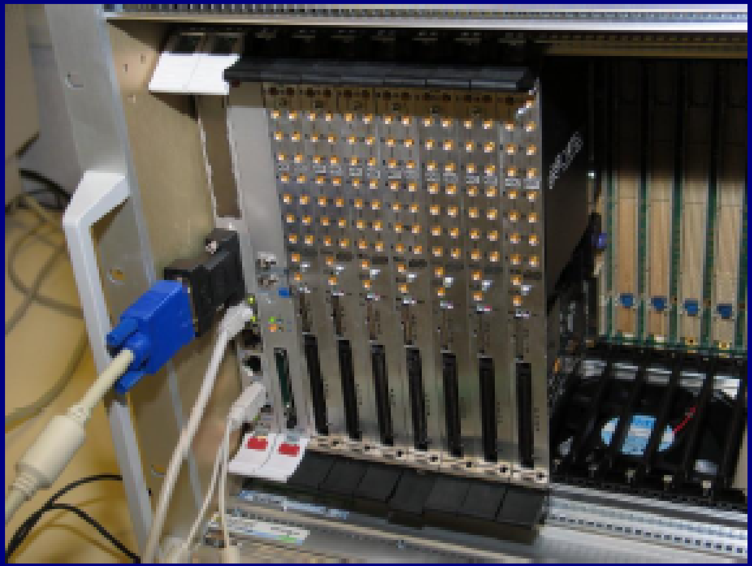
$$$$

Software **Hardware**

→ **$$**

Lyrtech Solution : 12 VHS-ADC cPCI boards

Implementation: Signal Processor



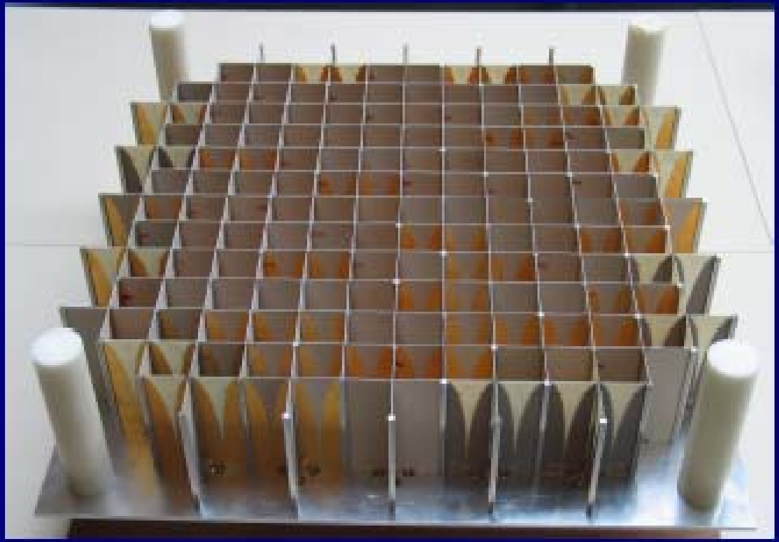
Lyrtech (www.lyrtech.com)

- ▷ 105 MS/s @ 14-bits
- ▷ 16 channels/card
- ▷ 128 MB RAM per card ⇒ 1 MHz BW for 4 sec
- ▷ One Xilinx Vertex-II FPGA per card
- ▷ Matlab/Simulink programming interface
- ▷ Goal to have 192 channels

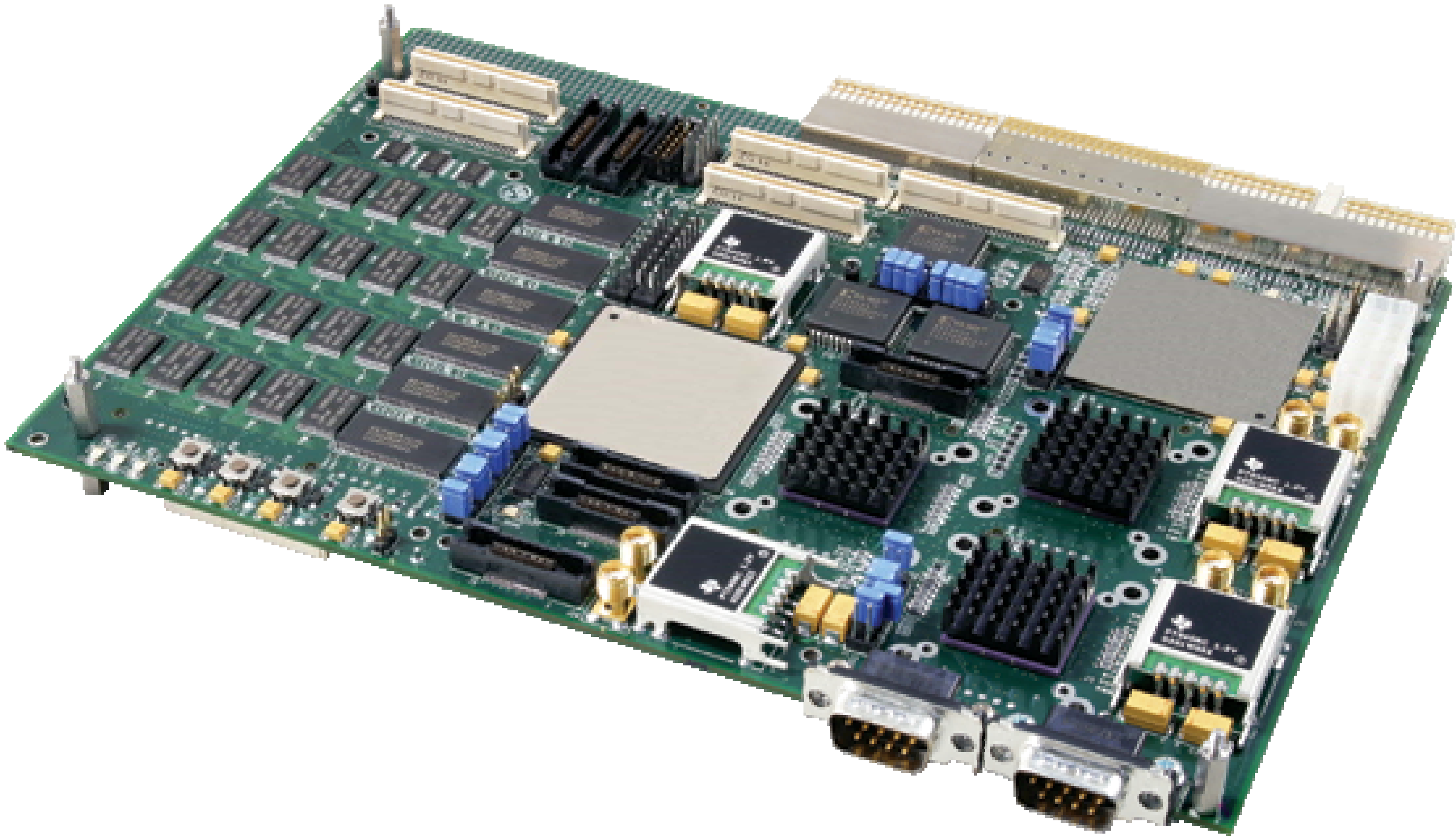
LYRTECH

Radio astronomy : 192 Phased Synchronous ADCs

Implementation: Antenna Array



- 1.8–6 GHz
- $\lambda/2$ spacing at 3 GHz
- minimum spacing $= \lambda/3$
- 742 mm × 742 mm
- 340 elements
- Scale design to 1–2 GHz

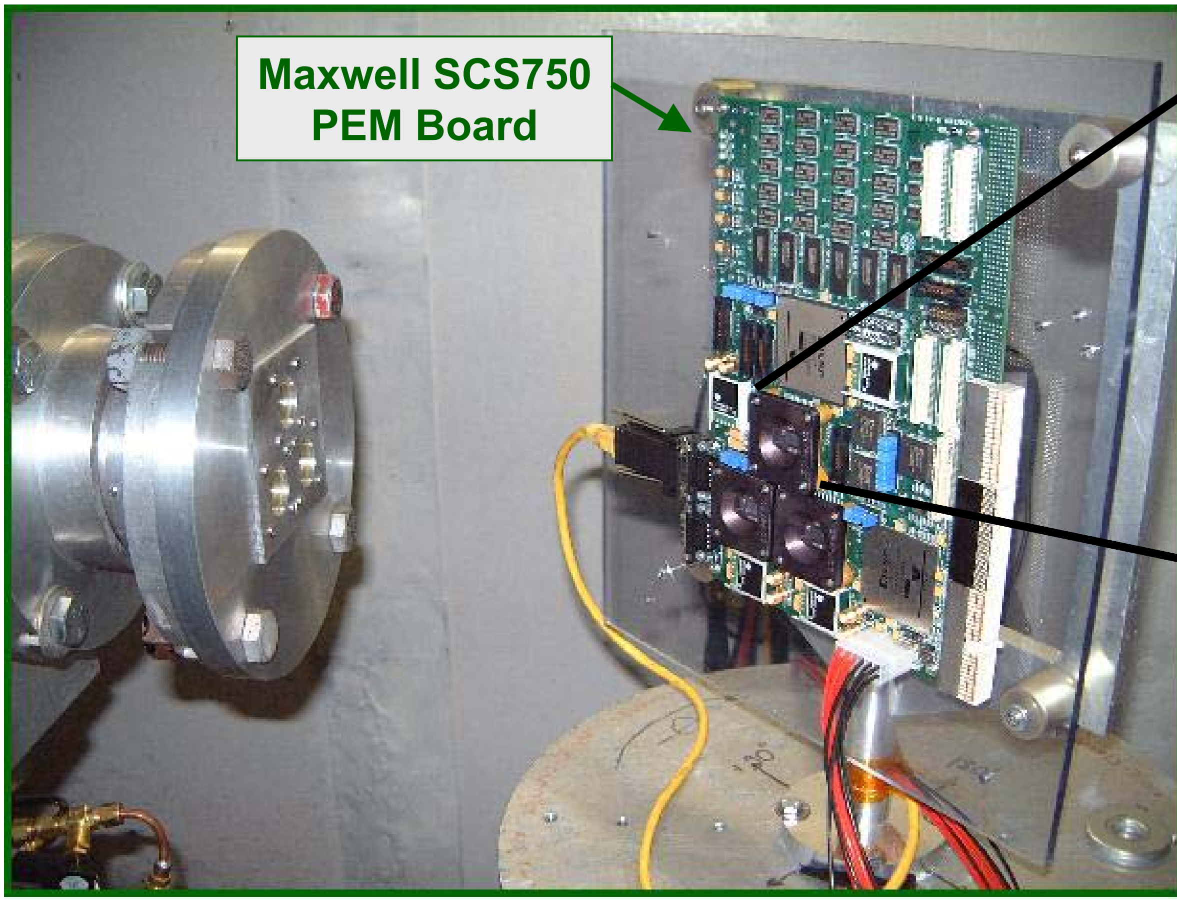


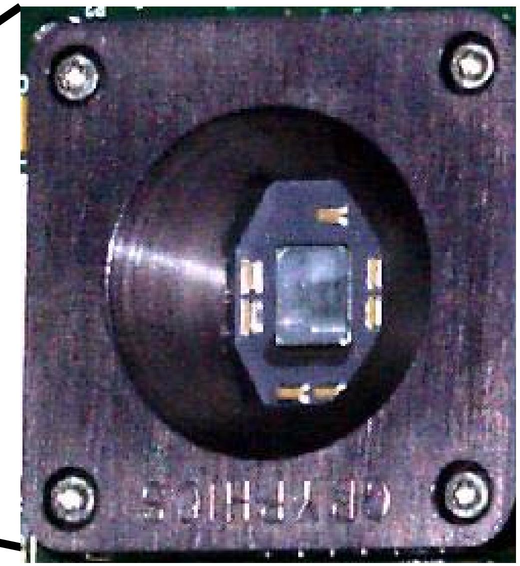
Prototype Engineering Module (PEM) – Early Dev. Platform

FM Boards will be conduction cooled with class S or equivalent components

Three Processor Test Setup

At the Texas A&M Cyclotron Facility:



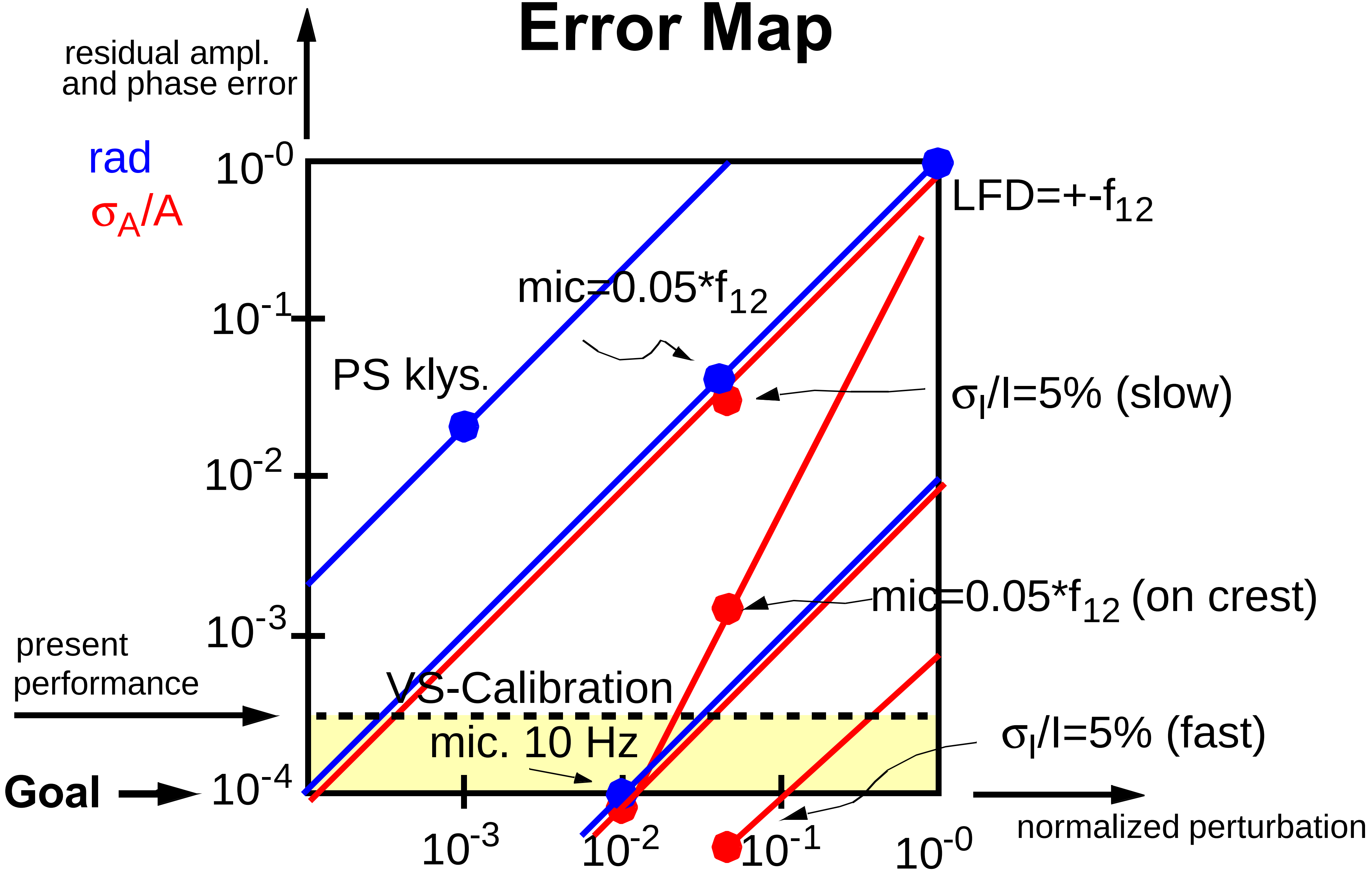


Achieving 0.01 deg. Phase Stability

- Short term (within in 1 ms pulse)
- medium term (pulse to pulse, several seconds)
- long term (thermal time scale, minutes to hours)

- Sources of cavity field perturbations
  - Lorentz force detuning
  - Microphonics
  - Beam loading
  - other (electronic noise in field detectors, phase noise and drifts of phase reference, ripple of klystron power supply, etc.)

Error Map


residual ampl.
and phase error
rad
σ_A/A
10^{-0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
present
performance
Goal
LFD=+-f_{12}
mic=0.05*f_{12}
PS klys.
σ_I/I=5% (slow)
mic=0.05*f_{12} (on crest)
VS-Calibration
mic. 10 Hz
σ_I/I=5% (fast)
10^{-3}
10^{-2}
10^{-1}
10^{-0}
normalized perturbation

LLRF Subsystems/Components Susceptible to Failure

- o RF phase reference
  - - from main driveline
  - - LO for downconverter
- o Timing System
- o Vector modulator
- o Downconverter
- o Digital Control (Fdbck + FF)
  - - ADC, DSP, DAC
  - - includes exception handling
  - - Redundant simple feedforward
  - - Redundant monitoring system
- o Transient detection
- o Interfaces to other subsystems
  - - includes interlocks

- o Waveguide tuner and controls
- o Cavity resonance control
  - - slow (motor) tuner
  - - fast (piezo) tuner
- o CPU in VME crate
- o Network to local controls
- o Cabels and connectors
- o Power supply for electronics
- o Airconditioning in racks
- o Software
  - - DSP (FPGA) code
  - - Server programs
  - - Client programs
  - - LLRF Parameters
  - - Finite State Machine

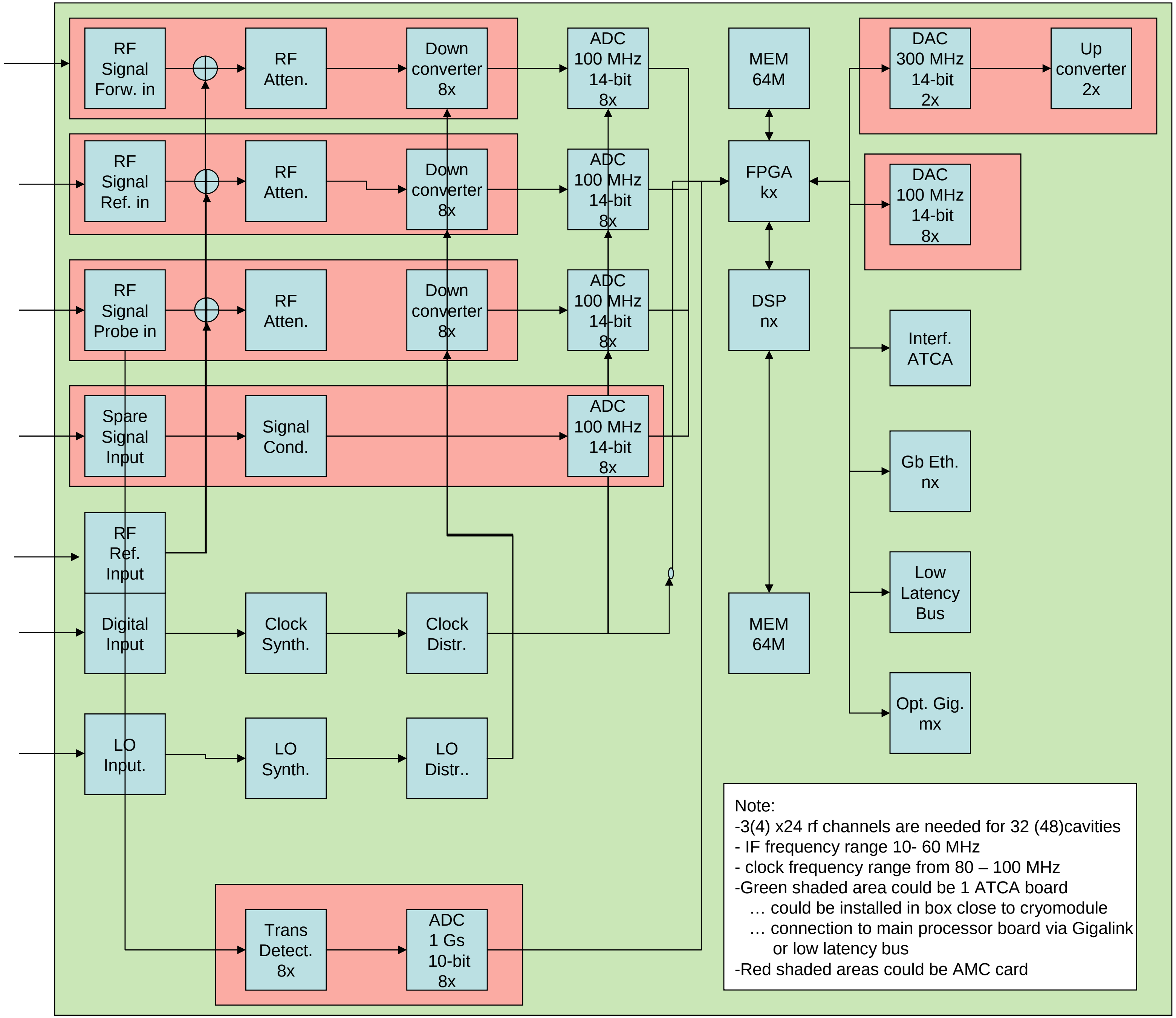
What can industry do ?

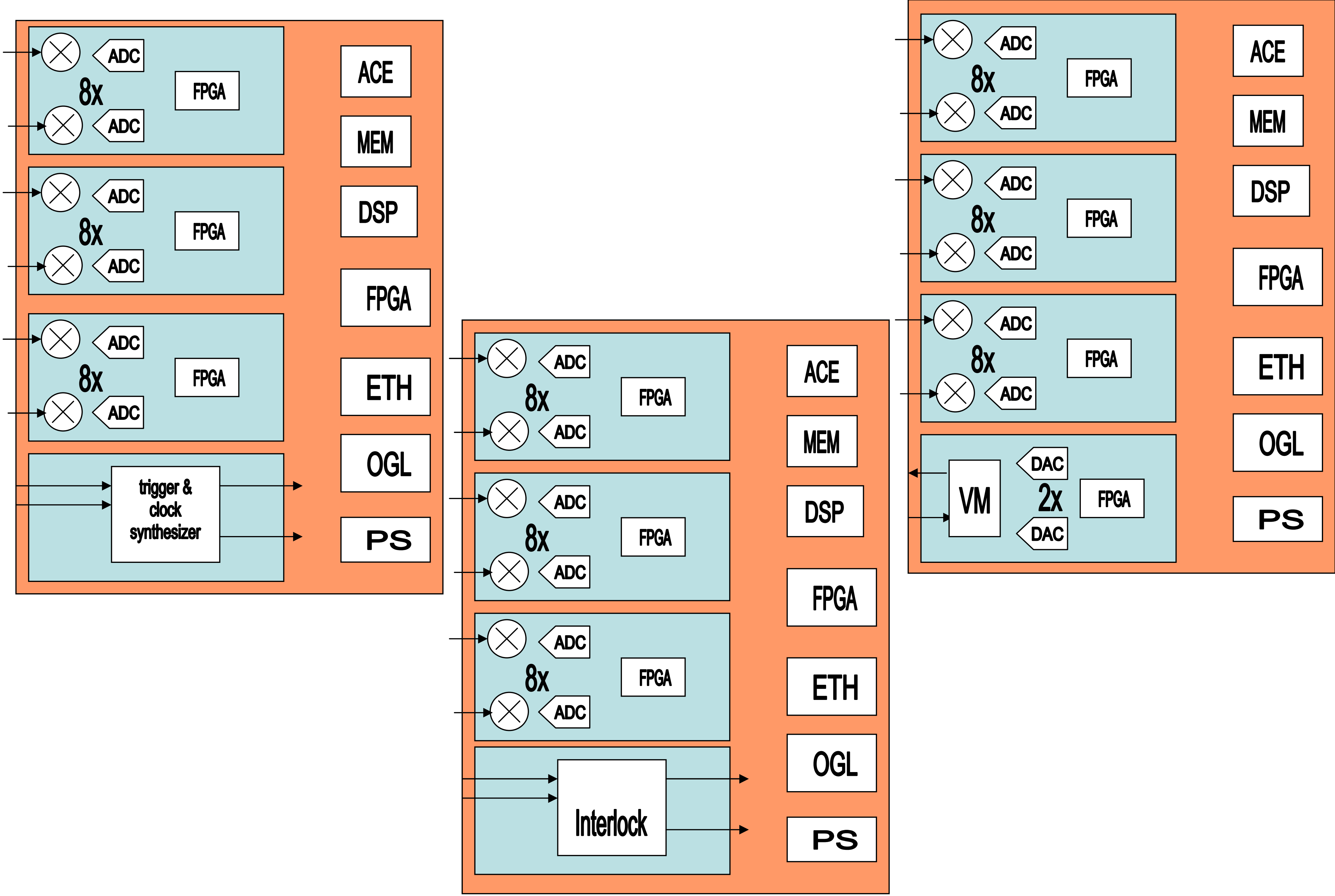
- Manufacture:
  - PC-boards, procure components, assemble boards
  - Crates, racks, power supplies
  - Cabling, cable assemblies
  - QA & QC, burn-in
- Supply
  - Components
  - Custom of the shelf (COTS) hardware
  - Customized hardware
- Design
  - Conceptual designs, architectures, standardization, choice of components and technologies
  - Detailed designs
    - PC boards (analog, digital, rf/microwave)
    - Spezialized hardware (e.g. master oscillator)
    - Packaging (crates, racks, rf shielding, airconditioning)
- Installation
  - crates, racks, cabling, power distribution
- Reliability estimates
- Software development ???
- CAD support, Documentation
- Maintenance

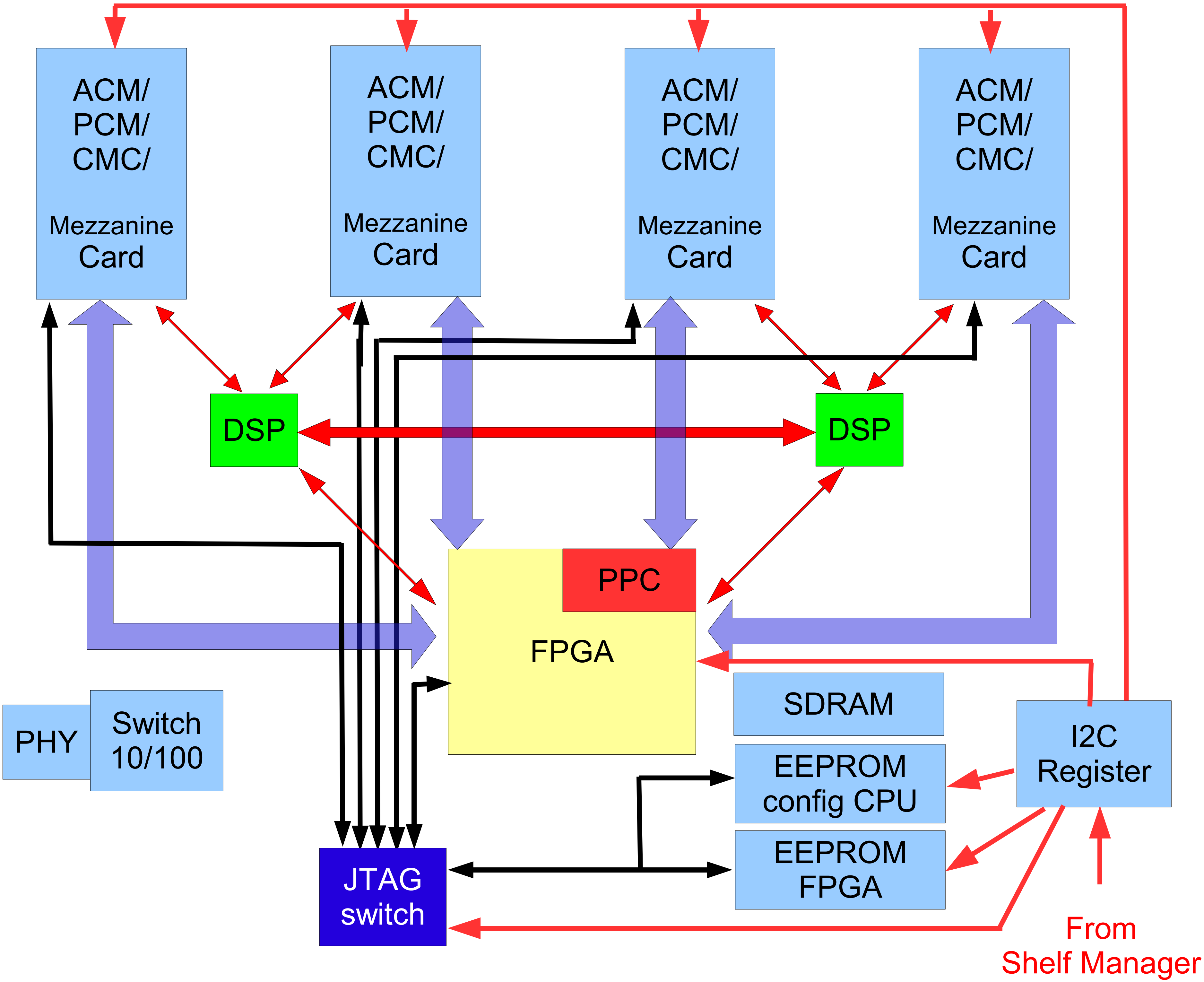
- Training and Supervision of students/ collaborators
- Project Management support
  - Planning of work
  - Cost/schedule/resource tracking
- Writing of requirements and specifications
- Critical R&D work

Schedule

- Prototype in FLASH : 2007/2008
  - Basic feedback/feedforward hardware and software incl. server
  - Frequency distribution
  - Automation
- Finalize Hardware Design 2008/2009
- Production Hardware 2009/2010
- Installation in Accelerator 2011
- Pre-commissioning 2012/13
- Commissioning with beam 2013


RF Signal Forw. in
RF Atten.
Down converter 8x
ADC 100 MHz 14-bit 8x
MEM 64M
DAC 300 MHz 14-bit 2x
Up converter 2x
RF Signal Ref. in
RF Atten.
Down converter 8x
ADC 100 MHz 14-bit 8x
FPGA kx
DAC 100 MHz 14-bit 8x
RF Signal Probe in
RF Atten.
Down converter 8x
ADC 100 MHz 14-bit 8x
DSP nx
Interf. ATCA
Spare Signal Input
Signal Cond.
ADC 100 MHz 14-bit 8x
Gb Eth. nx
RF Ref. Input
Low Latency Bus
Digital Input
Clock Synth.
Clock Distr.
MEM 64M
Opt. Gig. mx
LO Input.
LO Synth.
LO Distr..
Note:
-3(4) x24 rf channels are needed for 32 (48)cavities
- IF frequency range 10- 60 MHz
- clock frequency range from 80 – 100 MHz
-Green shaded area could be 1 ATCA board
… could be installed in box close to cryomodule
… connection to main processor board via Gigalink or low latency bus
-Red shaded areas could be AMC card
Trans Detect. 8x
ADC 1 Gs 10-bit 8x


ADC
8x
FPGA
ADC
ACE
MEM
DSP
FPGA
ETH
OGL
PS
trigger & clock synthesizer
Interlock
VM
2x
DAC


ACM/ PCM/ CMC/ Mezzanine Card
ACM/ PCM/ CMC/ Mezzanine Card
ACM/ PCM/ CMC/ Mezzanine Card
ACM/ PCM/ CMC/ Mezzanine Card
DSP
DSP
PPC
FPGA
SDRAM
PHY
Switch 10/100
EEPROM config CPU
EEPROM FPGA
I2C Register
JTAG switch
From Shelf Manager