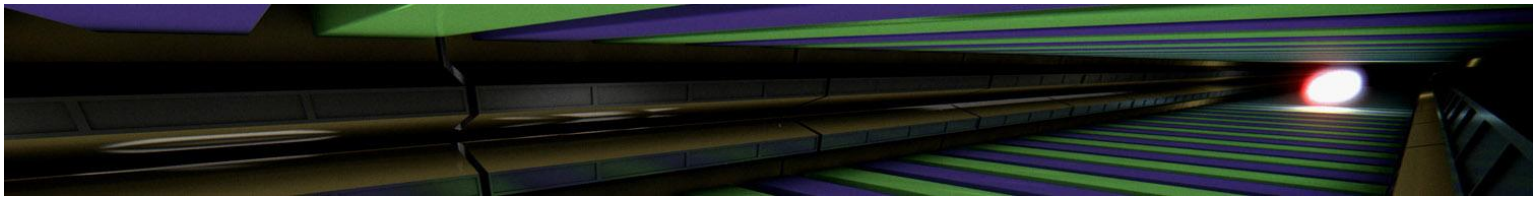


PZT Revision Status

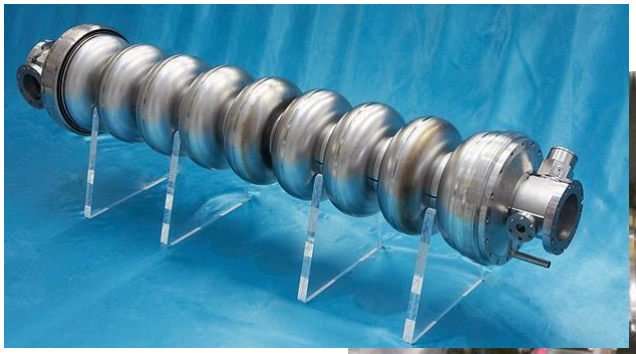
K. Przygoda

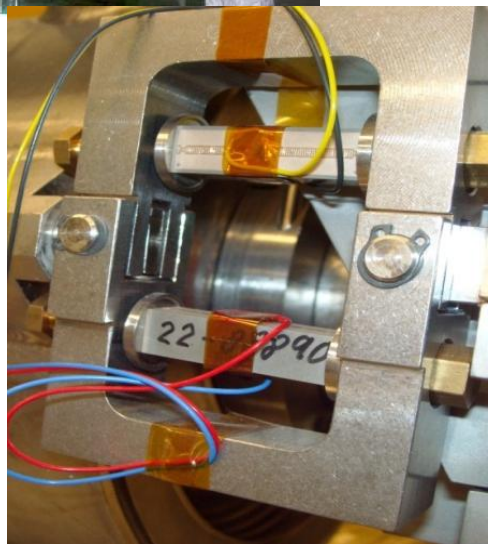
Advanced Techniques in LLRF control for XFEL
Collaboration Workshop

European XFEL

Agenda

- Requirements
- Block Diagram
- Operation Modes
- Hardware Status
- Firmware Status
- Laboratory Tests
- Software Status
- CMTB Tests
- Summary and Feature Plans





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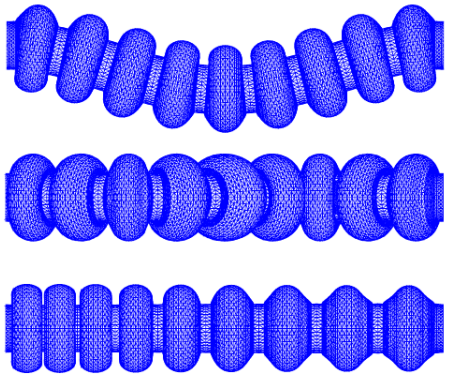
Requirements

Goal:

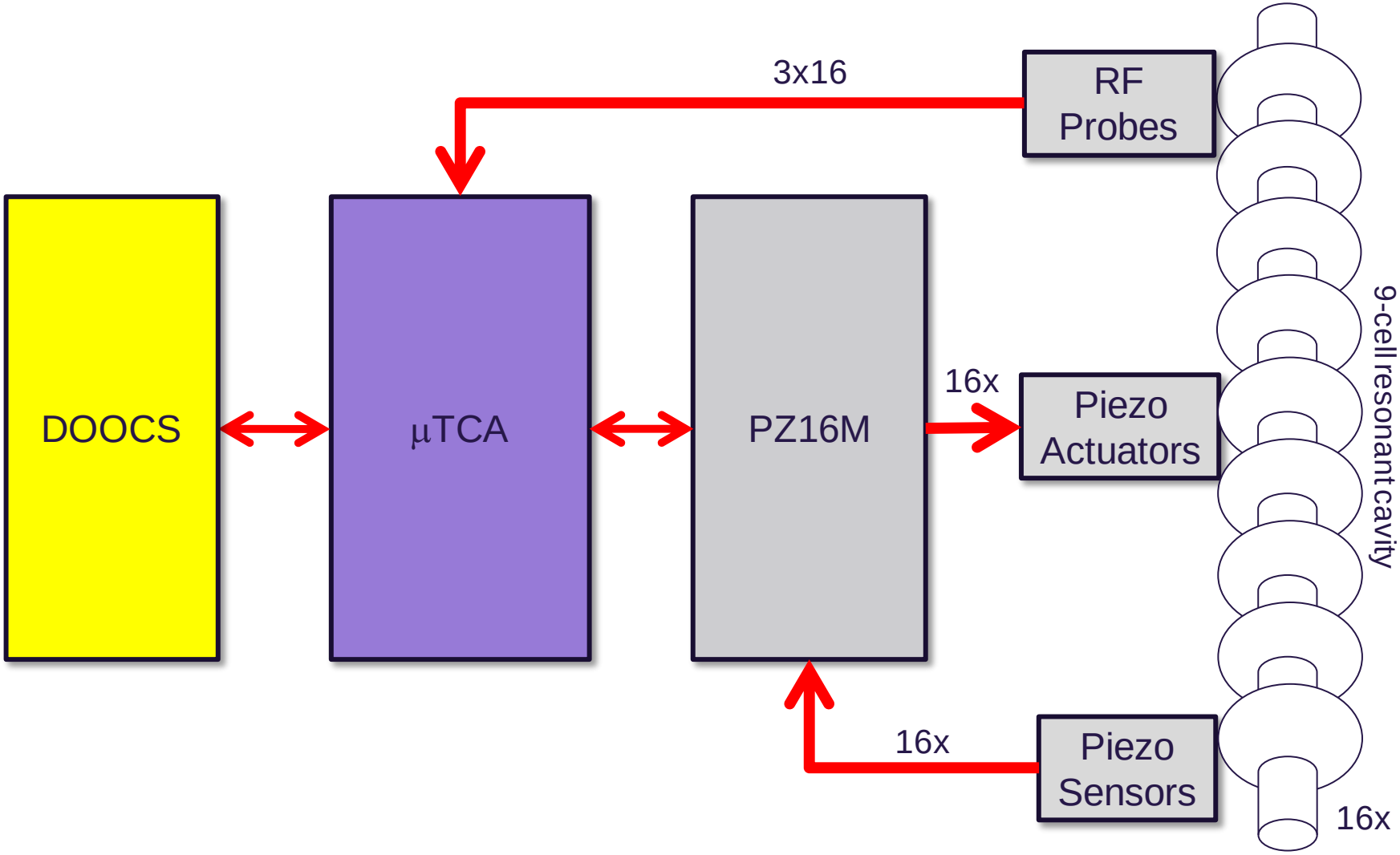
- Lorentz force detuning compensation below 10 Hz (during flattop)
- Cavity mechanical vibrations sensing and dumping possibilities

Specification:

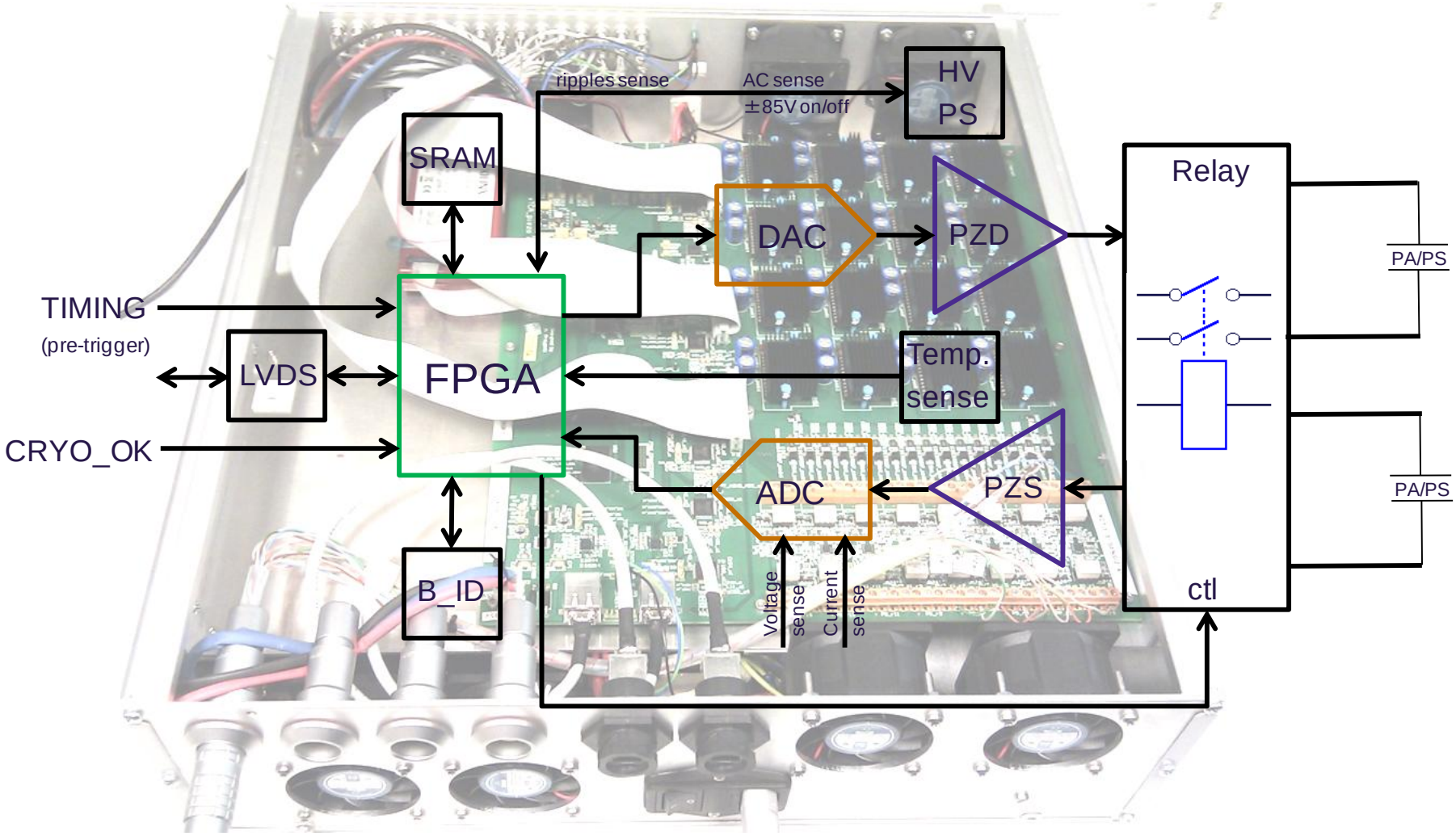
- Supervise 16 cavities (two accelerating modules) equipped with double stack piezo tuners
  - Processing power for driving piezo actuators and collecting data from piezo sensors
  - DACs/ADCs sampling frequencies: 100 times max. system frequency 200-300 Hz
  - Suitable for RF field repetition rates max. 25 Hz
- Remote switching between piezo actuator/sensor
- Piezo power supply: ±85 VDC (bipolar)
- Bipolar/Unipolar/Arbitrary control mode of piezo actuators
- Monitoring of power amplifiers output voltages, currents, temperature
- Serial/optical link connection to μTCA-based LLRF controller



Block Diagram (1)

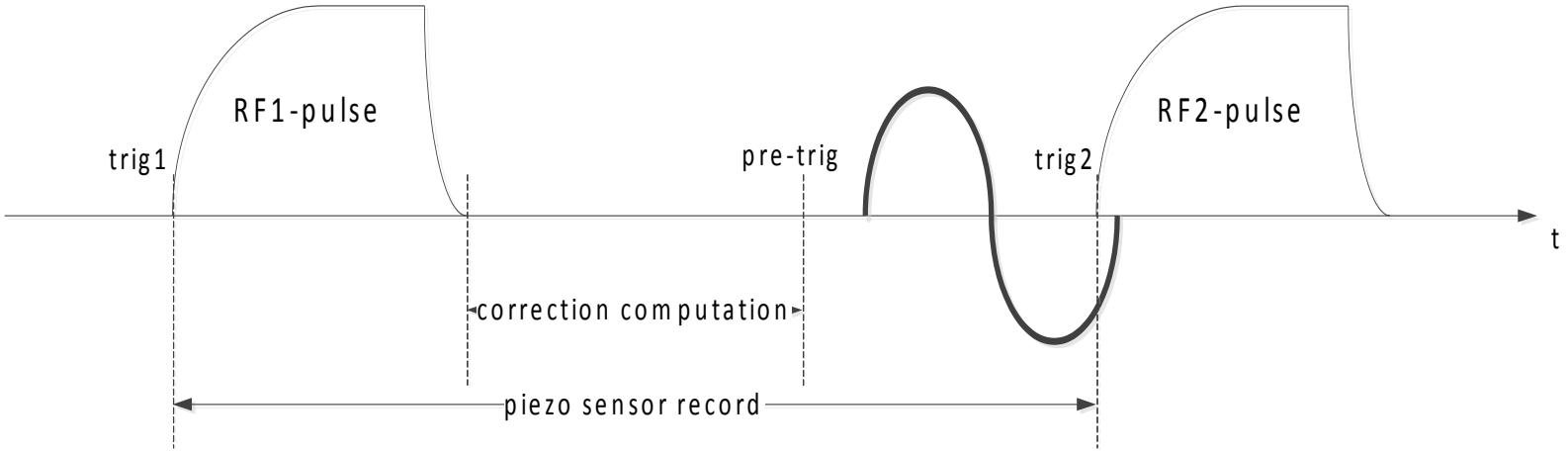


Block Diagram (2)

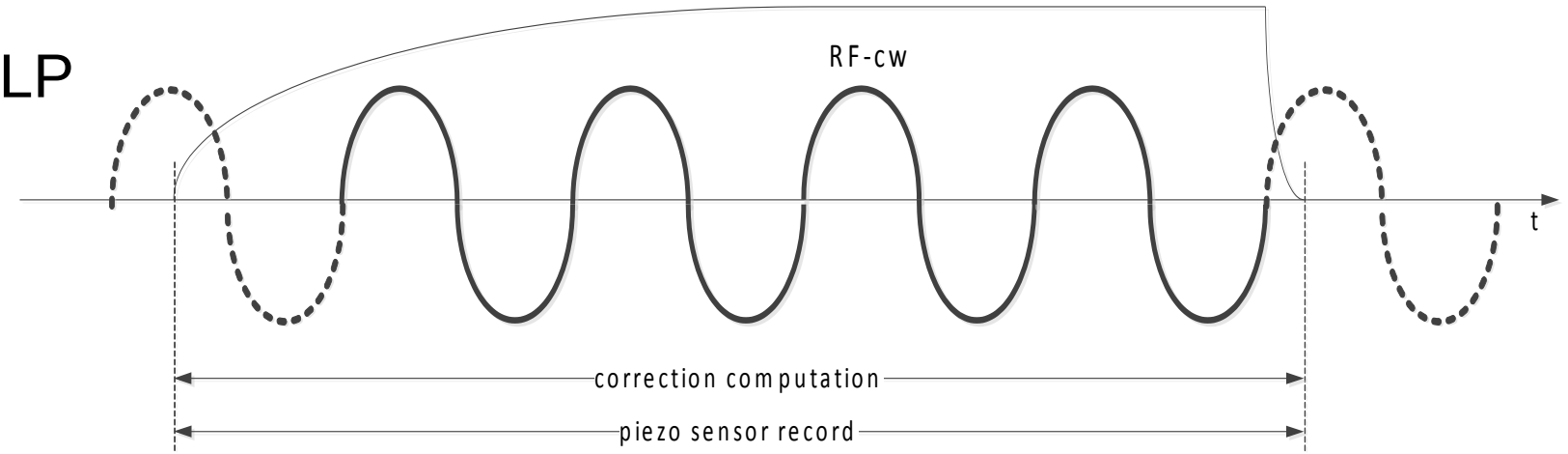


Operation - Pulse/CW

- Pulse mode



- CW/LP mode



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Hardware Status

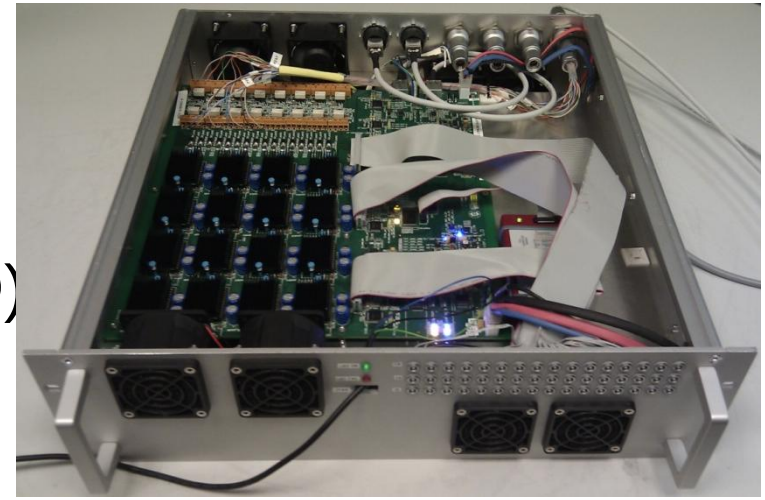
- We have 2 prototypes assembled, mounted and debugged

(#1 0x0004a3fffe2ecef8 – unique id)

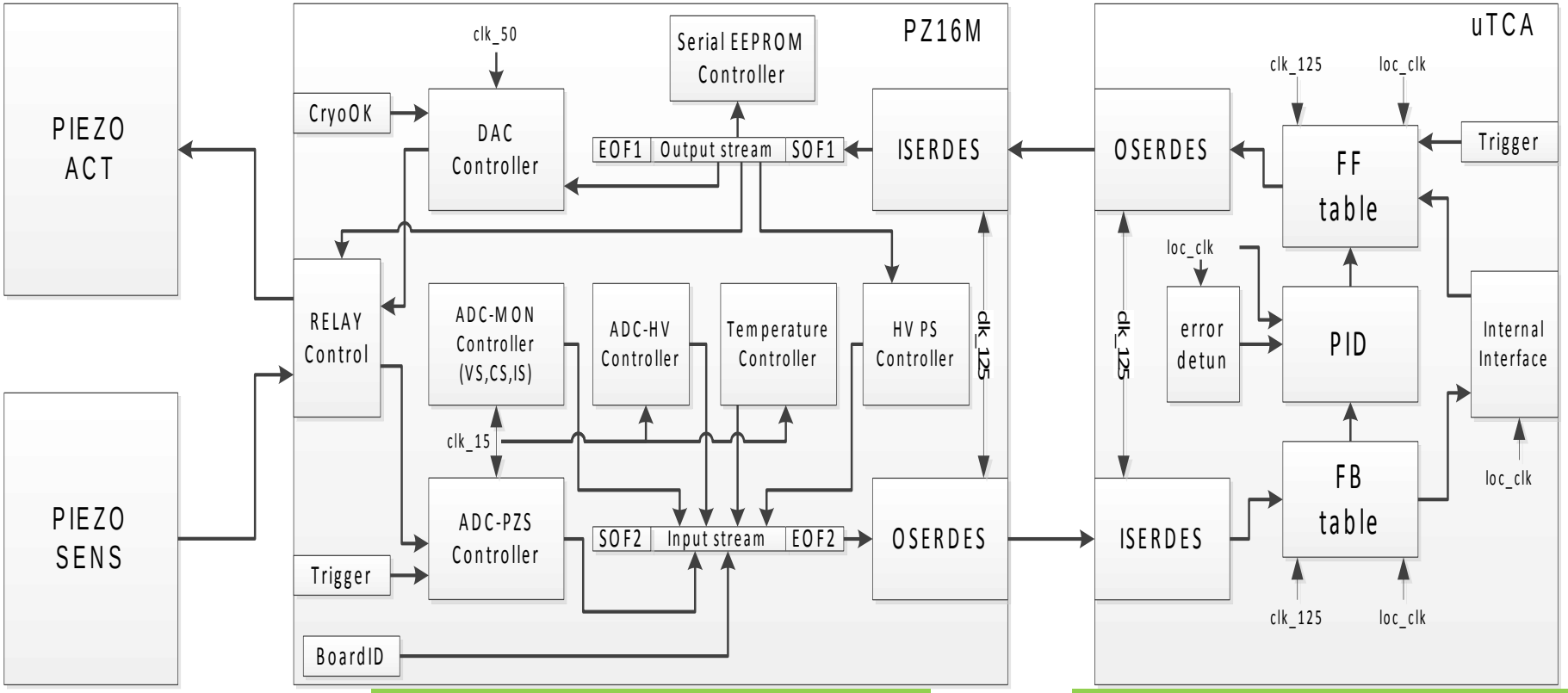
(#2 0x0004a3fffe2eb0e5 – unique id)

  - Switching relays
  - Power amplifiers
  - HV/LV PSU (Coolers)
  - DACs (PZD), ADCs

  (PZS, PZI, PZO, PZC, HVS)
  - Sensors (Temperature, Board ID)
  - FPGA / Eprom (SP6)
  - Communication (LVDS)

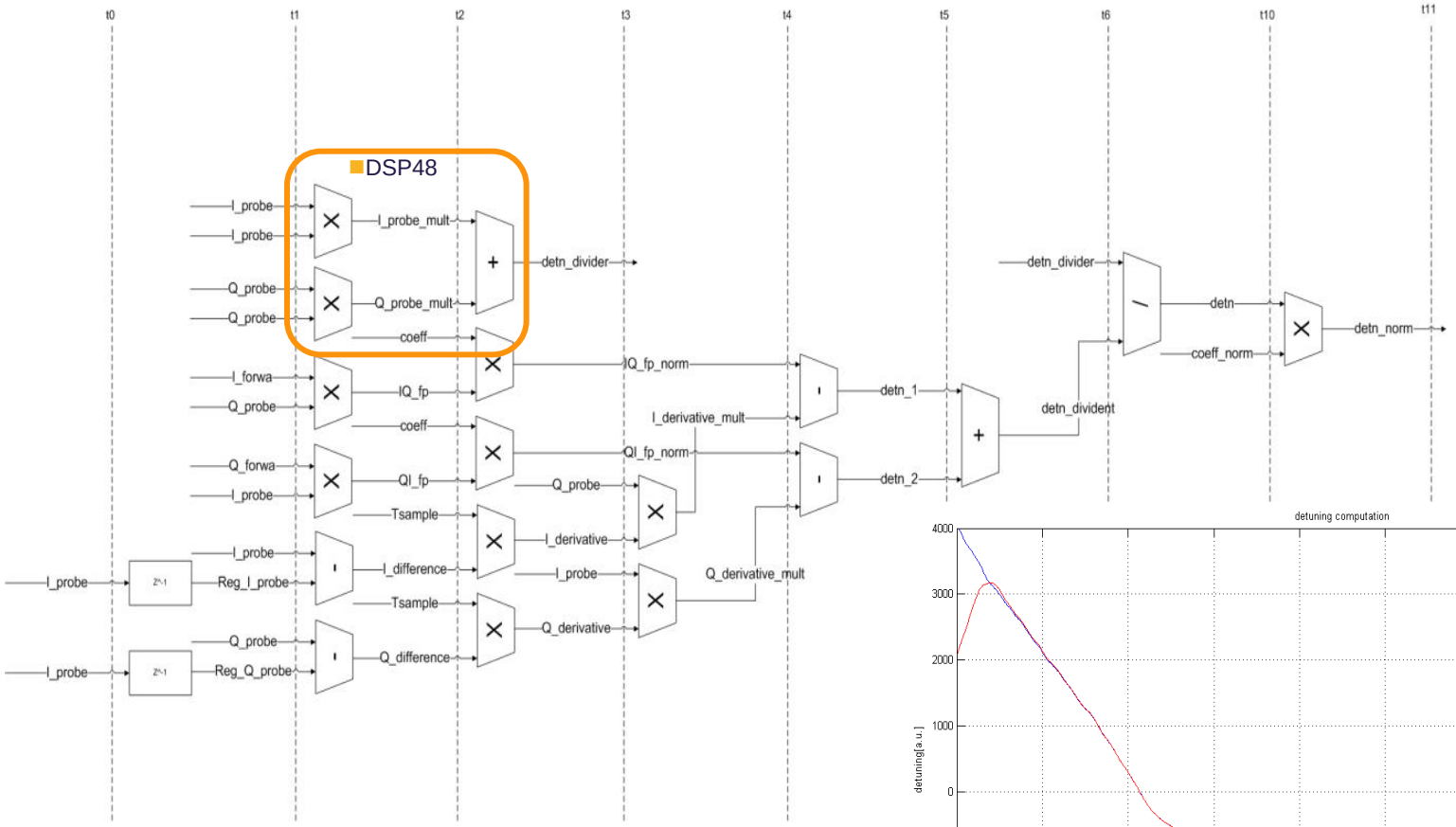


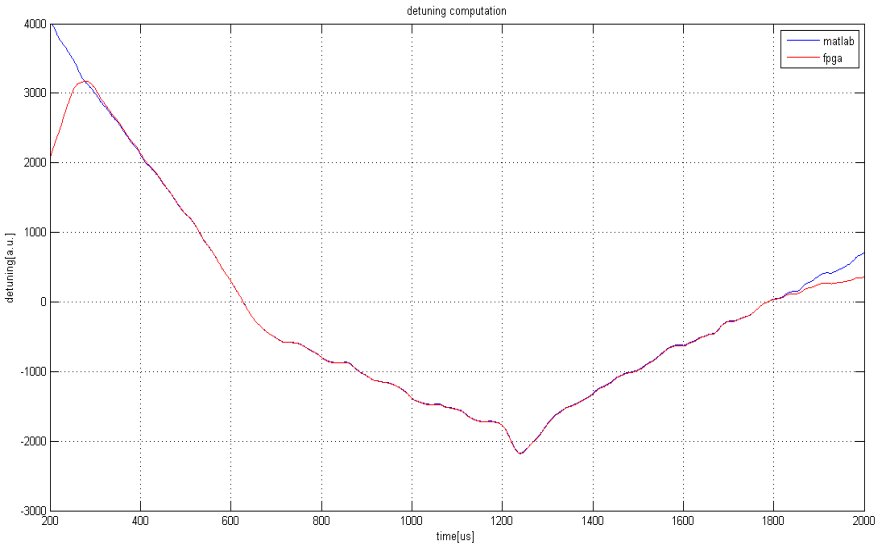
Firmware Status



- Spartan6 (6slx45tfgg484-2) logic utilization (33%)
- Virtex5 (5vsx95tff1136-2) logic utilization (23%)

Detuning Computation in FPGA





- IQ scheme

(no beam effect applied yet)

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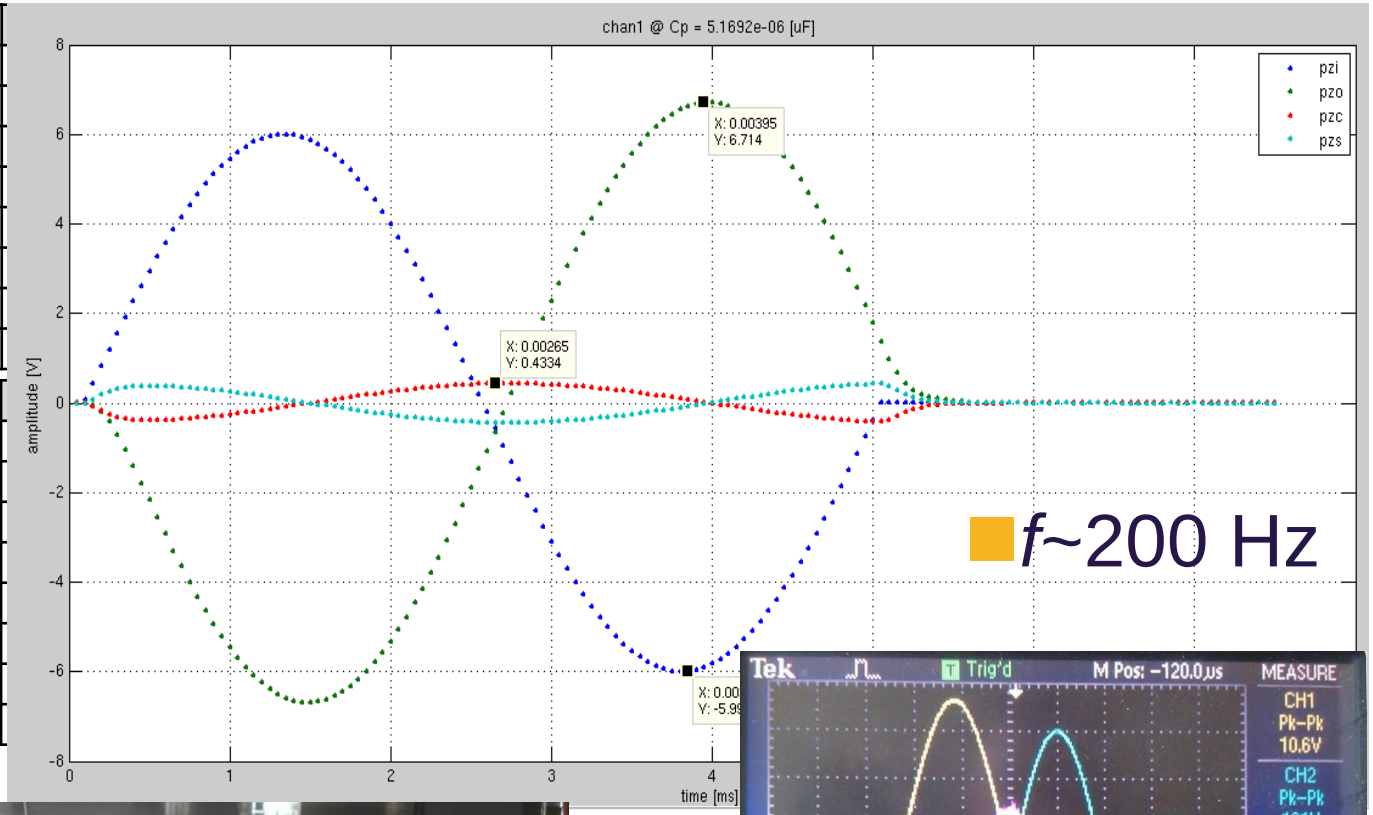
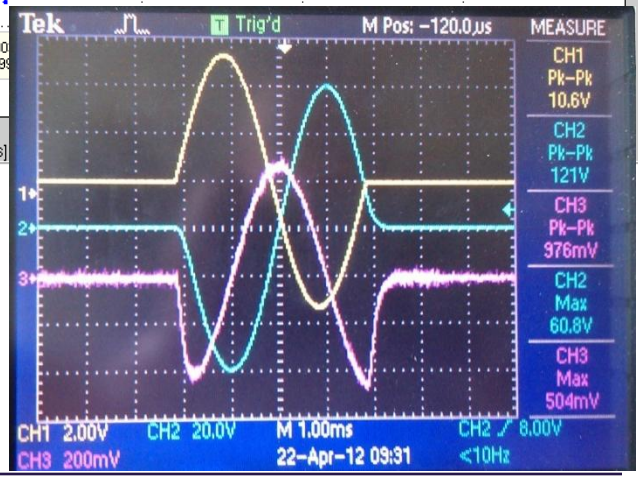
Tests Results - Laboratory Conditions (1)

Chan	V_{mi} [V]	V_{mo} [V/10]	I_{mo} [A]
1	5.99	6.71	0.43
2	5.99	6.61	0.40
3	5.99	6.89	0.44
4	6.00	6.66	0.41
5	5.99	6.64	0.43
6	5.99	6.81	0.42
7	5.99	6.68	0.44
8	5.99	6.67	0.41

Chan	V_{mi} [V]	V_{mo} [V/10]	I_{mo} [A]
9	5.99	6.67	0.43
10	5.98	6.68	0.40
11	5.99	6.64	0.40
12	5.98	6.68	0.42
13	5.99	6.65	0.41
14	5.99	6.79	0.41
15	5.98	7.04	0.45
16	5.99	6.72	0.43





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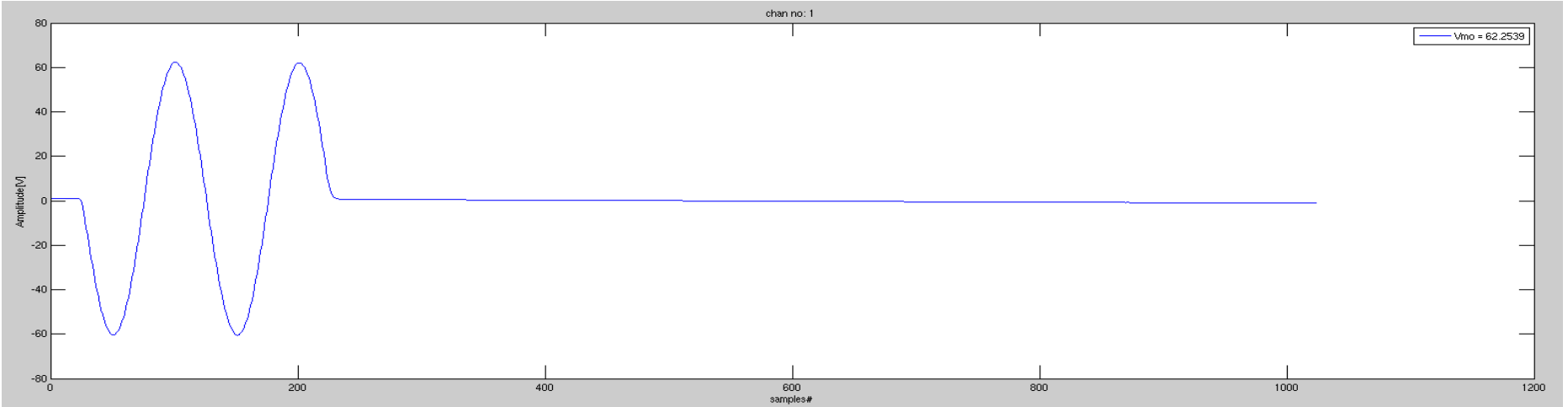
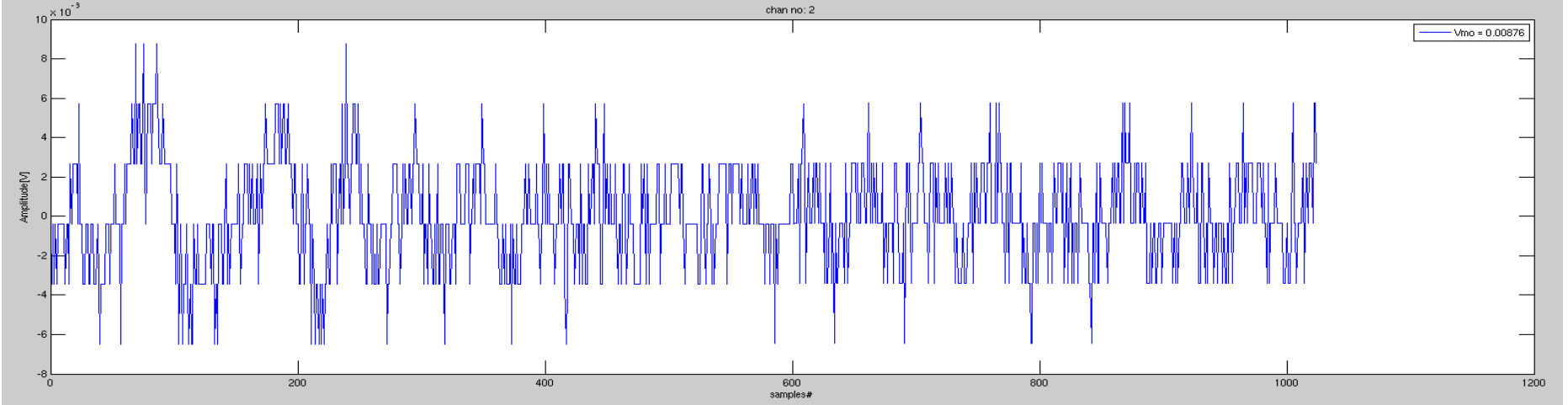
Tests Results - Laboratory Conditions (2)



Crosstalk ~ - 75dB



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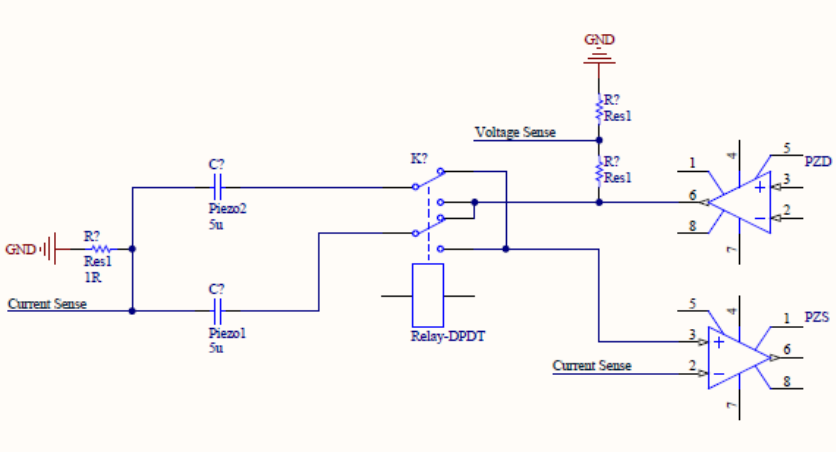
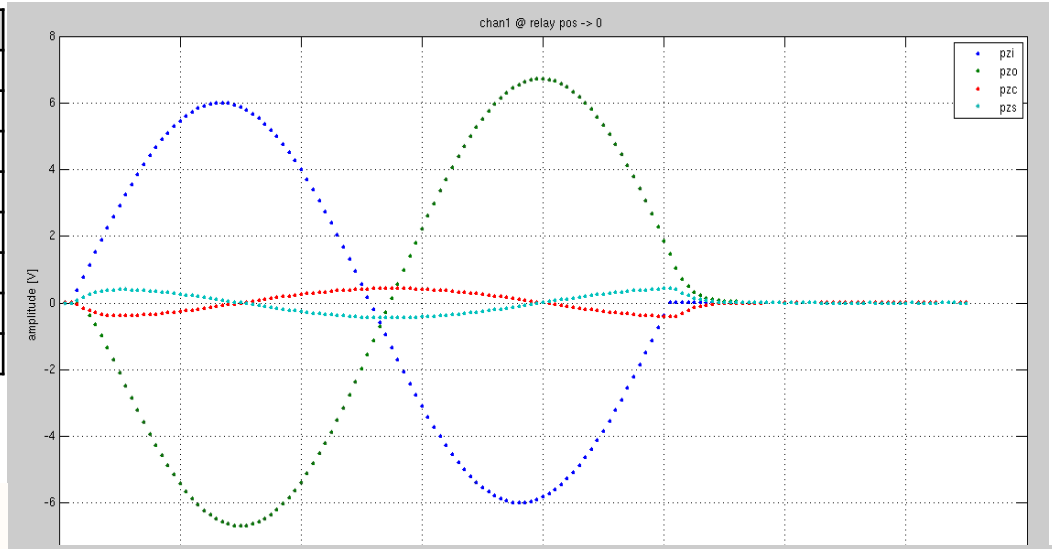
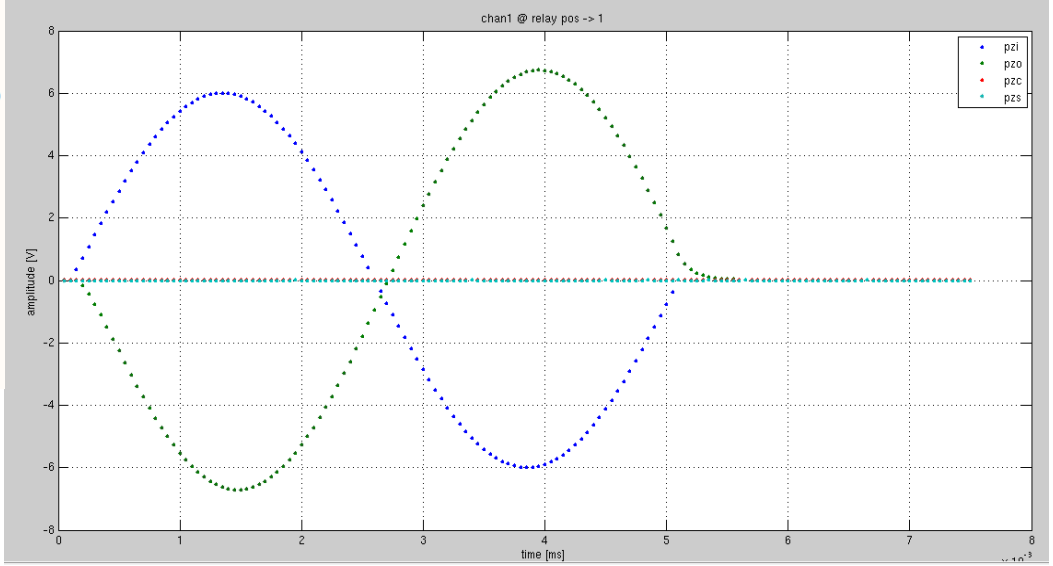
Tests Results - Laboratory Conditions (3)

Chan	Pos0	Pos1
1	Passed	Passed
2	Passed	Passed
3	Passed	Passed
4	Passed	Passed
5	Passed	Passed
6	Passed	Passed
7	Passed	Passed
8	Passed	Passed

Chan	Pos0	Pos1
9	Passed	Passed
10	Passed	Passed
11	Passed	Passed
12	Passed	Passed
13	Passed	Passed
14	Passed	Passed
15	Passed	Passed
16	Passed	Passed







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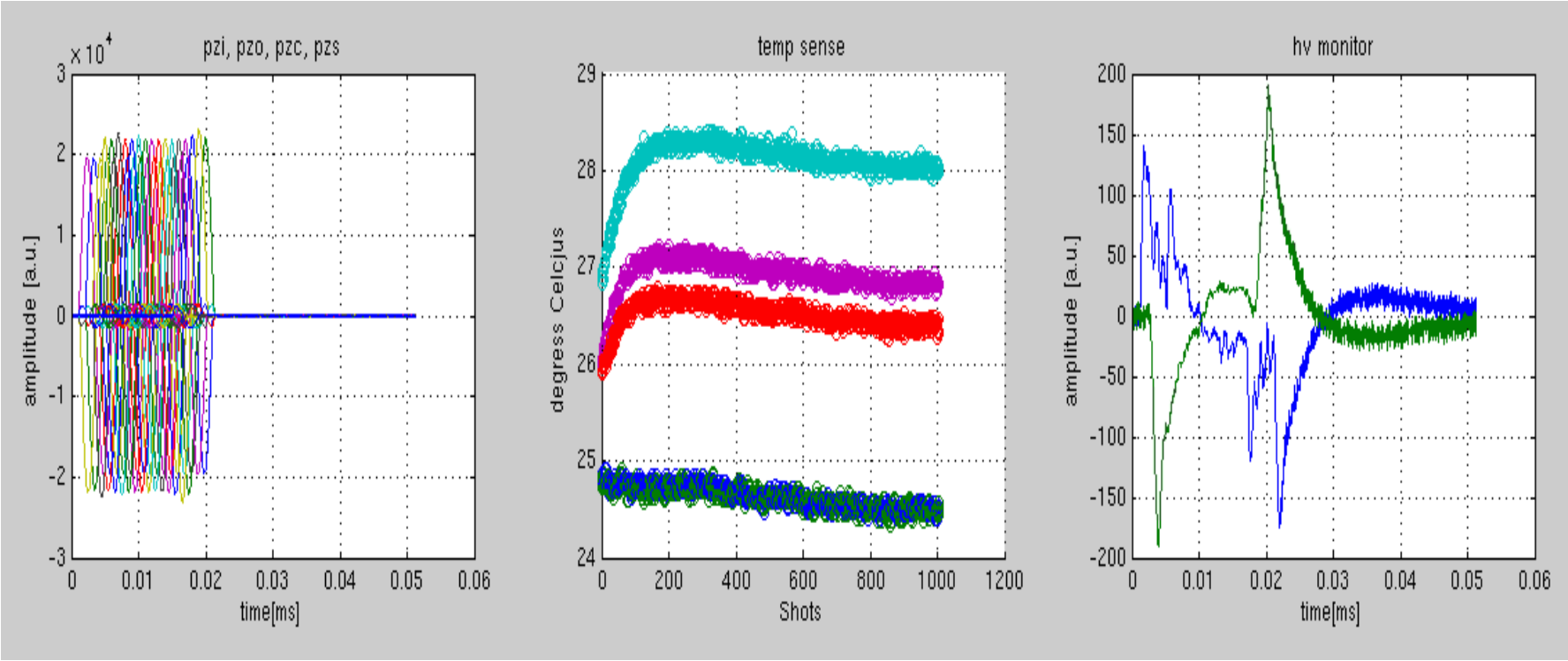
Tests Results - Laboratory Conditions (4)



- all DACs setup with maximum range ±32767 [bits]
- all piezo drivers outputs connected to ~5μF capacitors
- test taken for 1000 shots that means 1000 seconds
- (T_o~24 degress celcjus)

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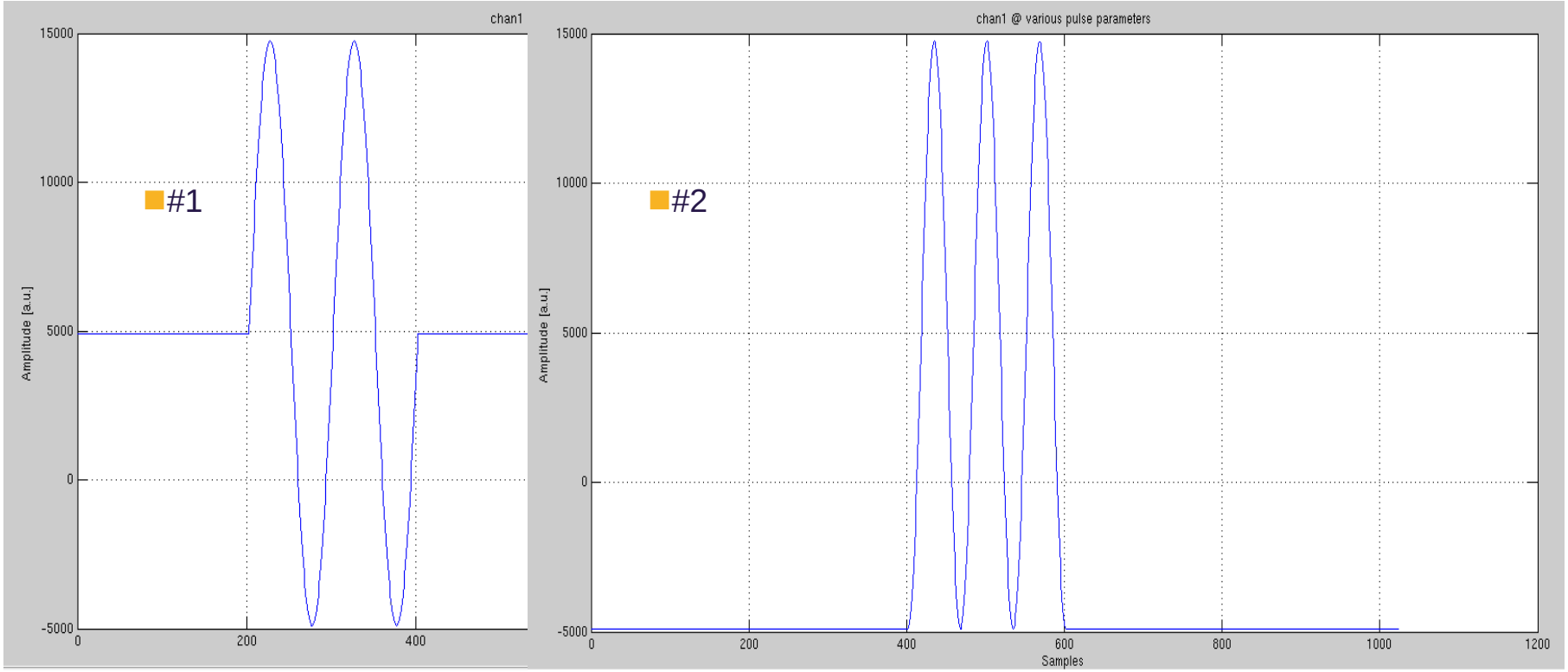
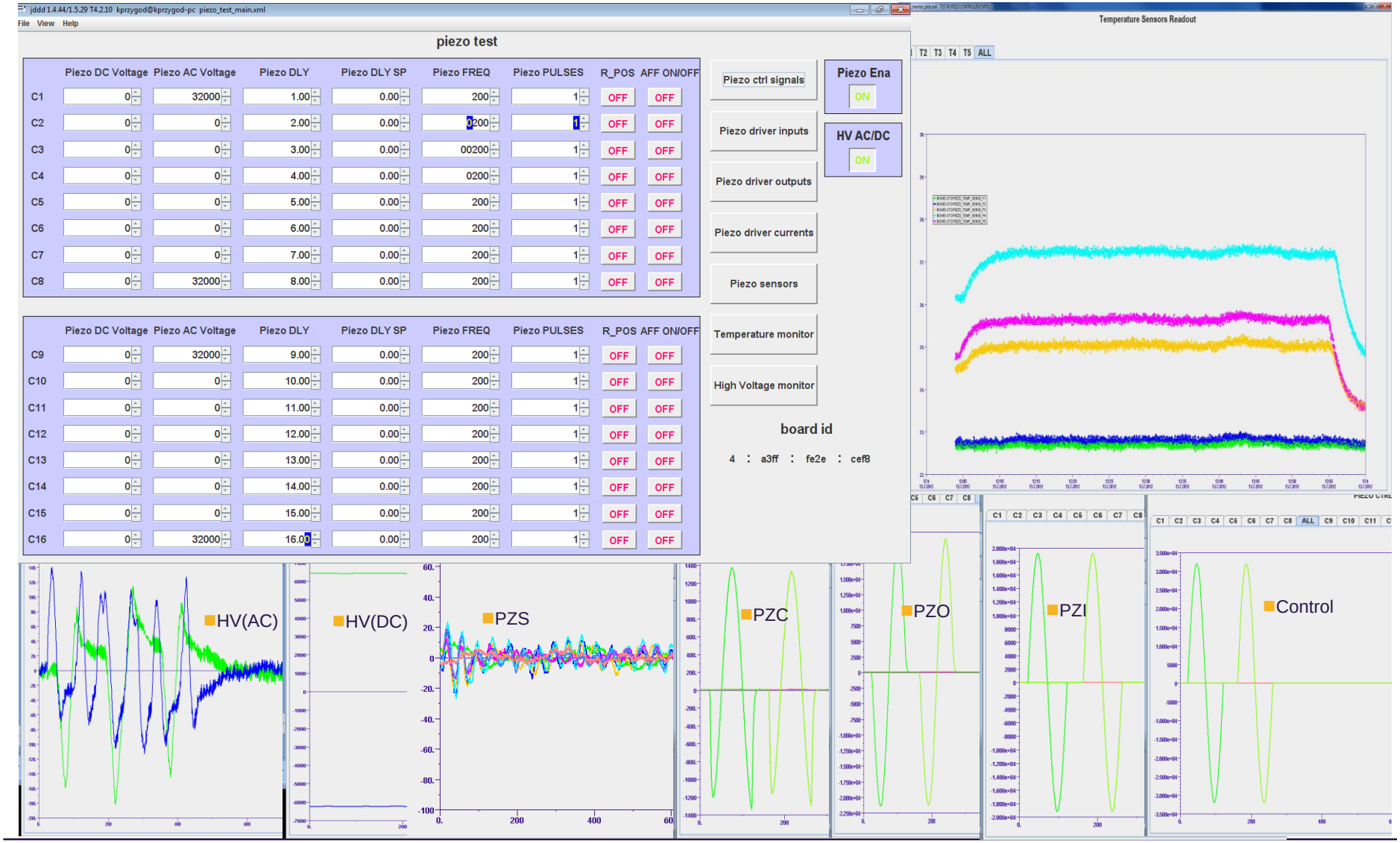
Tests Results - Laboratory Conditions (5)



- arbitrary waveform generators:
- #1 AC=32767/2[bits], DC=16384/2[bits], FREQ=200Hz, DLY=10ms, PULSES=2, BIPOLAR
- #2 AC=-32767/2[bits], DC=-16384/2[bits], FREQ=300Hz, DLY=20ms, PULSES=3, UNIPOLAR

Software Status (Jddd Panels)



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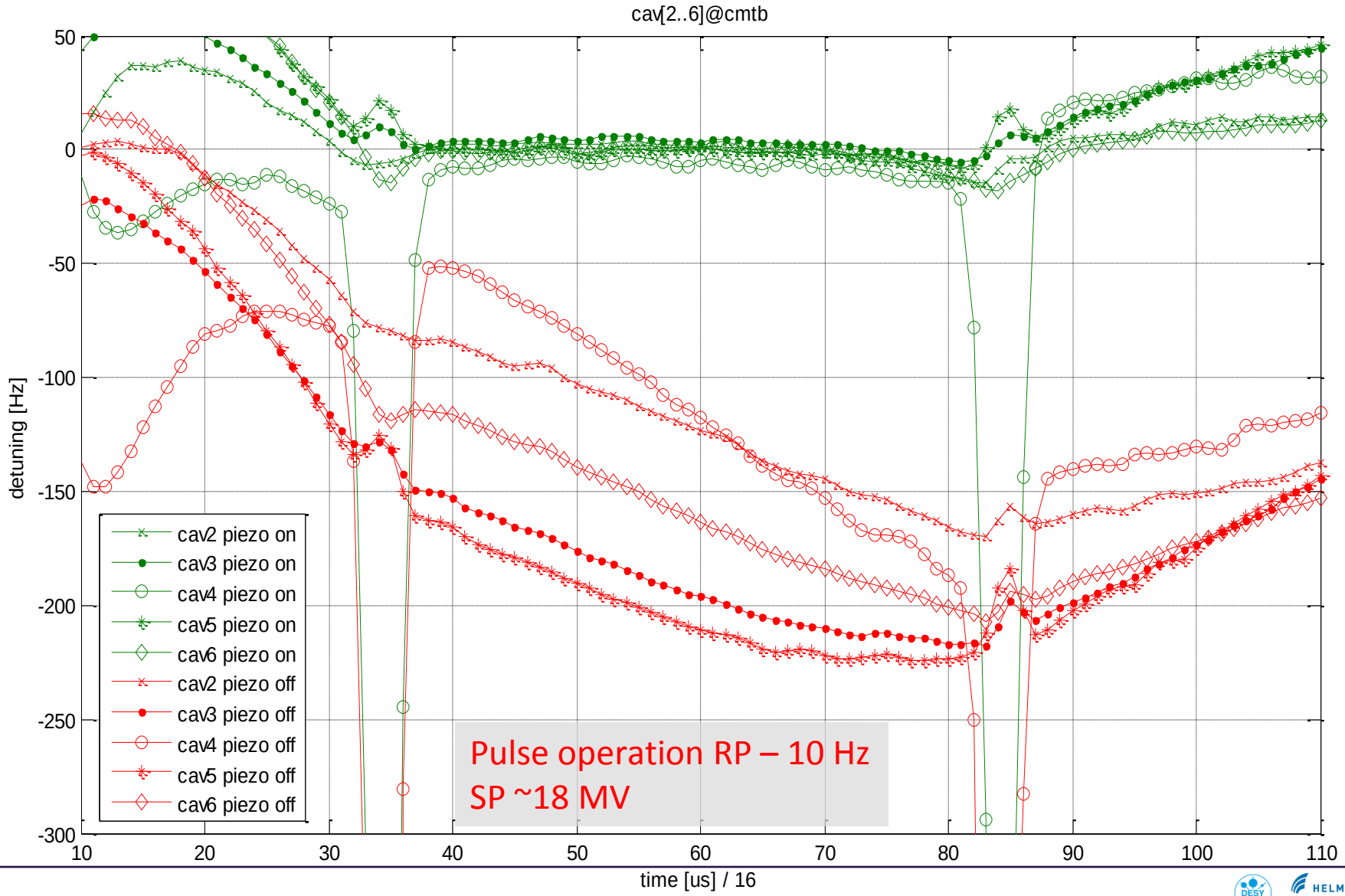
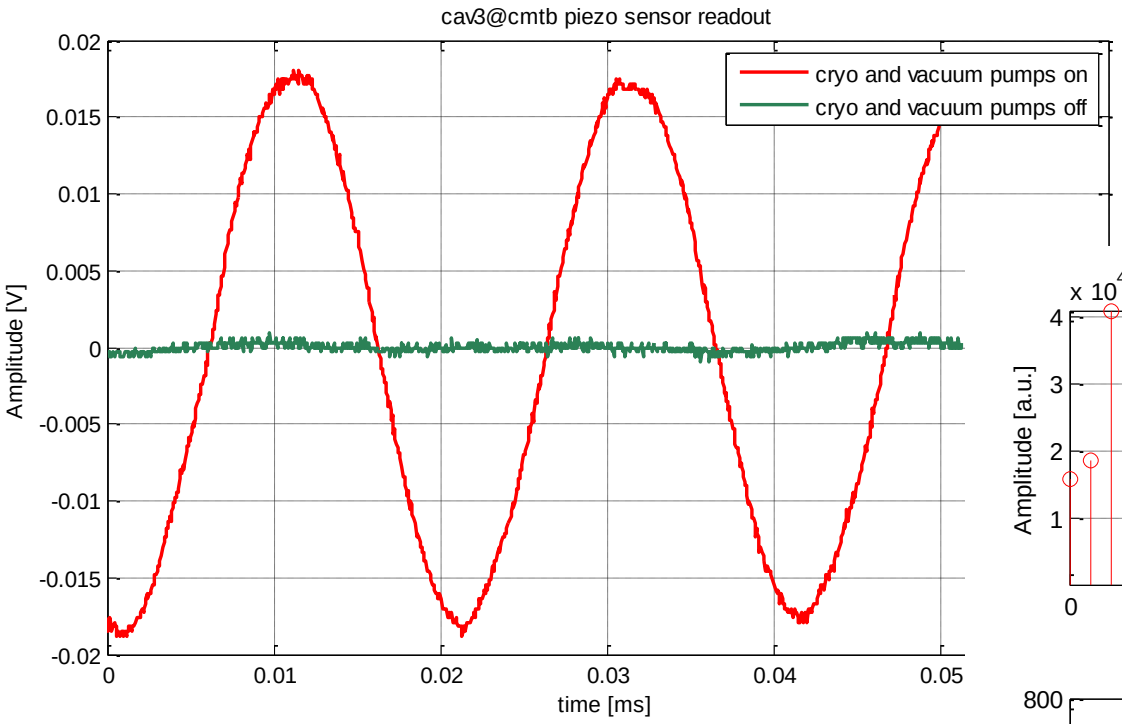
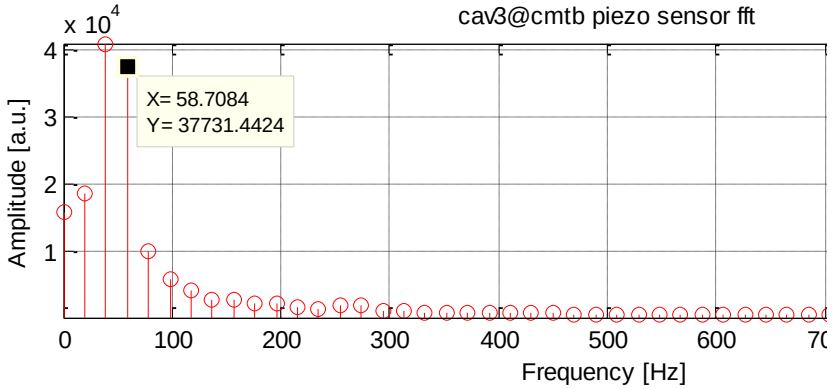
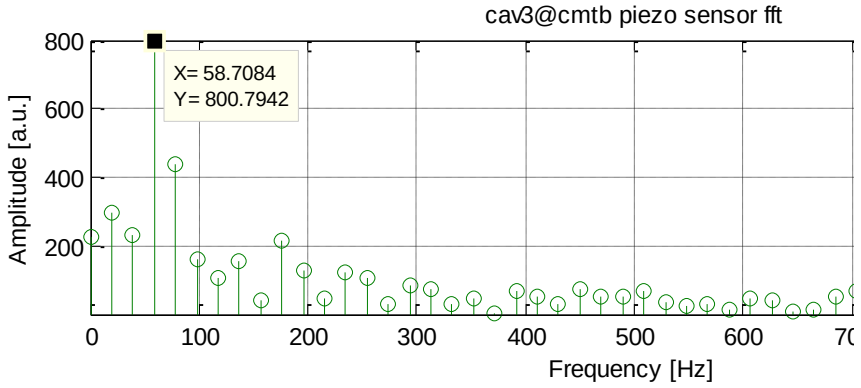
LFD Compensation



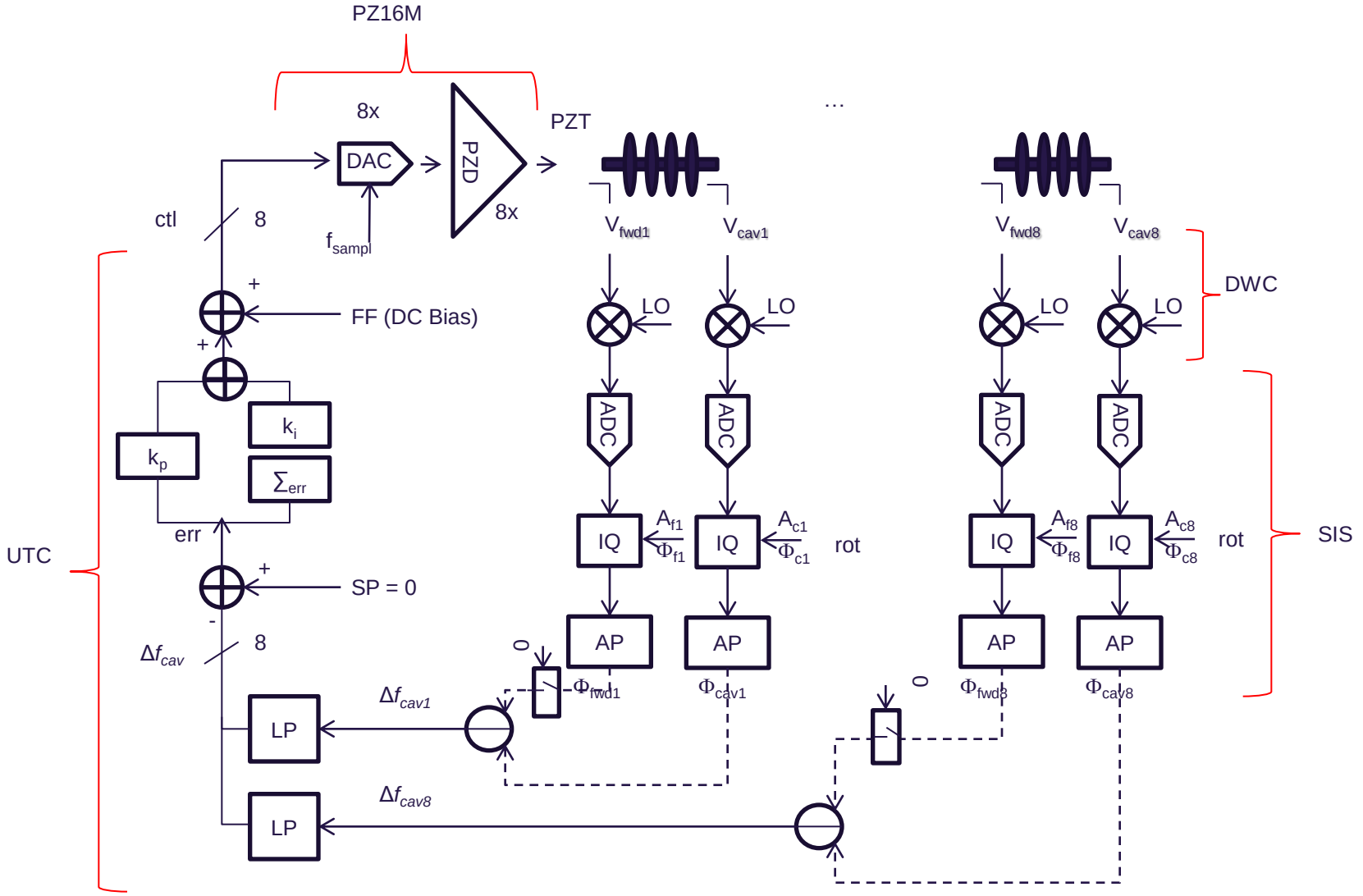
Main Microphonics Noise Source







Piezo Controller Block Diagram (CW tests)



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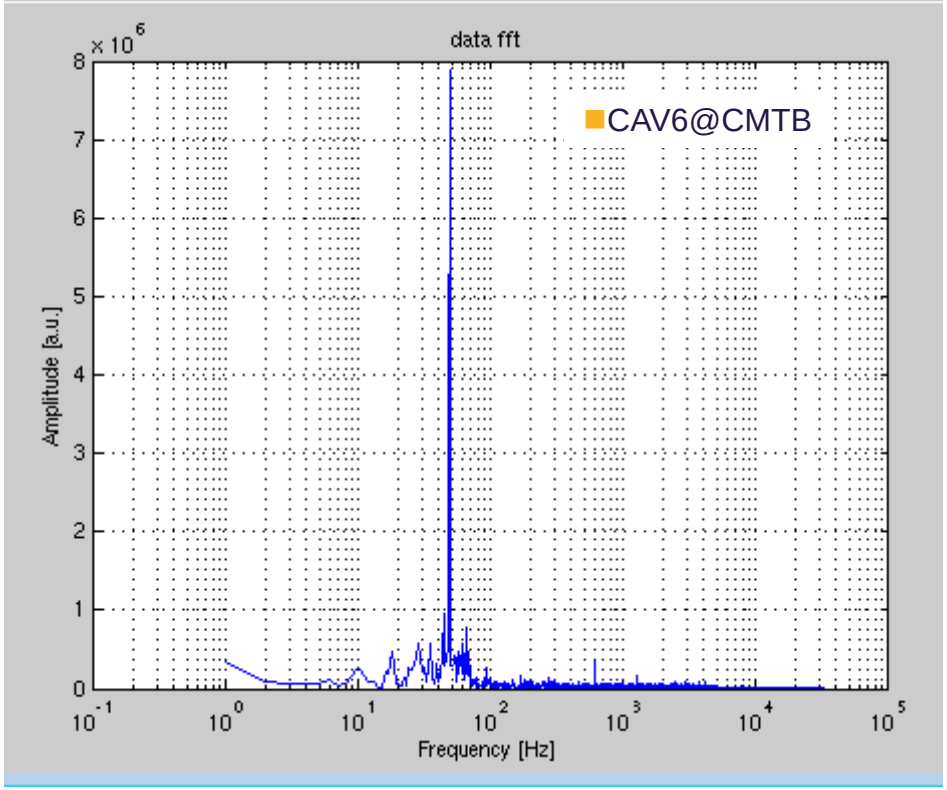
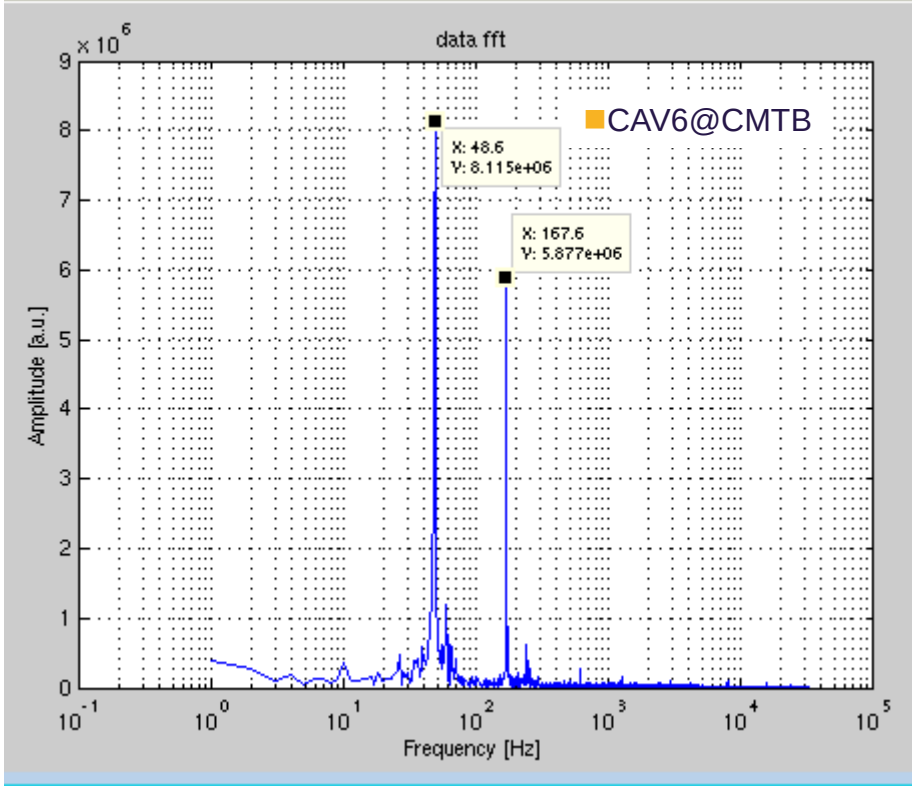
Piezo Controller (no LP filter applied)

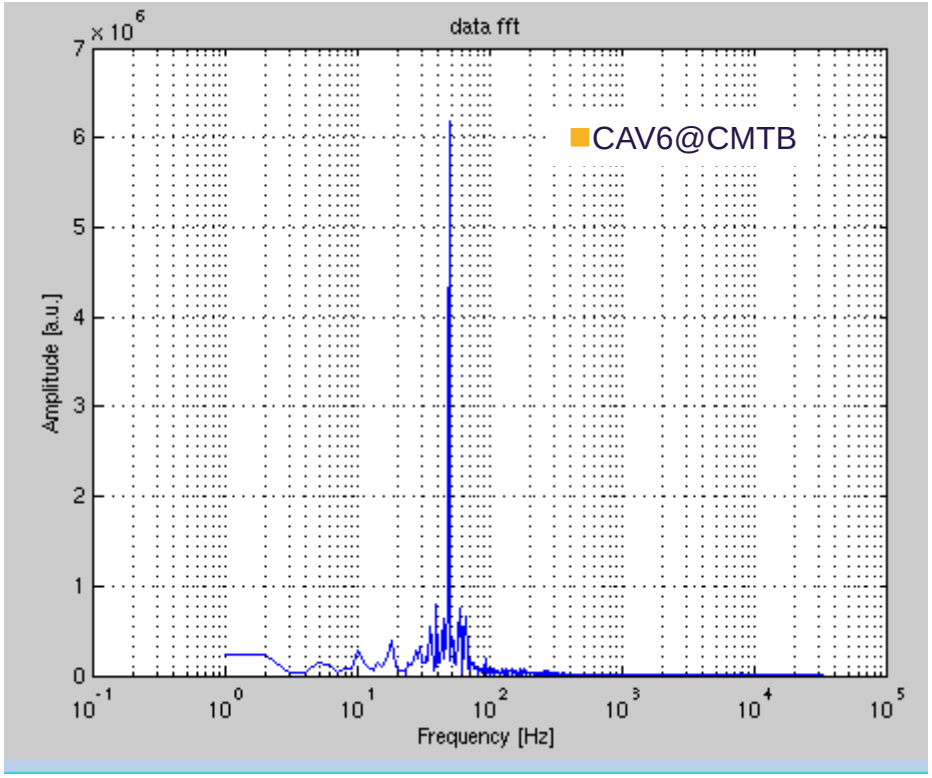


- FFT of piezo error signal,
- Piezo FB off

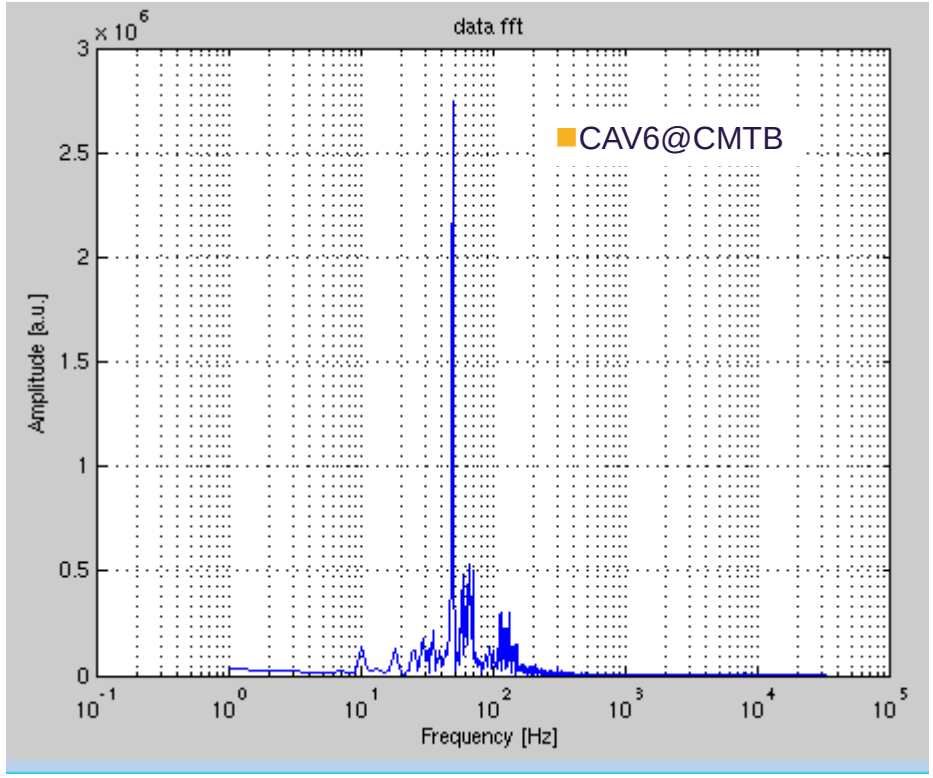


- FFT of piezo error signal,
- Piezo FB on (K_p=0.1, K_i=0.1)

Piezo Controller (LP filter applied f_{cut}=100 Hz)



- FFT of piezo error signal,
- Piezo FB off (LP f_{cut} = 100 Hz)



- FFT of piezo error signal,
- Piezo FB on (K_p=1, K_i=0.1)

Ideas for Further Improvements (CW)

- UTC (all calcs with 81 MHz) ⇔ DAC (PZ16) path latency (81/125 MHz comm. interf. clk ~ 1.18 / 0.7 μs) improvement (communication optimization, serial link ⇔ optical link)
  - i.e. for CMTB/CW (8 cavities api) we have DAC update rate 512kHz/8=64kHz, which means we need to deliver sample for each channel with time spacing of (1/64kHz*8=1/512kHz) ~2 μs
- DAC output analog low pass filters by-passing
- DAC output phase shifter
- IQ decoupling
- Migration from low pass to notch filters on the piezo control input/output (or both) for more precise cancelation of the neighboring/dominating (with closed loopback) frequencies
- Make standalone piezo feedback with only piezo sensors (from UTC we will need only PI gains and FF-DC Voltage)

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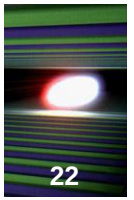
Hardware Bugs / Improvements Report



- Missing / re-placeing mounting holes
- Internal piezo cabling connectors footprint re-building
- Piezo driver capacitors model exchange (with smaller footprint)
- Some connectors rotating / moving (i.e. current sense, HV/LV, RJ45)
- HV ADC model exchange (AD7367 ⇔ AD7606-4)
- Temperature sensors replacing (maybe direct connection to piezo driver radiator with thermal pad)
- DAC output analog low-pass filters (RC or active with OpAmp)
- MLVDS buffer exchange (with higher bdw)
- We can also switch from MLVDS to optical link (SFP)

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THANK YOU FOR YOUR ATTENTION