ZONE 3
Classification

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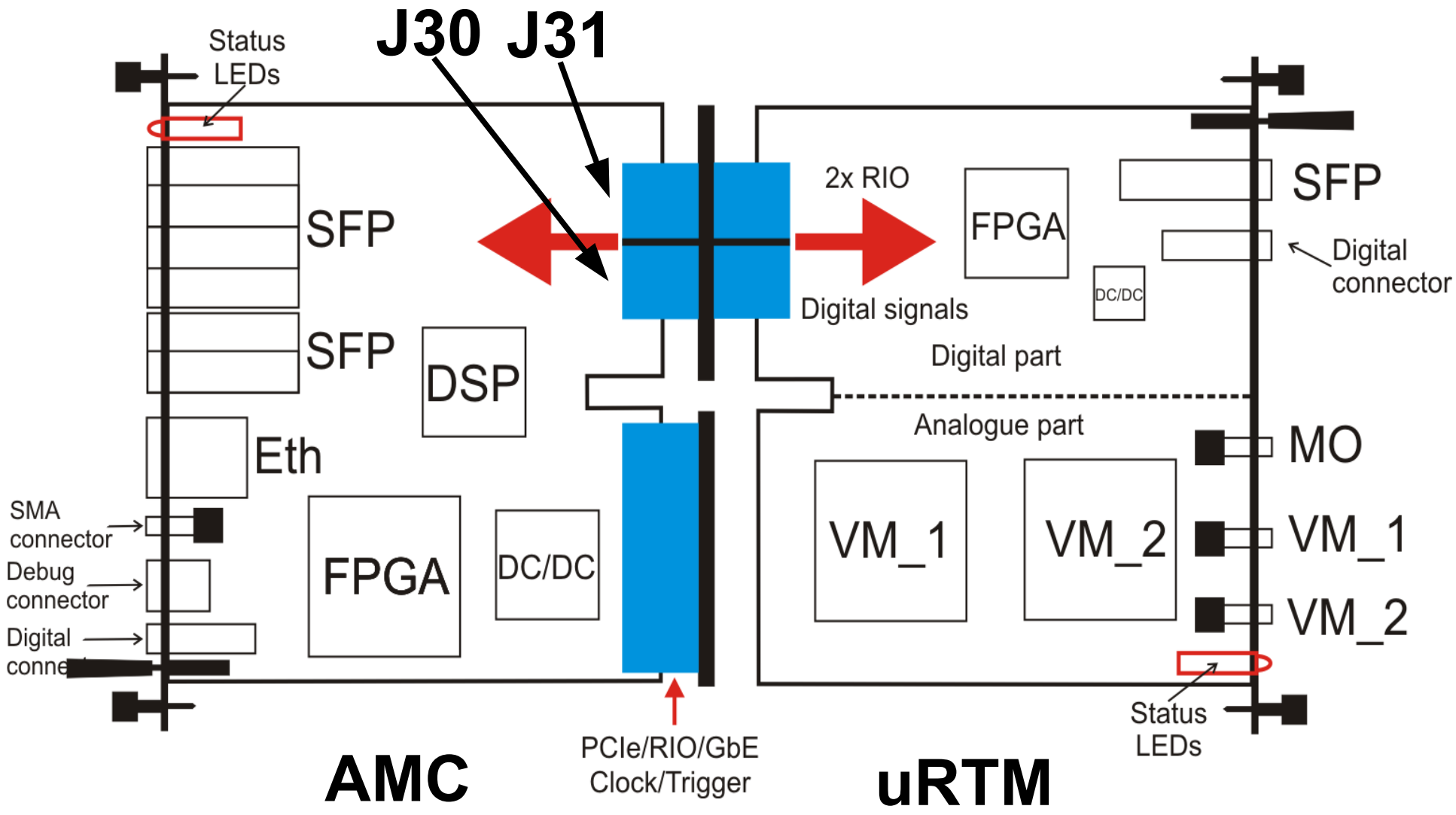
Agenda

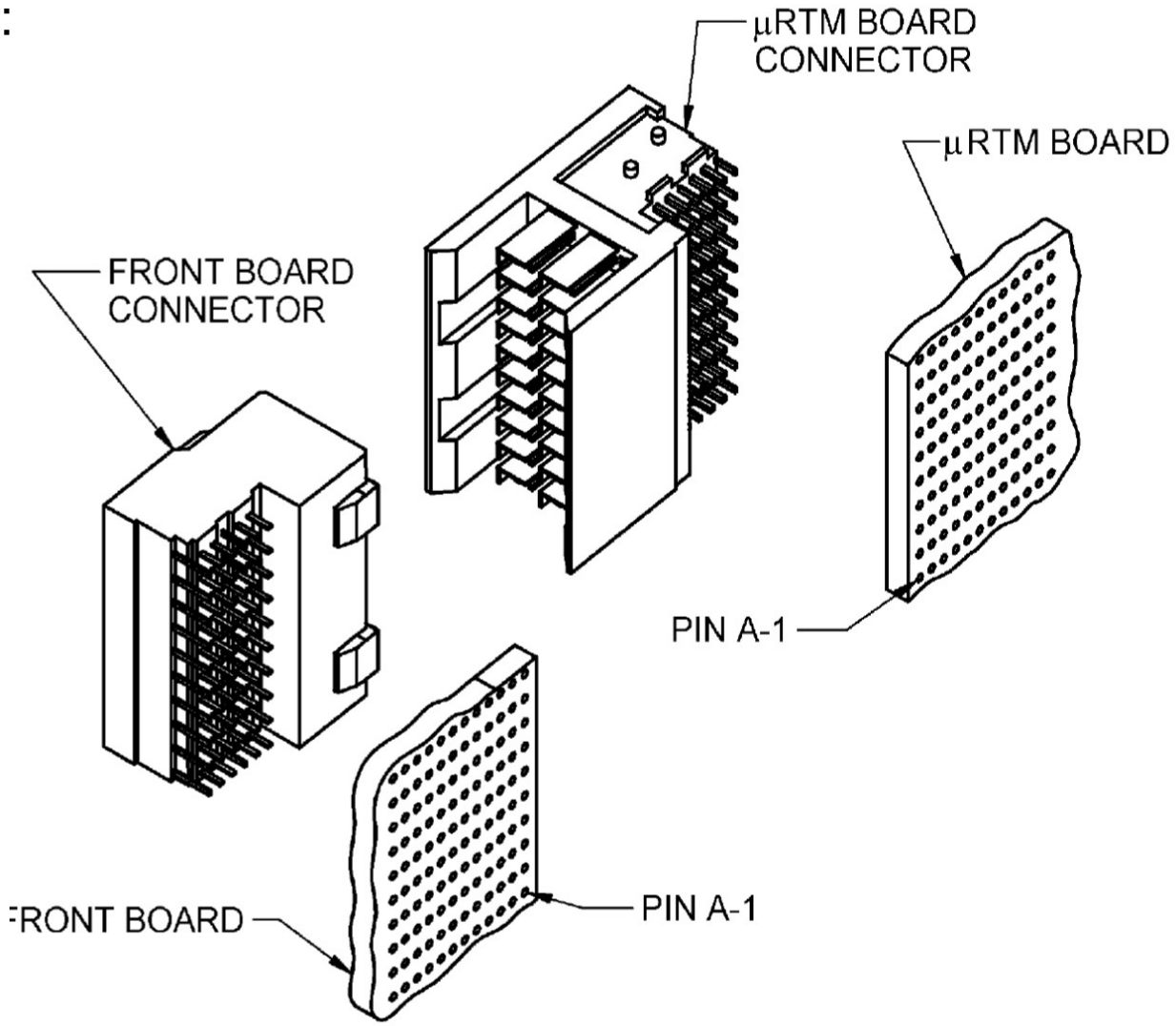
- Zone 3 in MTCA.4 Standard
- Signals on Zone 3
- Do we need More Standards ?
- Proposal for Digital Class of Zone 3 Connectors

MTCA.4 – Zone 3 Connectors (1)



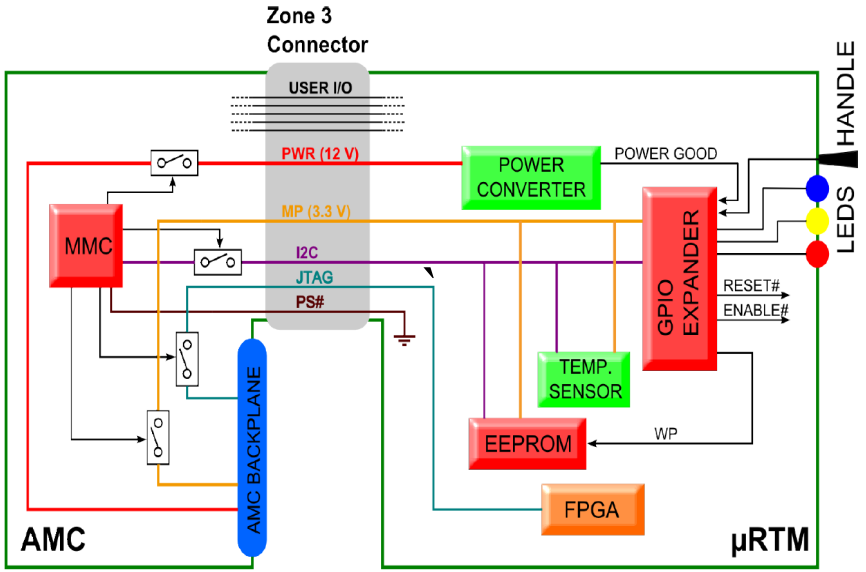
MTCA.4 – Zone 3 Connectors (2)

- MTCA.4 uses ADF connector:
  - ADF 20 Pair (Mid-size)
  - **ADF 30 Pair (Mid-size)**
  - ADF 40 Pair (Full-size)



Zone 3 Connectors – Standardized Signals

Name	Description	Name	Description
µRTM_PWR	+12 Volts (nom)	GND	Ground
µRTM_PS#	µRTM Present	µRTM_MP	+3.3 Volts (nom)
µRTM_SDA	I²C Data	µRTM_SCL	I²C Clock
µRTM_TCK	Optional JTAG TCK	µRTM_TDI	
µRTM_TDO	Optional JTAG TDO	µRTM_TMS	



	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS

Do we need More Standards ?

- Available boards compliant with MTCA.4 have various assignment of signals on Zone 3 connector:
  - SIS8300
  - uTC
  - uFMC25
  - DAMC2
  - TEWS TAMC 631
  - and more in the future...
- Signals on Zone 3 connector:
  - Analogue
  - Digital signals (bi-directional):
    - Single ended
    - Differential
    - High-speed serial links
  - Clocks (AMC clocks, RTM clocks)
  - Special purposes (interlock, reset, SPI, etc...)

Zone 3 Connector for Analogue Signals

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	SDA_E	SDA_I
2	PWR+12V	PWR+12V	MP+3.3V	SCL	SCL_E	SCL_I
3	SFP1-TX+	SFP1-TX-	SFP-CLK+	SFP-CLK-	SFP2-TX+	SFP2-TX-
4	SFP1-RX+	SFP1-RX-	Dx+	Dx-	SFP2-RX+	SFP2-RX-
5	ADC-SPI1	ADC-SPI1	ADC-SPI1	ADC-SPI2	ADC-SPI2	ADC-SPI2
6	KLM-FIO1	KLM-FIO2	KLM-FIO3	KLM-FIO4	Dx+	Dx-
7	RESET+	RESET-	gnd	gnd	gnd	gnd
8	RTM_CLK4+	RTM_CLK4-	RTM_CLK2+	RTM_CLK2-	RTM_CLK5+	RTM_CLK5+
9	RTM_CLK0+	RTM_CLK0-	RTM_CLK3+	RTM_CLK3-	RTM_CLK1+	RTM_CLK1-
10	gnd	gnd	gnd	gnd	gnd	gnd
1	CH9_PA+	CH9_PA-	QDAC+	QDAC-	CH9_TF+	CH9_TF-
2	CH8_TF+	CH8_TF-	gnd	gnd	CH9_PA+	CH9_PA-
3	CH9_PA+	CH9_PA-	QDAC+	QDAC-	CH7_TF+	CH7_TF-
4	CH6_TF+	CH6_TF-	gnd	gnd	CH9_PA+	CH9_PA-
5	CH9_PA+	CH9_PA-	QDAC+	QDAC-	CH5_TF+	CH5_TF-
6	CH4_TF+	CH4_TF-	gnd	gnd	CH9_PA+	CH9_PA-
7	CH9_PA+	CH9_PA-	QDAC+	QDAC-	CH3_TF+	CH3_TF-
8	CH2_TF+	CH2_TF-	gnd	gnd	CH9_PA+	CH9_PA-
9	CH9_PA+	CH9_PA-	IDAC+	IDAC-	CH1_TF+	CH1_TF-
10	CH0_TF+	CH0_TF-	gnd	gnd	CH9_PA+	CH9_PA-

We need common region for interlock signals

Zone 3 Connector of uTC and uFMC25

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS
3	SFP1-TX+	SFP1-TX-	SFP1-RX+	SFP1-RX-	INTERLOCK 1	INTTERLOCK 2
4	SFP2-TX+	SFP2-TX-	SFP2-RX+	SFP2-RX-	RTM_D5+	RTM_D5-
5	RTM_D6+	RTM_D6-	RTM_D7+	RTM_D7-	RTM_D8+	RTM_D8-
6	RTM_D9+	RTM_D9-	RTM_D10+	RTM_D10-	RTM_D11+	RTM_D11-
7	gnd	gnd	81MHz+_O	81MHz-_O	gnd	gnd
8	gnd	gnd	RTM_CLK2+_I	RTM_CLK2-_I	MGT_CLK+_O	MGT_CLK-_O
9	URTM_CLK0+_O	URTM_CLK0-_O	gnd	gnd	SP6_CLK1+_O	SP6_CLK1-_O
10	RTM_main+_I	RTM_main-_I	gnd	gnd	gnd	gnd
1	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
2	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
3	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
4	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
5	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
6	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
7	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
8	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
9	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
10	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-

Zone 3 Connector of DAMC2

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS
3	CLK_EC_RTM+_O	CLK_EC_RTM-_O	RTM1+	RTM1-	RTM1+	RTM1-
4	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
5	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
6	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
7	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
8	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
9	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
10	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
1	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
2	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
3	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
4	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
5	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
6	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
7	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
8	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
9	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
10	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-

Zone 3 Connector of TEWS TAMC651

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS
3	RTM_CLK0+_O	RTM_CLK0-_O	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
4	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
5	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
6	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
7	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
8	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
9	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
10	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
1	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
2	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
3	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
4	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
5	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
6	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
7	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
8	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_CLK1+_O	RTM_CLK1-_O
9	GTP1_CLK0+_I	GTP1_CLK0-_I	GTP0_Rx+	GTP0_Rx-	GTP0_Tx+	GTP0_Tx-
10	GTP1_CLK1+_I	GTP1_CLK1-_I	GTP1_Rx+	GTP1_Rx-	GTP1_Tx+	GTP1_Tx-

Zone 3 Connector of NAT MCH

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS

...more problems:

- Digital signals
- Gb Ethernet
- SATA
- PCIe x4/x8
- more sophisticated signals...

Proposal for Digital Class – High-speed Links

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	AMC_SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	AMC_SCL	RTM_TDI	RTM_TMS
3	SFP1-TX+	SFP1-TX-	SFP_AMC_CLK+	SFP_AMC_CLK-	SFP2-TX+	SFP2-TX-
4	SFP1-RX+	SFP1-RX-	SFP_RTM_CLK+	SFP_RTM_CLK-	SFP2-RX+	SFP2-RX-
5	INTERLOCK 1	INTERLOCK 2	P30_IO+	P30_IO-	P30_IO+	P30_IO-
6	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
8	AMC_CLK1+	AMC_CLK1-	AMC_CLK2+	AMC_CLK2-	AMC_CLK3+	AMC_CLK3-
9	RTM_CLK1+	RTM_CLK1-	RTM_CLK2+	RTM_CLK2-	RTM_CLK3+	RTM_CLK3-
10	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
3	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
4	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
7	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
8	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
9	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
10	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-

Proposal for Digital Class – Low-speed Links

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	AMC_SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	AMC_SCL	RTM_TDI	RTM_TMS
3	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
4	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
5	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
6	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
8	AMC_CLK1+	AMC_CLK1-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
9	RTM_CLK1+	RTM_CLK1-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
10	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
3	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
4	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
7	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
8	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
9	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
10	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-

Summary

- We propose Zone 3 signals for digital class devices
- We need to provide guideline how to use this signals
- Connection of all digital signals consumes a lot of FPGA Ios
- How to include other interfaces (PCIe, GbE, SATA, sRIO, etc.)
- Do we need reset in digital class ?

Thank you for your attention

Any suggestions, comments?