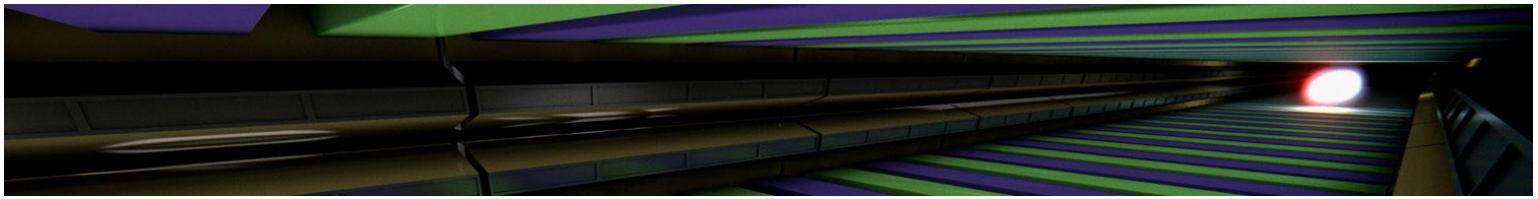


Overview of the MTCA.4 and ATCA based DAQ electronics and concepts for the XFEL

MicroTCA Workshop for Industry and Research

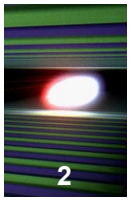
11th – 12th December 2012

Patrick Gessler

European XFEL GmbH

European XFEL

Agenda



- Usual applications at photon experiments and diagnostics
- DAQ challenge and data management architecture
- MTCA and ATCA hardware and concepts to implement the DAQ
  - Architecture
  - MicroTCA and ATCA Modules and Interfaces
  - VETO System
- High-level FPGA firmware development

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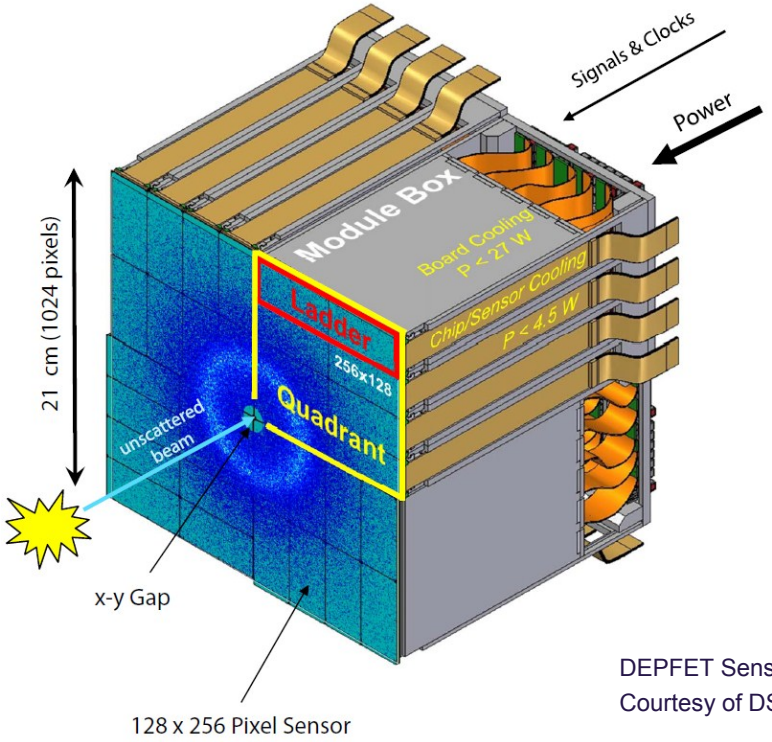
Usual Applications at Experiments

- Energy measurement
- Photon counting
- Time of Flight type measurements
- 2D picture detection
  - ➔ Example: DSSC



DEPFET Sensor with Signal Compression (DSSC)
Courtesy of DSSC Consortium

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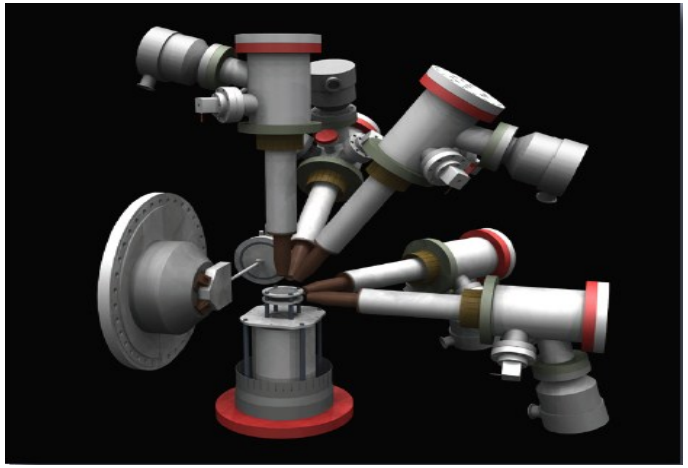
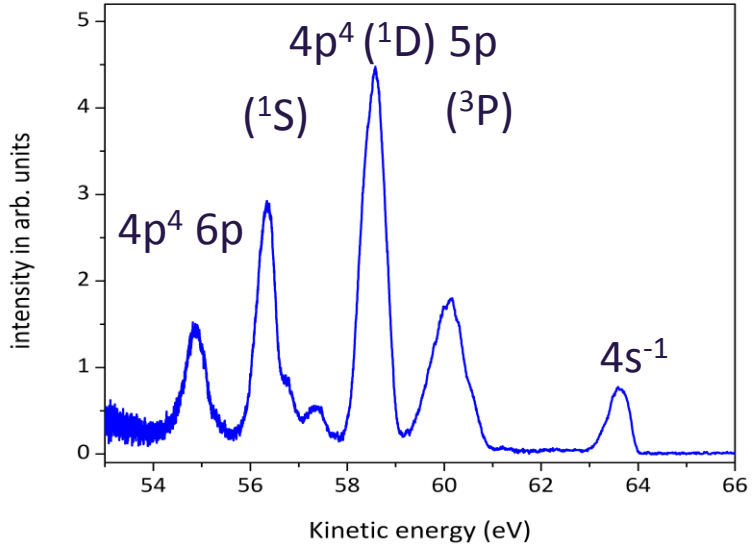
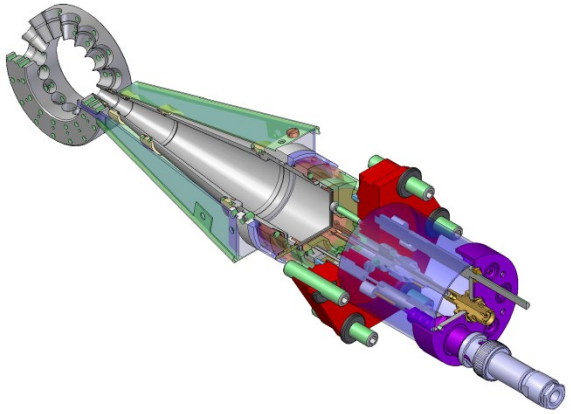
Applications: Time of Flight measurements



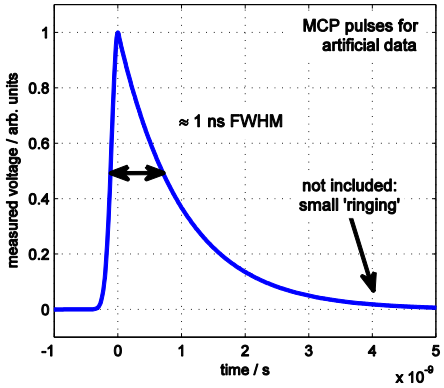
Courtesy of John Bozek (AMO endstation at LCLS)

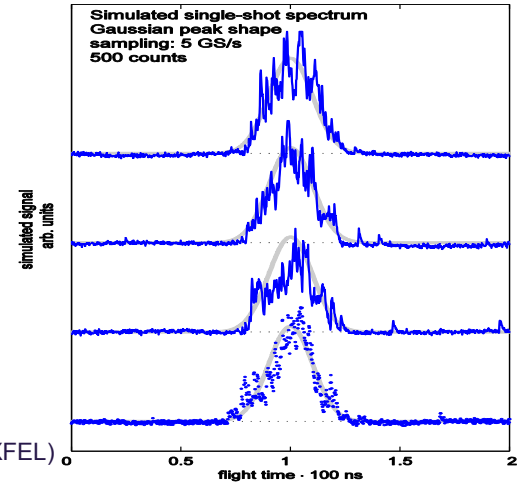


Courtesy of T. Mazza, M. Meyer SQS (XFEL)



Courtesy of Frank Scholz, Jens Viefhaus (DESY)





Courtesy of Jens Buck (XFEL)

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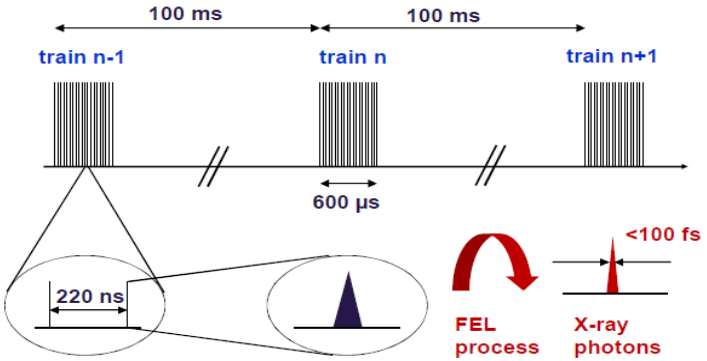
DAQ challenge

- Readout rate driven by bunch structure
  - 10 Hz train of pulses
  - 4.51 MHz pulses in train
- Data volume driven by detector type



Detector type	Sampling	Data/pulse	Data/train	XFEL/sec	LCLS/sec
1 Mpxl 2D camera	4.5 MHz	~2 MB	~1 GB	~10 GB	~300 MB
1 channel digitizer	5 GS/s	~2 kB	~6 MB	~60 MB	~0.2 MB

Challenges:

- Per detector data volumes are large, sometimes very large
- Modular and electronic design of large detector front ends requires
  - down stream image building, pixel reordering
  - multiplexing of control signals
- Overcoming limitations in front end signal (pipeline) storage depth
- Gathering and storing of data from many detectors per experiment

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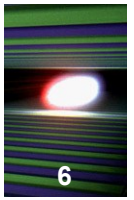
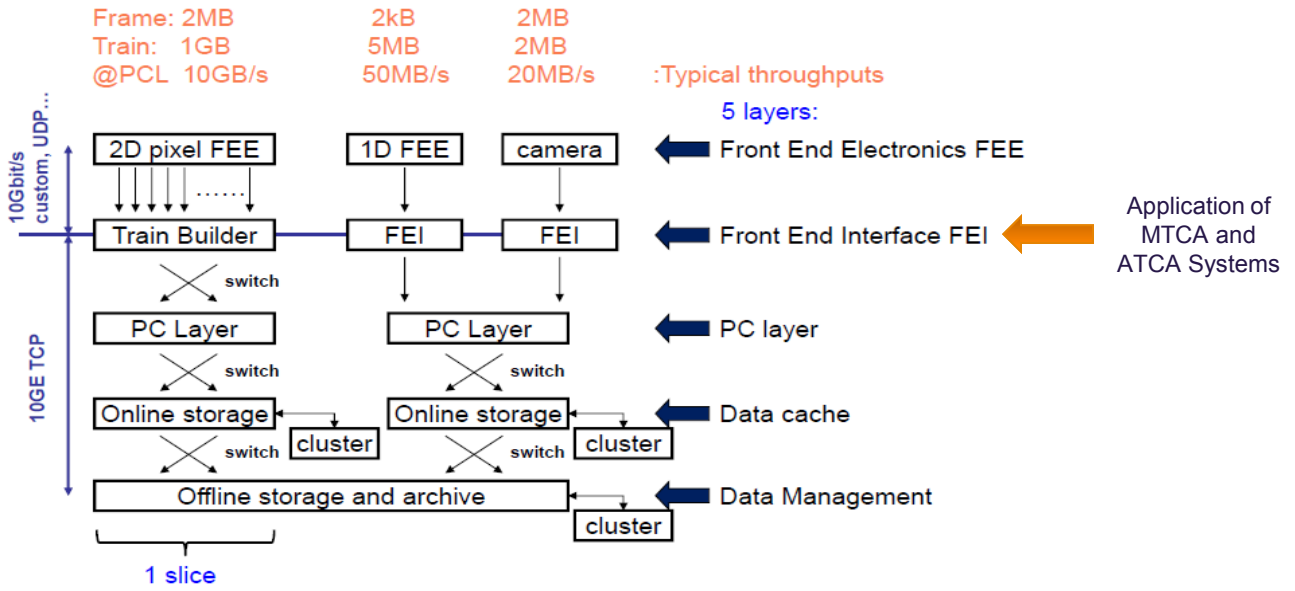
Data management architecture



Large data volumes, their acquisition, storage and analysis and changing experiment configurations are issues the PBS system architecture is trying to solve

Architecture chosen



- Multiple layers with well defined APIs
  - to allow insertion of new technology layers
- Multiple slices for partitioning and scaling
  - camera sizes will increase and slice replication will be one solution
- Allow full speed write through to online storage, but discourage usage
  - sometimes this capability is needed to understand measurement
- Enforce data reduction and rejection in all layers
  - early data size reductions and data rejection are needed to reduce storage resources

Day one 2015/16
10PB offline disk storage.

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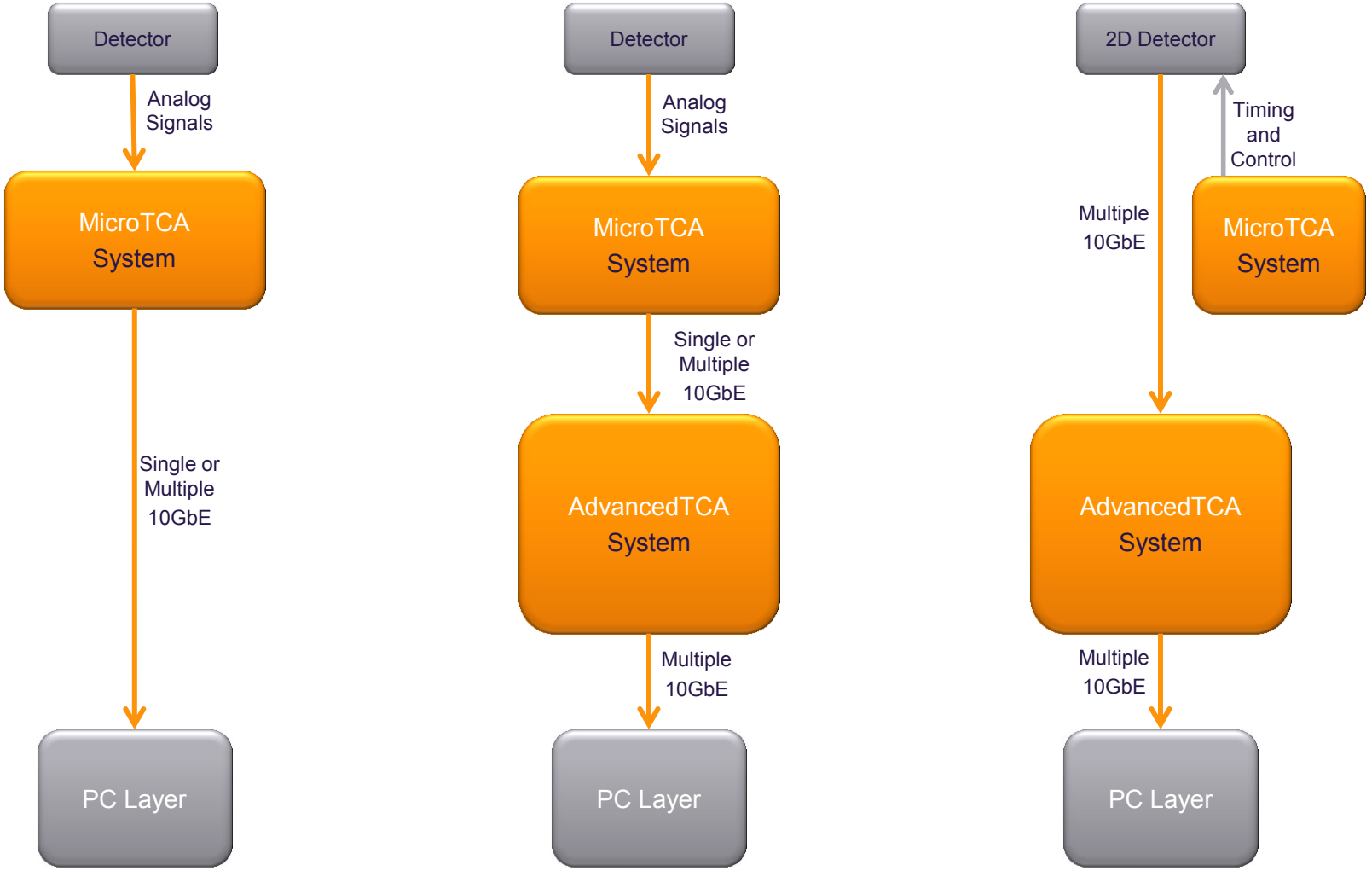
MTCA and ATCA Hardware and Concepts



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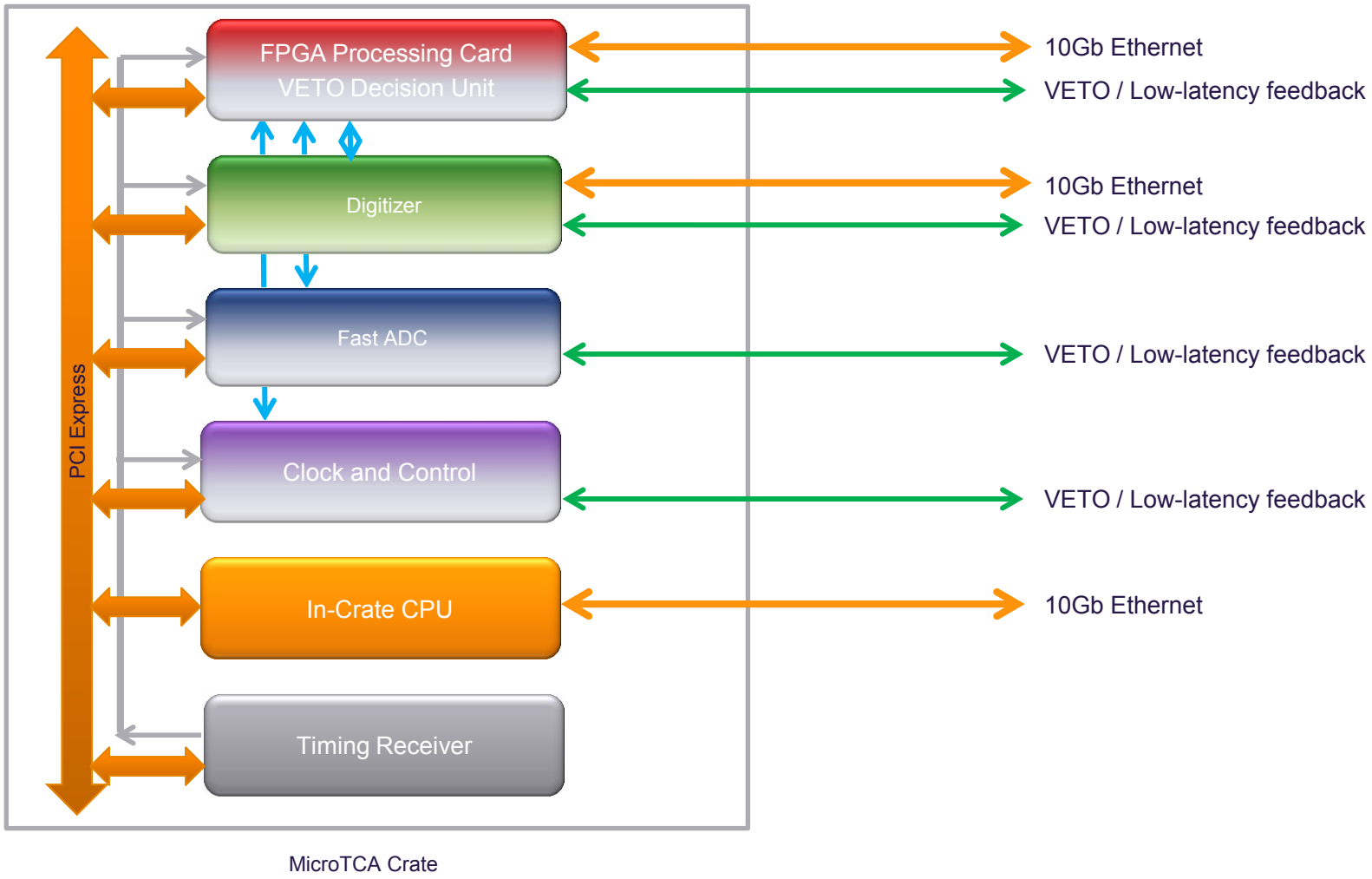
MicroTCA Modules and Interfaces



MicroTCA Crate

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MicroTCA Modules and Interfaces

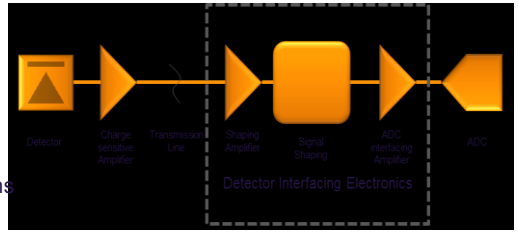
- Digitizers
  - ADQ Family from SP Devices
    - → 1.6GSPS / 14bit / 1 channel
    - → 2GSPS / 12bit / 4 channels
    - → 4GSPS / 12bit / 2 channels
    - → 7GSPS / 8bit / 1 channel
  - 10GbE on front panel (SFP+)
  - VETO / Low-latency feedback on front panel (SFP)
  - Xilinx Virtex 6 FPGA
  - FPGA access for custom algorithms

ADQ412-3G from SP Devices Sweden AB

- Fast ADCs
  - SIS8300 from Struck Innovative Systems
  - 125MSPS / 16bit / 10 channels
  - Xilinx Virtex 5 FPGA
  - Full access to FPGA for custom firmware
  - RTM support
    - → Used for signal shaping (pulse stretching)

SIS8300 from Struck Innovative Systems

Pulse Stretcher RTM for SIS8300
(Peter Goettlicher, DESY)



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MicroTCA Modules and Interfaces

- Timing Receiver
  - Development of DESY and Stockholm University
  - Providing facility wide synchronized
    - Clocks
    - Triggers
    - Machine information

XFEL Timing Receiver (X2TIMER)
(Stockholm University/DESY)

- Clock and Control System
  - Based on DAMC2 (DESY) and custom RTM (UCL)
  - Synchronizes to the Timing Receiver
  - Provides 16 outputs to a 1MPix 2D detector for
    - Reference clock
    - Triggering
    - Machine information
    - VETO information
  - For larger detectors multiple modules are used and synchronized in a crate

Clock and Control RTM
(University College London)

DAMC2
(DESY, FEA)

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MicroTCA Modules and Interfaces

- FPGA Processing Card and
- VETO Decision Unit
  - uTC Module from DMCS and DESY
  - Planning to use the upcoming version (not shown)
  - Provides
    - → Many input/output high-speed serial links
    - → Powerful FPGA
    - → On-board Memory

High-performance DSP and FPGA board (uTC) (DMCS/DESY)

- CPU
  - Looking for a standard CPU (usually i7 based) with
    - → 10GbE (maybe dual) support
    - → Unfortunately not found yet!
  - Currently
    - → Using Concurrent and ADLink CPUs (1GbE only)
    - → Investigating QorIQ based module from N.A.T. with 10GbE

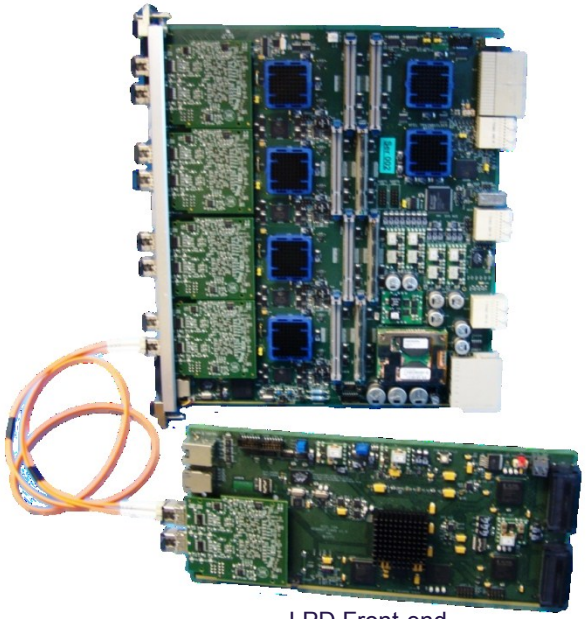
AM310 Intel based CPU (Concurrent)

P4080 QorIQ based CPU with FPGA (N.A.T.)

ATCA Module and Interfaces

- Train Builder Blade
  - Used for data concentration and processing
    - → Mostly 2D detectors, but also
    - → Digitizer data
  - Module from Rutherford Appleton Lab (STFC)
  - With FMC Modules from DESY/FEA
  - Provides
    - → Up to 8x 10GbE on SFP+
    - → 4x Xilinx Virtex 5 FPGAs for processing
    - → DDR2 and QDR memories
    - → Crosspoint switch for flexible interconnections to Zone 3 connector used to
      - Connect to further Train Builders
    - → 1GbE interface to 5th FPGA for management and control

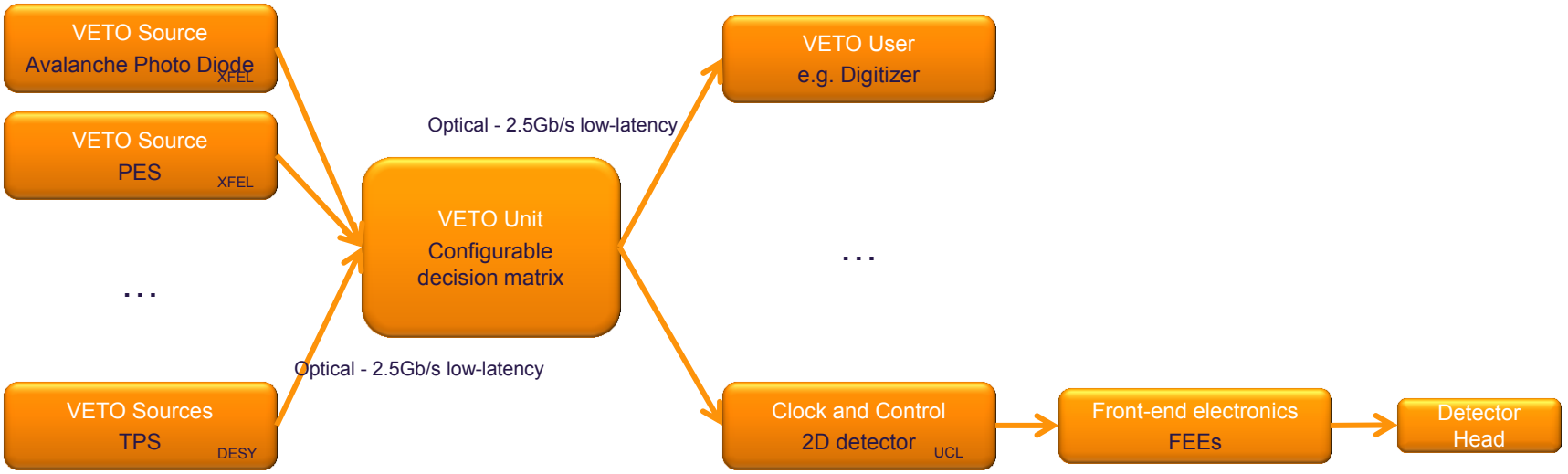
Train Builder



LPD Front-end module (FEM)

VETO System for data reduction and memory optimization

- Optimize picture quality of 2D detectors
  - Limited frame capacity in ASICs (~300-700 frames)
  - Replace bad frames with new ones in ASIC before read out and transmission
- Data reduction
  - Discard useless data before transmission
- Implementation
  - FPGAs of diagnostics and detectors provide bunch information with low-latency
  - Configurable central VETO unit per experiment decides on bunch quality
  - FPGAs of detectors (maybe also diagnostics) receive the decision and react on it
  - Using a common protocol with beam based feedback system



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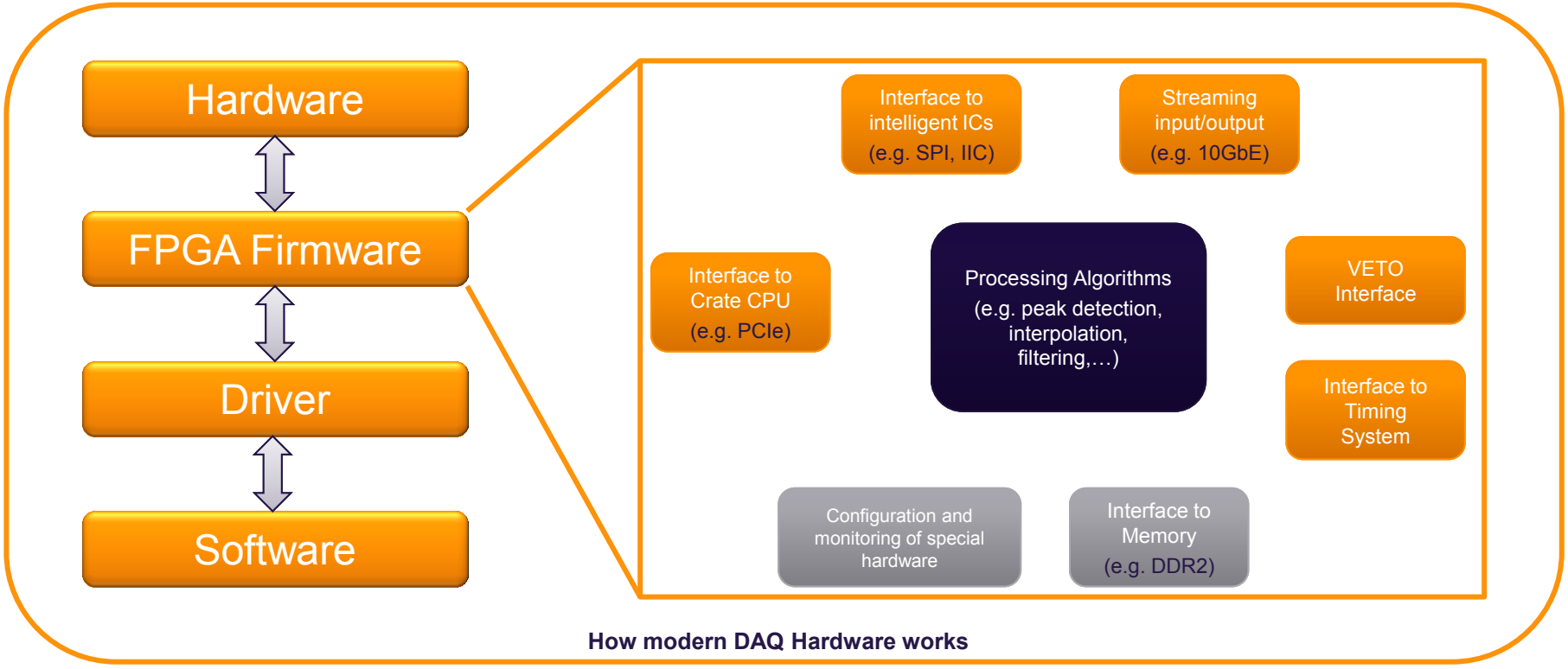
FPGA Framework - Overview

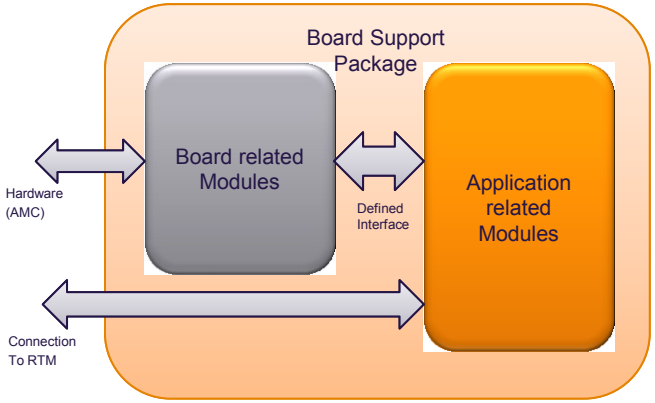
- Three important factors
  - 100% of the DAQ related modules use FPGAs (Complex programmable logic)
  - FPGA programming is time intensive and requires specialized people
  - Many hardware is used in different projects by different people

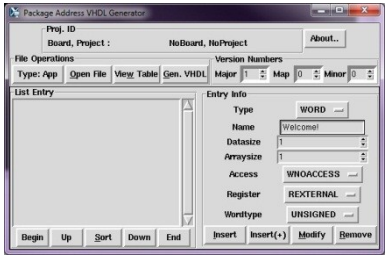


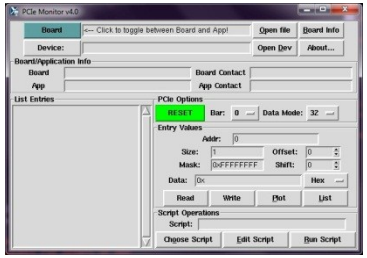
How modern DAQ Hardware works

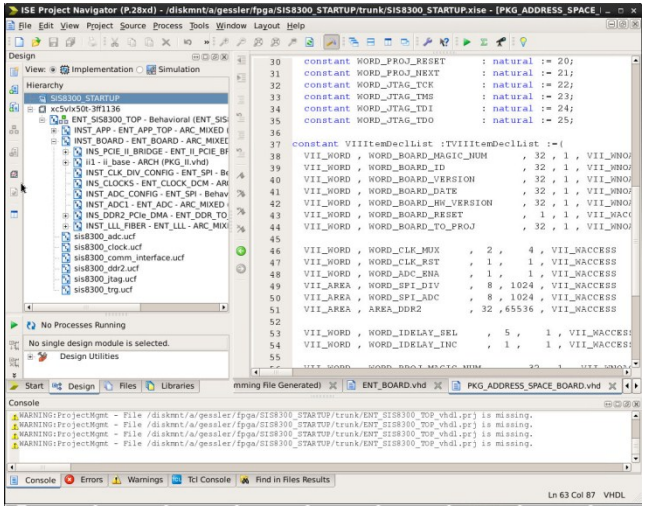
FPGA Framework – Status (Low-Level)

- Implementation of low-level Framework ready
  - Includes code from DESY, XFEL, Collaborators, Open platforms
  - Tutorials had been done
  - Improvements and adding of features ongoing
  - Limited documentation available
- Software tools developed and available
  - Register/Memory access with plotting
  - Register and memory map generation
  - Firmware upload
  - PCIe and driver management









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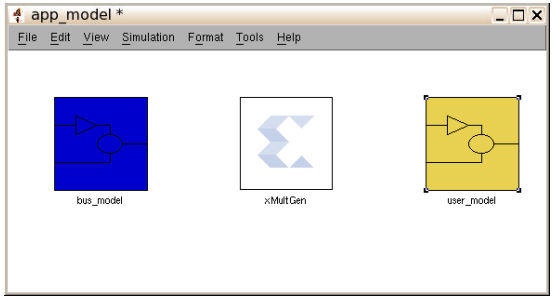
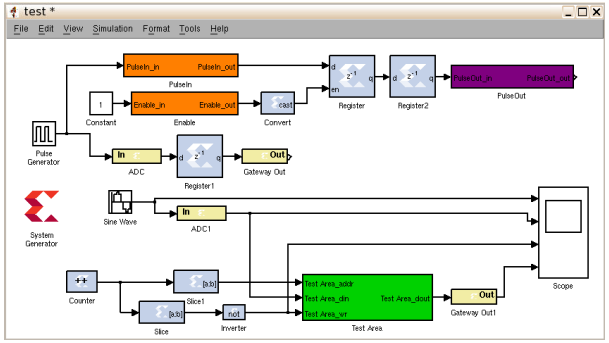
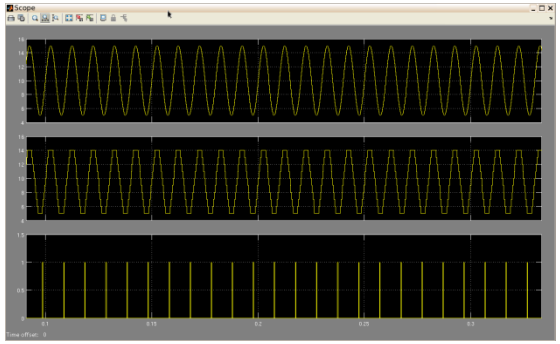
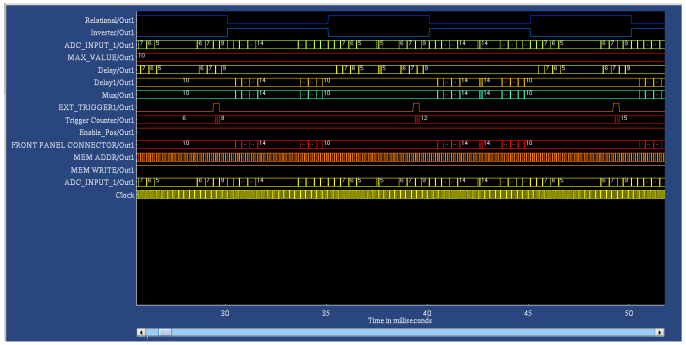
FPGA Framework – Status (High-Level)

- We are in prototyping stage
  - Tests of features like
    - Automatic register and memory mapping
    - Integrated image generation and deployment
    - Algorithms for detector signal handling
    - Library organization and distribution
  - Successfully generated firmware for our digitizers
- Plan to consolidate and then collaborate with similar Framework developed for Astrophysics (e.g. SKA) within EU FP7 CRISP project









Time for questions and discussion…