Signal Processing Devices Sweden AB

SP Devices DAQ MTCA.4 offering for demanding applications in Physics

L.Weber December 11th, 2012

SP Devices

Signal Processing Devices DAQ MTCA.4 offering for demanding applications in Physics. AGENDA

➢ High vertical resolution & High speed digitizers needs.

➢ Extended real time data processing.

➢ Multi-Channel Synchronization for MTCA4 Digitizers.

SP Devices

SP Devices in brief

- ✓ Signal Processing Company with IP business model
- ✓ Founded 2004
  - ✓ Spin-off from Linköping University
  - ✓ Research since 1998
- ✓ Several patent applications
- ✓ About 25 employees, 8 PhD
- ✓ Approx 5 MUSD total funding by SEB Venture Capital
- ✓ Swedish company with US
- ✓ Offices in Linköping, Sweden

Our History

SP Devices
Signal Processing Devices

Infineon
Never stop thinking

In 2007 SP Devices acquired the Infineon office in Linköping. In Linköping, Infineon designed A/D and D/A converters.

Linköping University

All founders share a background from Linköping University. One founder works in our San Diego office.

ERICSSON
TAKING YOU FORWARD

Approximately one third of the engineers at SP Devices have a background within Ericsson Microelectronics (which was acquired by Infineon)

SP Devices

Company Expertise & Products

LEADING EDGE R&D AND KNOW-HOW

Well respected research

- ➢ Authors of respected books in the industry
- ➢ Research projects together with universities and research departments at Ericsson, Infineon, ST and others.

OFFERING

Silicon, FPGA Increasing performance of existing and future ADC solutions leading to Software IP

- ➢ ADX - Interleaving of ADC (ADX2, ADX4, ADX8)
- ➢ ADL - Linearization of ADC

High-speed digitizers

- ➢ DAQ Boards
- ➢ Acquisition & Generation board
- ➢ Custom systems
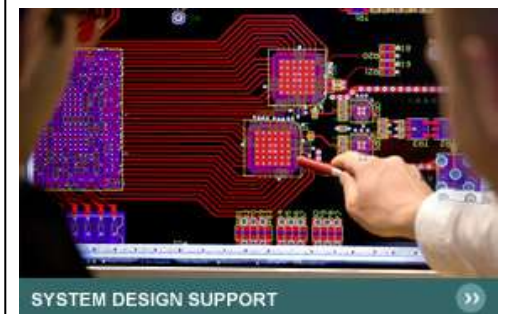
SILICON & FPGA IP

HIGH SPEED DATA ACQUISITION

SYSTEM DESIGN SUPPORT

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Signal Processing Devices Company Profile

SP Devices provides innovative, advanced data acquisition expertise to a global customer base of leading physicists seeking high-performance technologies.

Thanks to his leading edge R&D and Know-how on increasing performance of existing and future ADC, SP Devices is very well connected with both ADC and FPGA community (*) (**).

ABOUT OUR DIGITIZING OFFERINGS

Thanks to a very significant level of expertise in the analog design, waveform processing, digital design and system architecture, SP Devices became a leader in high speed data acquisition and gained worldwide recognition for the design and production of high speed/ high resolution digitizers (14-bit, multi GSPS) associated to top end processing (Xilinx Virtex 6 & 7)
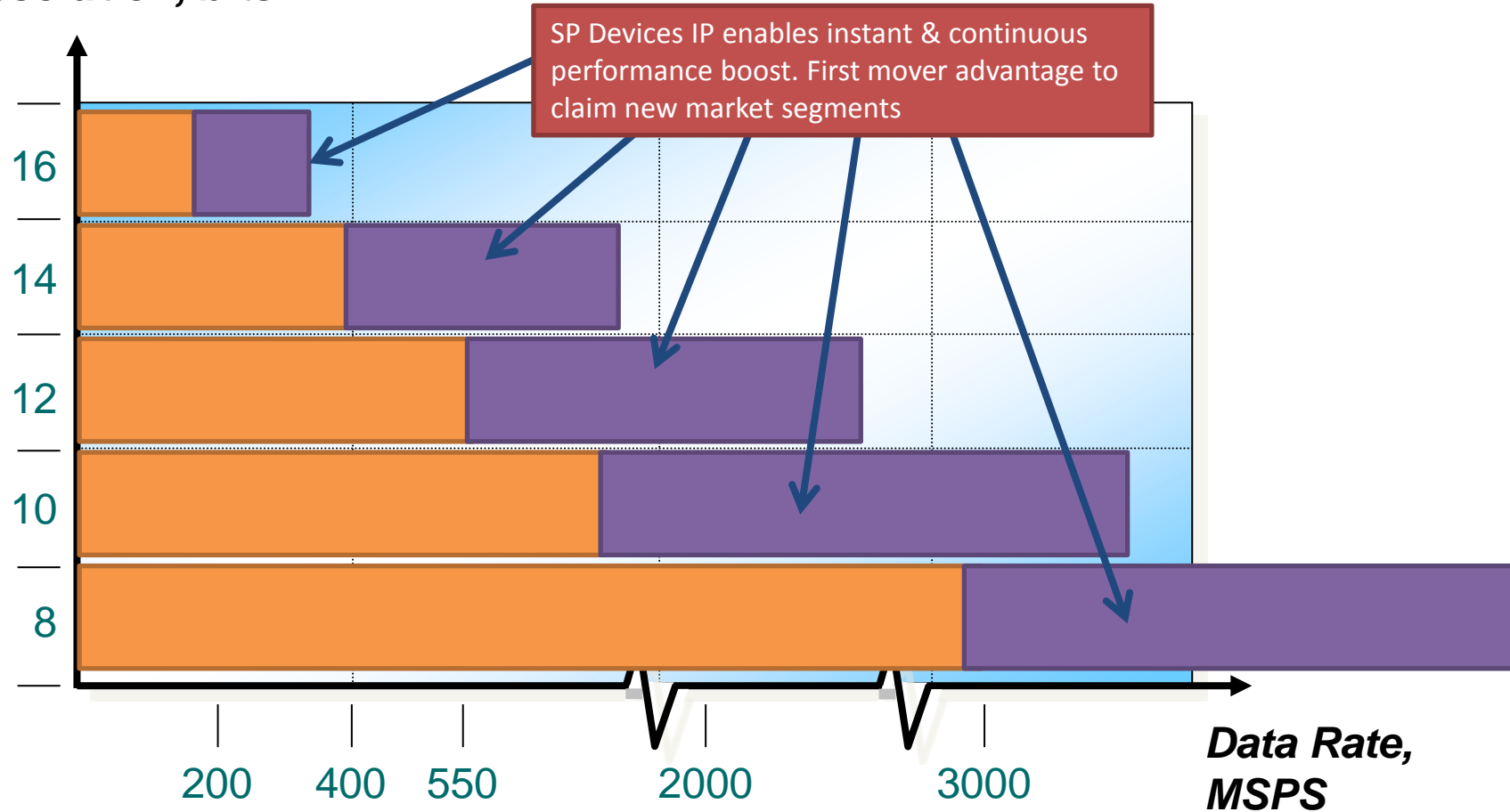
(*) SP Devices partner of TI, Analog Devices, Intersil, NXP
(**) SP Devices partner of Xilinx

ADX Series Performance Leap

Resolution, bits

SP Devices IP enables instant & continuous performance boost. First mover advantage to claim new market segments

200 400 550 2000 3000

Data Rate, MSPS

16

14

12

10

8

SP Devices

Digitizer Technology Offers

➤ Analog front end is optimized for signal fidelity

➤ SP Devices' IP for enhancing the performance of ADCs

➤ Designed for flexibility

- Software API

- Open FPGA

➤ Four levels of design service

- Off-the-shelf solutions

- Software design service for application design and systems integration

- FPGA design service for real time DSP integration

- Full custom solutions including hardware design

SP Devices

COTS Digitizer Customer Value Proposition

Better Measurement Fidelity.

- Interleaving technology
- ADX Series Performance Leap
- Incorporates SP Devices FPGA-IP for enhancing the performance of ADCs

More flexibility

- Designed for flexibility
- Delivered with software API:s
- Customers can develop and deploy custom signal processing FPGA code, using multiple modules

Higher Measurement throughput with architectures based on

- Top existing resources like Xilinx Virtex 5 and Virtex 6
- PCIe 4 & 8 lanes bus

Lower total cost of ownership

- USB versions of all products
- ADQ API/ ADCapture Lab/ Matlab interface/ Documentation

SP Devices

ADQ V6 Platform Concept

➢ Based on a Carrier / Mezzanine board concept

➢ Xilinx Virtex 6, memory, power supply, PXI and PCI Express interface and USB interface available on motherboard.

➢ ADCs and clocking on daughterboard

➢ *Available mezzanine boards*:

   – 1 channel,   7 GS/s,   8-bit
   – 1 channel, 1.6 GS/s, 14-bit
   – 2 channels, 3.6 GS/s, 12-bit or 4 channels, 1.8 GS/s,12-bit
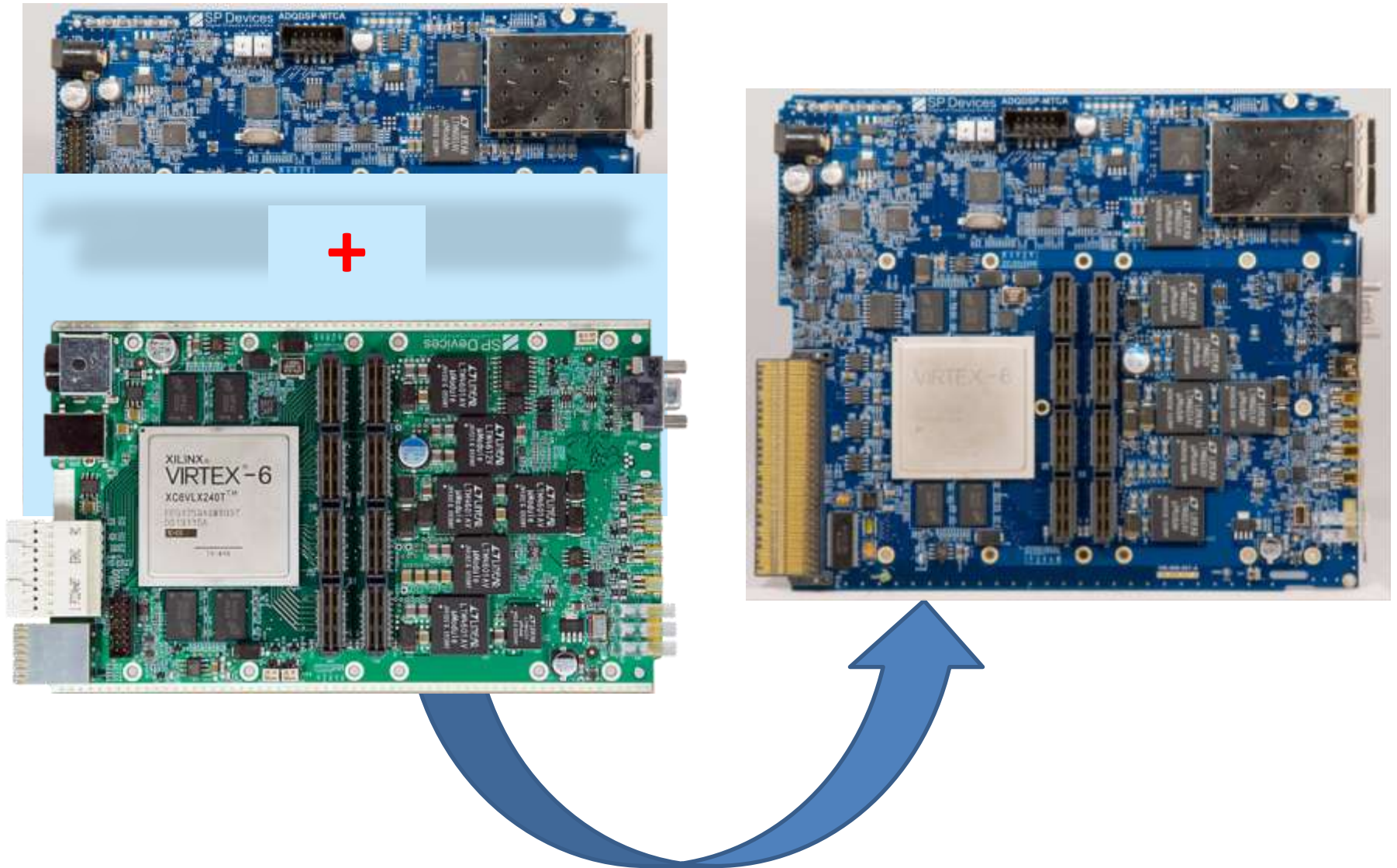   – 2 channels, 800 MS/s, 14-bit ADC and 2 channels, 1,6 GS/s, 14-bit DAC

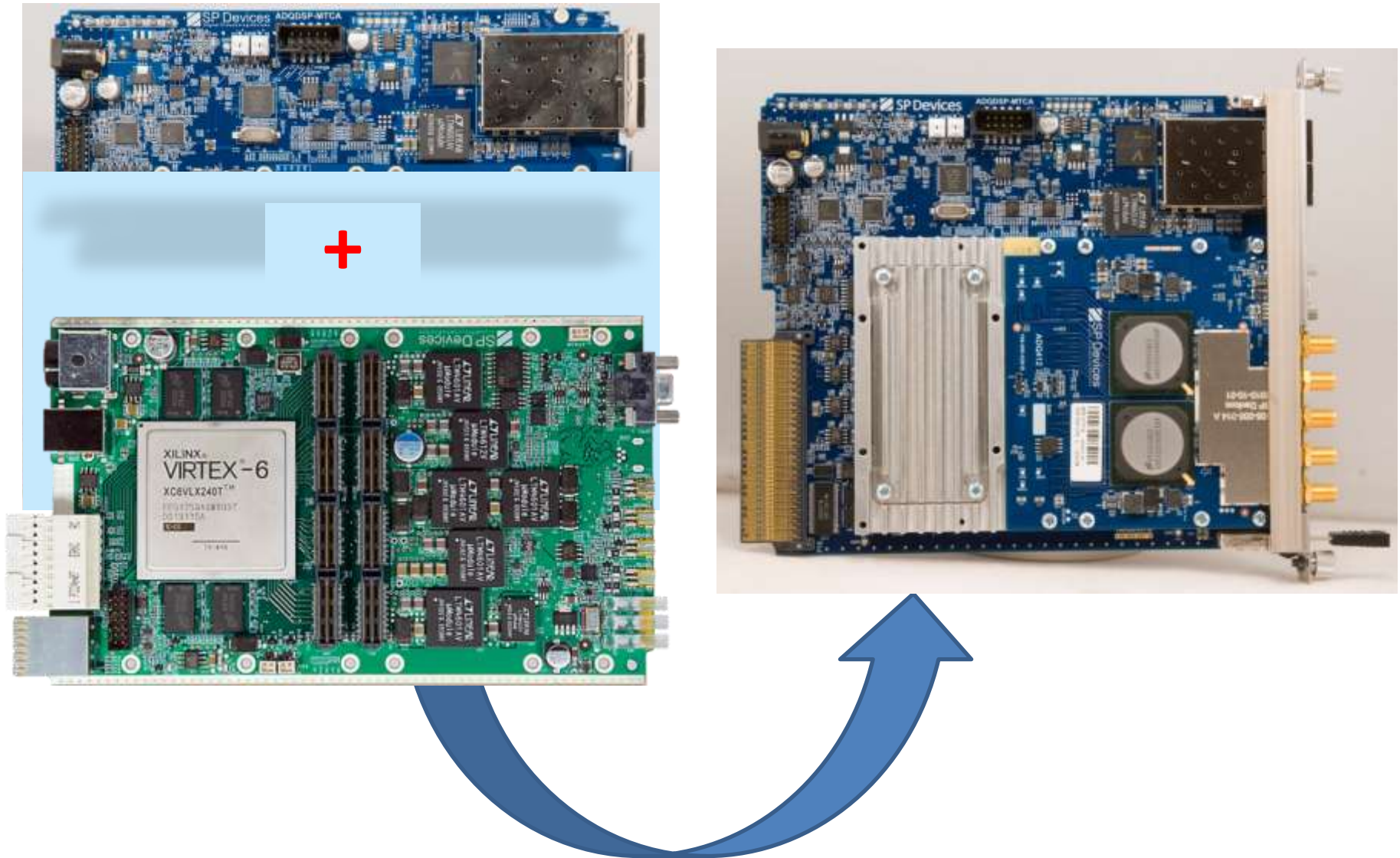**Carrier with mounted Mezzanine board**
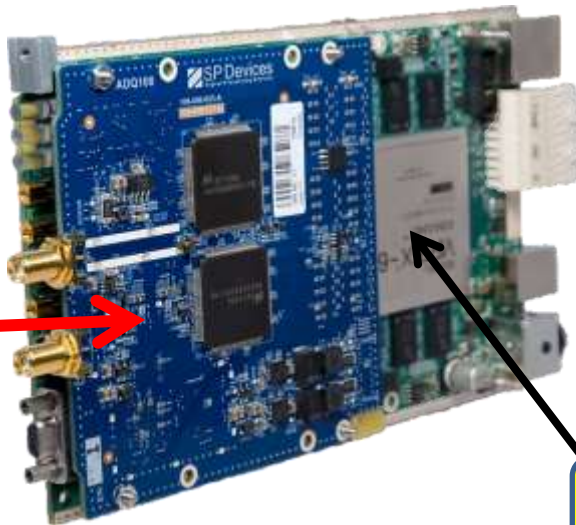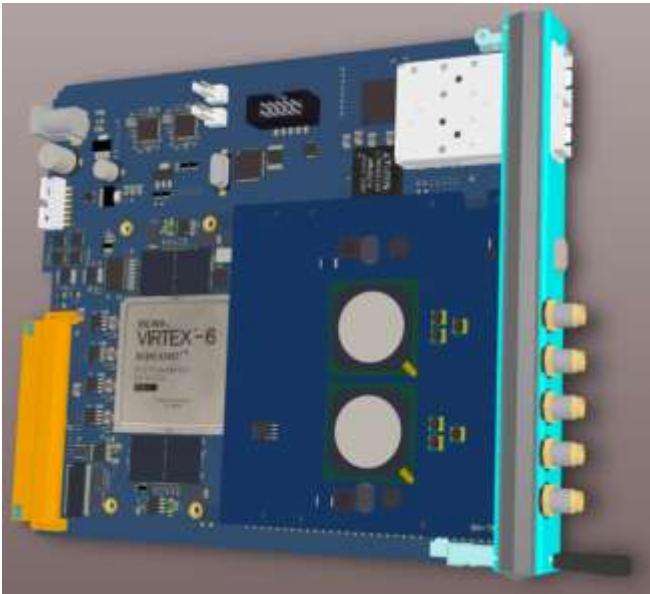
The ADQ V6 Carrier board

Mezzanine Board
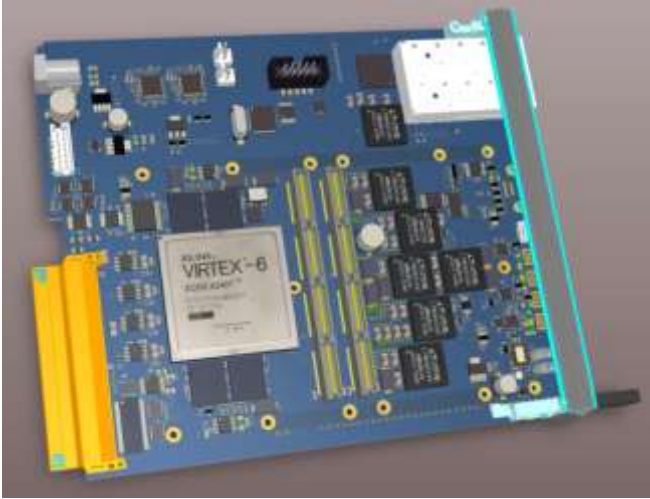
Carrier Board

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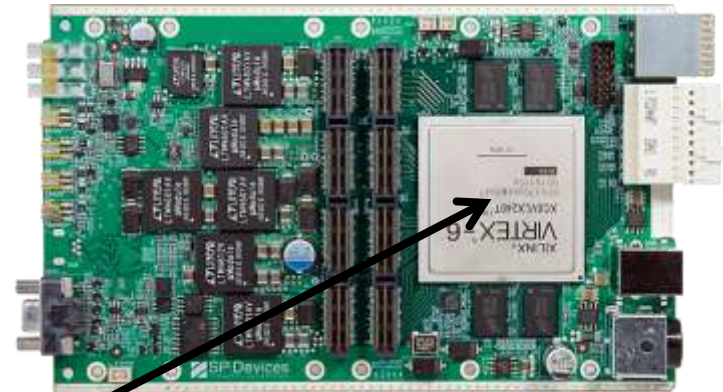
AMC Module : Expanded functionalities (prototype)

SP Devices

AMC Module : Expanded functionalities (production)

ADQ AMC screenshots
(with & without a daughter board)

ADQ V6 Series available in double width Mid-size AMC.0 MTCA.4 form factor

| Product	Function	Resolution	Sample Rate	# Channels	Memory	Interfaces
ADQ108	Digitizer	8 bit	7 GS/s	1	1024 MS	USB/PXIe/ PCIe/ MTCA4.
ADQ208	Digitizer	8 bit	4 GS/s on 2 channels	2	1024 MS	USB/PXIe/ PCIe/ MTCA4.
ADQ412	Digitizer	12 bit	1 GS/s on 4 channels 2 GS/s on 2 channels	4	700 MS	USB/cPCIe/PXIe/ PCIe/ MTCA4.
ADQ412-3G	Digitizer	12 bit	1.8 GS/s on 4 channels 3.6 GS/s on 2 channels	4	700 MS	USB/cPCIe/PXIe/ PCIe/ MTCA4.
ADQ412-4G	Digitizer	12 bit	2 GS/s on 4 channels 4G/s on 2 channels	4	700 MS	USB/cPCIe/PXIe/ PCIe/ MTCA4.
ADQ1600	Digitizer	14 bit	1.6 GS/s	1	512 MS	USB/cPCIe/PXIe/ PCIe/ MTCA4.
SDR14	Digitizer Generator	14 bit	800 MS/s ADC 1.6 GS/s DAC	2	256 / 256 MS	cPCIe/PXIe/ PCIe/ MTCA4.
ADQ416	Digitizer	16 bit	250 MS/s on 4 channels	4	512 MS	USB/cPCIe/PXIe/ PCIe/ MTCA4.
ADQDSP	Processing unit	-	-	-	1 GByte	USB/cPCIe/PXIe/ PCIe/ MTCA4.
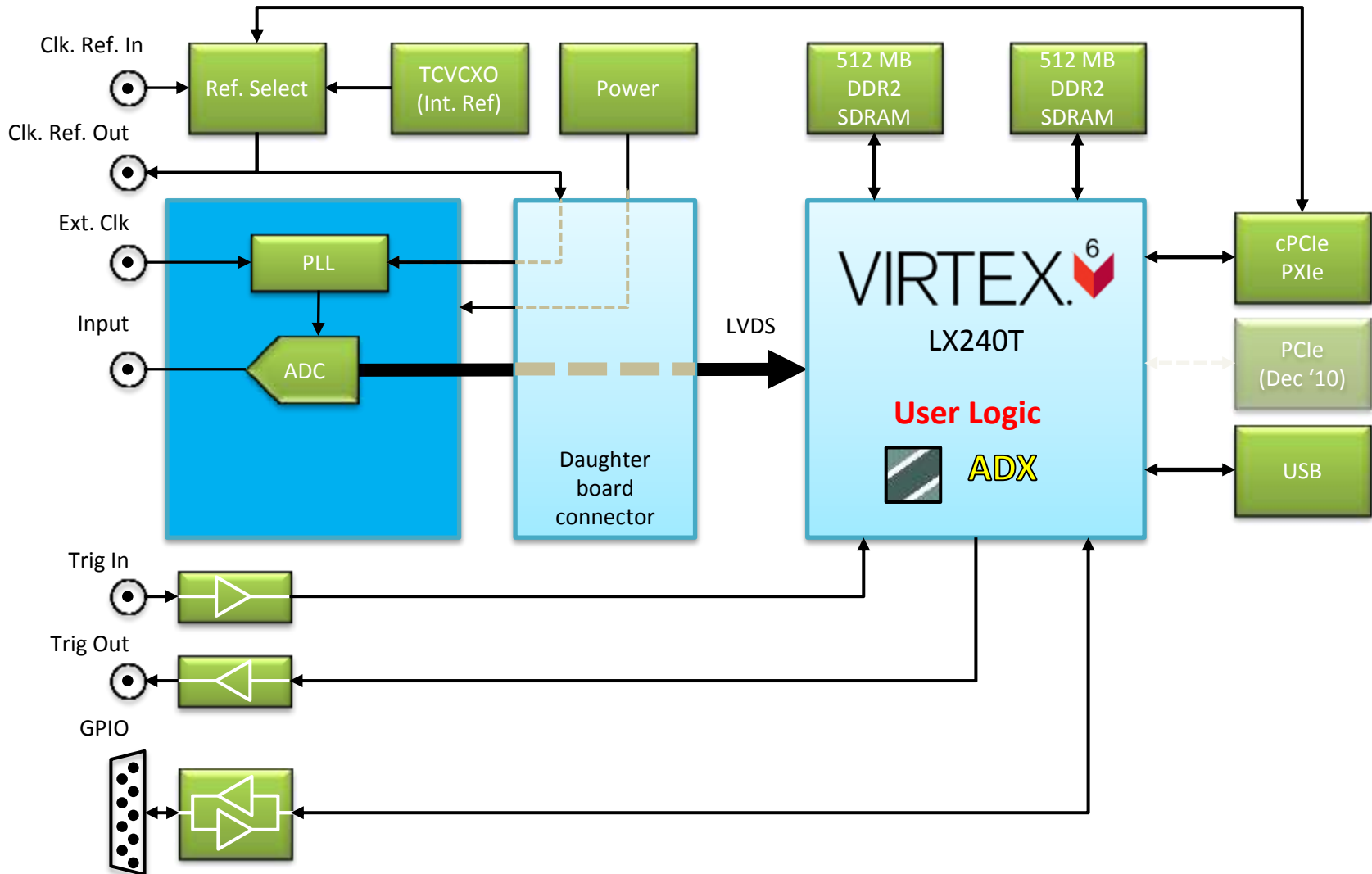
V6 Digitizer Concept

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Software Development Kit

Software Development Kit (SDK)

- ✓ **C/C++/C# API ("ADQ API")**
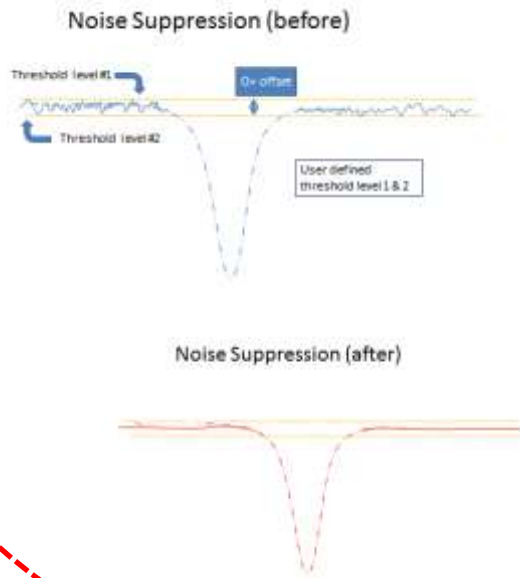- ✓ **ADCaptureLab**
- ✓ **Matlab**
- ✓ **Dynamic Link Library (DLL)**
- ✓ **Documentation**

Included in all product packages

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ADQ Development Kit

Accelerating your customization of ADQ-series DAQ cards!

Example of embedded processing:
- *Noise suppression*
- *Zero suppression*
- *Digital filtering*
- *Decimation*
- *FFT*

Noise Suppression (before)

Threshold level #1

0v offset

Threshold level #2

User defined
threshold level 1 & 2

Noise Suppression (after)

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ADQ Development Kit

- Xilinx ISE design project for custom FPGA code integration

- Enables custom real time operations

- Digitizer functions and hardware interface as NGC files

✓ SP Devices Source Code
✓ DSP Library Functions
✓ Reference Projects
✓ Documentation
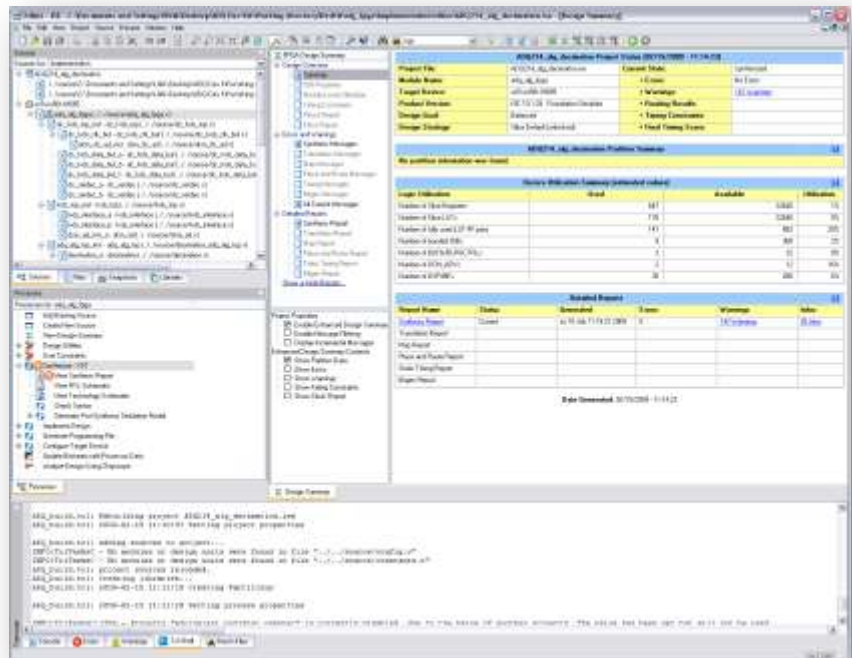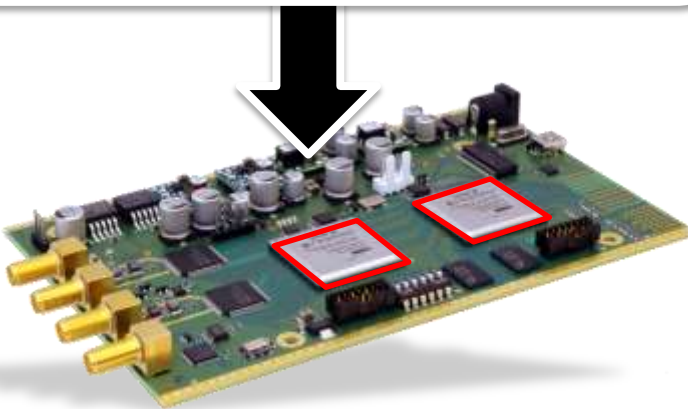
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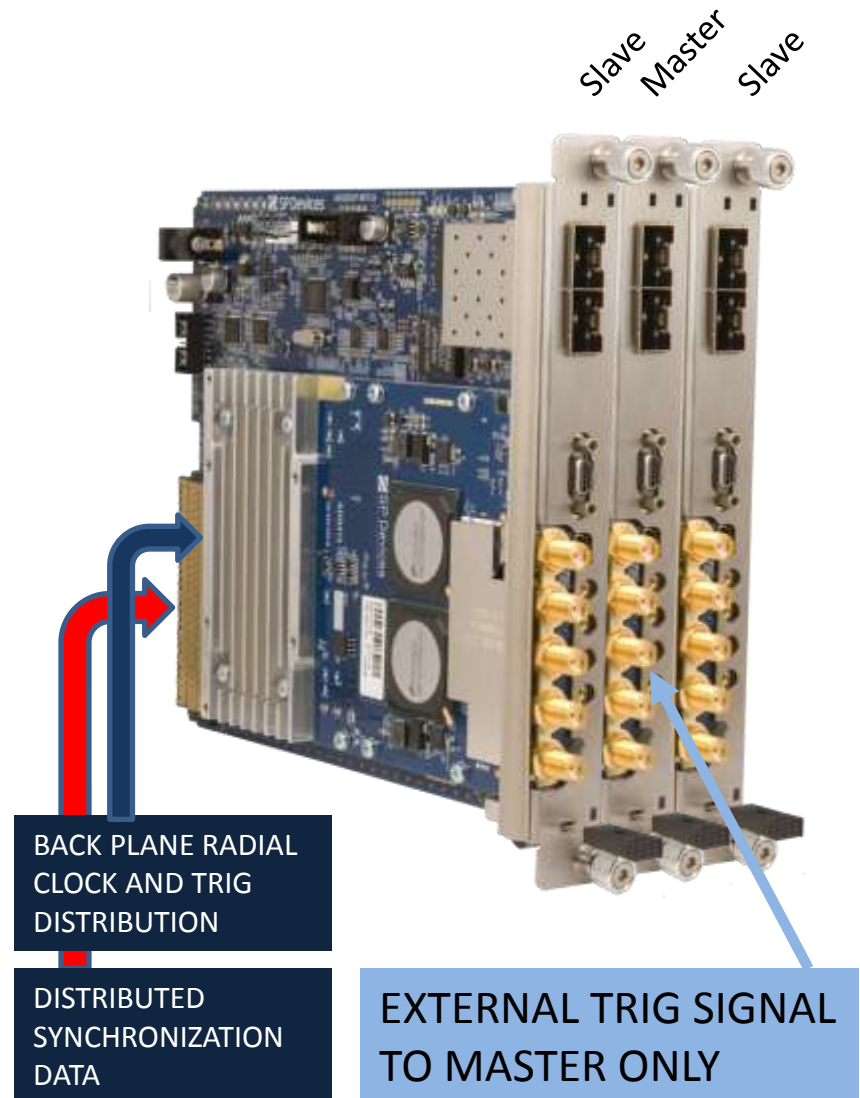

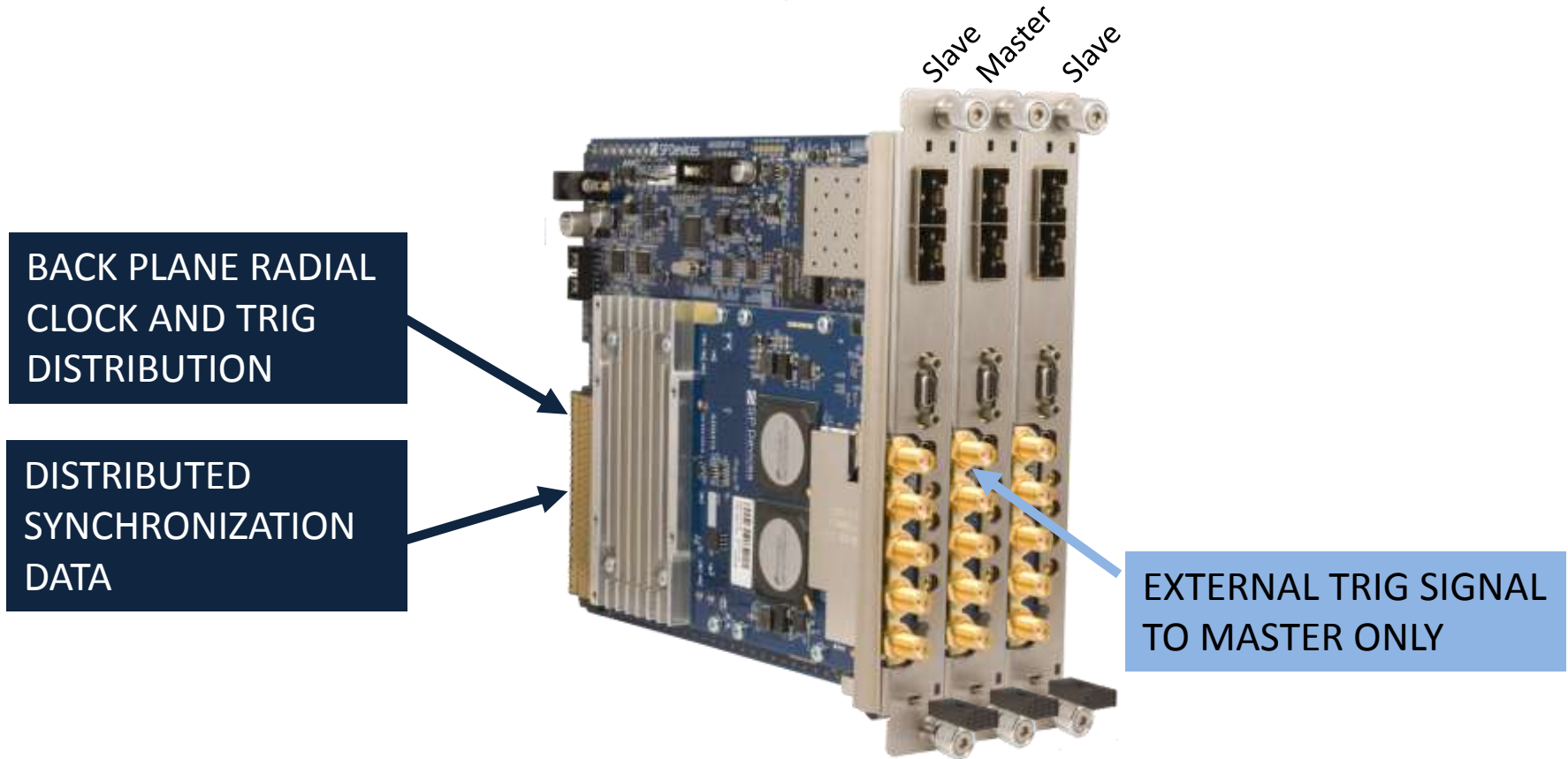SP Devices

Master-Slave Synchronization

A Master unit is defining the trigger time instant.

- It captures that time instant using for example an external trigger signal with a high-precision ext trig function.
- Thereafter, it distributes a trig signal on the back plane to all (multiple) Slave units along with a digital timing adjustment data value.
- The distributed trig signal is synchronous with the common back plane clock (for example 20 MHz) and the digital timing adjustment data value tells all Slave units the distance in samples between the sent out distributed trig signal and the trigger time defined by the Master unit.

All Slave units then produce the correct synchronism by reading out their data from their pre-trigger delay FIFOs adjusted to correct timing.

Slave   Master   Slave

BACK PLANE RADIAL CLOCK AND TRIG DISTRIBUTION

DISTRIBUTED SYNCHRONIZATION DATA

EXTERNAL TRIG SIGNAL TO MASTER ONLY

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Master-Slave Synchronization

BACK PLANE RADIAL CLOCK AND TRIG DISTRIBUTION

DISTRIBUTED SYNCHRONIZATION DATA

Slave   Master   Slave

EXTERNAL TRIG SIGNAL TO MASTER ONLY

- All digitizer channels in the system can take their samples synchronously at a time defined by one single trigger event.
- It requires that the MTCA4 chassis MCH (Micro-TCA Carrier Hub) can generate back plane clock signals of frequencies that distributes a low-jitter clock of suitable frequency (e.g. 10 MHz, 20 MHz, 50 MHz or 100 MHz) on TCLK1 or TCLK2 to serve as the reference frequency for all the digitizers and that such back plane clock is not too noisy.

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