

# MicroTCA Evaluation and Developments in the CERN PH-ESE Group

# MTCA Workshop for Industry and Research DESY, 11. December 2012

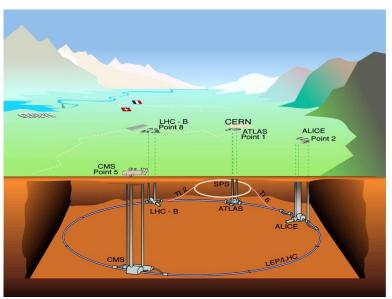
S. Baron, V. Bobillier, M. Di Cosmo, <u>S. Haas</u>, M. Joos, M. Barros Marin, S. Mico, F. Vasey, P. Vichoudis

#### Outline

- Introduction
- CERN PH-ESE MicroTCA evaluation project
  - Evalutation of commercial MicroTCA equipment
  - MicroTCA developments
    - MMC mezzanine
    - AMC and RTM load modules
  - MicroTCA power supply testing
- Gigabit Link Interface Board (GLIB)
  - Architecture
  - Hardware
  - Applications & status
- Summary

#### Introduction

- Major upgrades of the LHC experiments at CERN are foreseen over >10 years
  - Aligned with LHC upgrade long shutdowns: 2013/14, 2018, 2023
- Off-detector electronics of the LHC experiments mostly based on VME
  - Working very reliably
  - "Old" technology and doubts about long-term availability
- Experiments planning to use MicroTCA & ATCA for upgrades of their back-end electronics
  - MicroTCA: CMS
  - ATCA: LHCb & ATLAS
- xTCA advantages
  - Choice of form factors
  - Backplane bandwidth and protocols
  - Cooling and power supply
  - Redundancy (PSU, cooling)
  - Infrastructure monitoring features
- MicroTCA and ATCA developments already on-going at CERN and collaborating institutes
- Accelerator sector is also investigating MicroTCA
  - Front-end controller upgrade and linear collider project (CLIC)



# **xTCA Evaluation Project**

- Electronic Systems for Experiments (PH-ESE) group at CERN
  - Custom electronics design services for the experiments
  - Centralized services and support for modular electronics, instrumentation and power supplies
- MicroTCA evaluation project in CERN PH-ESE group launched in 2011
  - Technical evaluation of components for MicroTCA and MTCA.4 systems
  - Development of tools (H/W and S/W) for the testing of commercial components
  - Conduct market surveys
  - Report results (e.g. to the <u>xTCA Interest Group</u>)
- Recently expanded the evaluation project to also include ATCA
- Focus is on xTCA infrastructure components
  - Shelves and power supplies (electrical and cooling performance)
  - Shelf management
- Keep close contact with the xTCA development projects in the experiments
- Longer term goal
  - Try to standardize MicroTCA and ATCA shelves and power supplies at CERN
    - Could be difficult because many options (backplanes, cooling, RTMs, power supply, ...)
  - Define acceptance test procedures
  - Provide centralized support for these items

# **Commercial MicroTCA Equipment**

#### Equipment acquired & evaluated

- Vadatech 12 slot MicroTCA shelf (VT892)
- Schroff 6 slot MTCA.4 shelf
- Kontron MCH (with PCIe switch)
- NAT MCH (with PCIe switch)
- Kontron processor AMC (AM5030)
- Concurrent Technologies processor AMC (AM310)
- ELMA AMC load module
- ESD ADIO-24 AMC
- Polaris Networks xTCA tester S/W
- Evaluation results
  - Built up working systems using components from different vendors
  - Successfully integrated in-house designed AMC modules
  - Developed MicroTCA expertise in the section and disseminated results via the xTCA interest group
  - Many (mostly minor) interoperability problems encountered (IPMI related)
  - Components providing the same function (e.g. shelf or MCH)
     can have very different features and user interfaces (S/W)
  - Many options and possible customizations
    - Cooling, PSUs, data transfer protocols, backplane topology, ...



Vadatech shelf



Schroff shelf

## **MMC & Tester AMC Development**

- MMC hardware
  - Based on design from CPPM/Marseille
  - Small production made (<100)
  - Used on AMCs developed in-house
  - Distributed to external users
  - Plan to also turn into reference design for integration directly on an AMC module
  - Proposed as a standard for AMC designs in ATLAS
- MMC software
  - Based on code received from DESY
  - Clean split between generic and module specific code
  - RTM support tested with MMC tester and RTM load module
  - Code available in CERN SVN repository
- MMC tester AMC
  - MMC debugging & S/W development
  - On-board sensors, LEDs and test points
  - RTM emulation

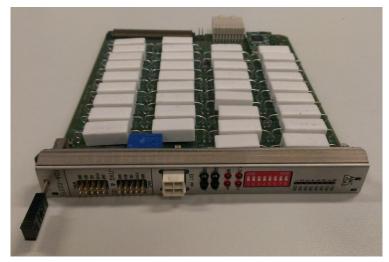
**MMC** mezzanine



**MMC test AMC** 

## **AMC & RTM Load Development**

- AMC and RTM load modules developed inhouse
  - Based on switched resistive loads
  - Control via MMC or front-panel
  - Temperature monitoring to evaluate cooling performance
- Produced enough modules to fully populate and load a 12 slot MicroTCA shelf
- Enables comprehensive power supply and cooling performance measurements



AMC load board

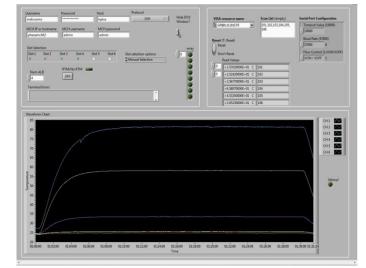




**RTM load board** 

# **MicroTCA Power Supply Testing**

- Electrical tests
  - Static load tests: payload voltage versus load
  - Dynamic load tests: payload voltage for load step
  - Payload voltage ripple
  - PSU efficiency test
- Thermal tests
  - On-board temperature gradient
  - Slot temperature variation
- Labview GUI to control load modules and acquire measurement results developed
- Initial tests with Schroff 6-slot MTCA.4 shelf
  - Small voltage variation under load and ripple
  - Efficiency ~85%
- Tests with 12-slot Vadatech shelf on-going
  - No RTM support
  - Requires 2 power modules under full load (12 x 80W) and external AC/DC supply



Labview GUI



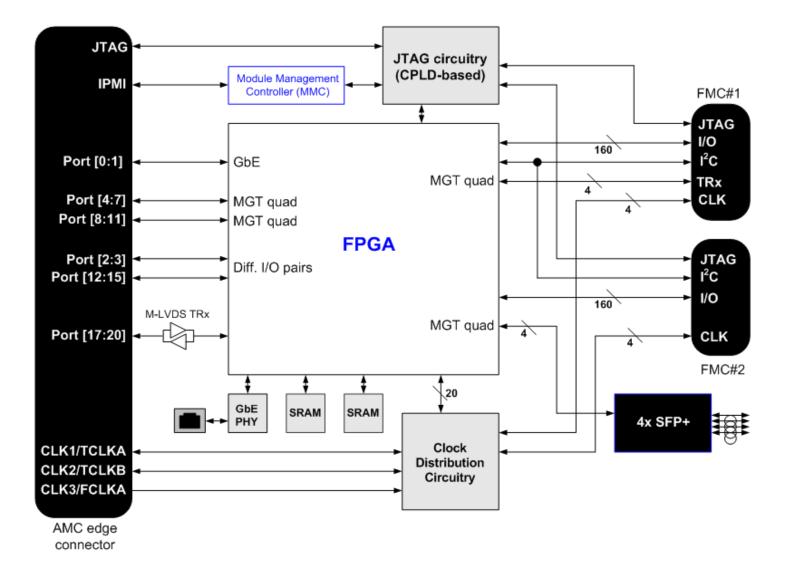
Test setup with Vadatech shelf

# **Gigabit Link Interface Board (GLIB)**

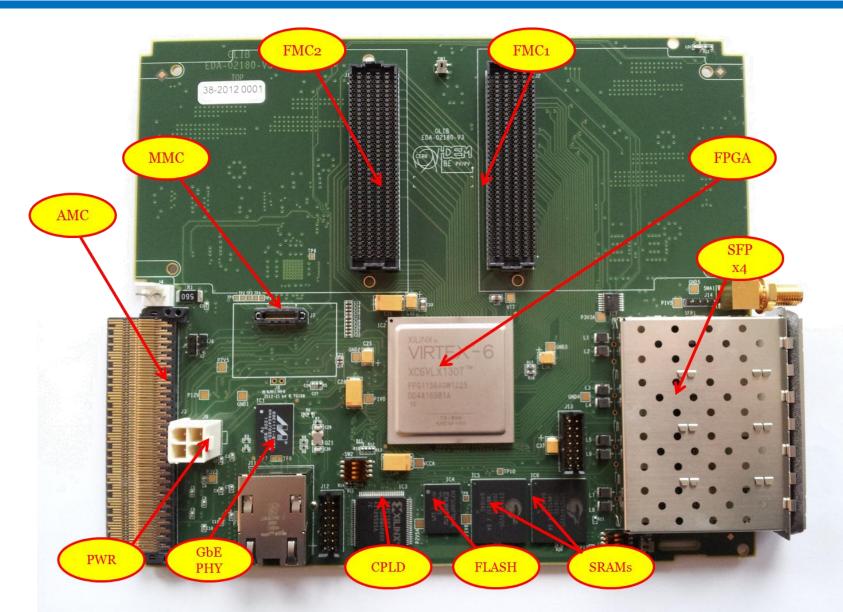
#### Features

- Mid/full-size double-width AMC
- 4 on-board SFP+ transceiver modules
- I/O extension via 2 FMC slots (HPC)
  - Commercial or in-house developed FMC mezzanines
- Virtex-6 FPGA (XC6VLX130T)
- Flexible clock distribution
- Copper GbE PHY for bench-top operation
- 2 on-board 72 Mb SRAM chips
- Control via Ethernet or PCIe
- Applications
  - Flexible FPGA-based module for high speed optical links in high energy physics experiments
  - Optical link evaluation in the laboratory
  - Control, triggering and data acquisition in beam or irradiation tests
  - Bench-top setup or in MicroTCA crate

#### **GLIB** Architecture

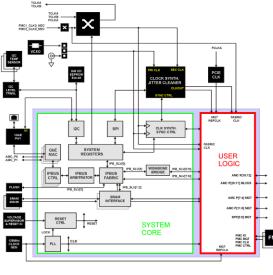


#### **GLIB Hardware**



## **GLIB Ancillary Developments**

- Firmware
  - Common firmware framework developed
  - Clean separation between common and user specific parts
- GLIB GUI
  - Java based graphical front-end to control and monitor the common GLIB configuration and status registers
- TTC FMC
  - Interface to the Trigger, Timing and Control (system) of the LHC experiments
  - Optical input and Clock & Data Recovery (CDR), protocol in GLIB FPGA



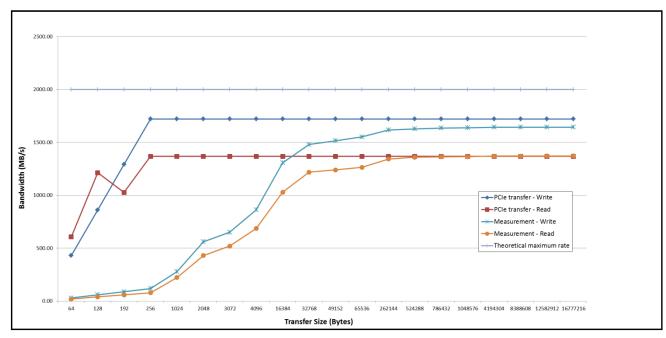
**Firmware** 

Construction by Gilb by 192 153 153 Gilb port 00000 File Registers Tele Registers Select Zelf File Lead Registers Tele Select Zelf File Lead Registers Select Zelf File Execute Instructions Select Zelf File E	GENERAL CLOCKING	SFP LOW LEVEL ACCES	S DEBUG USER	
E teronggopditregetes int Select Zeri Fie Select Zeri F	Ethernet	Glib ip 192	168.0.111 Glib port	50001
Selector Tile Lead Registers File Instructions  Fil	File Registers			
File Instructions       Select Xinif File       Exact Instructions       Read Based Info       Based Info       Uncolor       Seriell Number 000043561000       Seriell Number 000043561000       Seriell Number 000043561000       Seriell Number 00004356100       Seriell Number 000043561000       Seriell Number 000043561000       Seriel	E Vorenalgagaldis	fregisters.xml		
Select Xen (Version           Read Based Info           Based Info           Uversion         11.3 (2012/00413)           Seriel Number:         000443561000           Seriel Number:         000443561000           Version         1.3 (2012/00413)           Seriel Number:         000443561000           Version         0.00           Version         0.00           Version         0.00           Version         0.00           Version         0.00           Version         0.00	Select Xml File	Load Registers		
Select Xen (Version           Read Based Info           Based Info           Uversion         11.3 (2012/00413)           Seriel Number:         000443561000           Seriel Number:         000443561000           Version         1.3 (2012/00413)           Seriel Number:         000443561000           Version         0.00           Version         0.00           Version         0.00           Version         0.00           Version         0.00           Version         0.00	File Instructions			
Board Info           Board Info           Wenson         113.00100013)           Version         113.00100013)           64         FPGA           24         FPGA           24         FPGA           25         FRONT           33         REAR           VFL0         TMC1 presence           100         Coold Synthesized				
Board Info           Board Info           Wenson         113.00100013)           Version         113.00100013)           64         FPGA           24         FPGA           24         FPGA           25         FRONT           33         REAR           VFL0         TMC1 presence           100         Coold Synthesized	Colort Yml Eile	Execute Instructions		
Board Info         Board Temperature           Version         11.3.0012000133)         4         FRGA           Seriell Rumber         000000000000000000000000000000000000	JUNCE AND FILE	EXecute instructions		
Wersion         113_C01200133         Beard Temperature           4         FPGA           Sensi Number         000435EE000           34         FRONT           38         FRONT           38         FRONT           38         FRONT           38         FRONT           38         FRONT           38         FRONT           394_3M         LAB	Read Board	Info		
Version         11.3 (2010/01/3)         44         FPGA           Send Bunder         0004/30E10/0         44         FPGA           basel, 34         0.00         33         REAR           vpt_JA         Mail	Board Info			
Senal Number         0004/35E1000         44         FPGA           Jat         FRONT         34         FRONT           Senal Number         33         REAR           Sys_JAL         LAB         Senal Number         30	Version	1.1.3 (2012/08/13)		
Nover_jul         GLB		000443658090	44 EI	PGA
sys_id UB FMC1 presence Clock Synthesizer Clock By			34 FI	RONT
FMC1 presence TES Clock Synthesizer Clock Synthesizer	board_id	GLIB	33 R	EAR
	sys_id	LAB		
FBC2 presence (0) Clock Phase Blakes (0000)	FMC1 pr	esence YES	Clock Synthesizer	LOCKED
	FMC2 pr	esence NO	Clock Phase Status	GOOD



#### **GLIB Status**

- Production version fully tested and working
- ~50 modules produced and partly distributed to outside users
- Strong interest from all LHC experiments
  - Users in CMS, ATLAS, LHCb & ALICE
- Used to interface to the radiation-hard optical link and ASIC chipset (GBT) developed for the LHC experiment upgrades
- PCIe GEN2 x4 DMA bandwidth measurements in MicroTCA shelf
  - Kontron processor AMC <-> MCH <-> GLIB AMC



#### Summary

- xTCA evaluation project on-going in the CERN PH-ESE group
  - Focus on infrastructure components
  - Shelves and power supplies (electrical & cooling performance)
  - Shelf and module management
- Commercial MicroTCA equipment acquired and evaluated
  - Shelves, MCH, power modules, processors AMCs
- MMC mezzanine card and controller software available
- AMC and RTM load modules developed for power supply tests
- Comprehensive MicroTCA power supply tests on-going
- Recently expanded project to include ATCA
- Future plans for MicroTCA
  - Continue evaluation program
  - Attempt to standardize MicroTCA and ATCA shelves and power supplies at CERN
- GLIB AMC
  - Flexible FPGA based module for optical link applications in HEP experiments
  - Double-width, mid/full-size AMC, expandable through 2 FMC sockets
- Strong interest from the experiments
- Production modules available
- Custom designed FMC modules available
- Development framework available (firmware, software, GUI)