Introductory Tutorial

MTCA - Hardware Platform Management Systems Basics

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Agenda

- Introduction and Overview
- Shelf Management in xTCA Systems
- xTCA for Physics Extension
- Examples of IPMI Implementation



Introduction and Overview



Keep it Running...

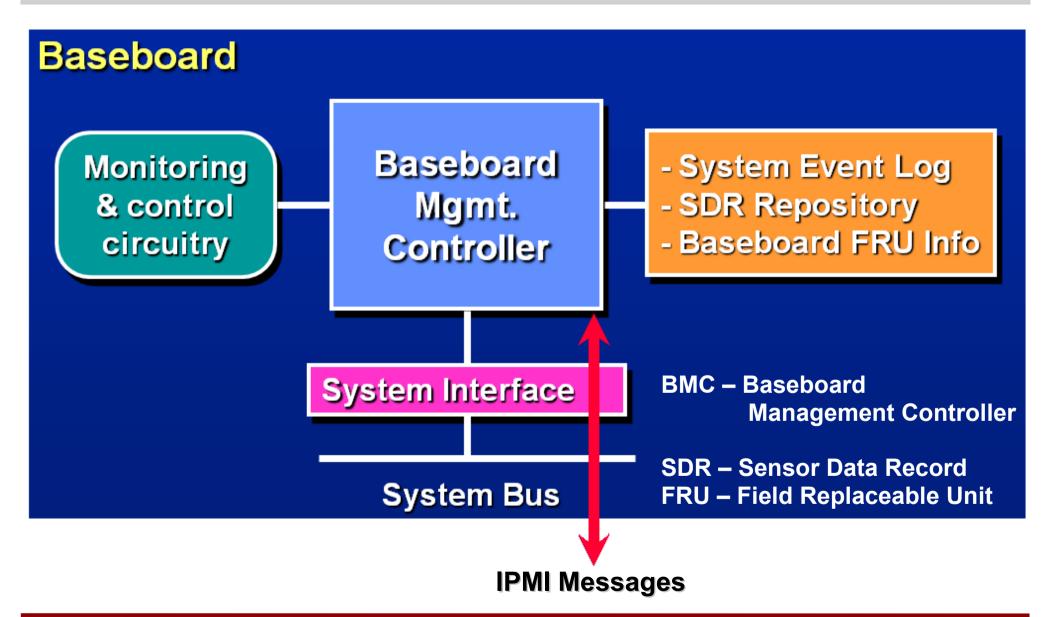
- Intelligent Platform Management Interface protocol initially developed by Intel, Hewlett-Packard, NEC and DELL consortium
- Used by system administrators for out-of-band management of computer systems and monitoring of their operation
- First draft available in Spring '98 (IPMI v0.9)
- RAS Features Focus:
 - Reliability
 - Availability
 - Serviceability
- Server oriented:
 - Remote administration
 - Expensive hardware
 - High costs of downtime and repair
- Plug and Play, Hot-swap



SuperBlade supercomputer source: www.supermicro.com

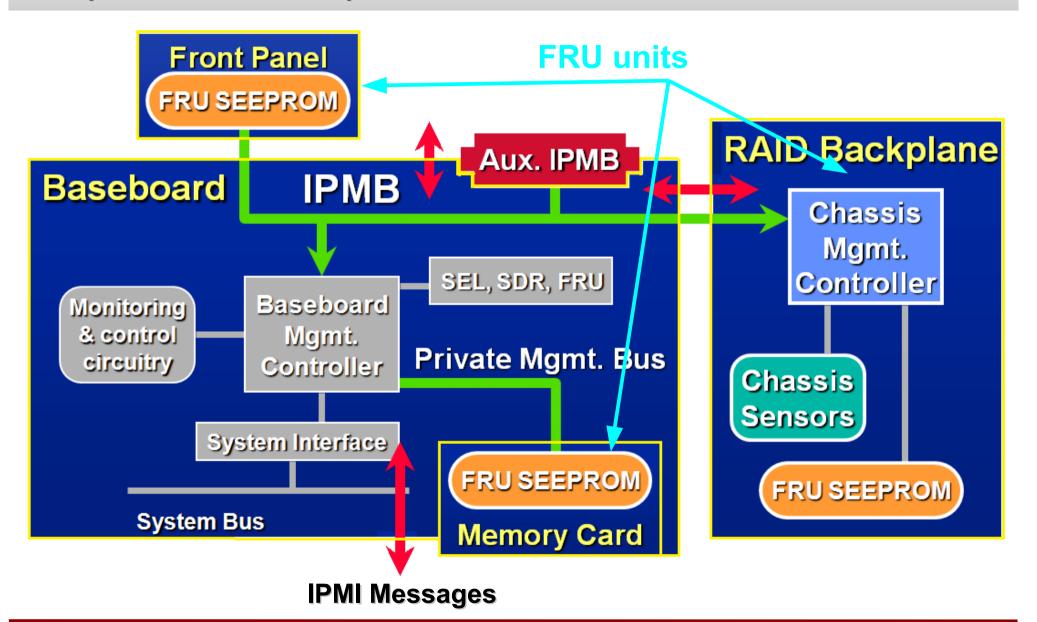


IPMI Components



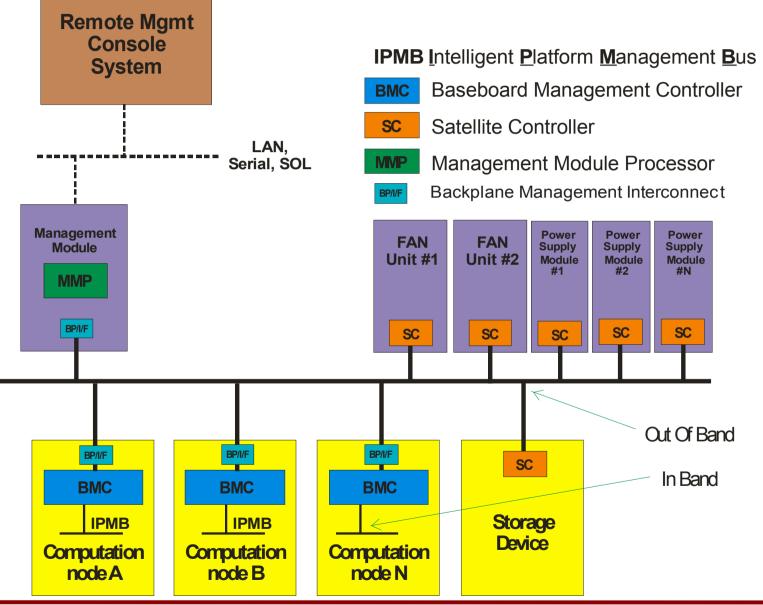


Computer Node - IPMI Implementation





Chassis Implementation





IPMI Elements (1)

- Baseboard Management Micro-Controller provides intelligence for IPMI
 - Out Of Band (OOB) access to computer
 - Autonomous monitoring and logging
 - System interface to internal IPMB (I2C)
 - Interface to IPMI Storage
 - Receives and logs events messages
 - Power control functions
 - BIOS access
 - OEM defined functions
 - System Watch-dog Timer



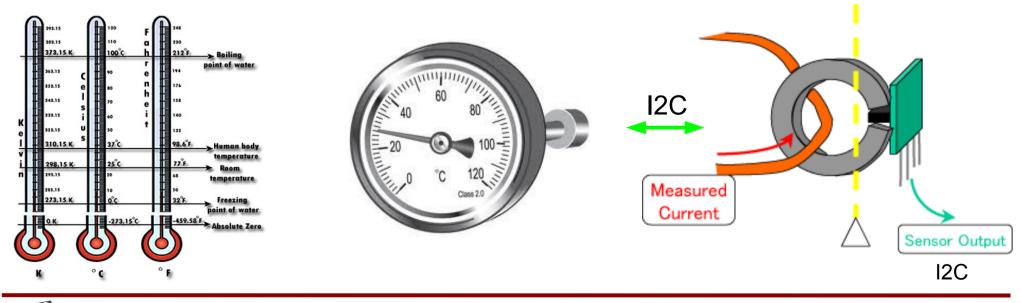
IPMI Elements (2)

Field Replaceable Unit (FRU)

Field replaceable components of the system such as a board, module, fan unit, power supply module, raid matrix, etc. FRU records are stored in a non-volatile memory.

Sensor Data Record (SDR)

Provide information about available on FRU sensors, events, management controllers, e.g. temperatures, voltages, sensors, etc.





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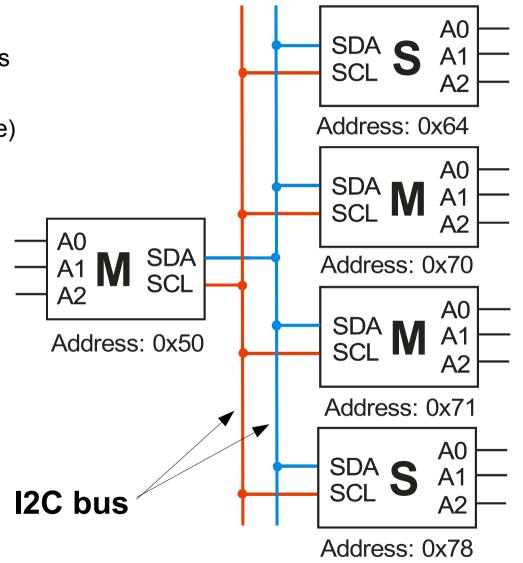
I2C

SCL

SDA

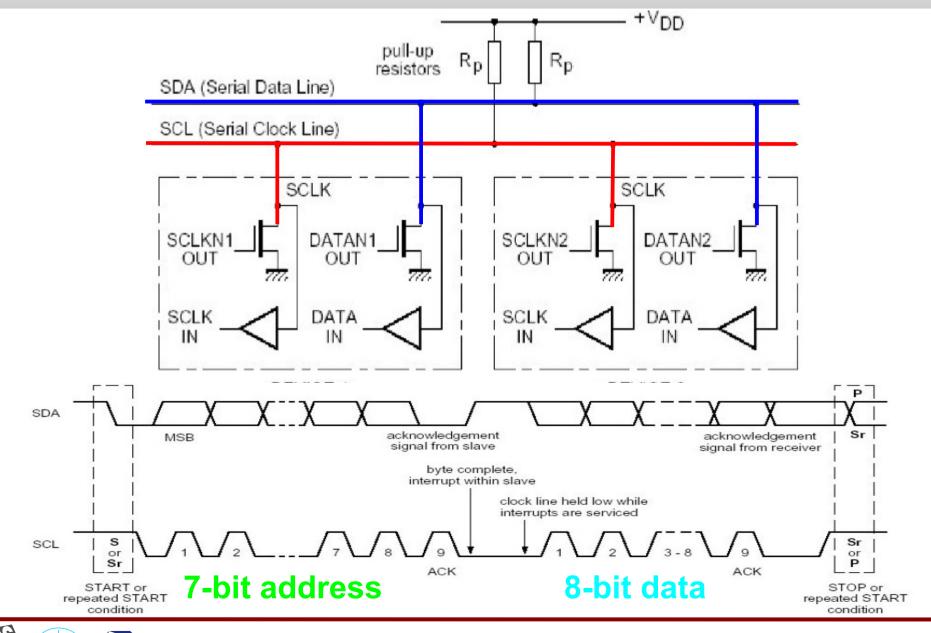
I2C Interface – IPMI Backbone (1)

- I2C Inter-Integrated Circuit bus
- Standard developed by Philips on early 80s
- Two wire synchronous, half-duplex interface (SDA – data line, SCL – clock line)
- Bidirectional multi master-slave transfers, 8-bit frames
- Transmission speed: 100 kbps, 400 kbps, 3.4 Mbps
- 7-bit or 10-bits device address
- Arbitration used for multi-master transmission





I2C Interface – IPMI Backbone (2)





Shelf Management in xTCA Systems

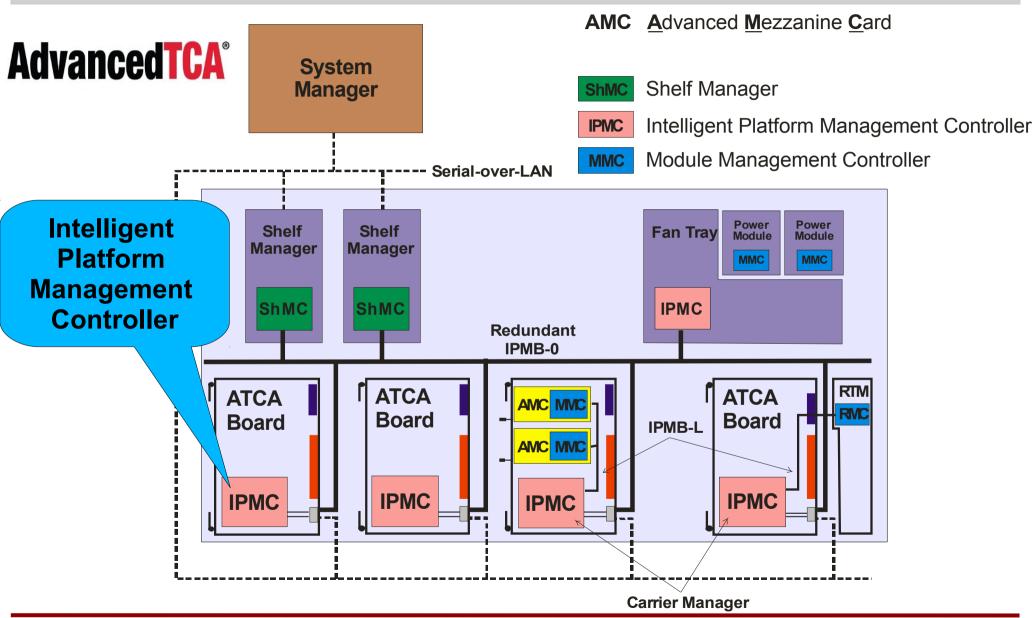


xTCA and **IPMI**

- IPMI introduced in PICMG 2.16 backplanes (CompactPCI systems) and later in AMC, ATCA and MTCA standards
- IPMI enables "diagnose-before-dispatch" automation
- Required for 99.999 percent high availability (HA) mark
- IPMI controller (shelf manager) is responsible for:
 - Monitoring overall shelf health
 - Communicating with remote System Management Software (SMS)
 - Hot-swap events (e.g. hardware component entry-removal events)
 - Latch/lock management
 - Power budgeting
 - In-rush current sequencing
 - Electronic keying (E-keying)
- PICMG 3.0 extension commands
- HPM.1 management firmware upgrade capability

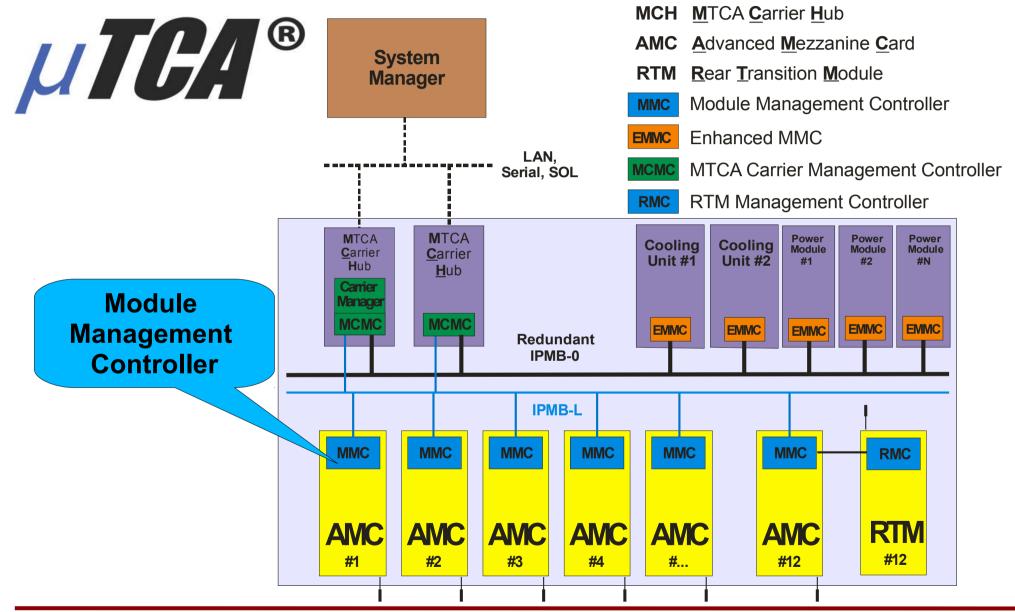


ATCA Shelf Management System

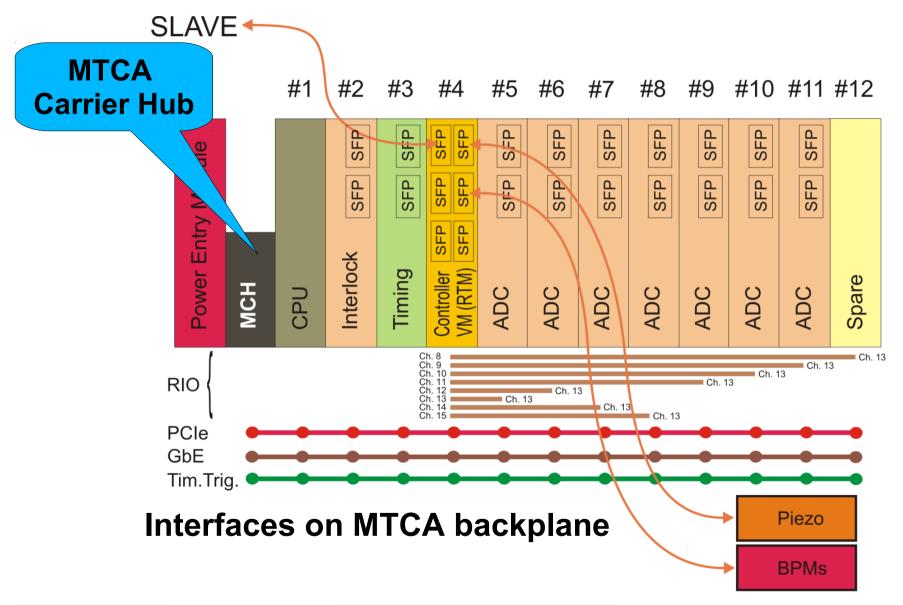




MTCA Shelf Management System



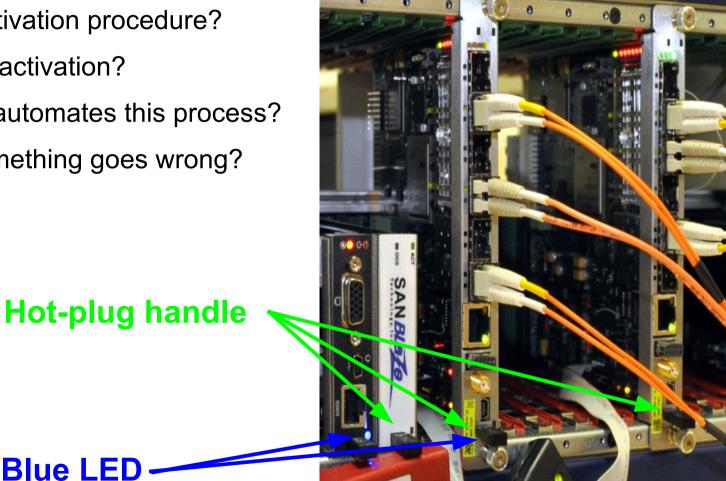
uTCA-based LLRF Control System of Accelerator





AMC Module Hot-plug

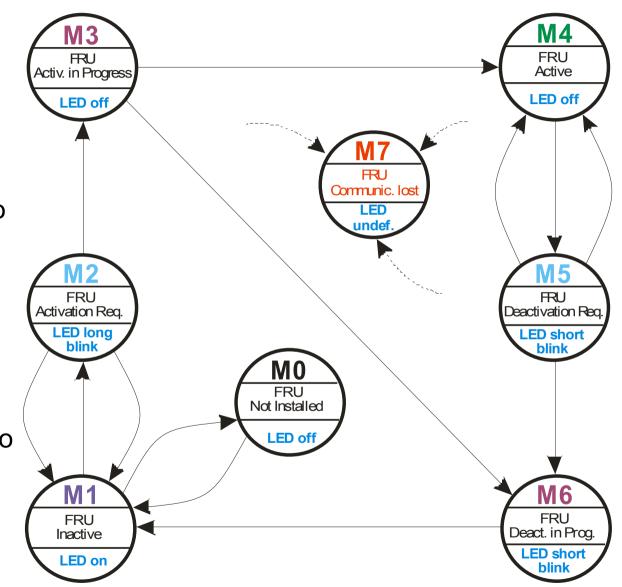
- What really happens when you plug AMC card into MTCA chassis?
- Module Activation procedure?
- Module Deactivation?
- How IPMI automates this process?
- What if something goes wrong?





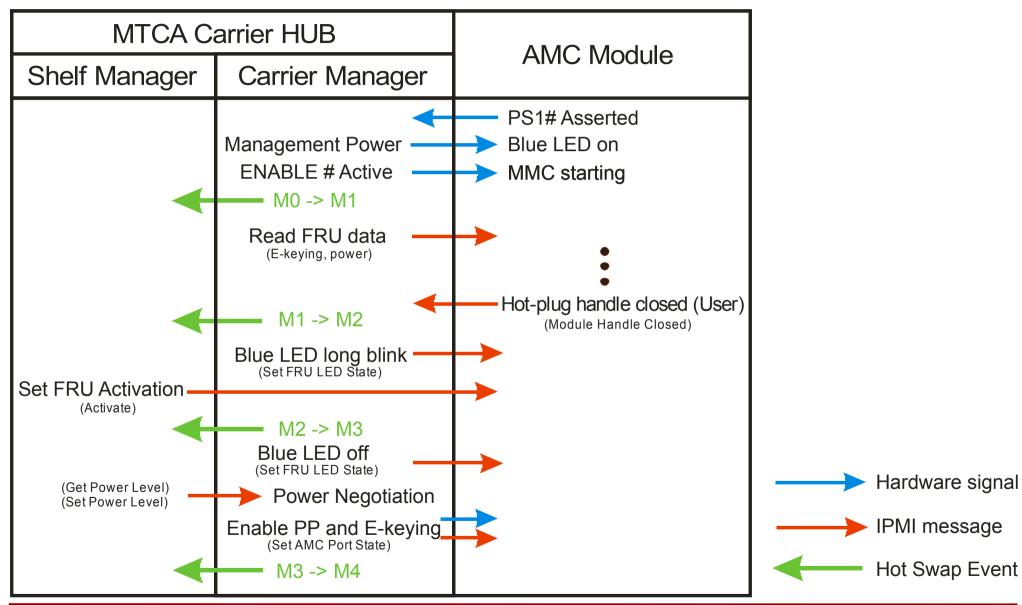
Module Activation/Deactivation

- PICMG 3.0 and AMC specifications define FRU states
- Activation pushes FRU into M4 state
- Deactivation moves FRU into M1 state
- If something wrong happen module goes into M7 state
- MCH decides if and when module can reach M4
- MMC uses a state machine to control hot-plug procedure



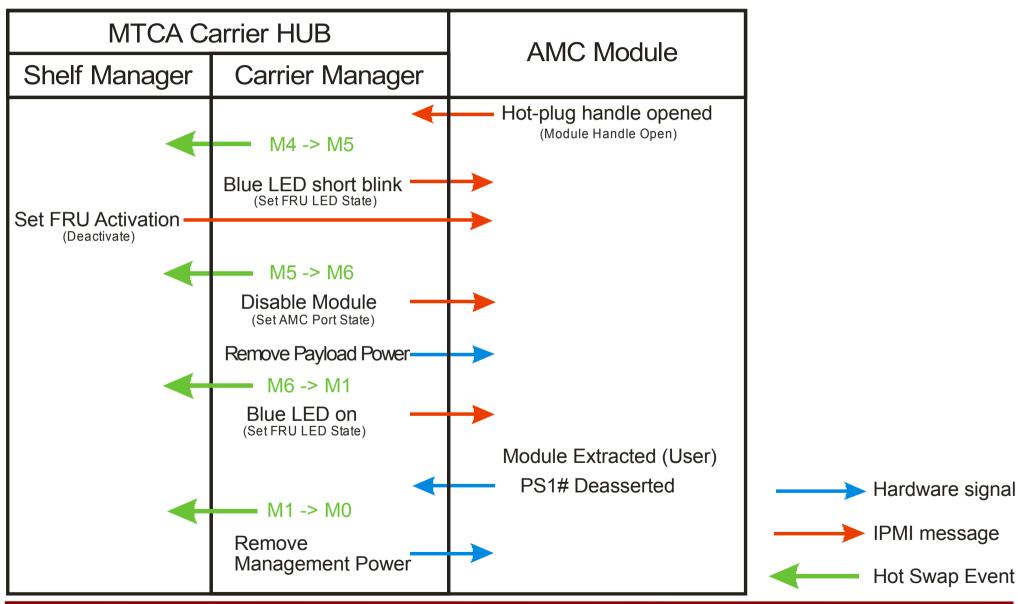


AMC Module Insertion



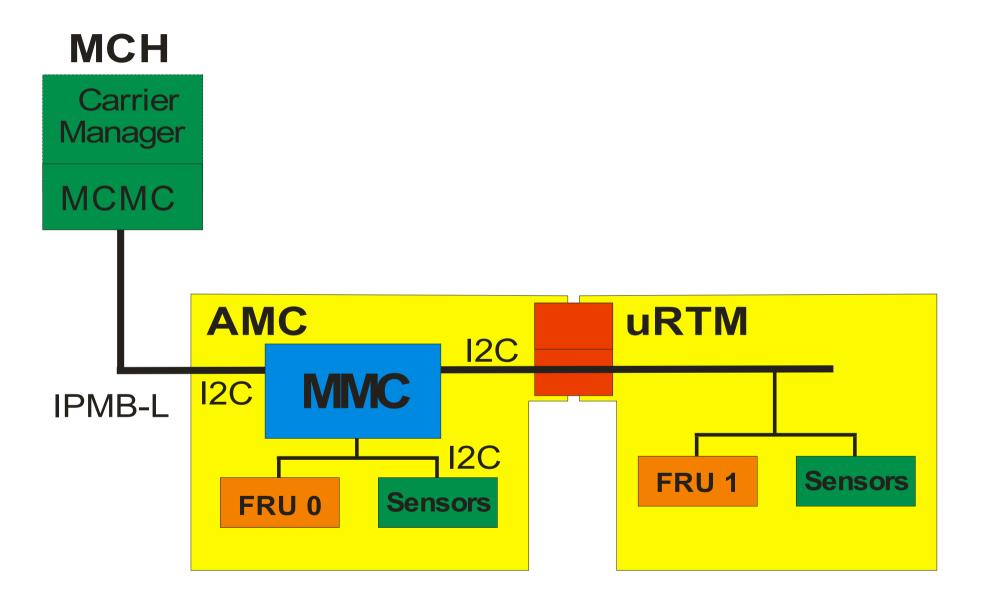


AMC Module Extraction



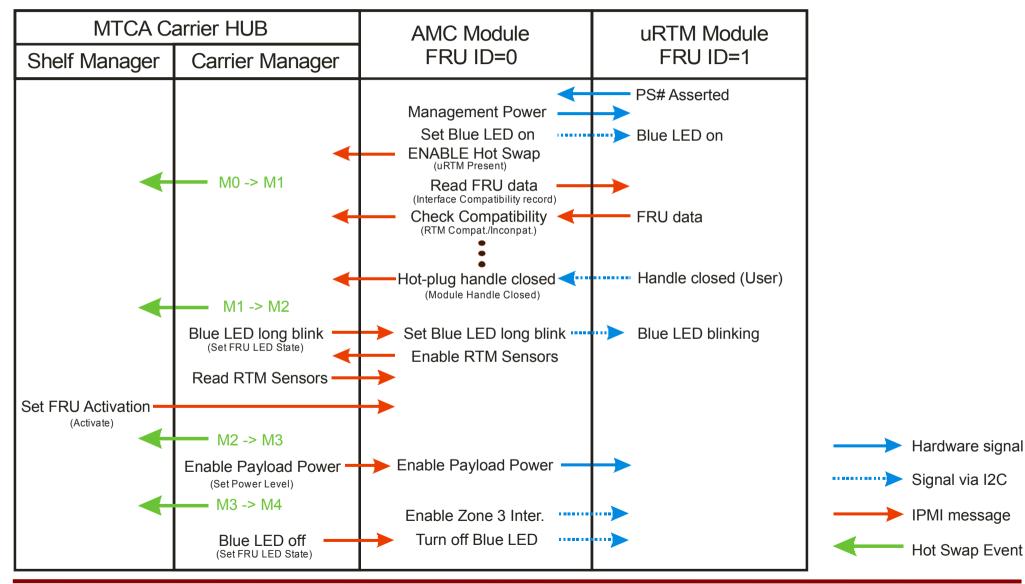


MTCA.4 – Hardware Management



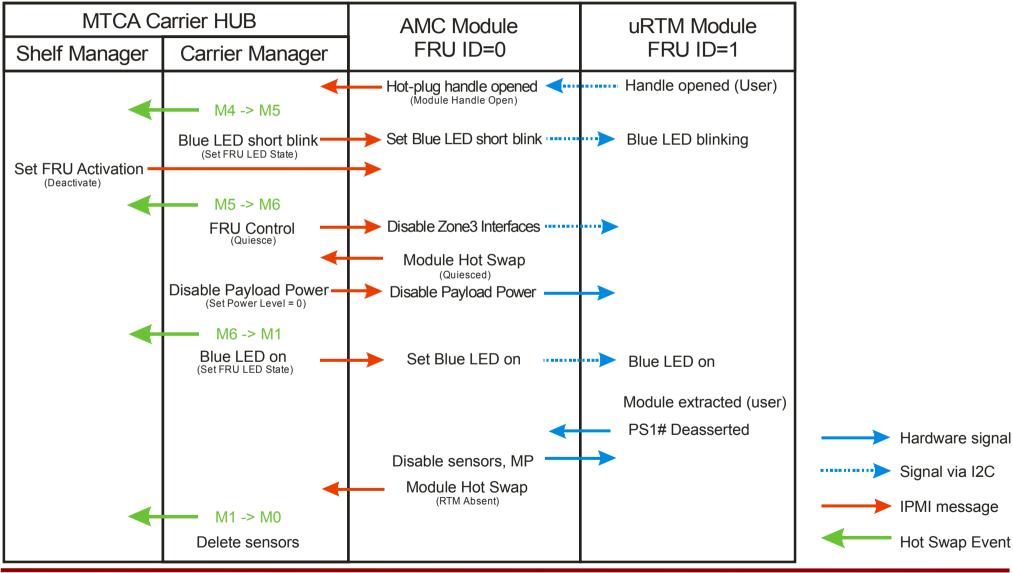


RTM Module Insertion





RTM Module Extraction





Electronic-keying – Connection Compatibility Management

- Allow using different standards (1/10 GbE, PCIe, SRapidIO, Inifiniband, Custom links)
- Provide connections compatibility
- Protect hardware

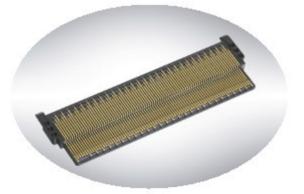




E-keying for MTCA Zone 1 Connector

MTCA Zone 1 connector divided into zones:

- Each module can receive or drive clock signals
- Star connection on ports 0 and 1
- P2P (Peer-to-Peer) connection on ports 2 and 3
- Star connection via switch on ports 4-7
- Star connection or P2P on ports 8-11
- P2P connection on ports 12-15
- Bus connection on ports 17-20



AMC 170 pin connector



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Region	Interface	Port		
	CLK1	TCLKA		
Clocks	CLK2	TCLKB		
	PCIe Clock	FCLKA		
Common Option	1 GbE	0		
	TODE	1		
	SAS/SATA	2		
	JAJ/JATA	3		
	PCIE	4		
Fat Pipe	10 GbE	5		
	SRIO	6		
	5140	7		
	PCIE	8		
Ext. Fat Pipe	10 GbE	9		
LAGITATTIPC	SRIO	10		
	P2P	11		
		12		
	P2P	13		
		14		
		15		
Extended Options	CLK	TCLKC/D		
	Triggers	17		
	Interlocks	18		
	Clocks	19		
		20		

25

E-keying in MTCA

- MCH will read FRU records from both modules
- Compare E-keying records of MCH and AMC3/AMC4
- Compare E-keying records of AMC3 and AMC4
- Activate interfaces with compatible protocols

AMC in slot 3		Decision		AMC in slot 4			
Region	Interface	Port	AMC 3	AMC 4	Region	Interface	Port
Clocks	CLK1	TCLKA	\checkmark	$\mathbf{\overline{A}}$	Clocks	CLK1	TCLKA
	CLK2	TCLKB	V	V		CLK2	TCLKB
	PCIe Clock	FCLKA		$\mathbf{\nabla}$		PCIe Clock	FCLKA
Common Option	1 GbE	0	V	V		1 GbE	0
		1					1
	SATA	2	×	V	Common Option	SAS	2
	SATA	3	V	V		SATA	3
	PCIE 1	4	\checkmark	$\mathbf{\overline{N}}$		PCIE 1	4
Fot Dino	PCIE 2	5	V	×	Fot Dino		5
Fat Pipe	PCIE 3	6	V	×	Fat Pipe		6
	PCIE 4	7		4			7
Ext. Fat Pipe	10 GbE	8	×	V	Ext. Fat Pi, e	SRIO	8
	10 GbE	9	×			SRIO	9
	10 GbE	10	×	$\mathbf{\nabla}$		SRIO	10
	10 GbE	11	×	$\mathbf{\nabla}$		SRIO	11
	GTX	12	×	×		P2P - LVDS	12
		13	×	×			13
	P2P - LVDS	14				P2P - LVDS	14
	P2P - LVDS	15	$\mathbf{\nabla}$			P2P - LVDS	15
Extended Options	CLK	TCLKC/D			Extended Options		
	Triggers Interlocks Clocks	17		V		Triggers Interlocks	17
		18		V			18
		19		$\mathbf{\nabla}$		Clocks	19
		20		V		CIUCKS	20

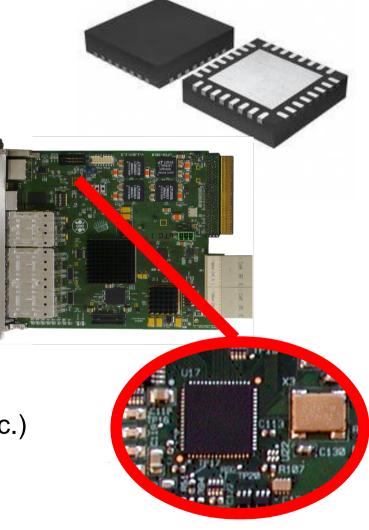


Module Management Controller



Tasks of MMC

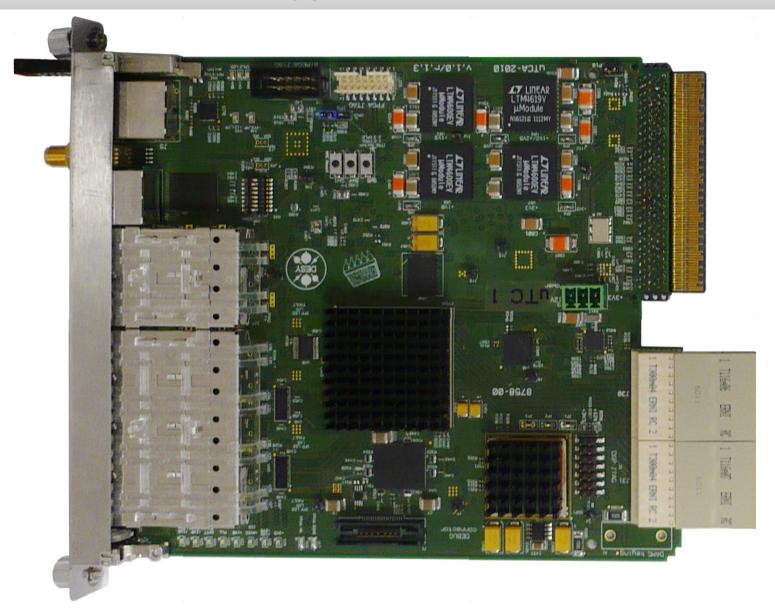
- Required for each Advanced Mezzanine Card
- Communication with the Carrier Manager
- Module management:
 - Module activation and deactivation
 - Warm and cold module reset
 - Power supply management
- Monitoring of module crucial parameters
 - Temperature
 - Supply voltages
 - Currents
 - Clocks, etc.
- E-keying mechanism (PCIe, GbE, sRIO, clocks, etc.)
- Supervision of RTM module (MTCA.4)



Advanced MC[™]



uTCA - based LLRF Controller (1)



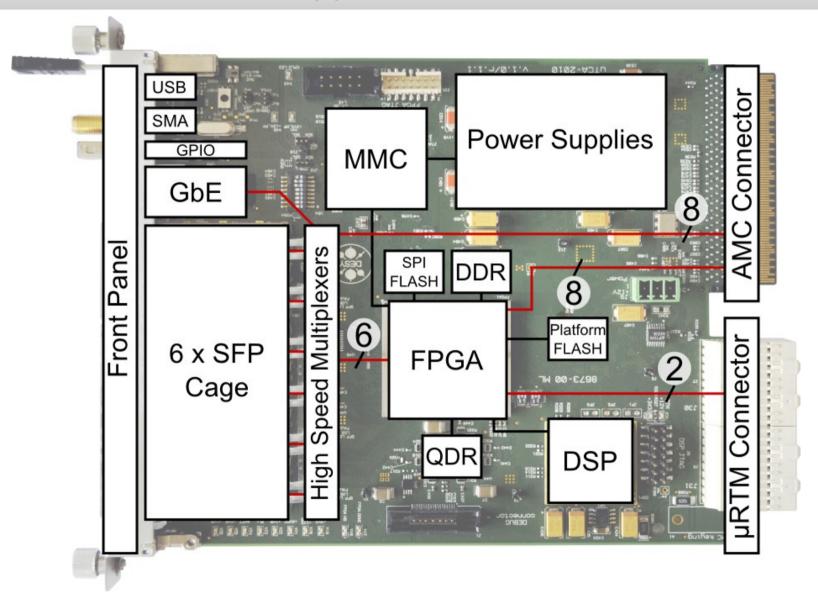


uTCA - based LLRF Controller (2)

- Two modes of operation:
 - Low Level Radio Frequency controller
 - Fast Beam-Based Feedback Processor
- Enough processing power for execution of the cavity field stabilizing algorithms (PID, feed-forward) in the feedback loop
- Dedicated low-latency P2P connections
- PCIe and Gigabit Ethernet
- Firmware upgrade feature
- Memory (QDR II/DDR2)
- Compliance with MTCA.4 standard

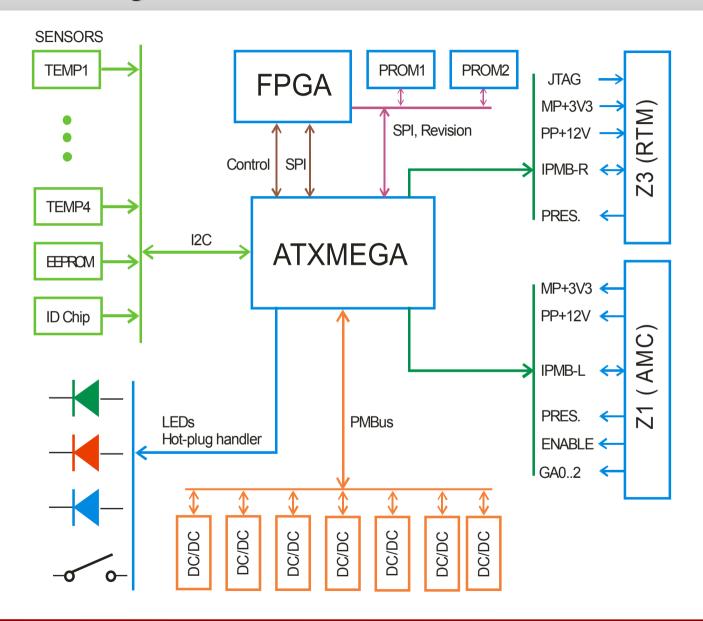


uTCA - based LLRF Controller (3)





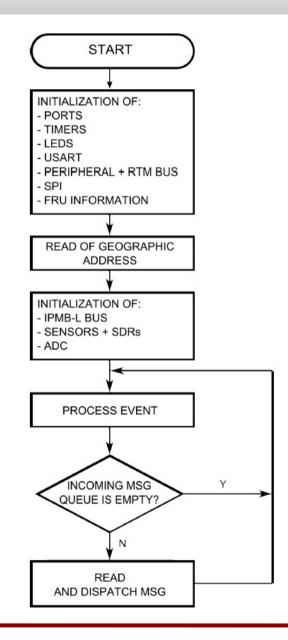
Hardware – Block Diagram of MMC





Software – MMC Implementation (1)

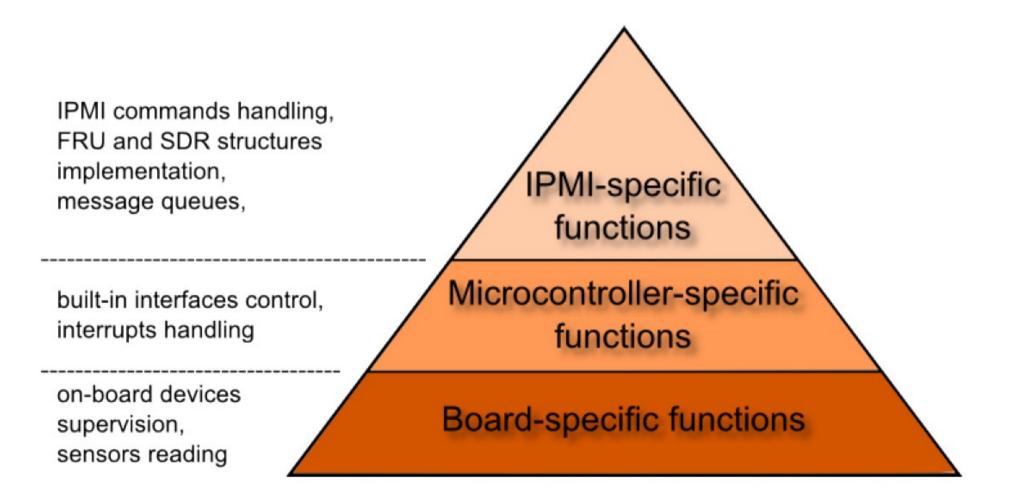
- Initialization
 - Initialization of software structures
 - Configuration of peripheral devices
- Main loop
 - Event processing
 - Messages handling





Software – MMC Implementation (1)

- Works aimed to code portability in progress
- Software layers





MMC – Summary

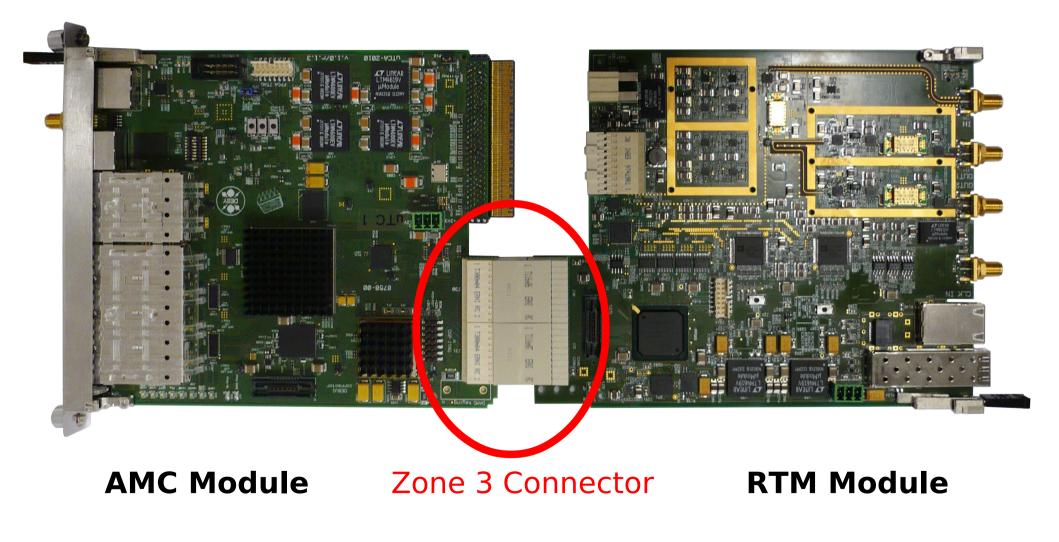
- Presented MMC meets basic requirements of MicroTCA and xTCA for Physics specification
- The MMC firmware was tested in the laboratory and various facilities at DESY
- Future plan is to prepare universal, portable firmware



xTCA for Physics Extension

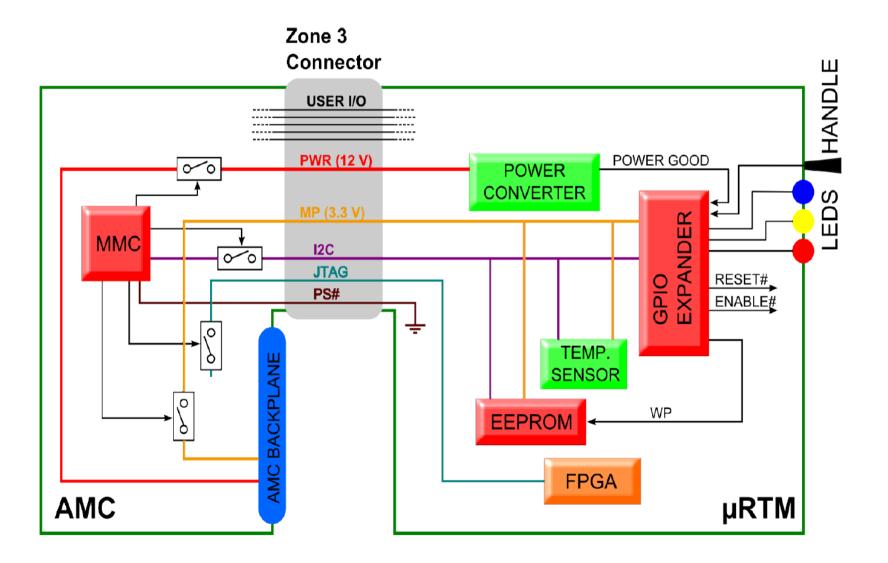


MTCA.4 RTM Extension



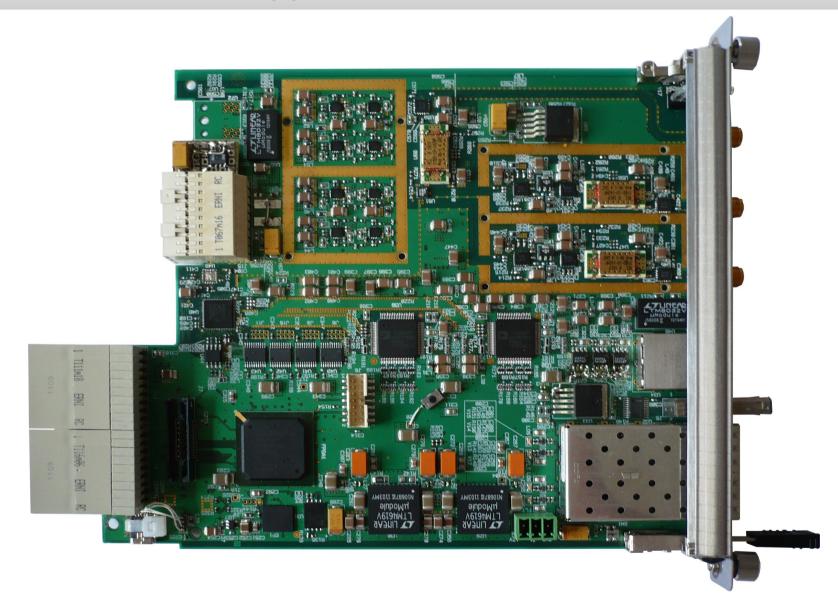


IPMI and RTM – MTCA.4 spec.



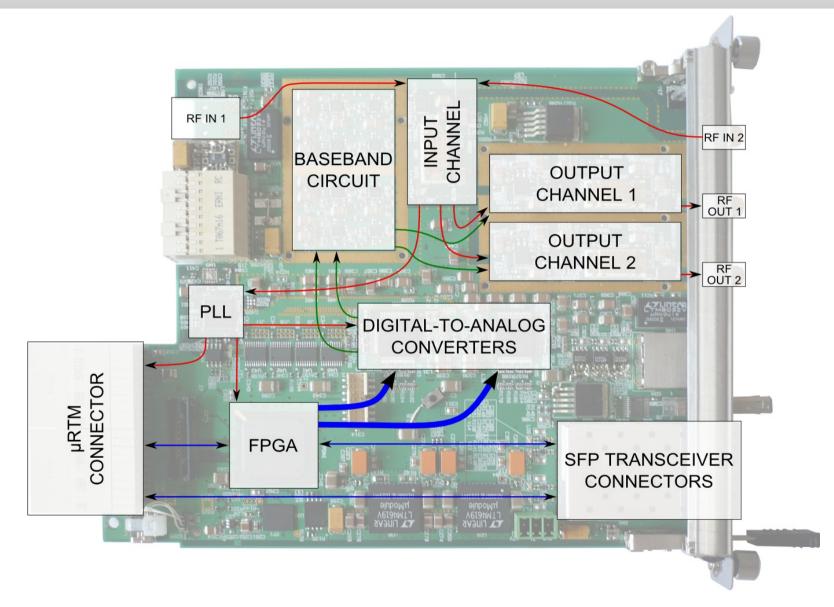


Vector Modulator as RTM (1)



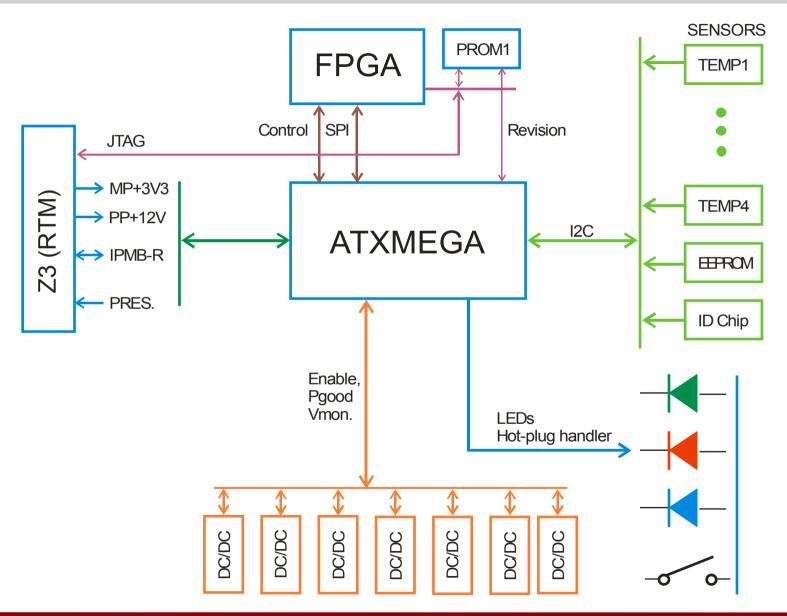


Vector Modulator as RTM (2)



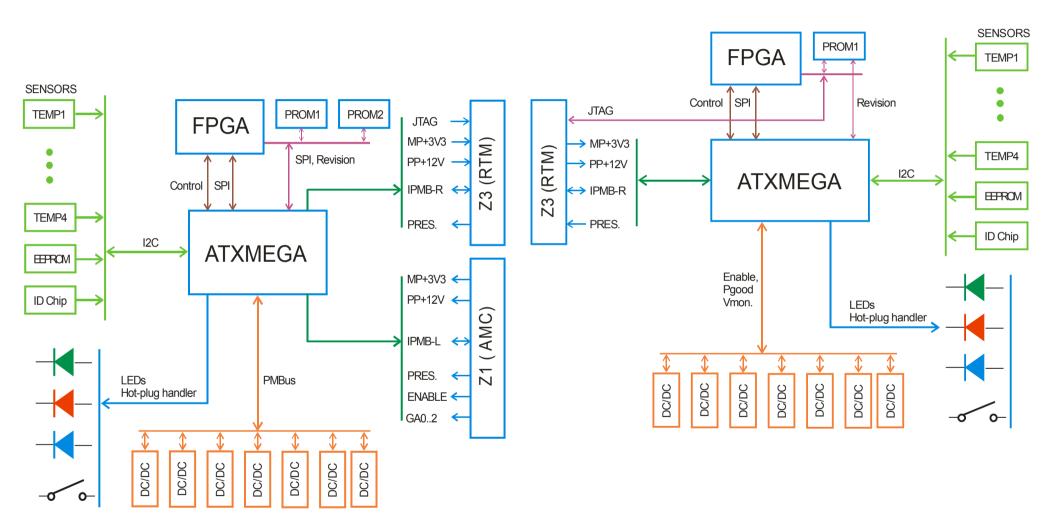


IPMI on Vector Modulator





AMC and RTM Management



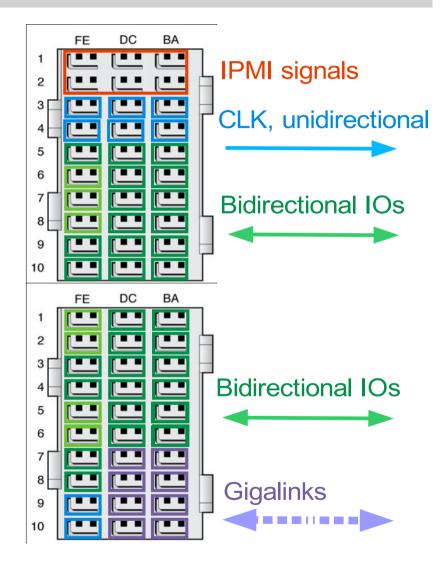


Zone 3 E-Keying

- DESY Zone 3 recommendation for digital and analogue classes
- Various, bidirectional analogue and digital signals
- MTCA.4 keying only verifies voltage levels
- Require E-Keying with MMC and RTM controller support to avoid signal collisions

Ν	Data Signal in Volts
1	LVDS
2	$0 - \pm 1$
3	>±1-±3.3
4	>±3.3 - ±10
5	>±10
6	Reserved
7	Reserved
8	Reserved





F. Ludwig, '...Zone 3 classes...'



Thank you for your attention Questions ? Comments ?

