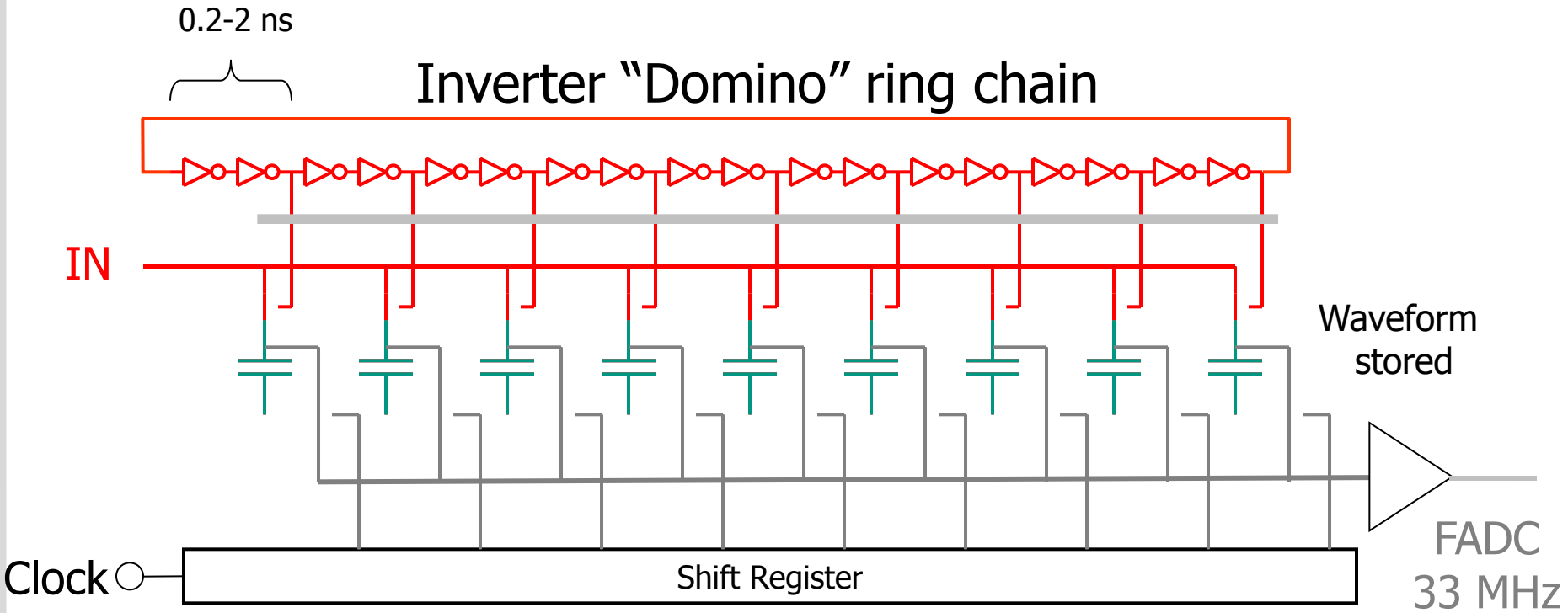
RTM Module based on DRS-4 waveform digitizing chip.

A.Menshikov, M.Balzer, M.Kleifges

Switched Capacitor Array



"Time stretcher" GHz → MHz

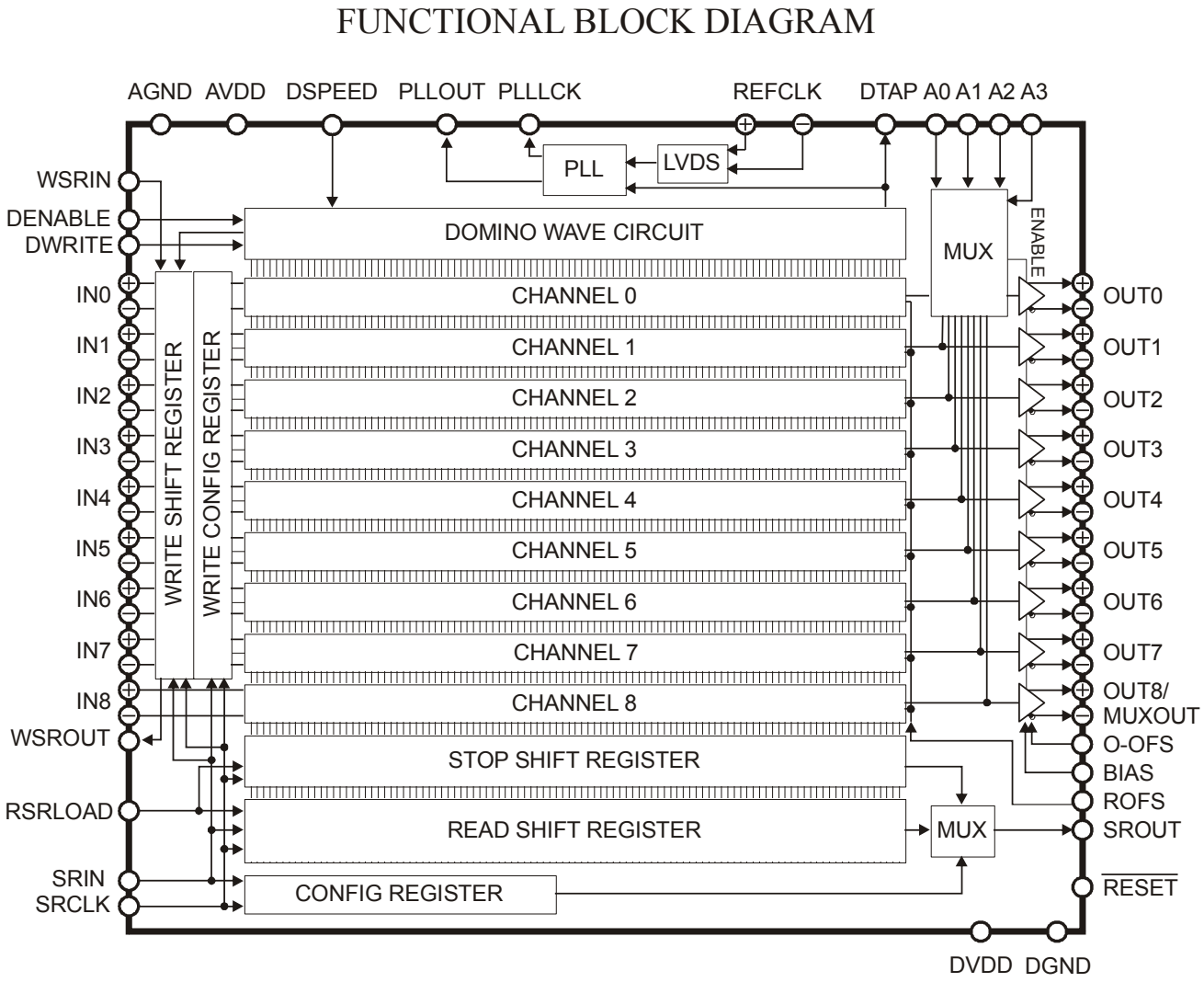
Source: PSI, Stefan Ritt, presentation „Very Fast Waveform Recorders."

DRS4 Chip.

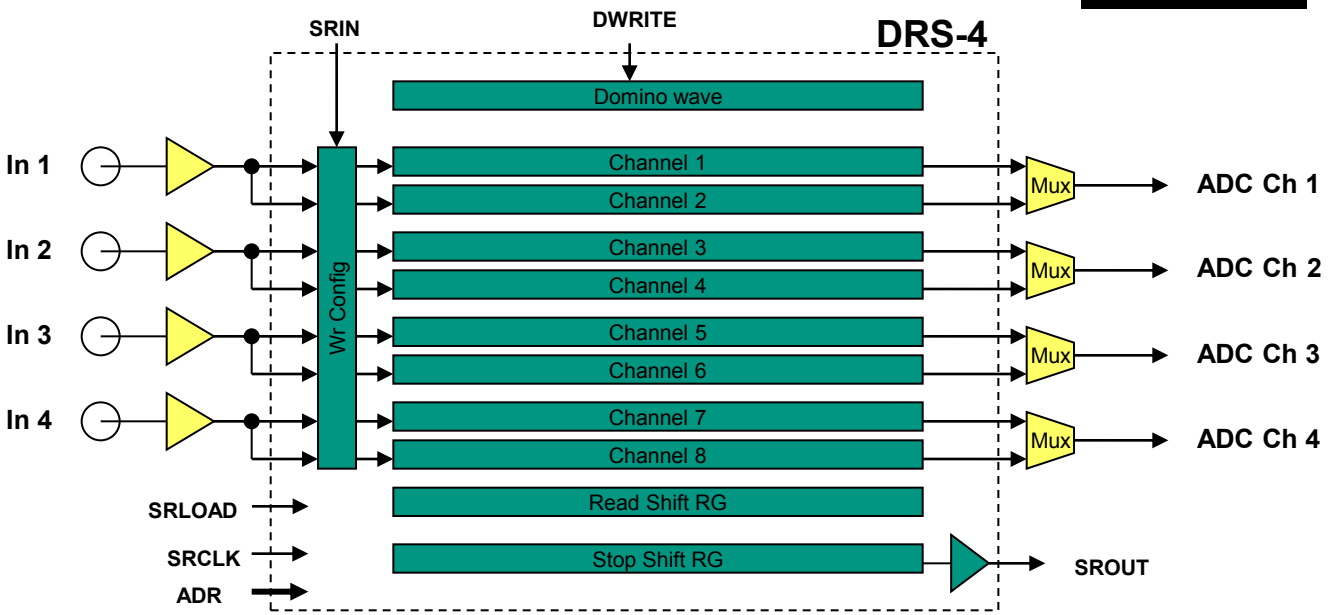
- 8+1 ch. each 1024 bins,
  4 ch. 2048, …, 1 ch. 8192
- Sampling speed
  700 MHz … 5 GHz
- On-chip PLL stabilization
- Readout speed
  33 MHz

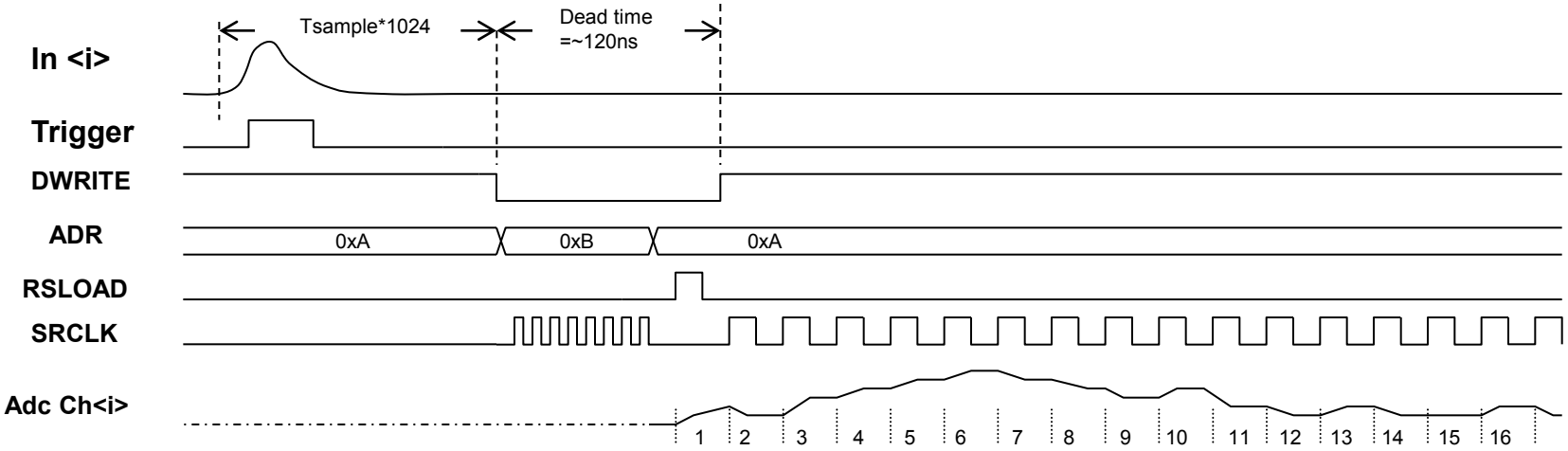
- fixed pattern offset error
- 11.5 bit amplitude resolution

- Fixed pattern jitter
- Can be corrected

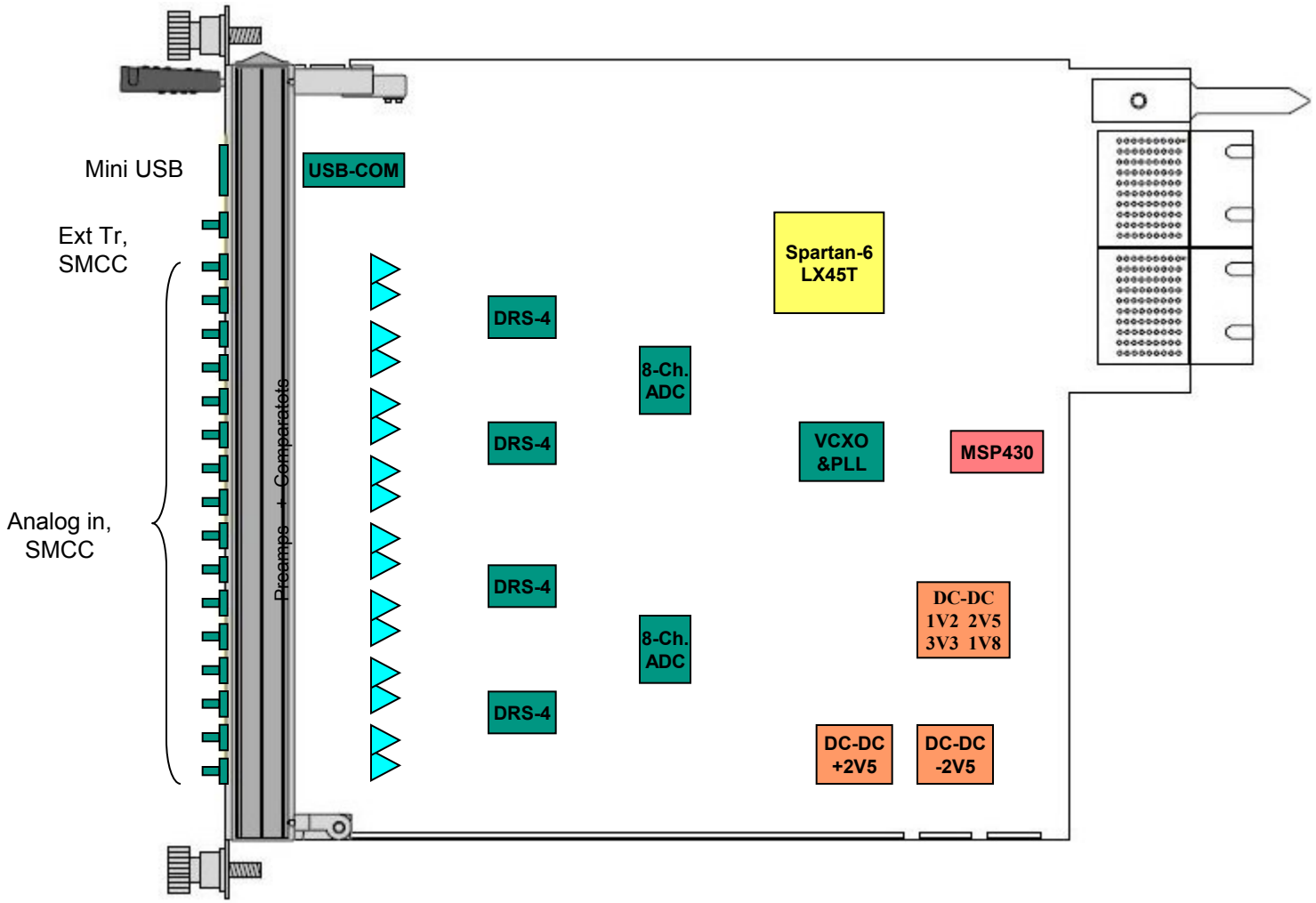


Sampling and digitization. Dead time





The Module layout



Analog Front End

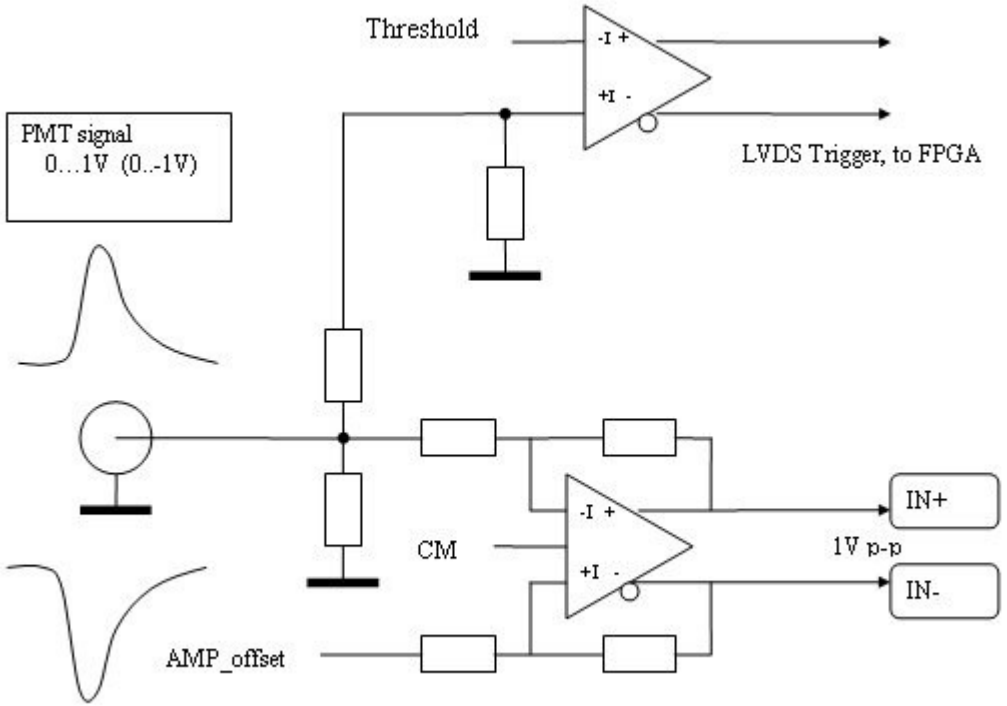
-Amplifier bandwidth ~750MHz

-Comparator delay < 1ns

-Adjustable signal range

-DC coupling

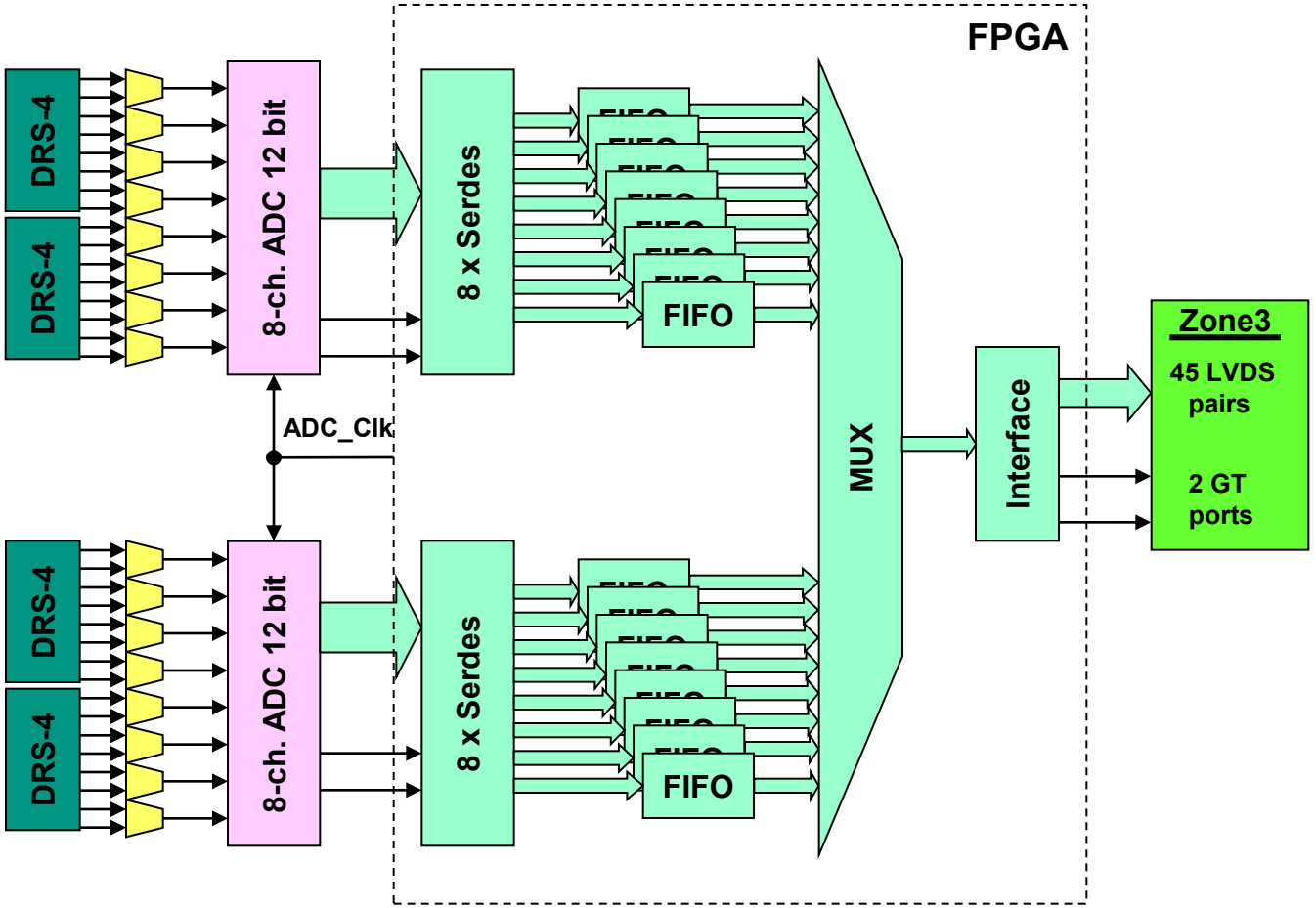
-Supply +-2,5V



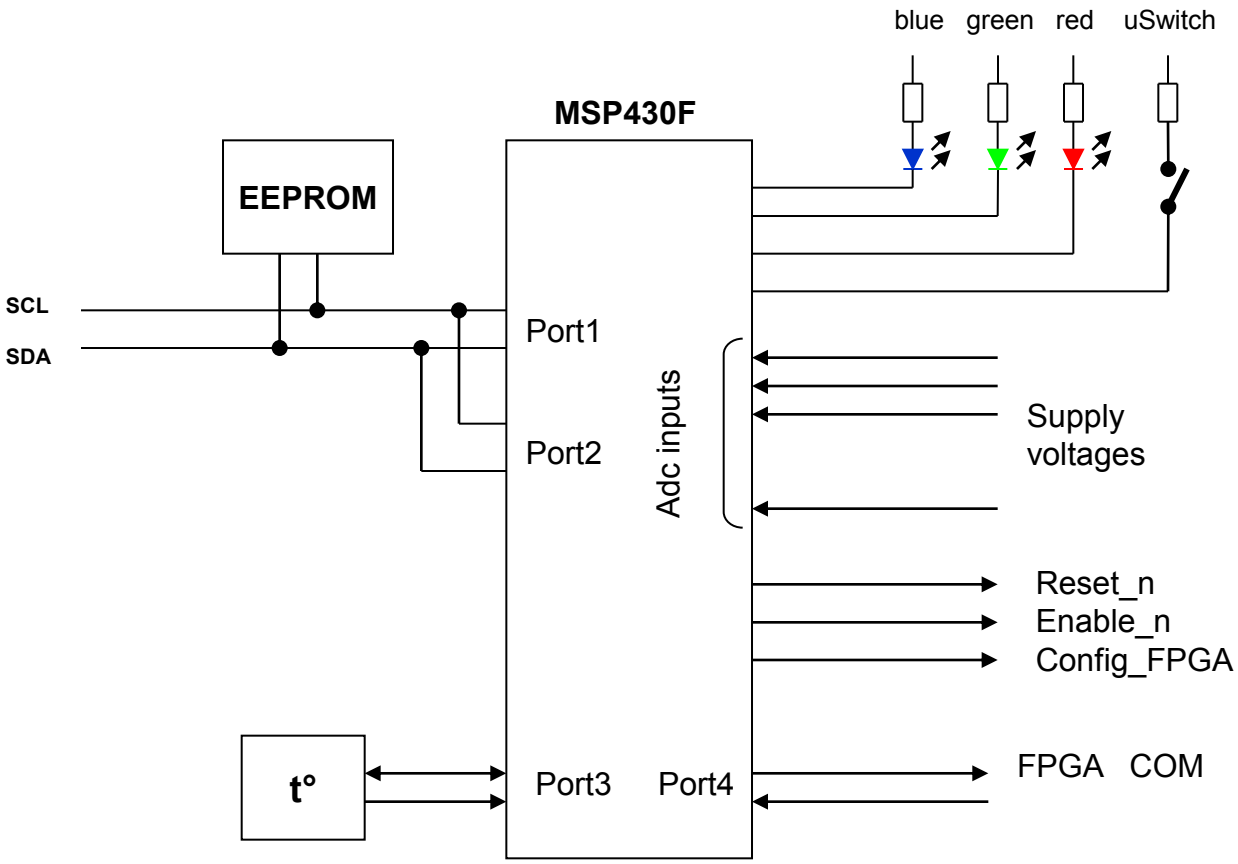
FPGA functionality.

- Steering four DRS4
- Reception of data from 16 ADC channels (each 360Mb/s)
- On-flight fixed-noise subtraction
- Interface to MTCA: a kind of SerDes and/or GT ports.
- Threshold adjustment in all channels
- Trigger logic

Data Paths (simplified)



uRTM Management



Summary

- 16 analog inputs, external trigger
- (DC-750MHz) bandwidth
- Programmable sampling rate 700MHz – 5GHz
- Precise synchronization to reference AMC clock (jitter < 0,5ps)
- Spartan-6 LX45T-LX100T
- Zone3 interface implemented in FPGA: two GT ports and 45 LVDS pairs
- Management functionality are done in microcontroller
- USB debug port
- JTAG access from AMC side for upgrading firmware