Universität Hamburg
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LEXI
LANDESEXZELLENZINITIATIVE HAMBURG

CMS Phase 1 Pixel Upgrade

LEXI Cluster Meeting

DESY, Hamburg, DE

11-12 October, 2012

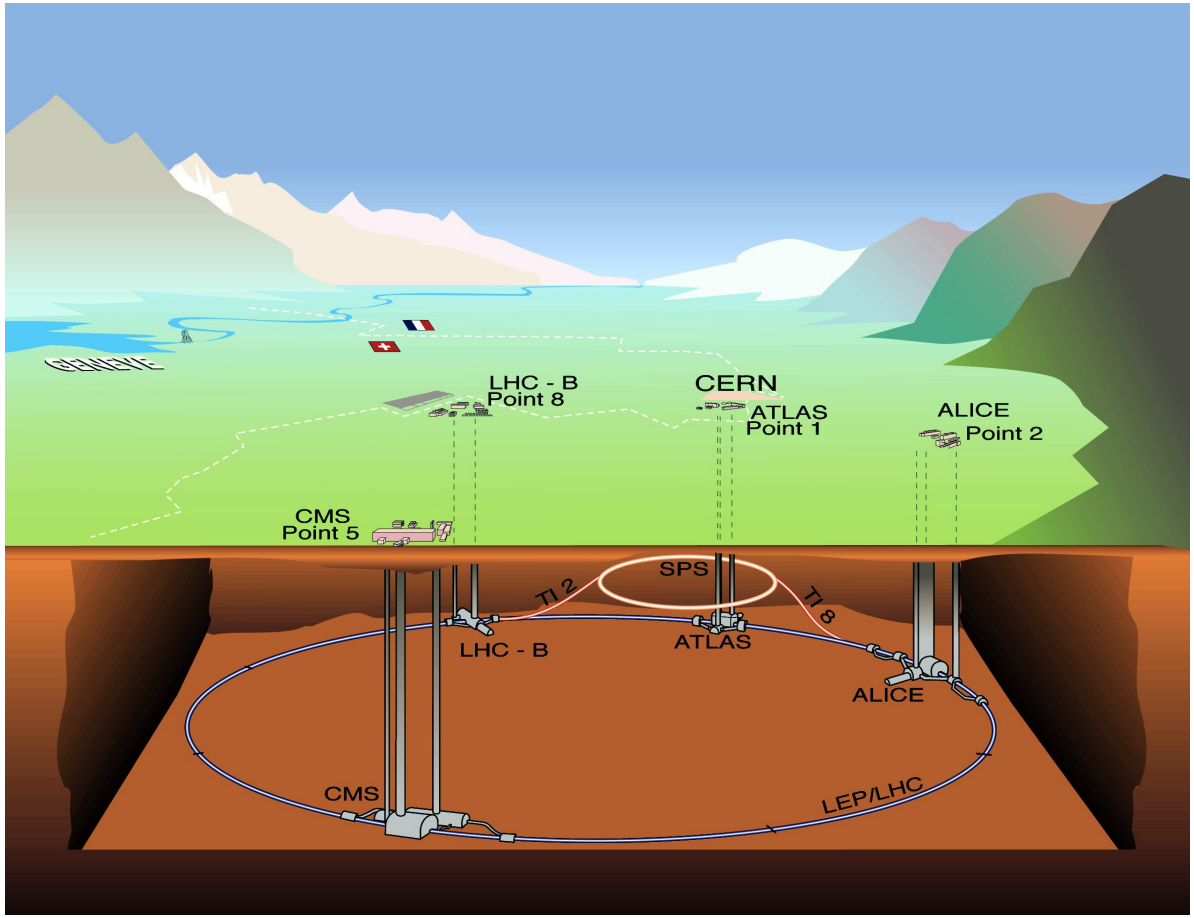
Jennifer Sibille

University of Hamburg

Outline

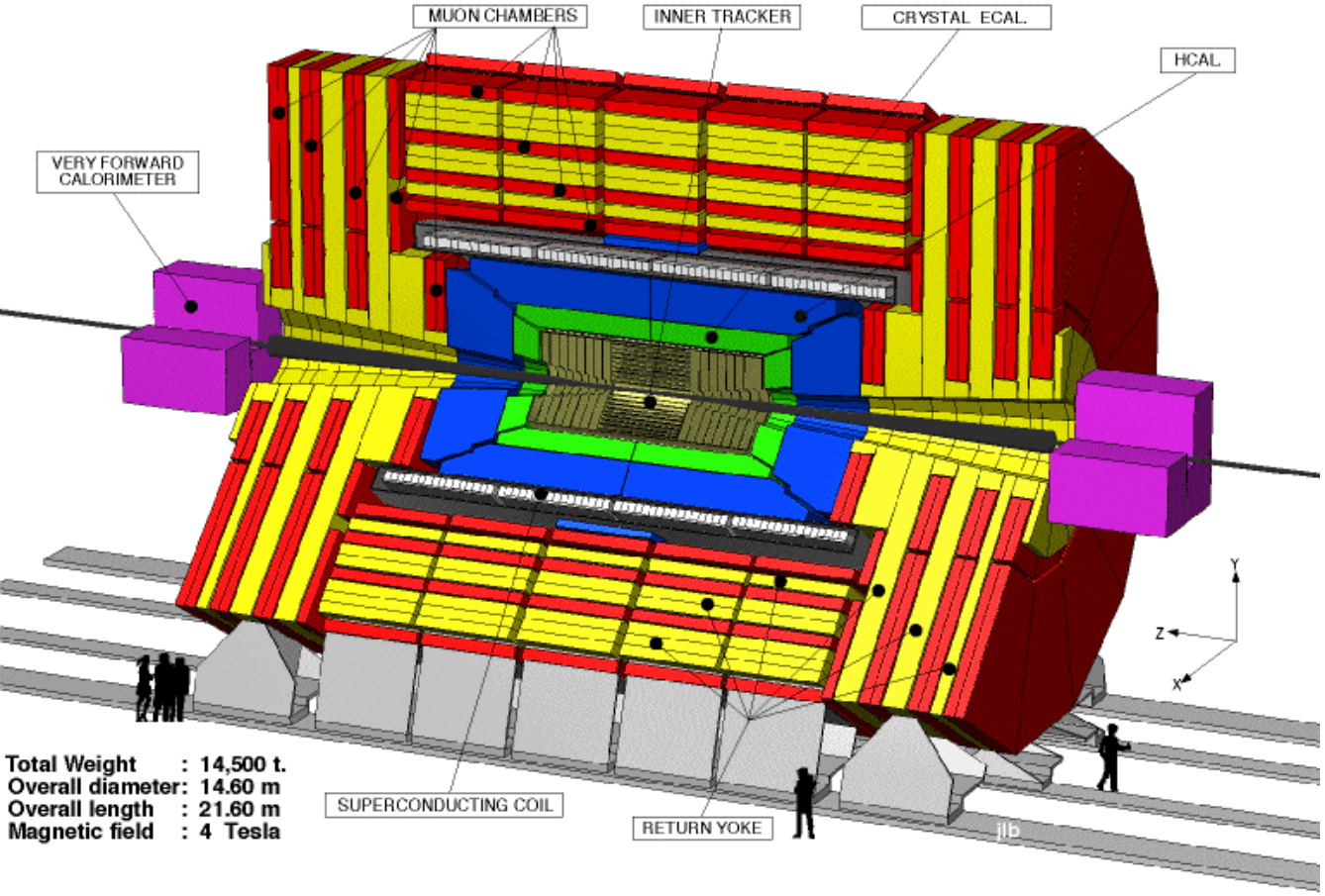
- Introduction
- Motivation for the upgrade
- The upgraded pixel detector
- Contributions of DESY/UHH
- Summary and Outlook

The Large Hadron Collider



- Located at European Center for Nuclear Research (CERN) along French-Swiss border
- pp collider with design center-of-mass energy of 14 TeV (currently 8 TeV), 27 km circumference

The CMS Detector



- 3.8 T solenoid magnet
- Silicon tracker
  - Strips ~9 million ch.
  - Pixels ~66 million ch.
- Electronic calorimeter
  - $PbWO_4$ crystals
- Hadronic calorimeter
  - Brass/scintillator
- Muon chambers embedded in return yoke

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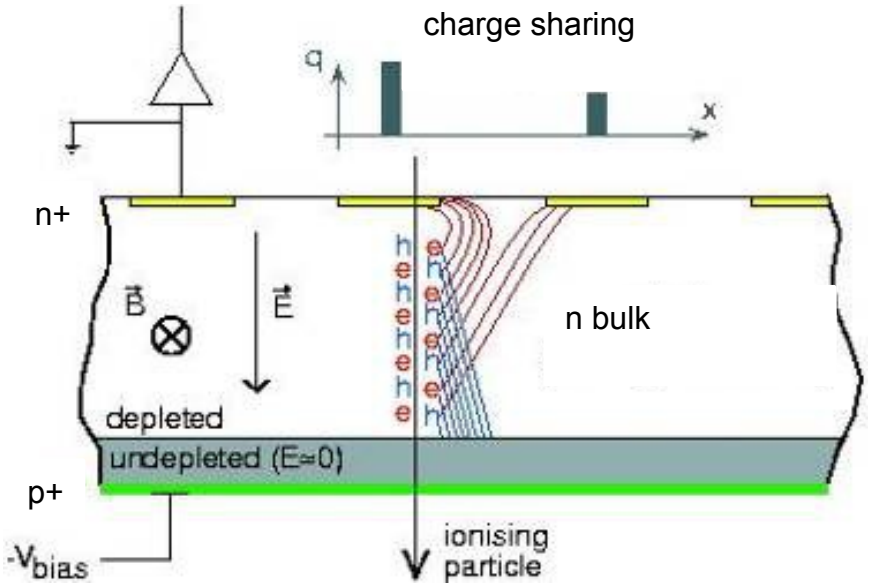
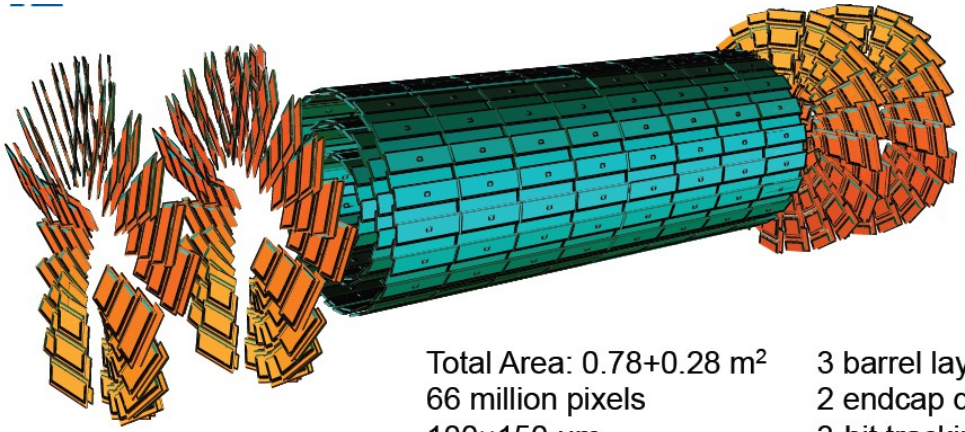
Operating Principle of a Silicon Pixel Detector

- Charged particle passes through silicon, creates electron/hole pairs
- Electric field in sensor causes electrons/holes to separate
  - Electrons are collected at pixel implant
- Magnetic field: charges experience Lorentz force
  - Charge shared between multiple pixels
- Charge sharing leads to better spatial resolution (~10 µm)

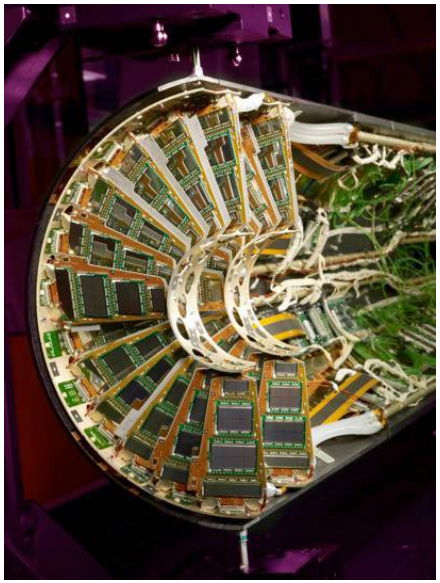


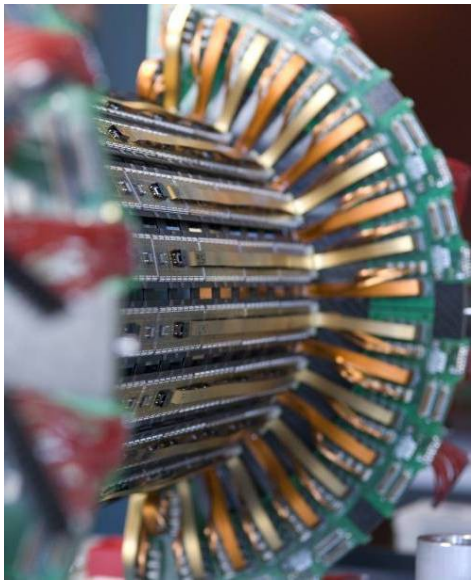
The Present Pixel Detector



Total Area: 0.78+0.28 m²
66 million pixels
100×150 μm

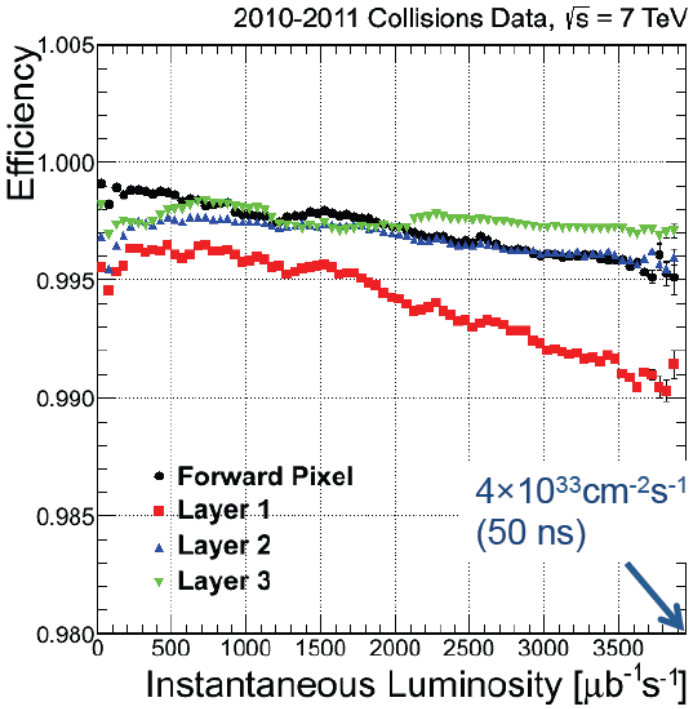
3 barrel layers @ 4,7,11 cm
2 endcap disks
3-hit tracking |η|<2.5





Motivation for the Upgrade

- Dead time of readout chip (ROC)
  - Can already clearly see drop in efficiency as a function of instantaneous luminosity
- Radiation damage in sensors leads to less charge sharing (smaller Lorentz angle)
  - Degradation of spatial resolution
- Replace entire pixel detector during extended year end technical stop in 2016/17!

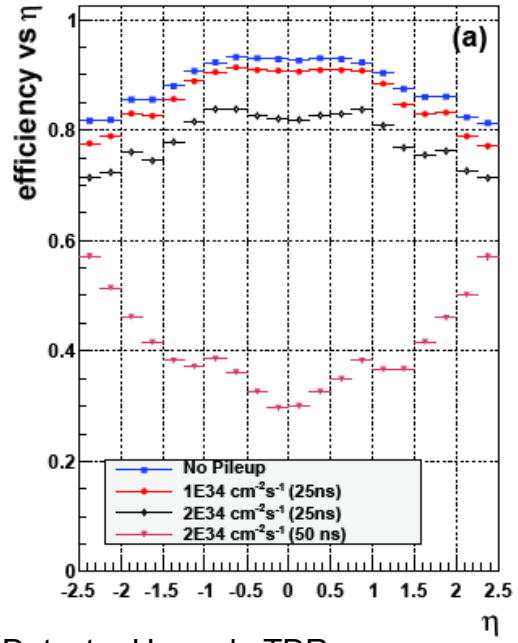


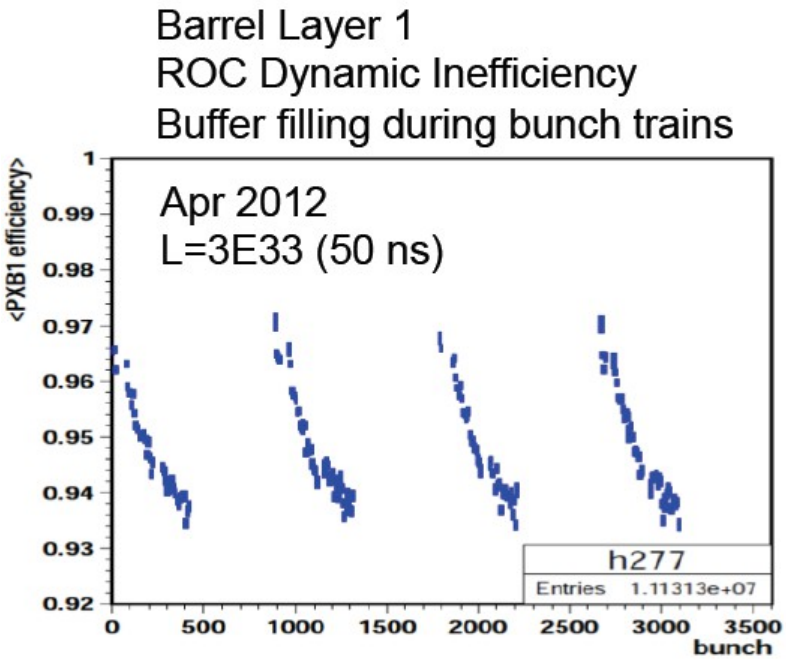
CMS Pixel Detector Upgrade TDR

A More Dramatic View…

- Note: L1 rate already beyond design expectation!
  - 0.6E34 = 30 PU @ 50 ns equivalent to 1.2E34 @ 25 ns
- Expectation at 2E34 @ 25 ns: 16% data loss at layer 1!

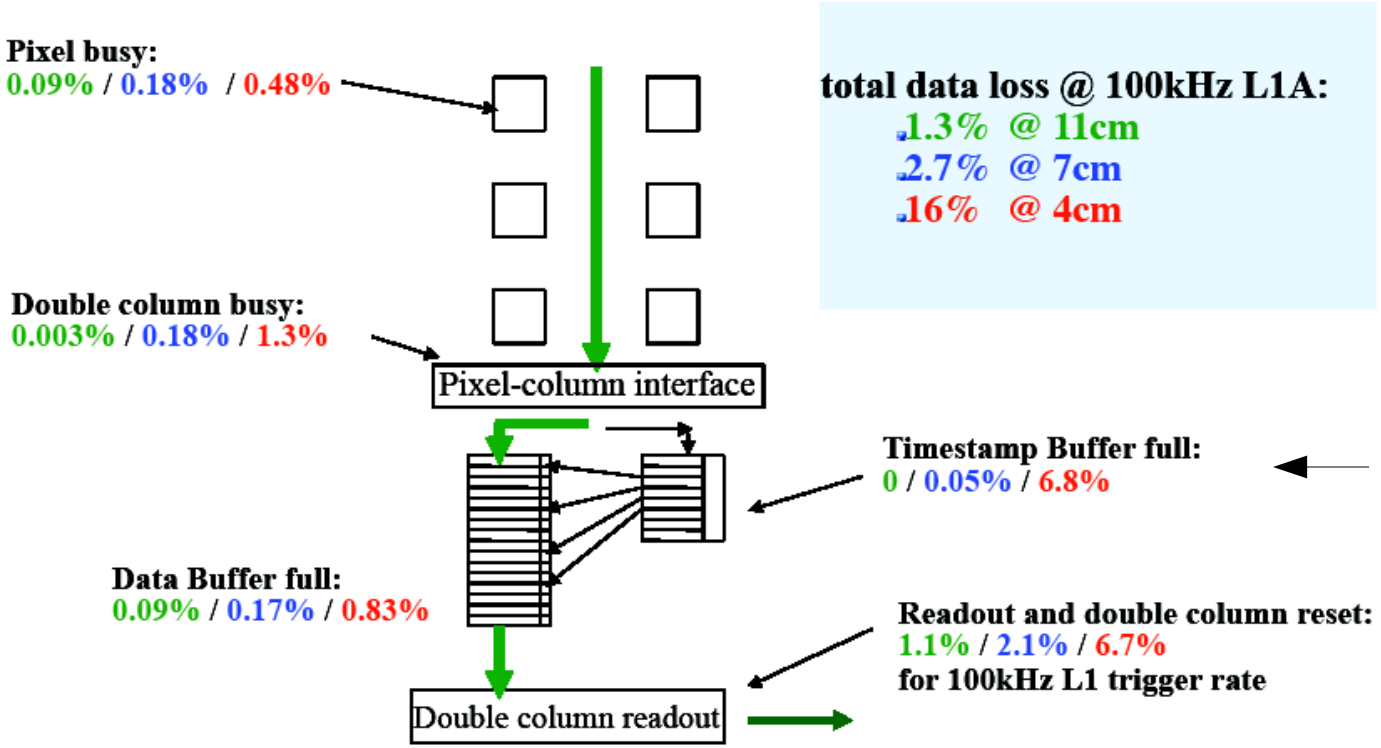
Efficiency vs. η in simulated $t\bar{t}$ events





CMS Pixel Detector Upgrade TDR

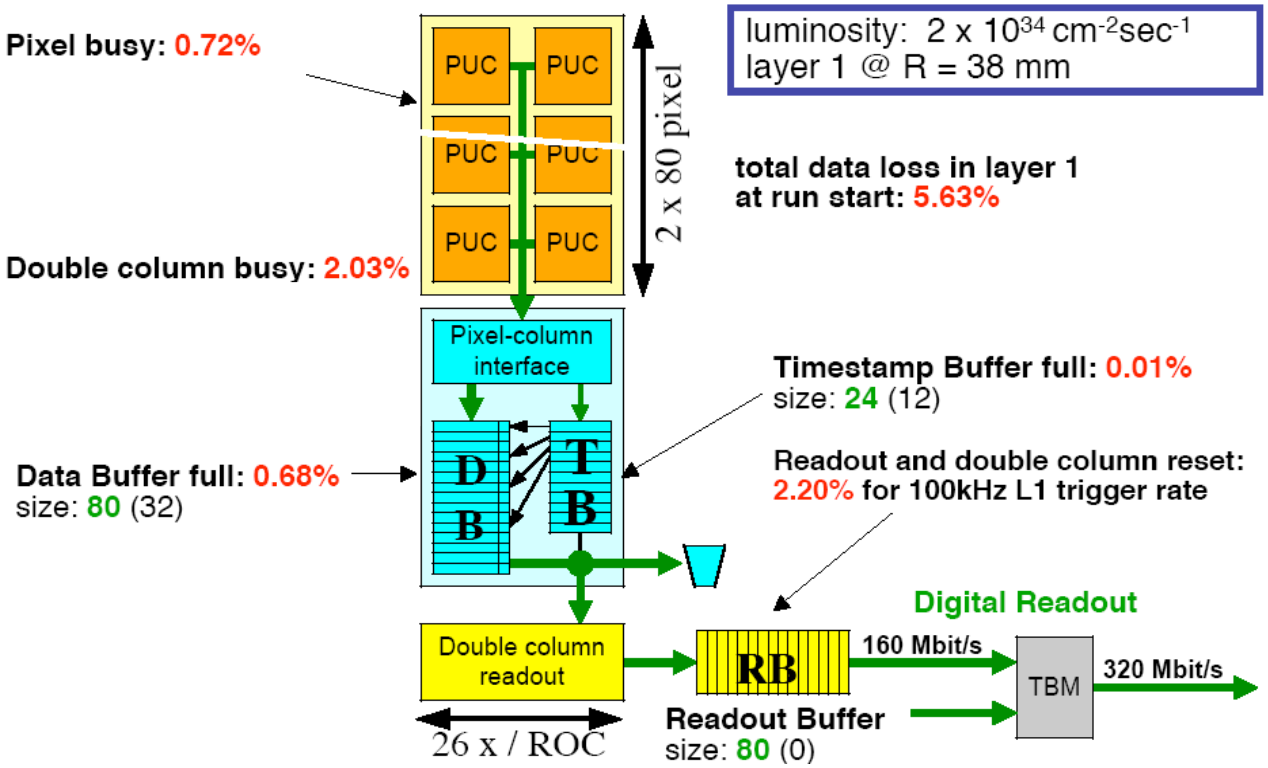
Data Loss Mechanisms: Current Chip



Present psi46 readout chip (ROC) simulated at 2x LHC design luminosity

H.C. Kaestli, Pixel upgrade meeting Oct 2008
http://indico.cern.ch/conferenceDisplay.py?confId=41745

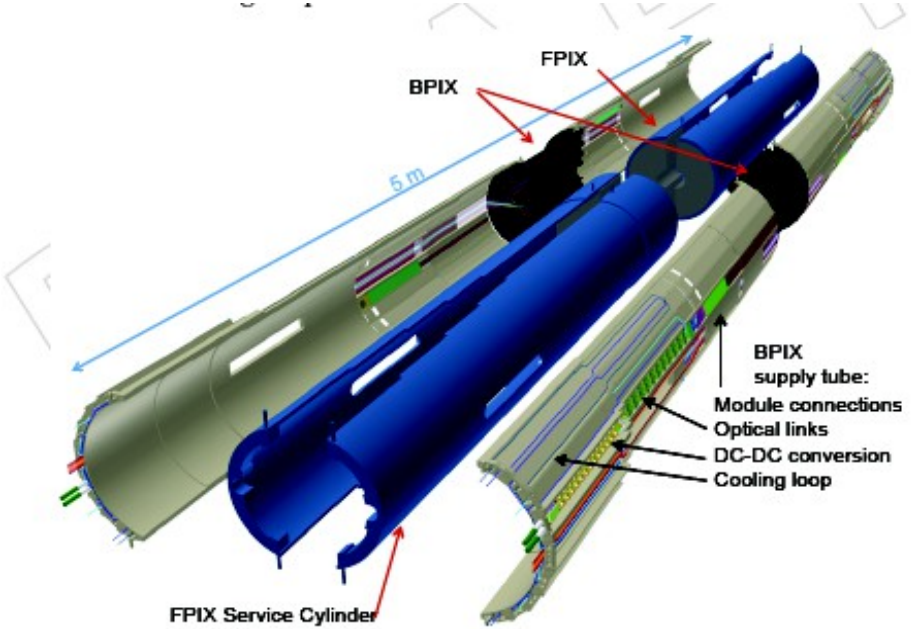
Data Loss Mechanisms: New Chip



- Increased timestamp and data buffers
- Added readout buffer
- Digital readout

H.C. Kaestli
Oct 2009

The Upgraded Pixel Detector



- 4 layer + 3 disk layout, reduced inner radius
- Low mass mechanics and service cylinders, move material out of active region
- New digital ROC, based on present psi46
- Optical readout: analog 40 MHz → digital 320 Mbit/s (x2)
- Powering with dc-dc converters, using existing cables
- Dual-phase CO_2 cooling, low mass/low temperature
  - Current detector uses C_6F_{14}
  - Has been operating at ~17 C (2010-2011) and ~10 C (2012), want to go to ~-10 C

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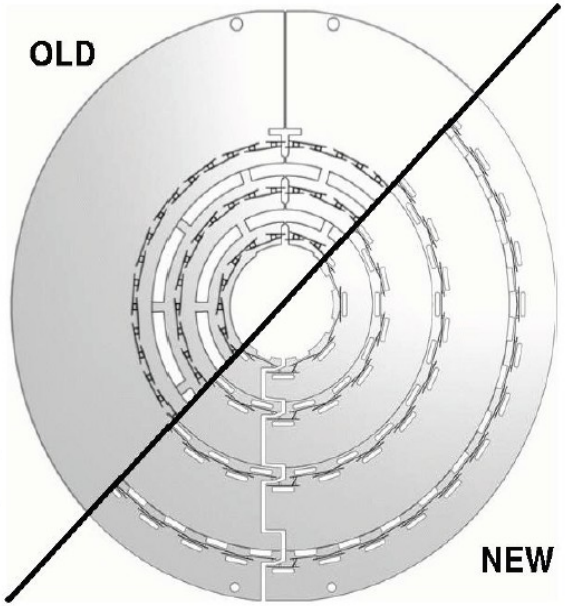
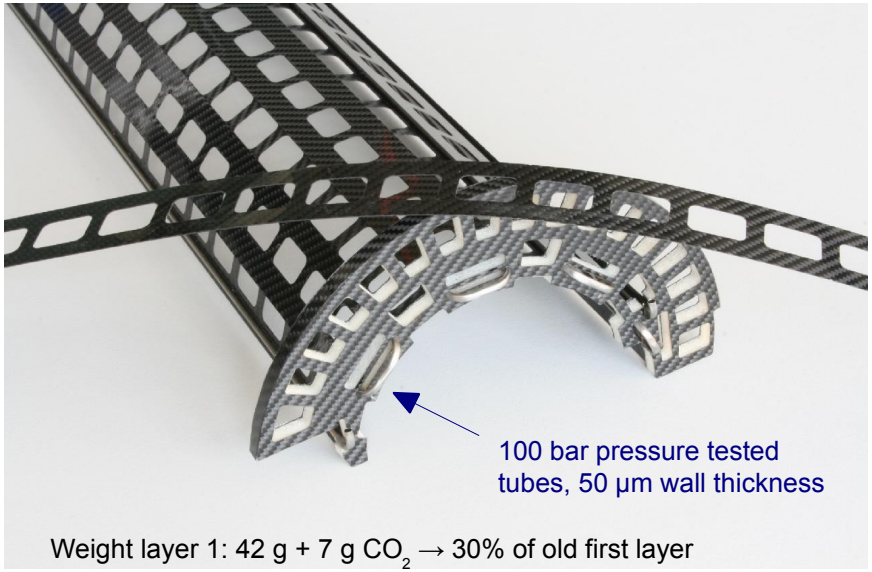
The Pixel Barrel Detector: Mechanics





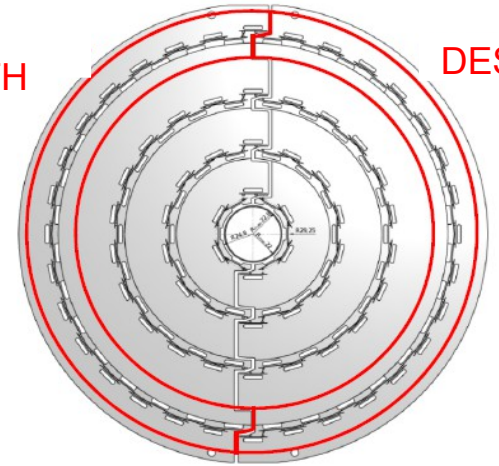
Weight layer 1: 42 g + 7 g CO_2 → 30% of old first layer X/X_0

2 identical half-shells with 1184 modules (79M pixels)

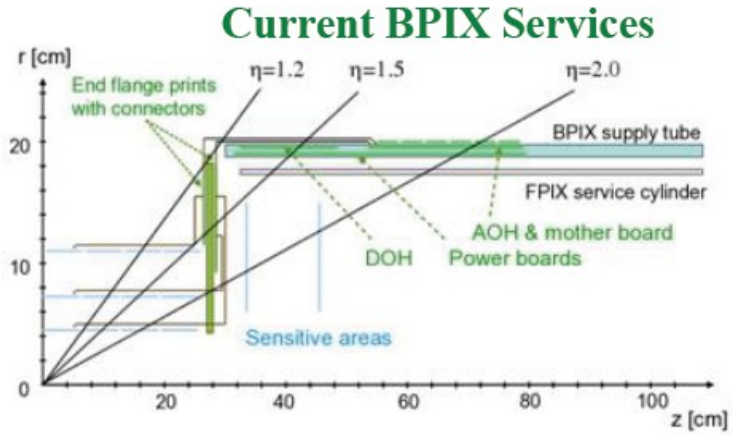
Layer	Radius (mm)	# modules	Group
1	29	96	CH (PSI)
2	68	224	CH (PSI)
3	109	352	CERN, IT, TW, FI
4	160	512	DE

KIT + RWTH Aachen

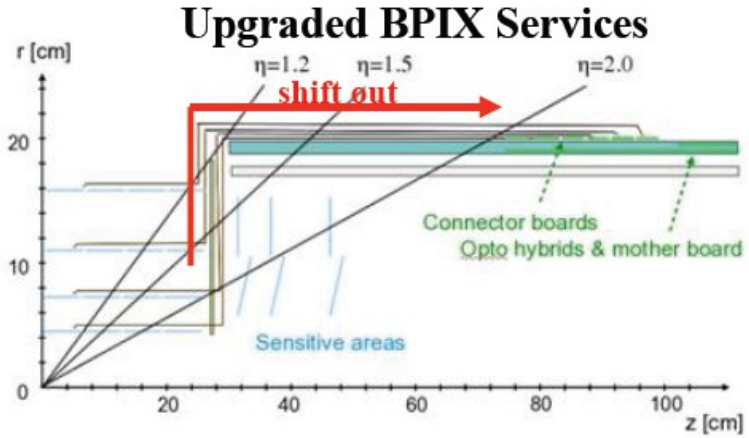
DESY + UHH



Material Budget

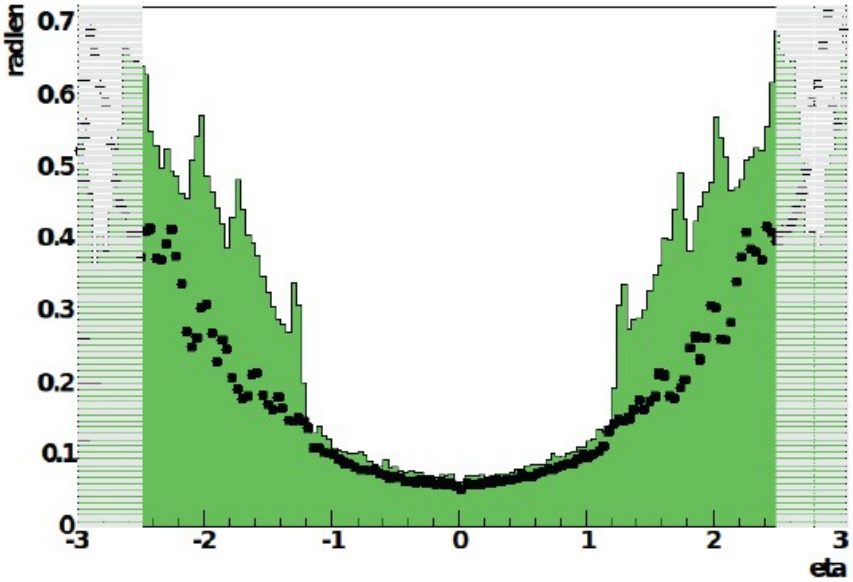


η<2.2 : weight = 16.9 Kg (3 layer)

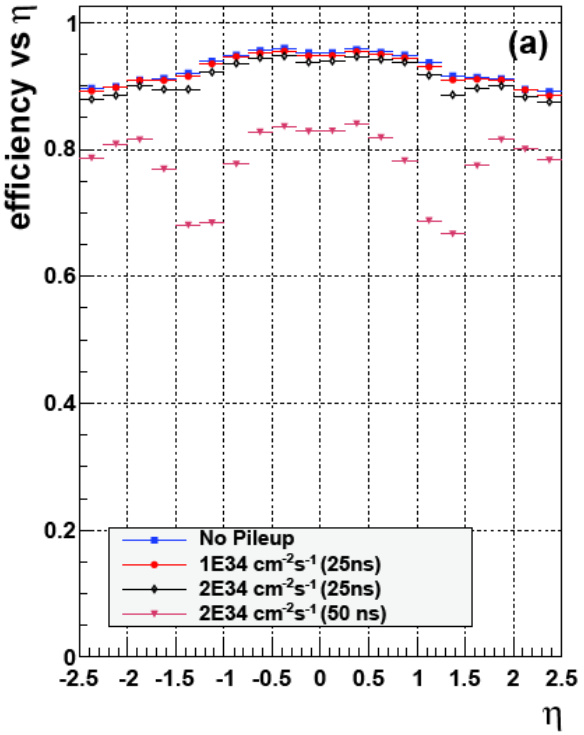


η<2.2 : weight = 6.5 Kg (4 layer)

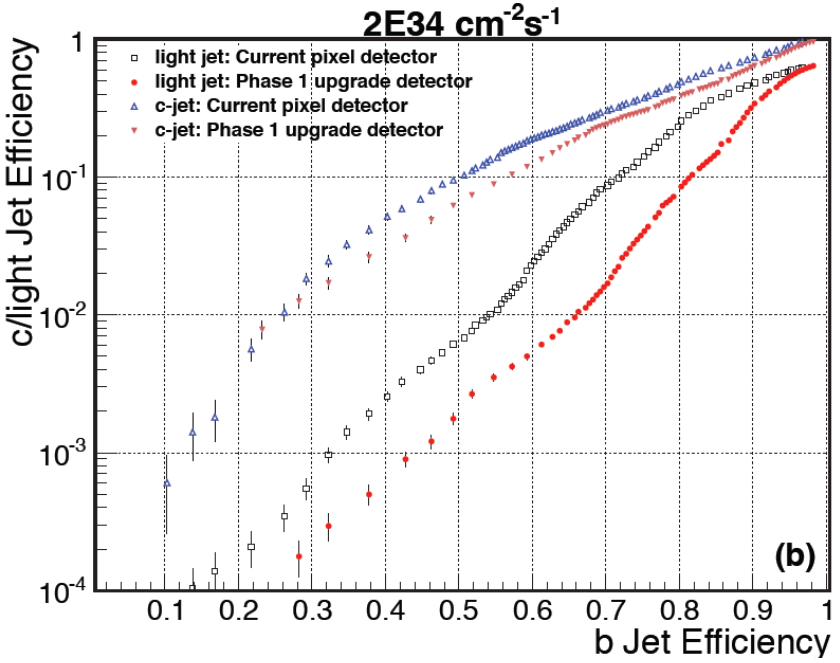
- Move services to higher rapidities outside tracker acceptance
- Optimize cooling/support/material
- Possible to add 4th layer without increase in X_0
- Substantial improvement in forward region



Performance of Upgraded Detector



Efficiency vs. η in simulated $t\bar{t}$ events

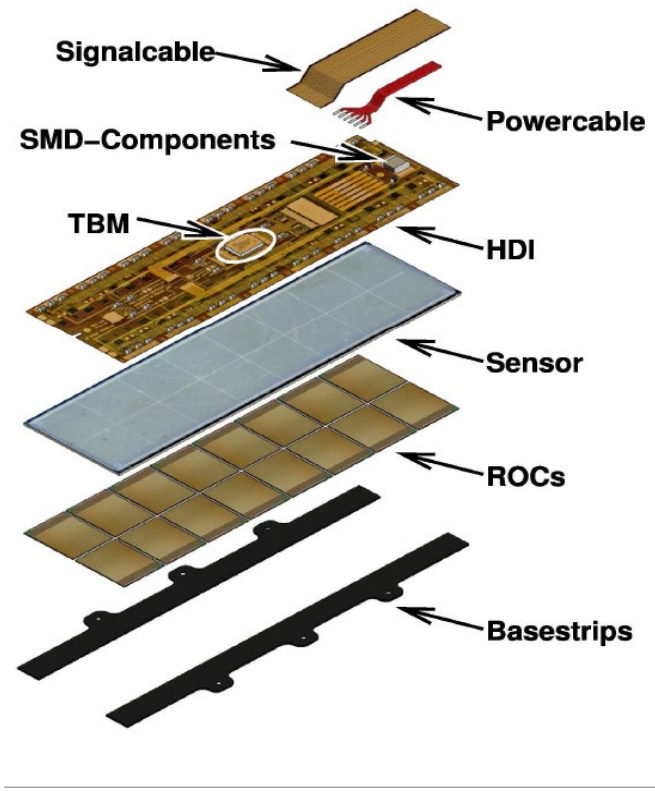


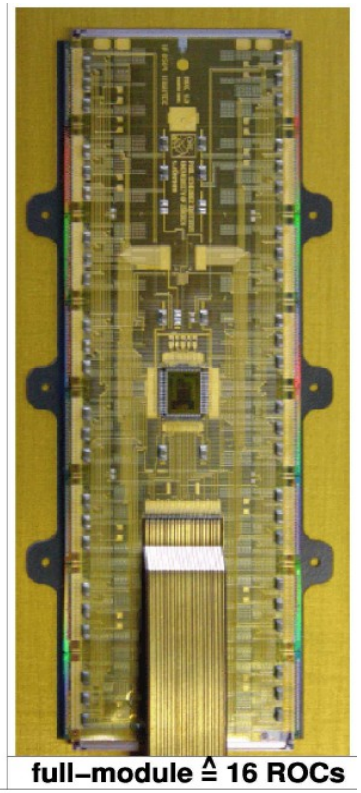
- Combined secondary vertex *b*-tagger
- Factor 2-4 better rejection of light quark jets (without further retuning of the algorithm!)

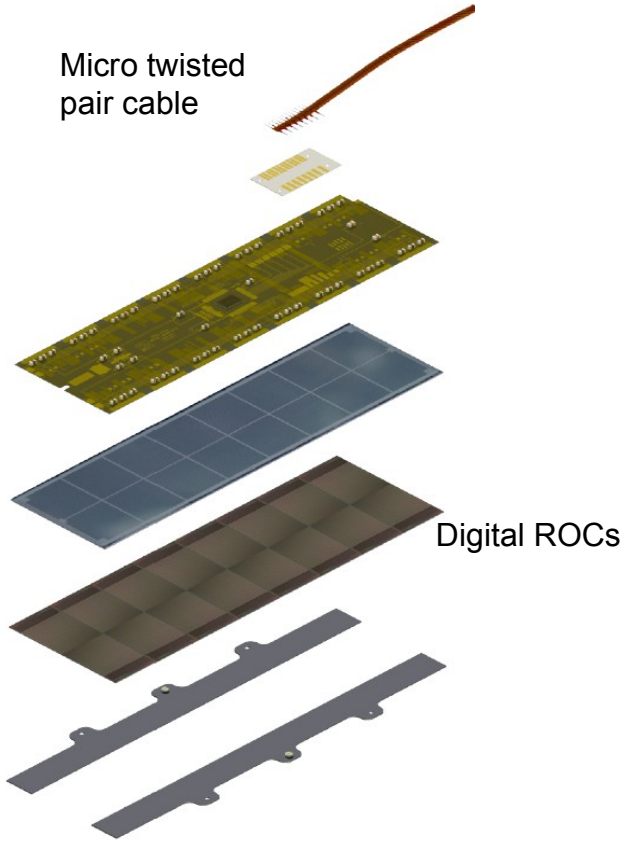
Reminder: 2E34 cm2s-1 (25 ns) with current detector only at ~80% efficiency!

CMS Pixel Detector Upgrade TDR

Module Building





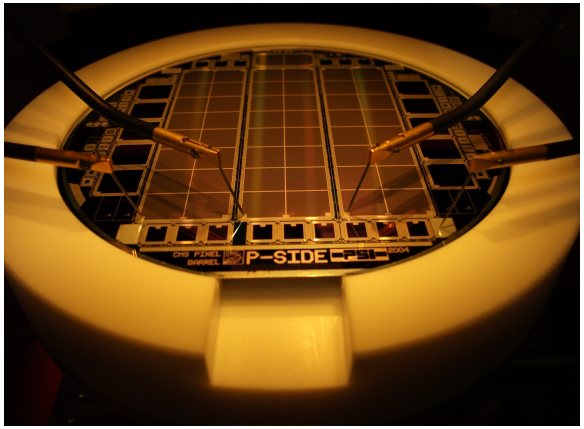


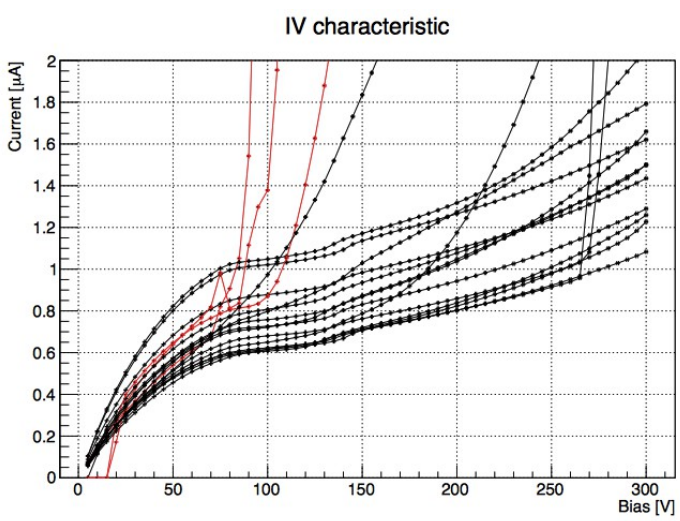
- Production of 4th layer split into two halves
  - DESY + UniHH
  - KIT + RWTH Aachen
- Throughput limited by bump deposition
  - 2 modules/day (350 modules/site)

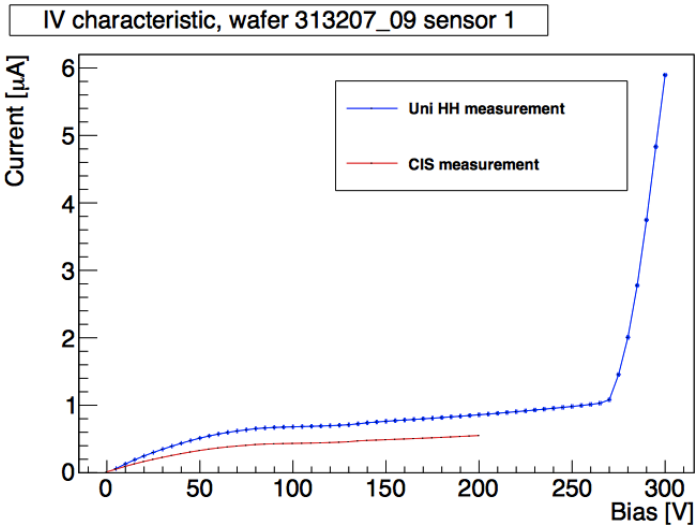
  → 175 days!

Wafer IV Measurements (UHH)

- Measure IV curves of sensors on-wafer to check quality before bump bonding
  - Scratches, etc. show up in early breakdown
- Measured first batch of sensors, measurements agree well with the data and measurements provided by manufacturer (CiS Erfurt)
- After under bump metalization and dicing, will measure IV curves again







Difference consistent with difference in temperature

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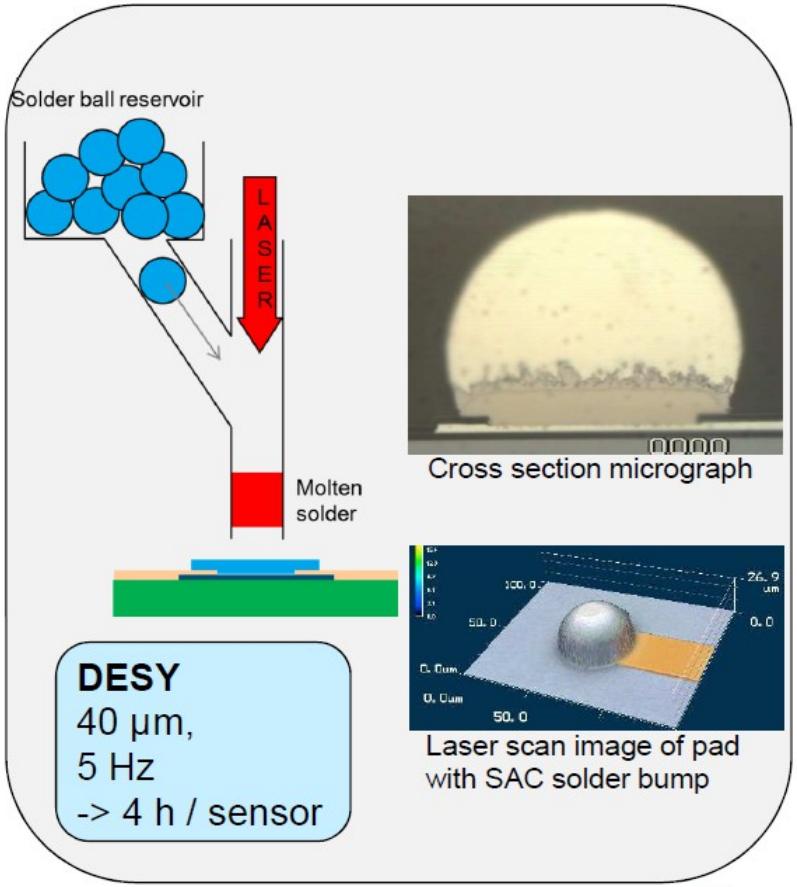
Module Building: Bump Bonding (DESY)

1. Bump Deposition

Pac Tech SB^2 Jet
66560 bumps/module



2. Flip-chip bonding

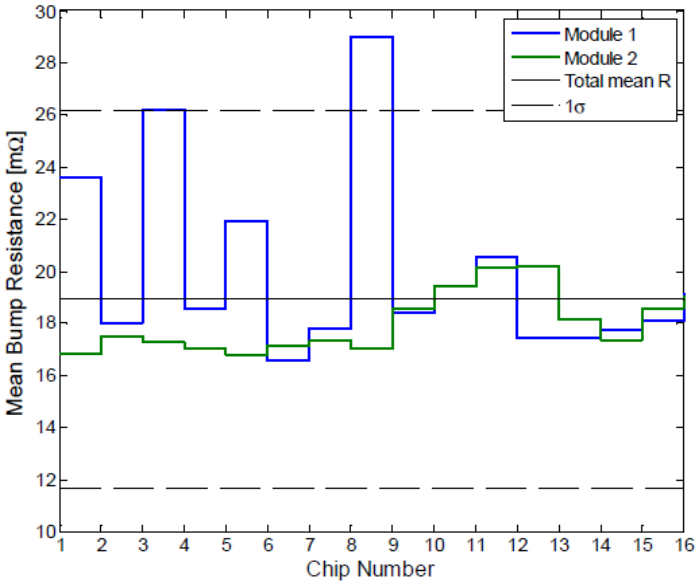
FEMTO flip-chip bonder from Finetech

- Accuracy < 1 µm
- KGD probing before bonding
- ~ 1 min./chip (without probing)
- Reflow ~ 3 min.

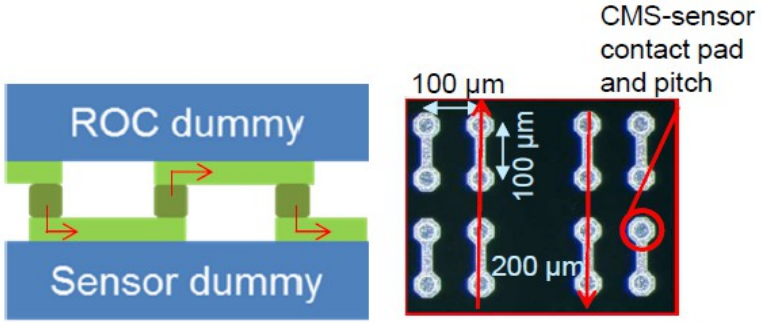
Jan Hampe, Phase 1 Pixel Upgrade Workshop, 28.08.2012

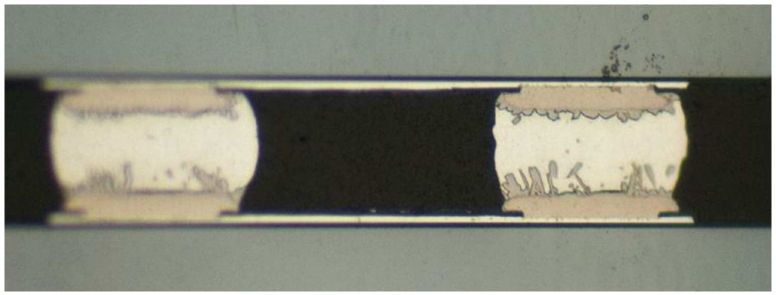
Module Building: Bump Bonding (DESY)

- 26 double columns/ROC, connected in daisy chain
- Resistance measurement
  - Single dead pixel → open circuit



First 8 chips of module 1 used several times to adjust bonding parameters!

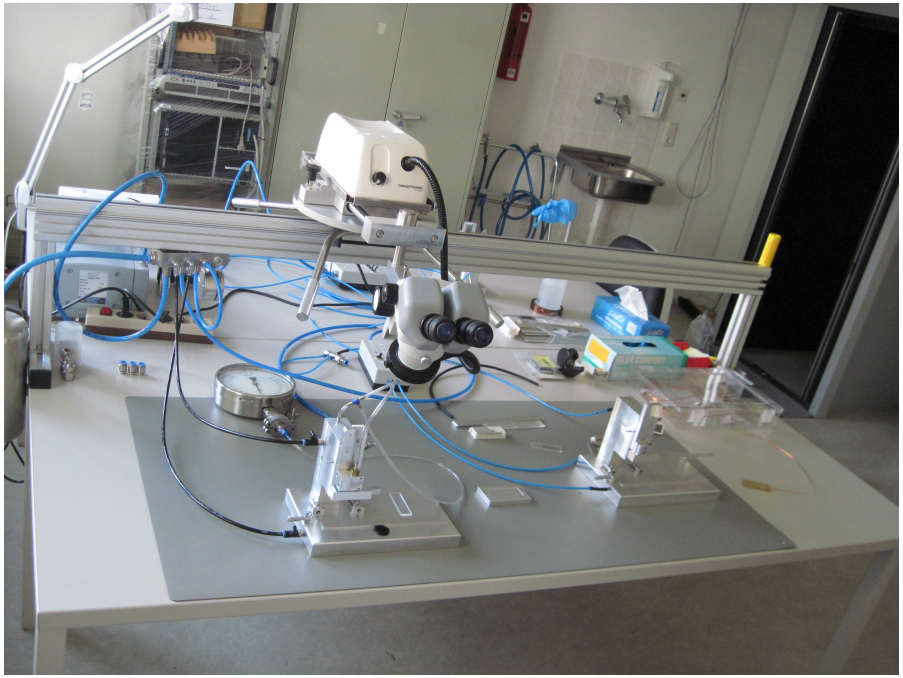


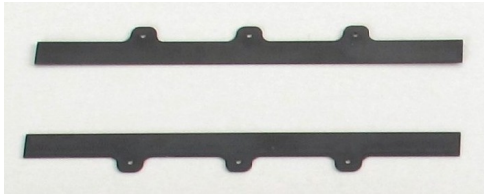


Jan Hampe, Phase 1 Pixel Upgrade Workshop, 28.08.2012

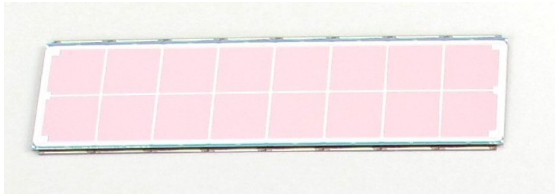
Module Building: Gluing (UniHH)

- Custom made tools, need some modifications from the ones used to build current detector
  - ROC slightly larger (increased buffers)
- Several gluing steps
  - Base strips to bare module
  - HDI to module
  - Cable to HDI/module
  - Curing takes 6 hours for each step

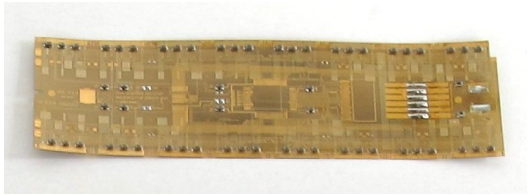




Base Strips



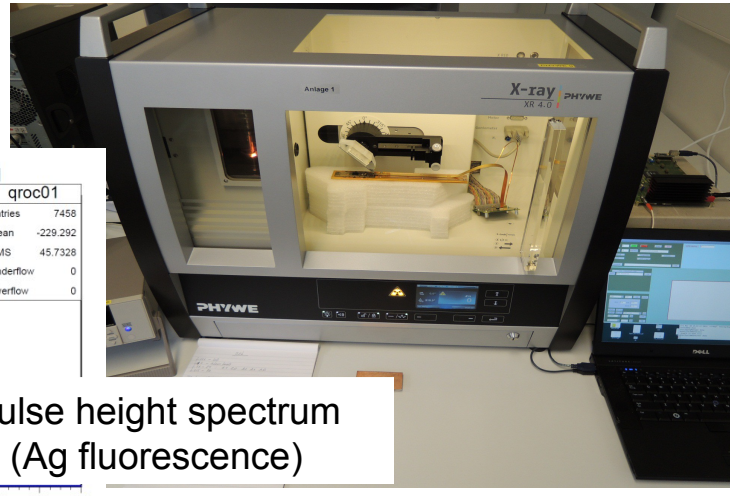
Bare Module

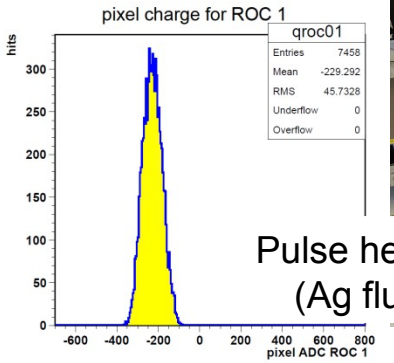


HDI

Module Calibration

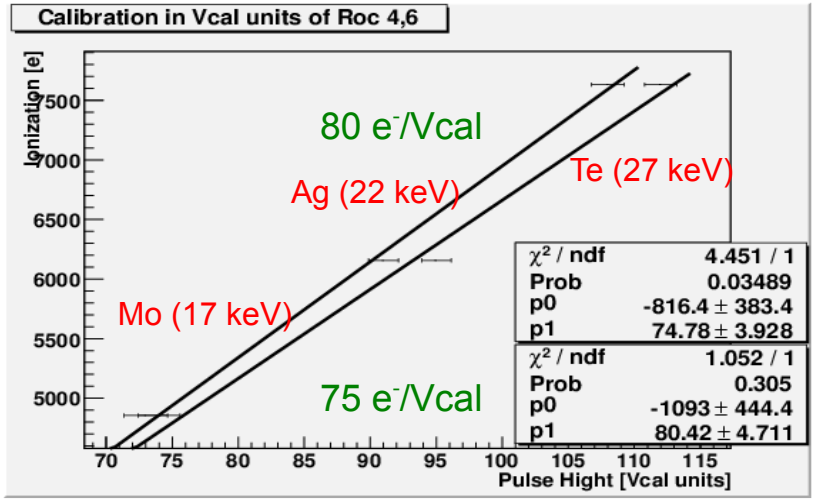
- Pixels have a threshold for sparsified readout
- The pixel thresholds are adjusted per pixel to obtain a uniform response using internal calibration pulses
- Absolute energy calibration using Xray source (Kα lines)





Pulse height spectrum (Ag fluorescence)

- Having the x-ray setups at each site means we can do many other studies, i.e.:
  - compare old and new modules
  - temperature dependence of energy calibration



Timeline (Preliminary!)

2012

- Setup infrastructure for bump bonding, module assembly testing
  - Establish bump bonding technology on existing module

2013

- Order sensors
- Prepare for series production
  - Spring: All production centers must be approved by CMS

2014/15

- Series production

2016

- Assemble 4th layer @DESY
- Group test
- Transport to Switzerland

- Installation in CMS at extended year end stop 2016/17

Summary and Outlook

Phase 1 Pixel Upgrade:

- Integrated luminosity (radiation damage) → degraded spatial resolution
- Increased instantaneous luminosity → severe dead time in present pixel chip
  - Need new pixel detector!

- Upgrading from 3 → 4 layers and improving material budget → better physics performance
  - i.e. *b*-tagging: Light quark rejection improves by at least factor 2-4
- New digital readout chip greatly reduces dead time/data loss

- Installation in 2016/17 extended year end shutdown

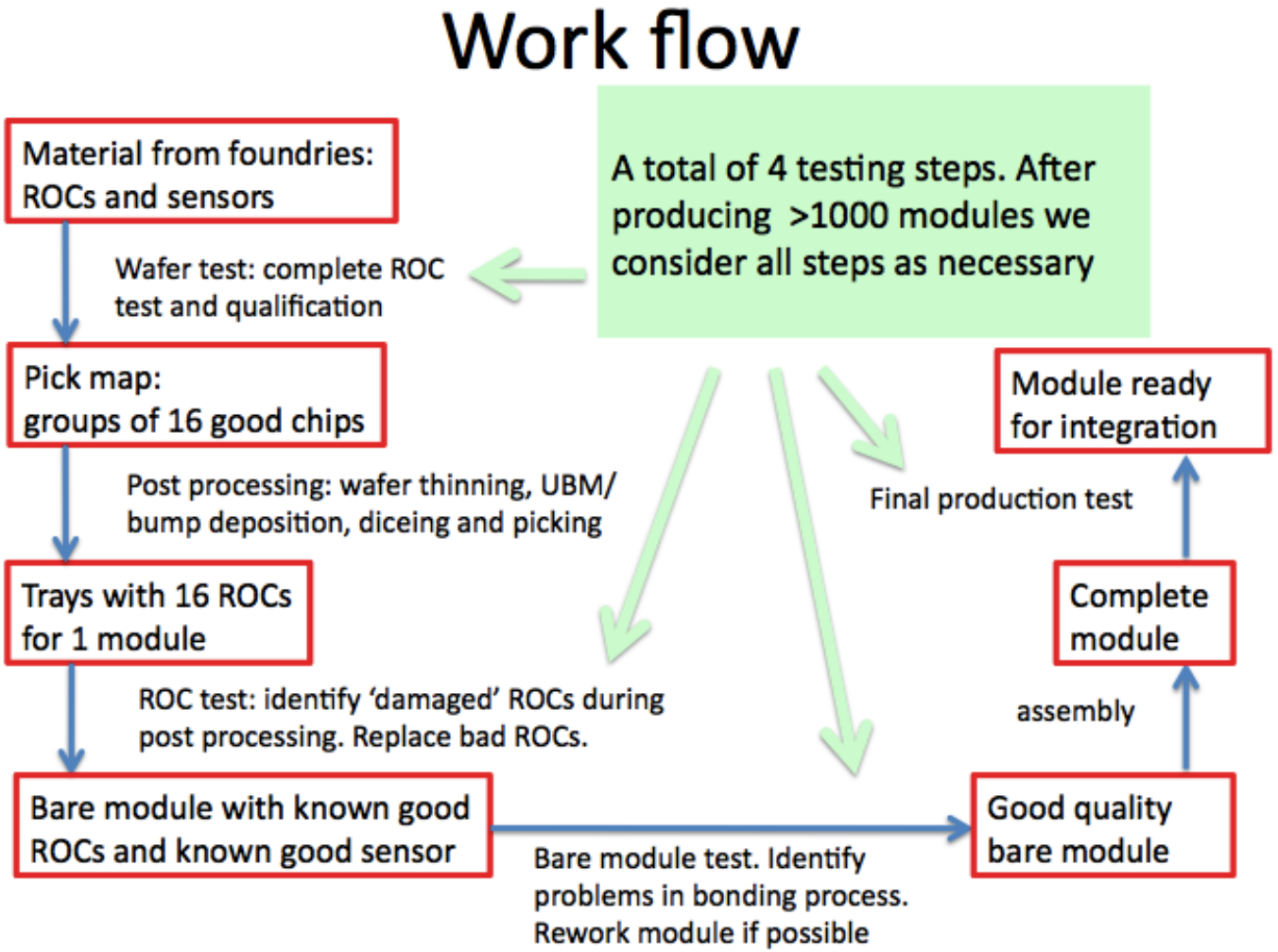
DESY/UHH:

- DESY + UHH will build half of the 4th layer (other half by KIT + RWTH Aachen)
- Many different construction and testing setups needed
  - wafer IV-tests
  - bump bonding
  - module gluing
  - module testing
  - x-ray calibration
  - testbeams

- Setups for all these tasks exist or are in progress, but still a lot of work to do!

Backup Slides

Module Work Flow

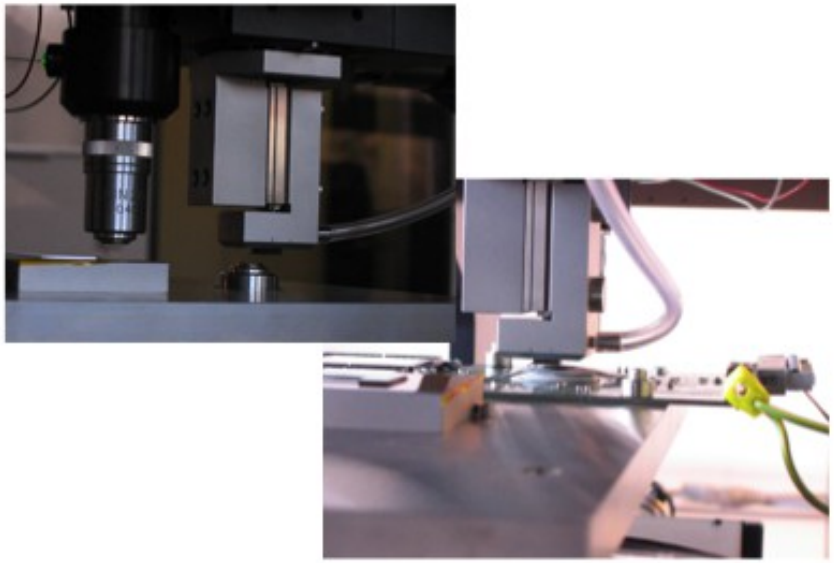


H.C. Kaestli, Pixel Phase 1 Upgrade Workshop Aug 2012
https://indico.cern.ch/conferenceTimeTable.py?confId=196414#20120828

Chip test on flip chip bonder

ROC test after post processing → individual (picked) ROCs
Painful from handling point of view
At PSI done on flip chip bonder. Chip on tool at well measured position anyway
Mandatory step: Chip failure on 1% level → 15 % level for module
Only quick functional test:

- Measure current consumption before/after initialization
- Check I2C interface
- Check token
- Set analog current
- read temp DAC
- Measure LVDS levels
- Measure analog levels
- Pixel alive test



H.C. Kaestli, Pixel Phase 1 Upgrade Workshop Aug 2012
https://indico.cern.ch/conferenceTimeTable.py?confId=196414#20120828

Bare module test

- Routinely made for all bare modules (time needed: ~15 minutes)
- **Very fast feedback to bumping / bonding process** (same day in our case)
  - Processes are never stable. Don't expect that once you made it through the learning curve, you will only produce good bare modules.
  - A quick feedback will save you a lot of money.
  - Ideally this should be done at the bump bond vendors place
- Last stage where module can be reworked.
  - Components to finish module (HDI, signal cables, base strips) are substantial contribution to budget
  - Rework can be done successfully (PSI: ~80% success for selected modules, IZM did it routinely for ATLAS modules, efficiency unknown to me)
- Tests done:
  - Sensor IV curve
  - ROC current consumption before/after initialization
  - I2C test
  - Token passage
  - Set analog current
  - Scan through all DACs
  - Analog level measurement
  - **Bump yield test**

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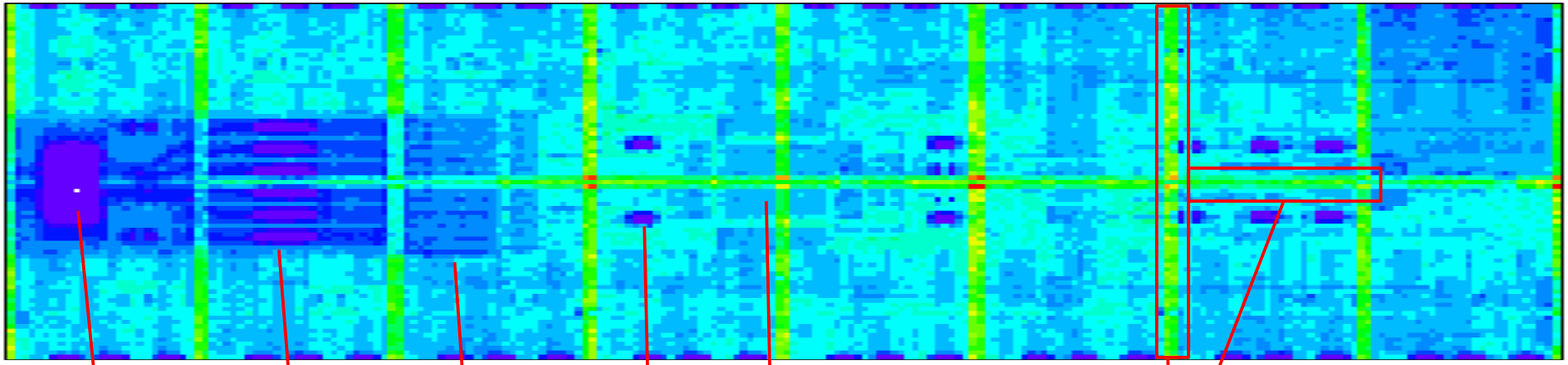
X ray map through the HDI



Bias filter cap.

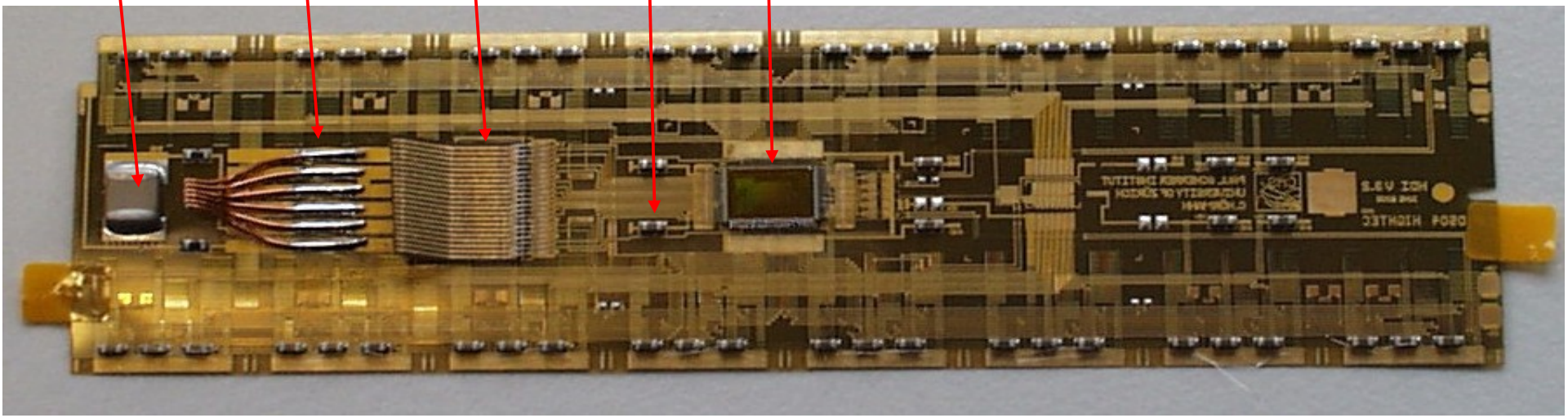
Power cable

Signal cable

SMD comp.

TBM

Edge pixels are bigger → more entries



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Performance Gain

Transverse Impact parameter: Muons, 50 pileup