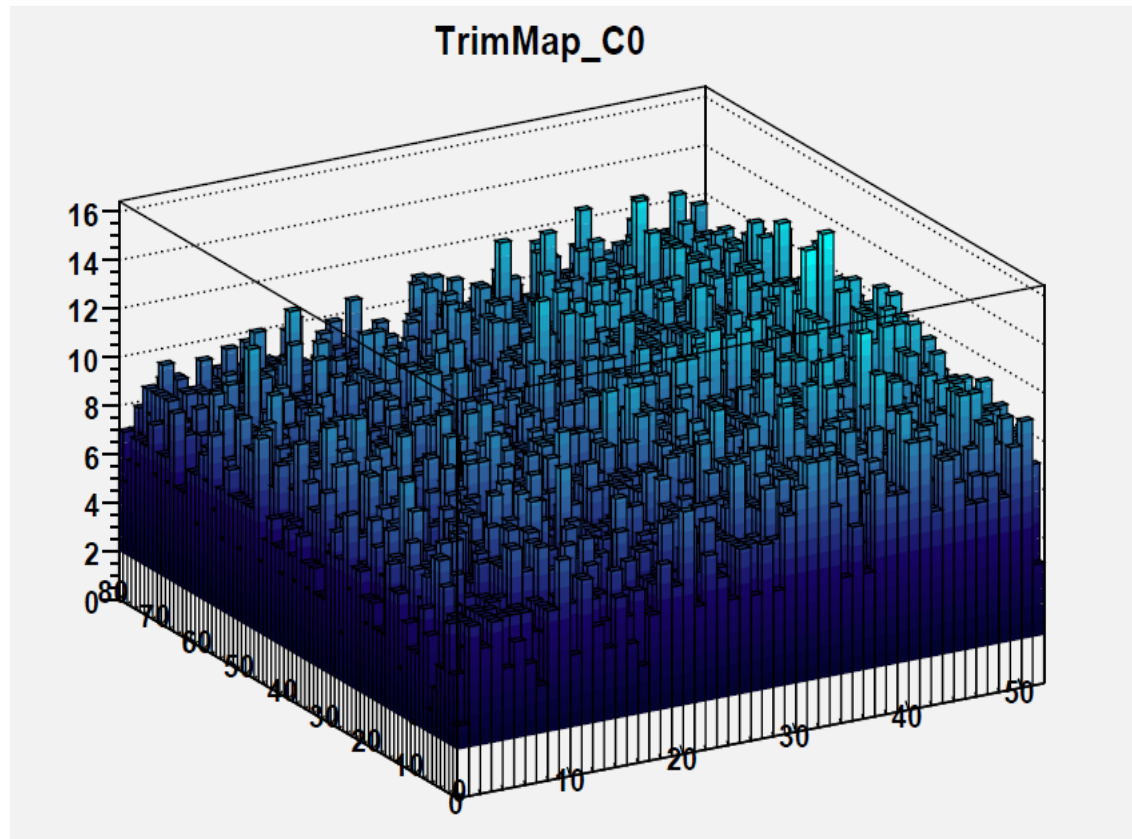


Analog tuning of the digital ROC

A. Petrukhin, D. Pitzl

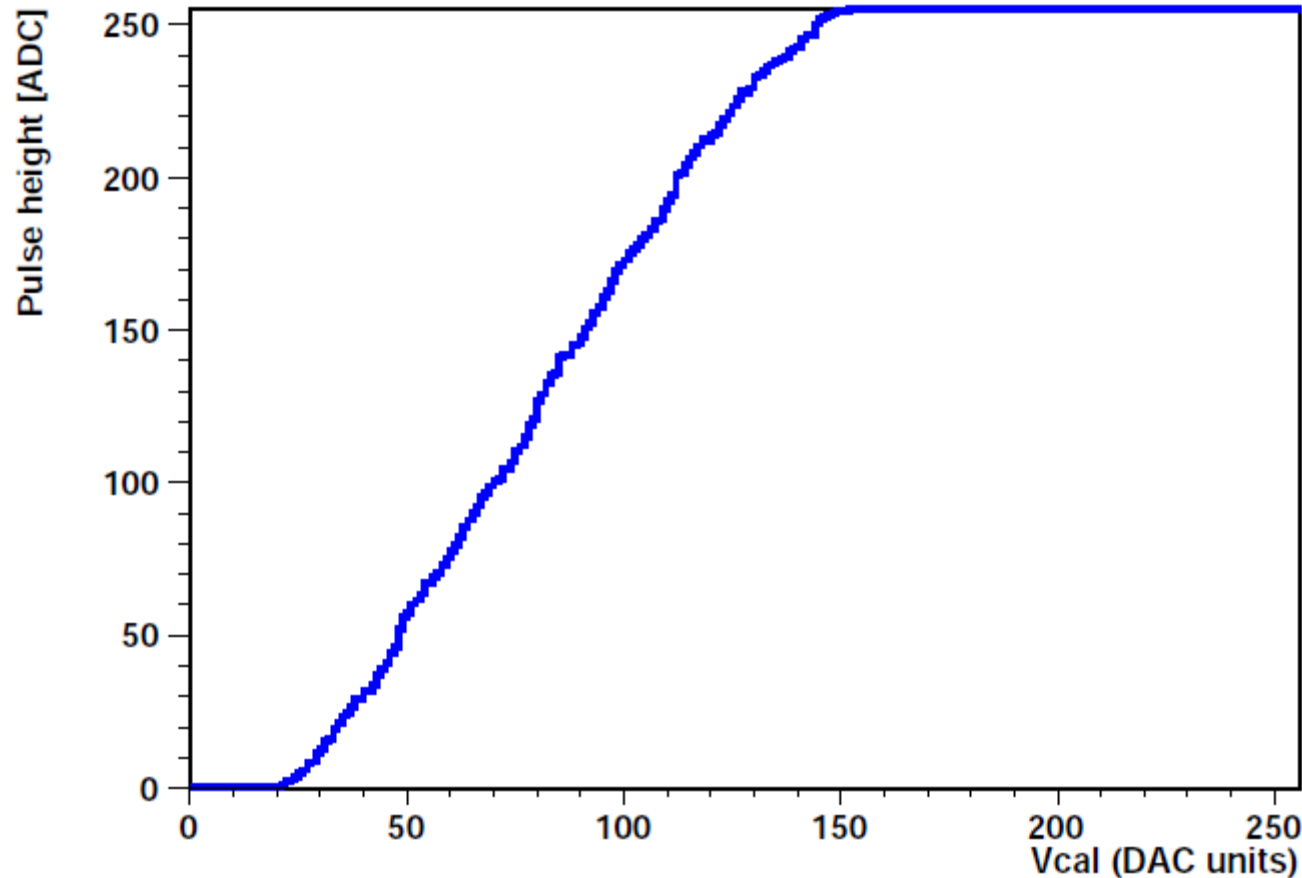
CMS pixel upgrade meeting, Grindelwald, 28.8.2012



- the problem
- tuning with DACs
- pulse height results

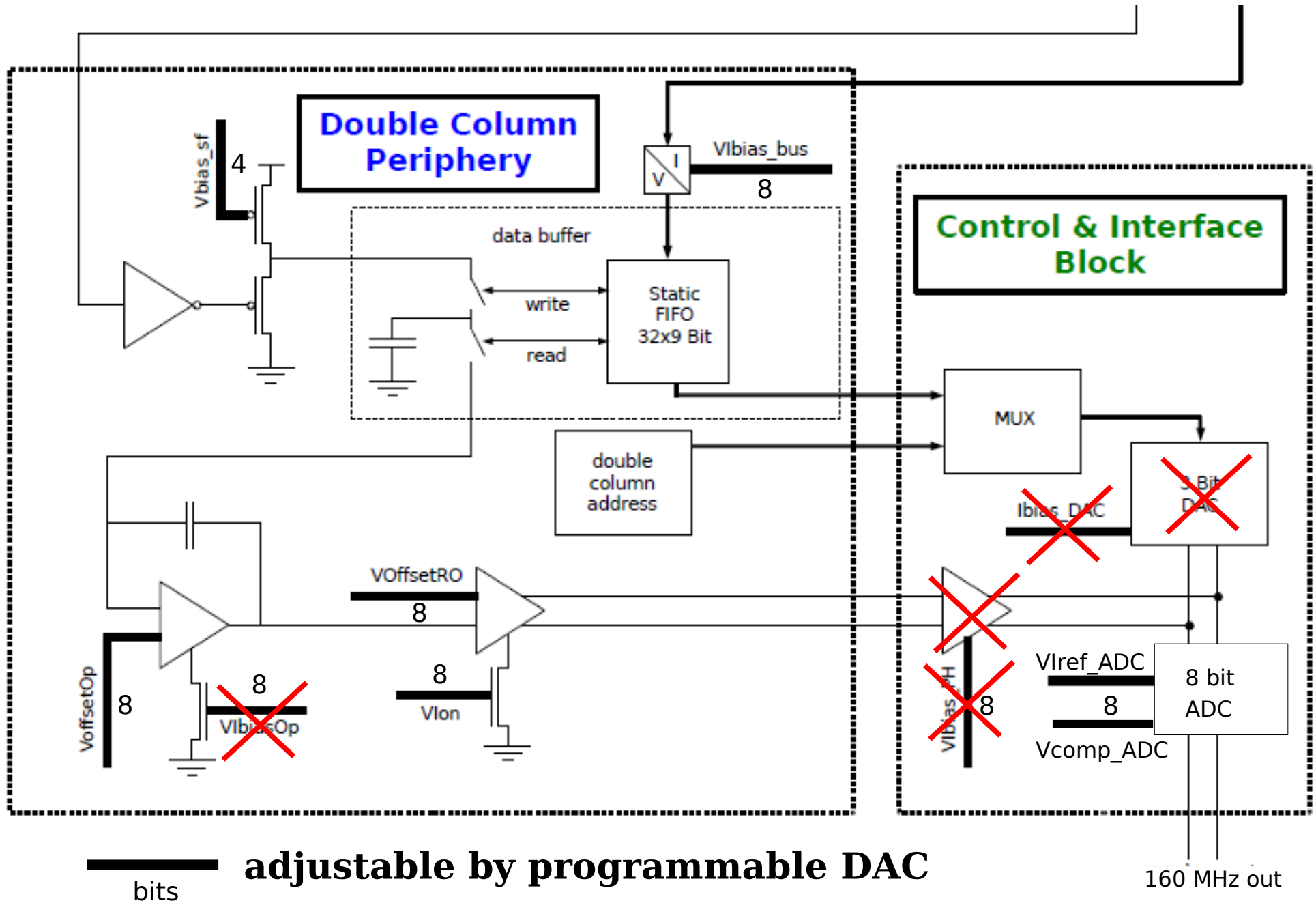
The problem

Pulse height vs calibrate signal:



- 8 bit ADC on the digital ROC:
 - range 0 to 255
- Pulse height vs large Vcal
- ADC overflow at large pulses
- ADC underflow at small pulses:
 - actual threshold is at 4 large Vcal
- need tuning procedure...

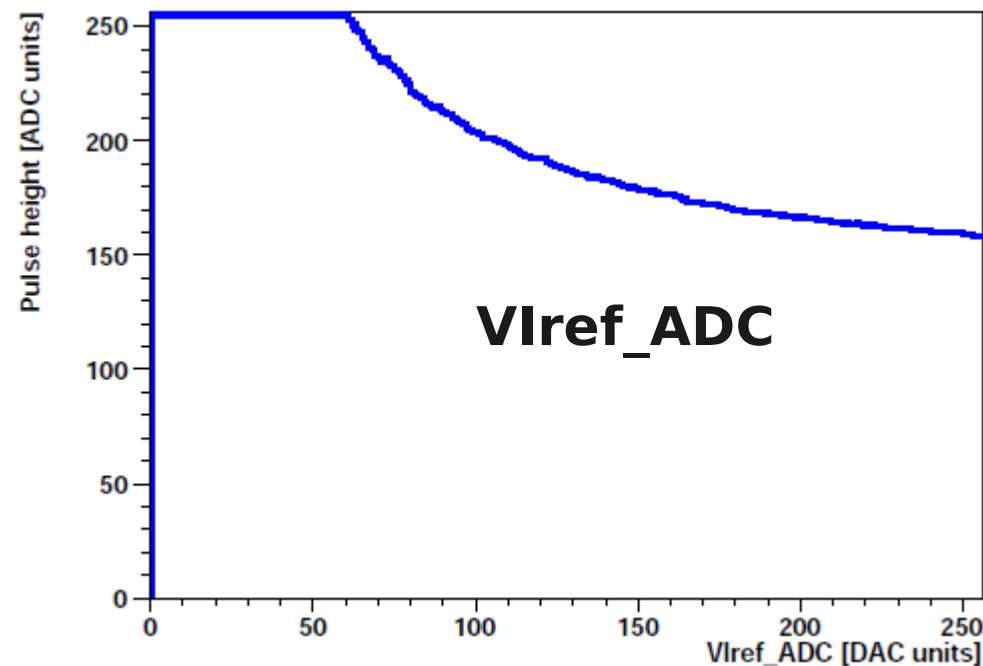
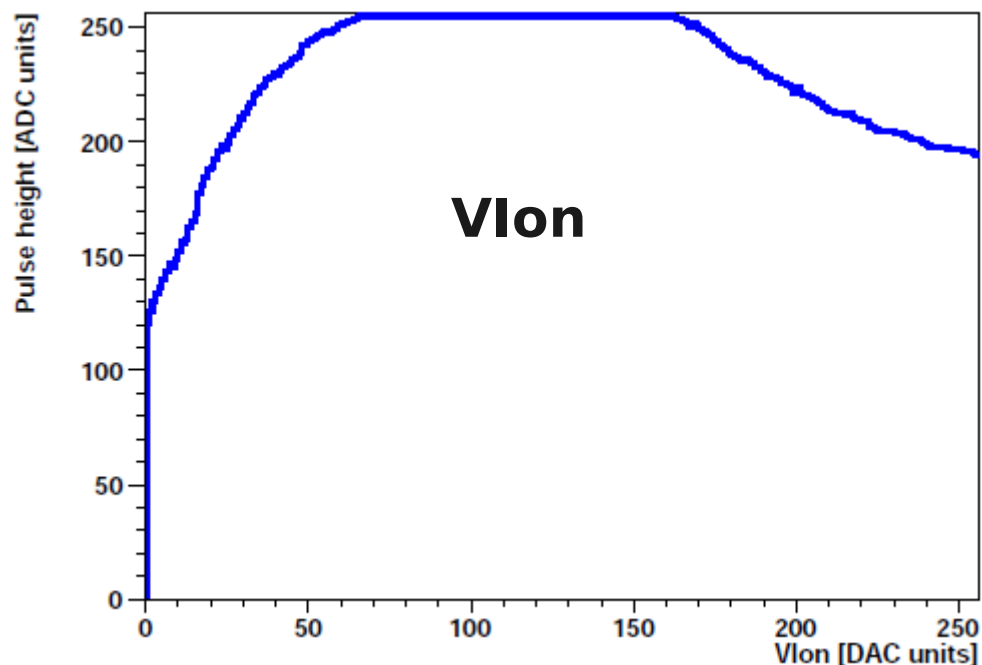
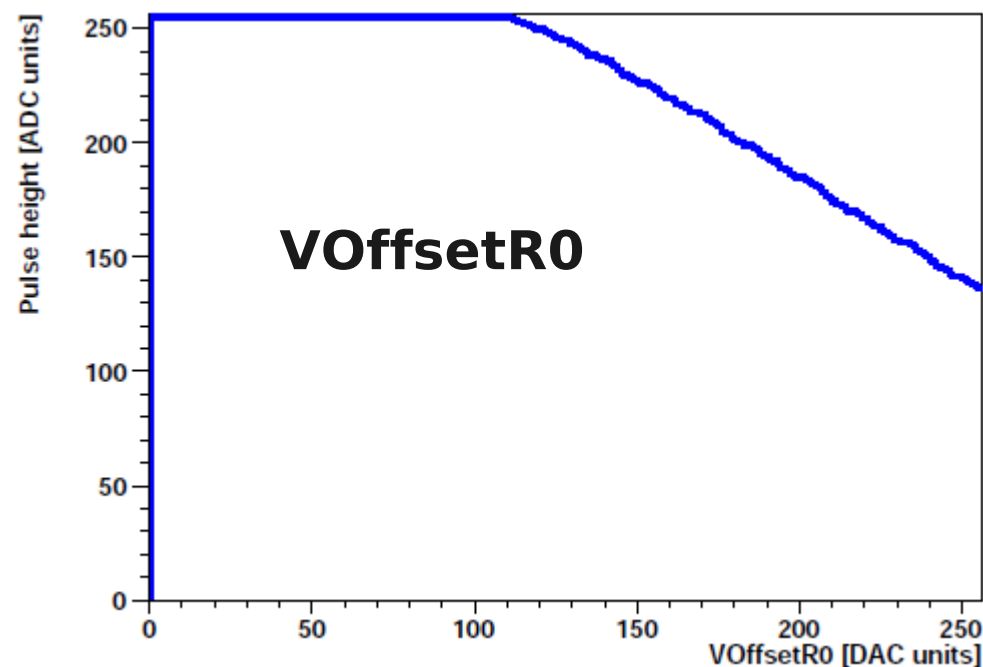
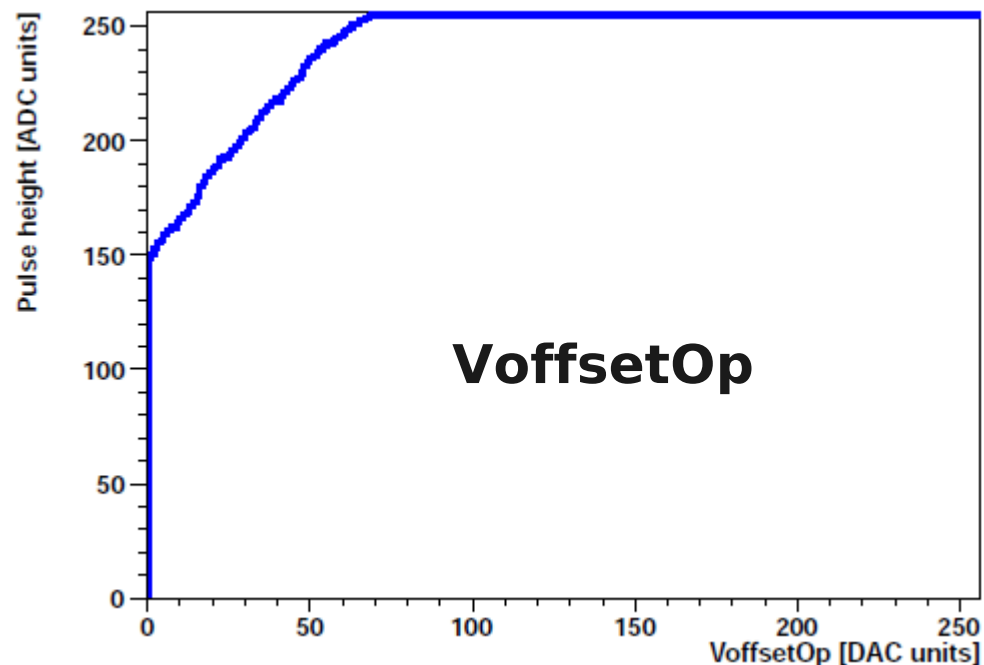
psi46dig readout



pix 3-3

DAC dependencies

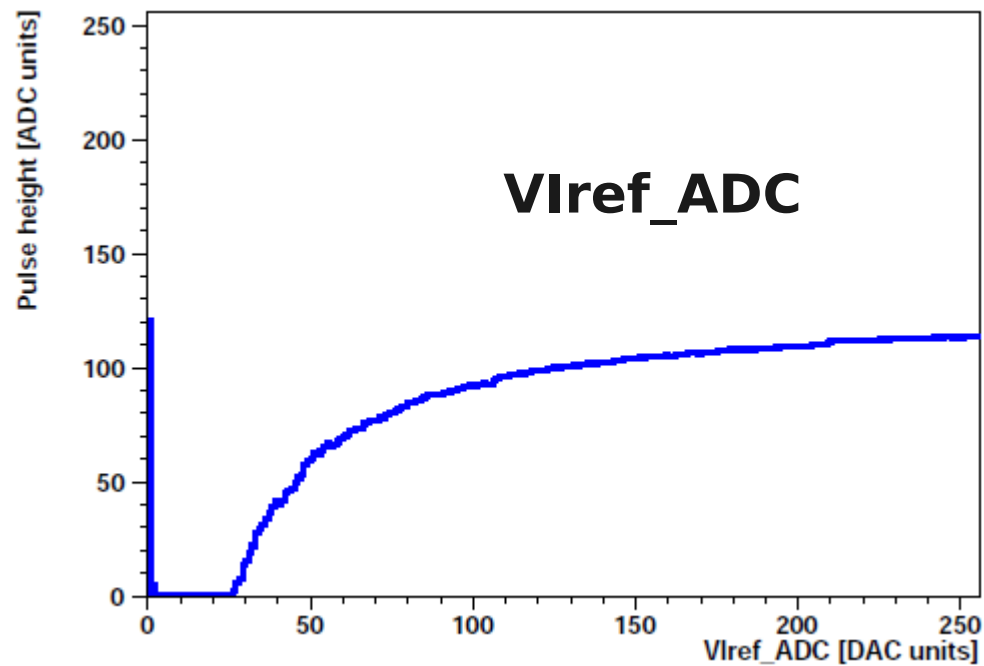
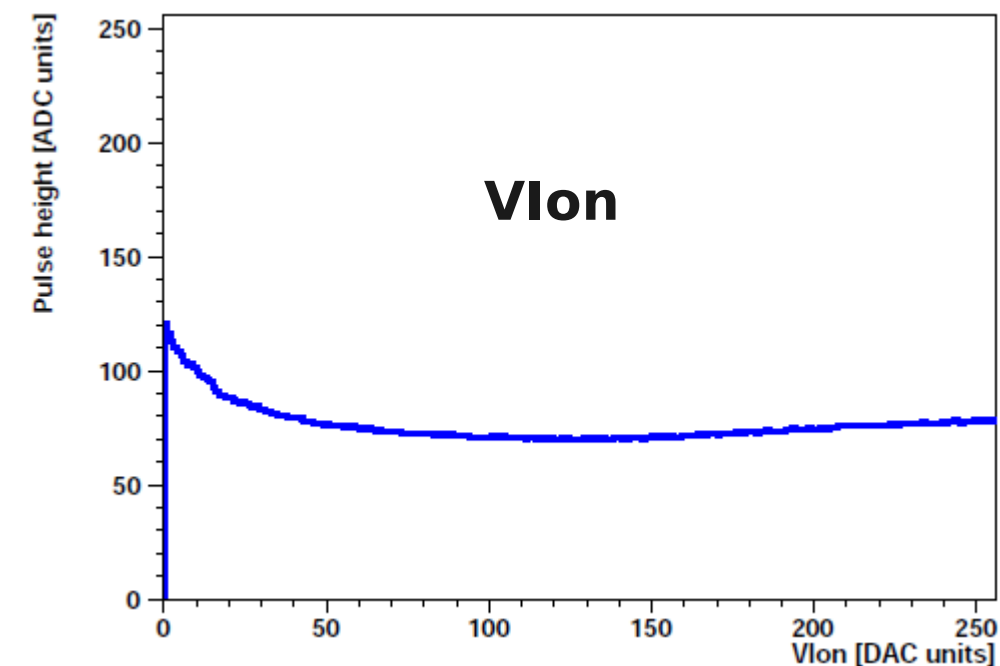
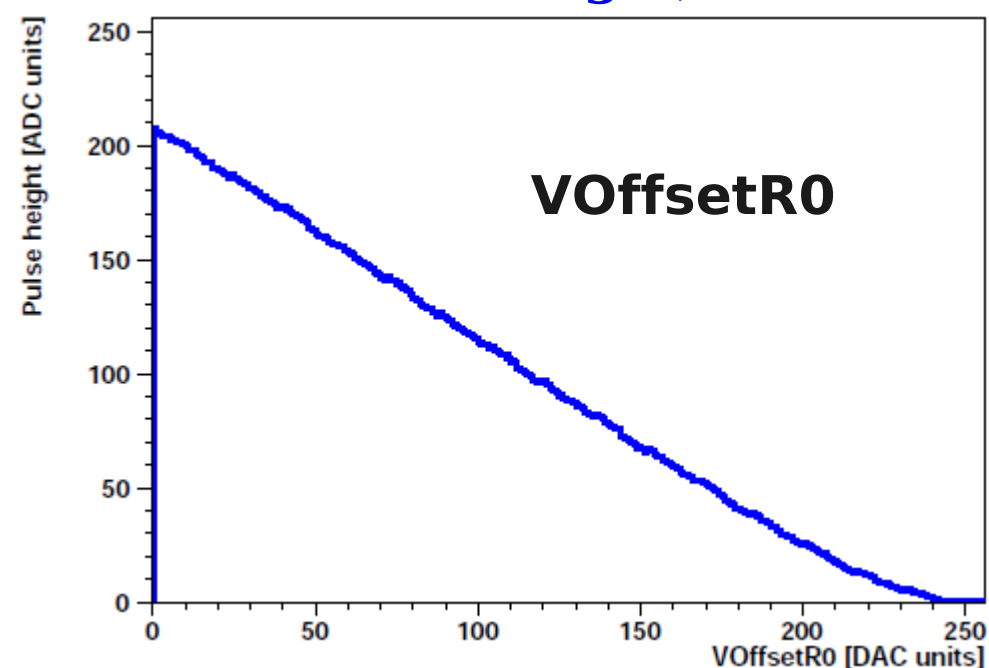
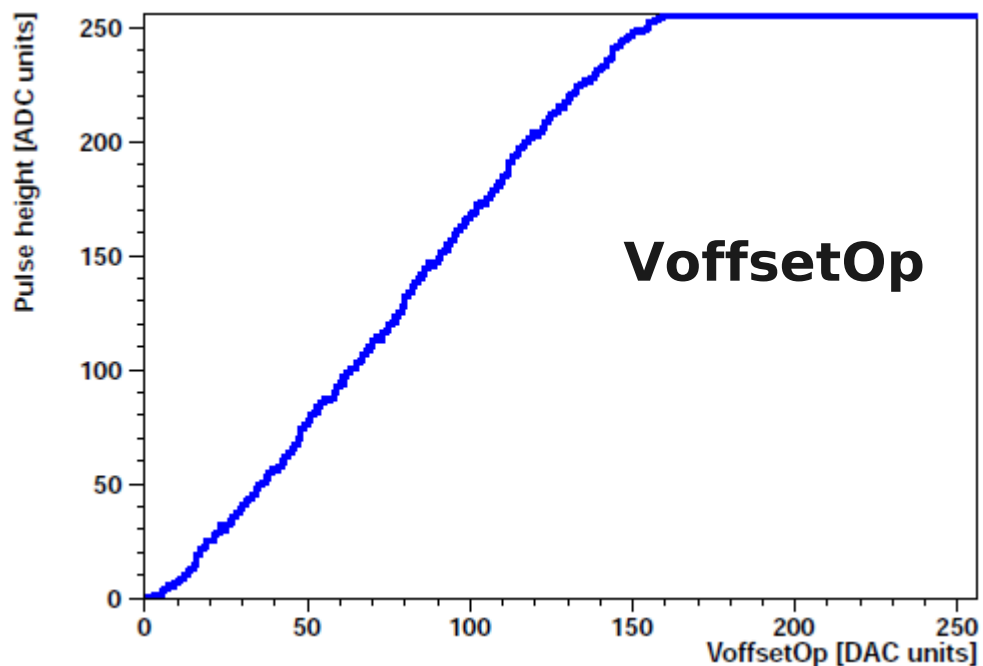
**large pulse:
CtrlReg 4, Vcal 255**



pix 3-3

DAC dependencies

**small pulse:
CtrlReg 0, Vcal 40**



Tuned psi46dig DAC parameters

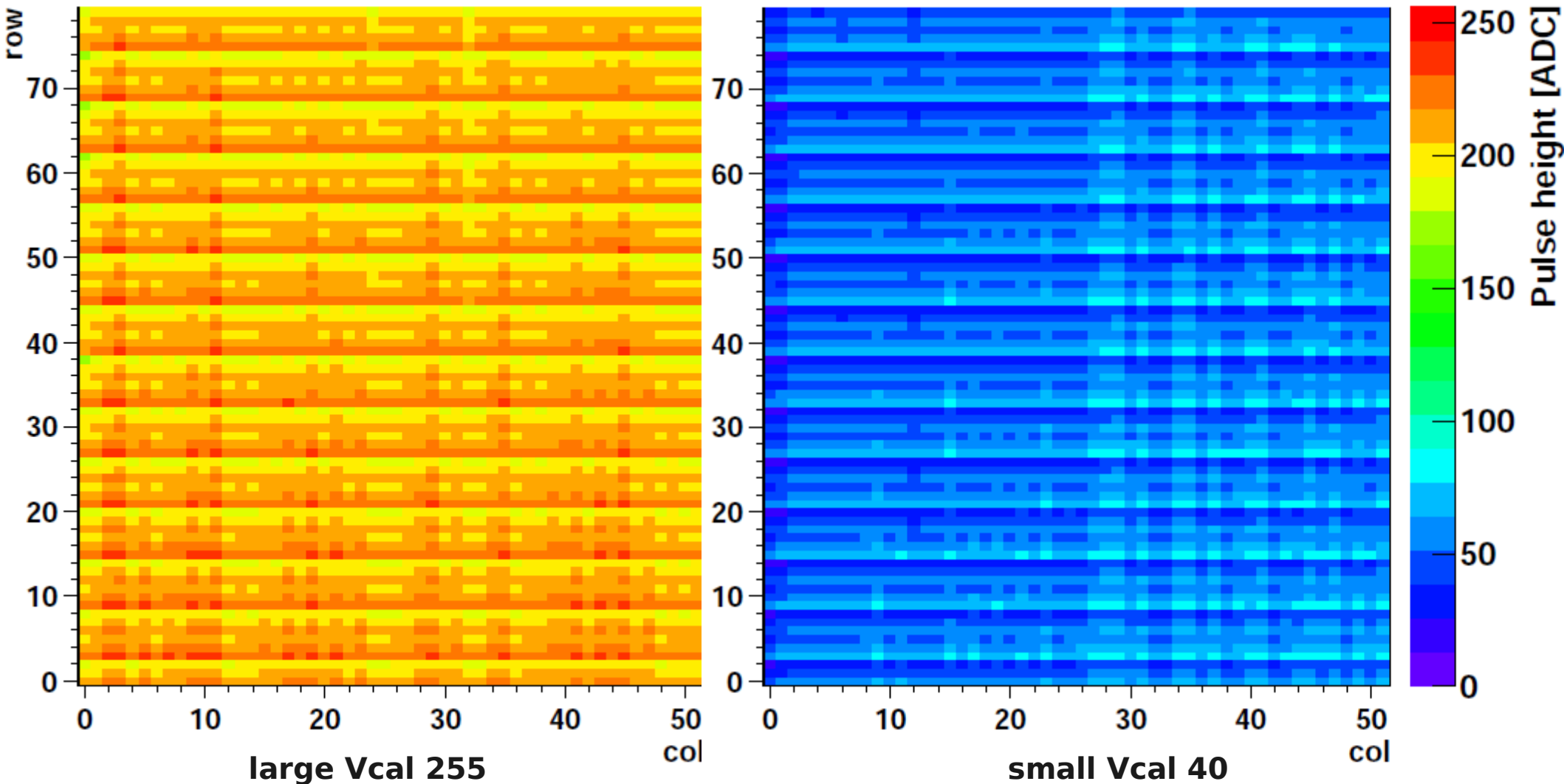
Ia 30 mA, threshold Vcal 30 DAC

1	Vdig	6	13	VIBias_Bus	20
2	Vana	127	14	Vbias_sf	14
3	Vsf	30	15	VoffsetOp	50
4	Vcomp	12			
			17	VOffsetR0	140
			18	VIon	45
7	VwllPr	60	19	Vcomp_ADC	100
			20	VIref_ADC	70
9	VwllSh	60			
10	VhldDel	252	22	VICol0r	100
11	Vtrim	106	25	Vcal	200
12	VthrComp	96	26	CalDel	158
			253	CtrlReg	0
			254	WBC	100

Pulse height range maps after tuning

largest pulse: 243 ADC

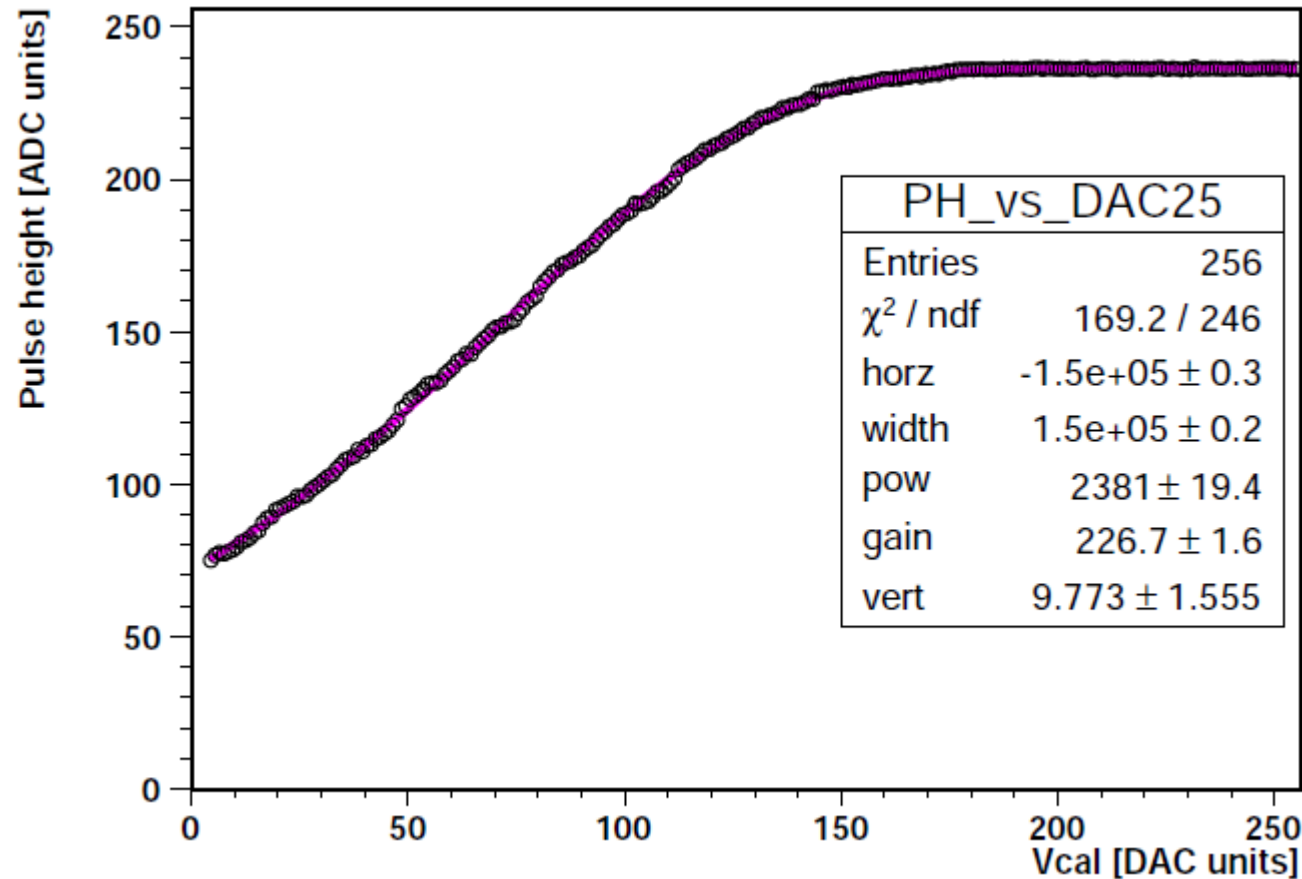
smallest pulse: 20 ADC



Need to find compromise across 4160 pixels

So far done interactively. Need to code algorithm...

Gain calibration

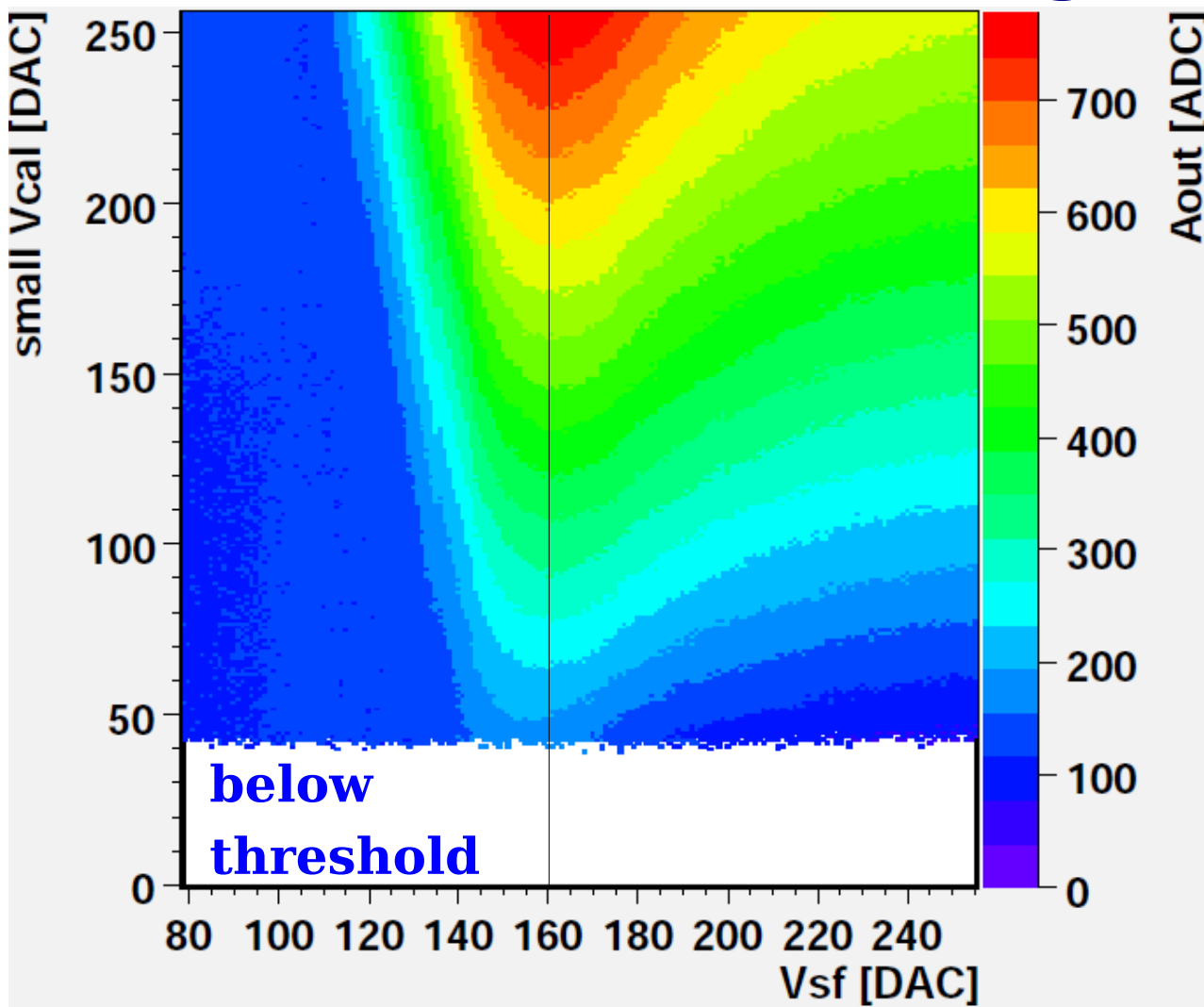


- Pulse height vs large Vcal
- (tanh does not give good fit)
- Fit by Weibull function:
 - good fit from threshold to saturation
 - 5 parameters

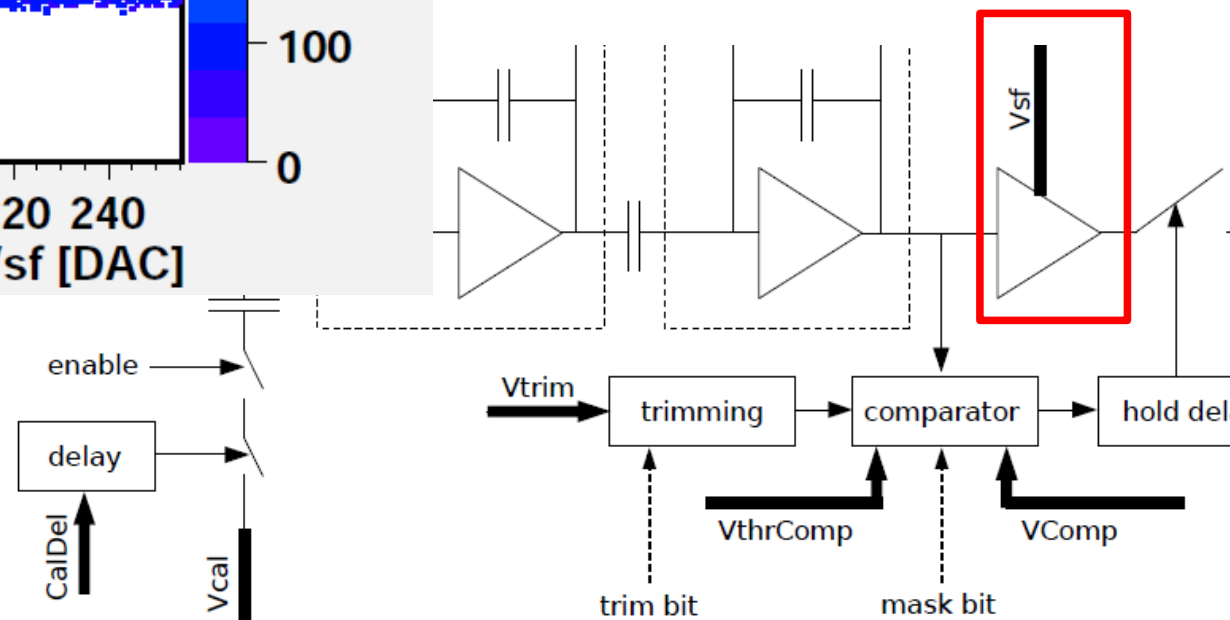
Weibull:
$$PH = p_4 + p_3 \left(1 - \exp \left(- \left((V - p_0) / p_1 \right)^{p_2} \right) \right)$$

inverse:
$$V = p_1 \left(-\ln \left(1 - (PH - p_4) / p_3 \right) \right)^{1/p_2} + p_0$$

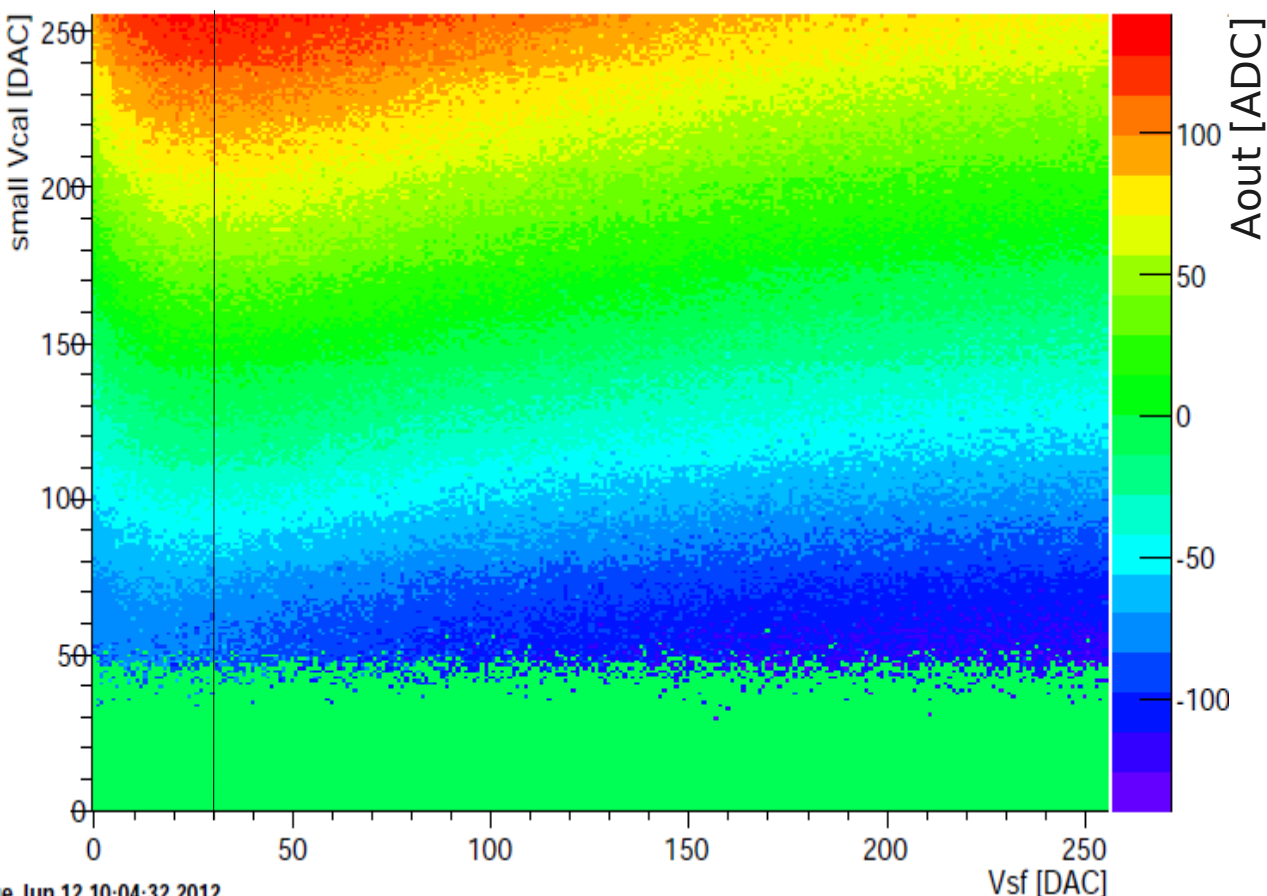
Remember: linear range vs Vsf on psi46v2



- psi46v2, one pixel
- Analog pulse height vs calibrate amplitude and source follower voltage.
- **Best linearity in valley.**

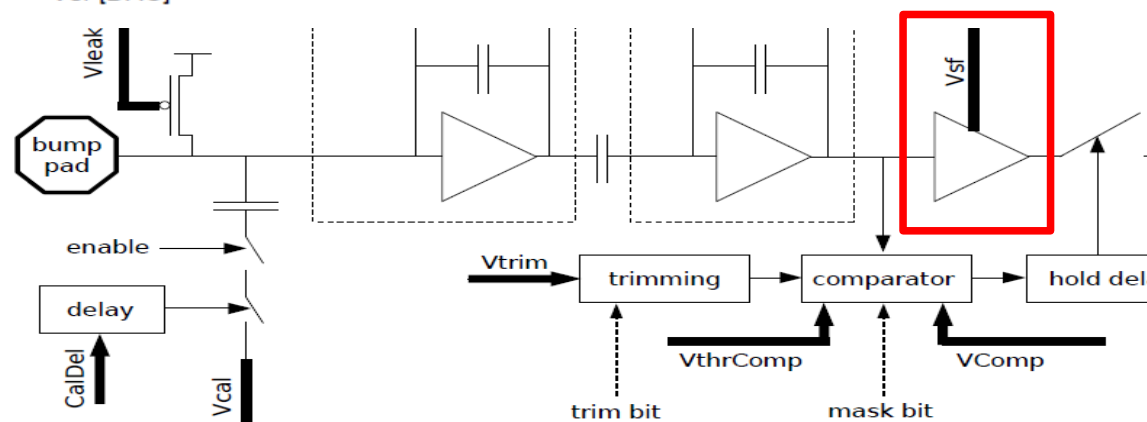


Linear range vs Vsf on psi46xdb

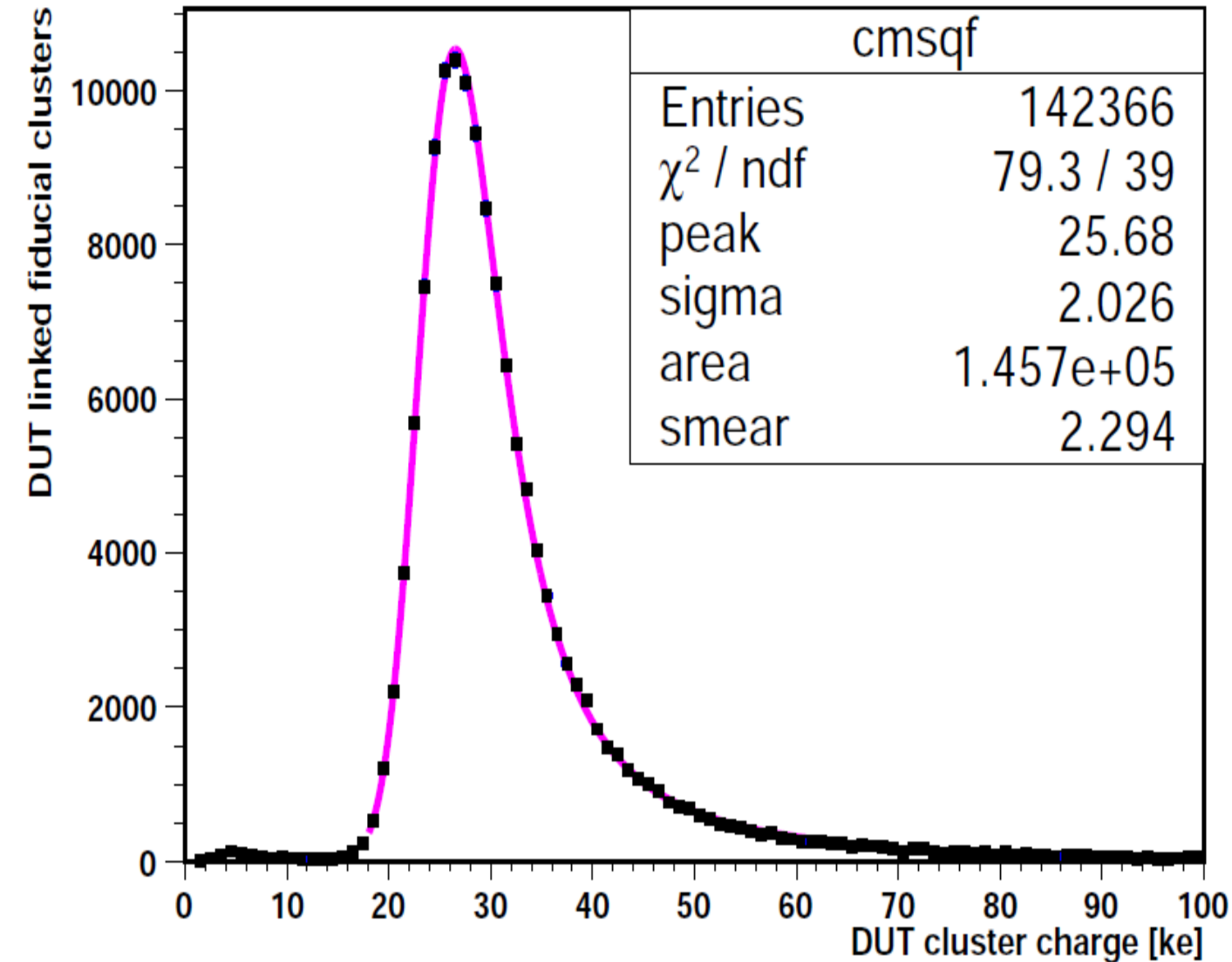


- One pixel
- Analog pulse height vs calibrate amplitude and sample hold voltage.
- Dependence is weaker
- Optimal Vsf is now around 30 DAC

Would be good to have support for the digital ROC on the test board FPGA...

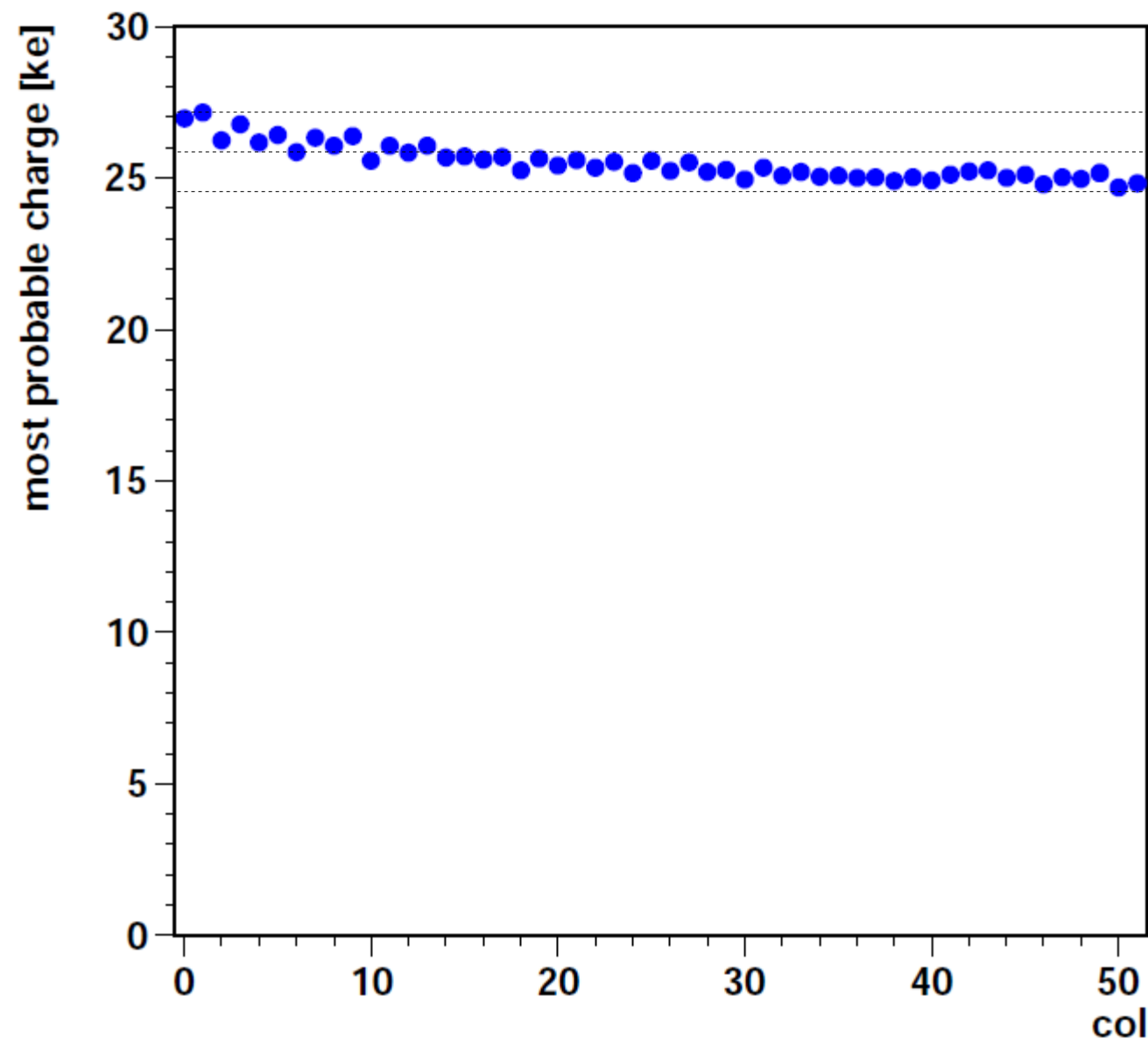


Landau distribution from digital ROC



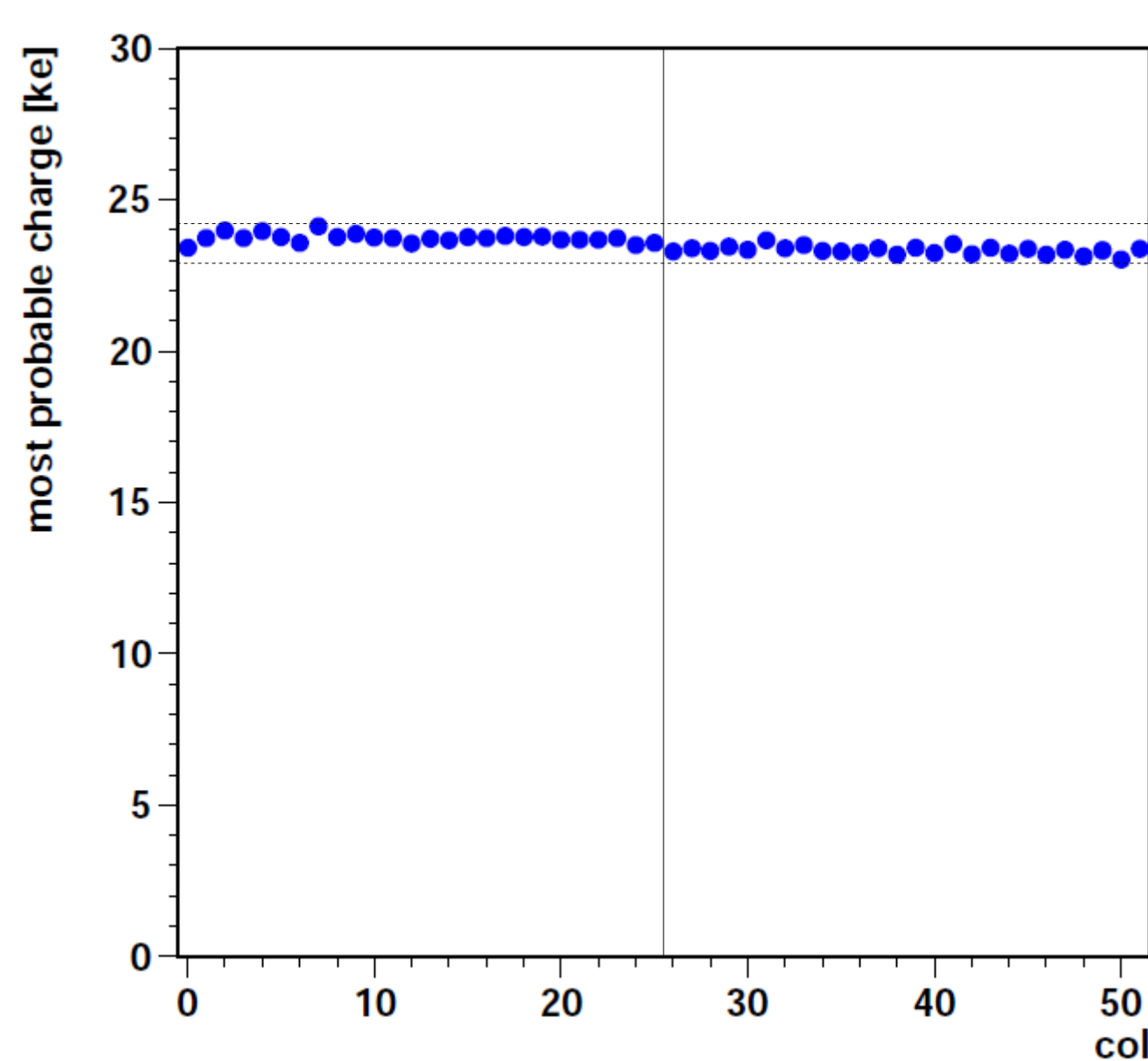
- digital chip 202
- run 4692:
 - bias -150V
 - threshold 2 ke
 - tilt 19°
- Weibull gain calibration applied
- Cluster charge distribution fit by Landau $\otimes$ Gauss
 - peak position adjusted, width OK
 - Gaussian smearing needed as usual

Cluster charge profile digital ROC



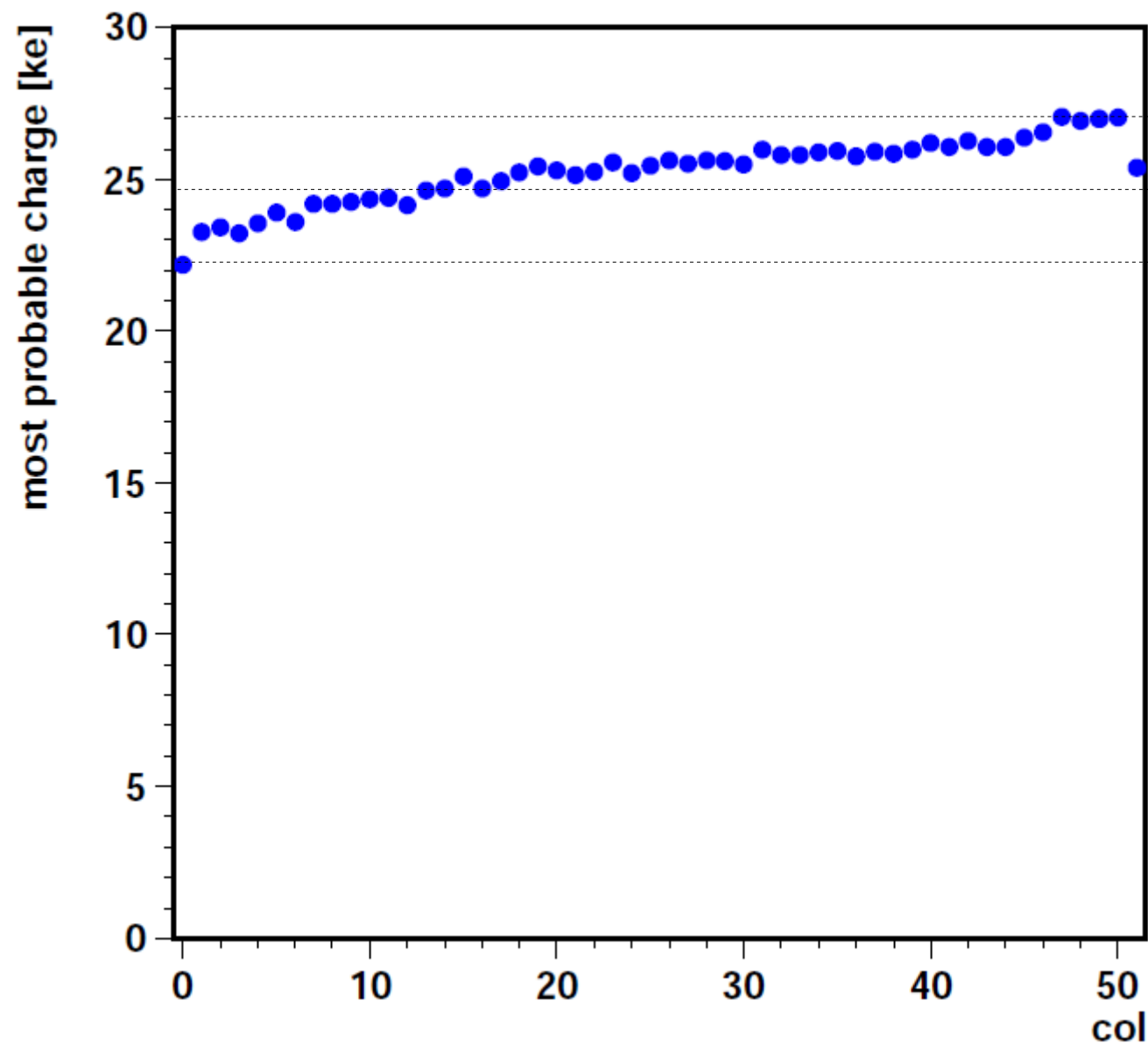
- chip202, 20° tilt
- 5.6 GeV, runs 5164-5180
- Test pulse gain calibration applied (Weibull fit)
- Landau peak per column
- **±4% trend across columns:**
 - better than psi46, worse than xdb?
- Mean value is adjusted to 24 ke for e⁺ in 285 μm Si
 - 350 e / large Vcal DAC
 - 50 e / small Vcal DAC

Cluster charge profile with psi46xdb



- xdb2, 0° tilt
- 4.8 GeV, runs 3903-3947
- Test pulse gain calibration applied (Weibull fit)
- Landau peak per column
- **Flat within $\pm 2\%$**
 - small difference between left and right half?
- Mean value is adjusted to 24 ke for e^+ in 285 μm Si
 - 350 e / large Vcal DAC
 - 50 e / small Vcal DAC

Cluster charge profile with psi46



- 4 GeV e^-
- chip 10, 20° tilt
- Test pulse gain calibration applied (tanh fit)
- Landau peak position per column
- **Observe $\pm 8\%$ gain variation across the chip**

Summary

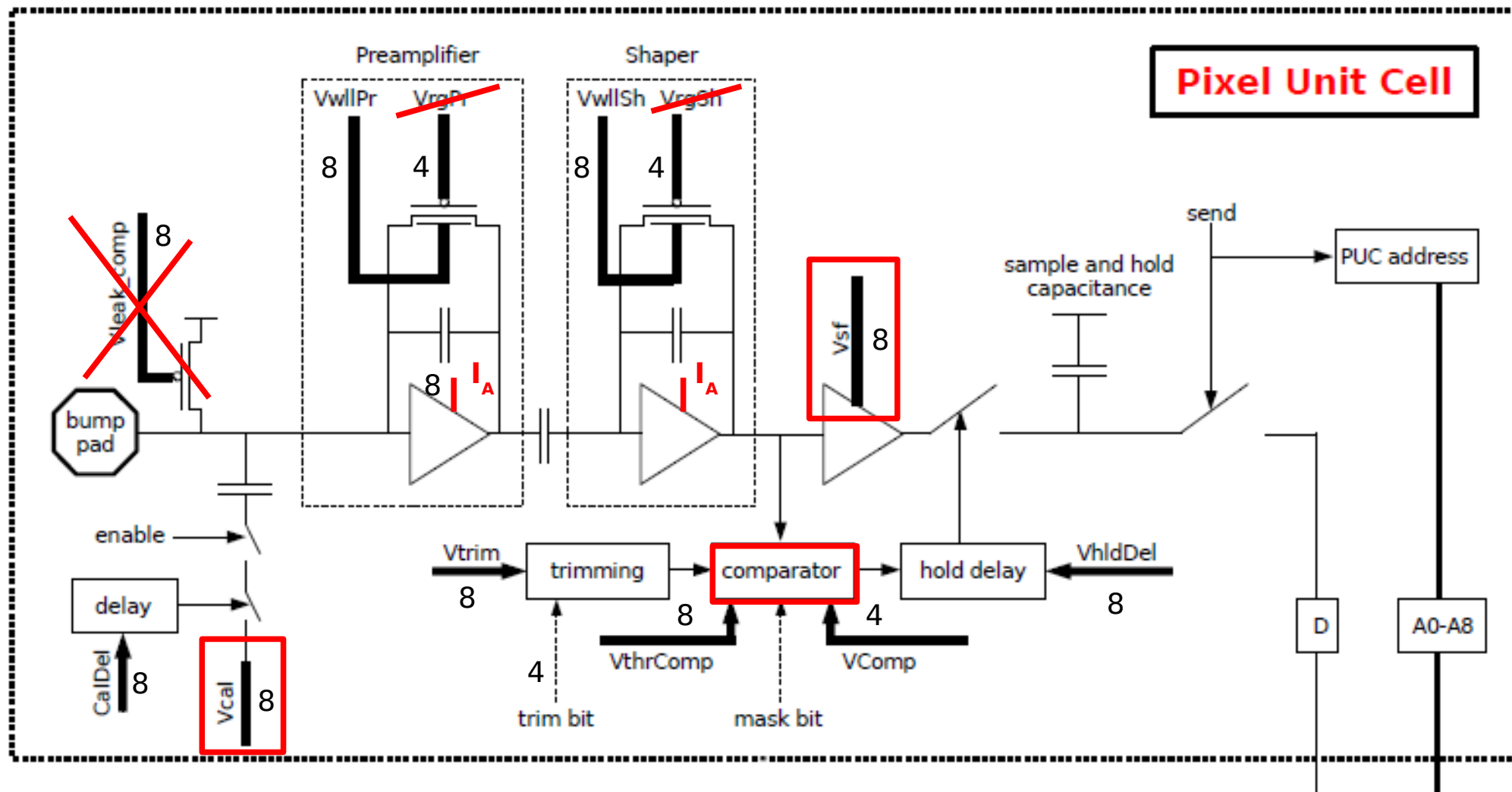
- The ADC on the psi46dig chip has limited analog input range:
 - the analog gain in the ROC must be adjusted
 - the full range should be exploited to avoid digitization noise
- DACs available:
 - VIon and Viref_ADC for gain
 - VoffsetOp and VOffsetR0 for offset
- Heuristic, interactive algorithm developed
 - code to be written...
- Gain calibration done with Weibull function instead of tanh
 - good fit from threshold to saturation
- Applied successfully in DESY beam test

Backup plots

Configuration at DESY

- New digital ROC with sensor and new adapter (arrived 9.8.2012)
- old PSI46 test board, with new FPGA firmware (binary file from Beat Meier downloaded using ALTERA USB Blaster via JTAG connector)
- run in 40 MHz mode
- Dell laptop running Scientific Linux 6.1 or Ubuntu 10.10.
- psi46expert software compiled using gcc-4-5-2 in AMD 64 bit.
- libftd2xx.0.4 for USB interface from FTDI:
<http://www.ftdichip.com/Drivers/D2XX.htm>

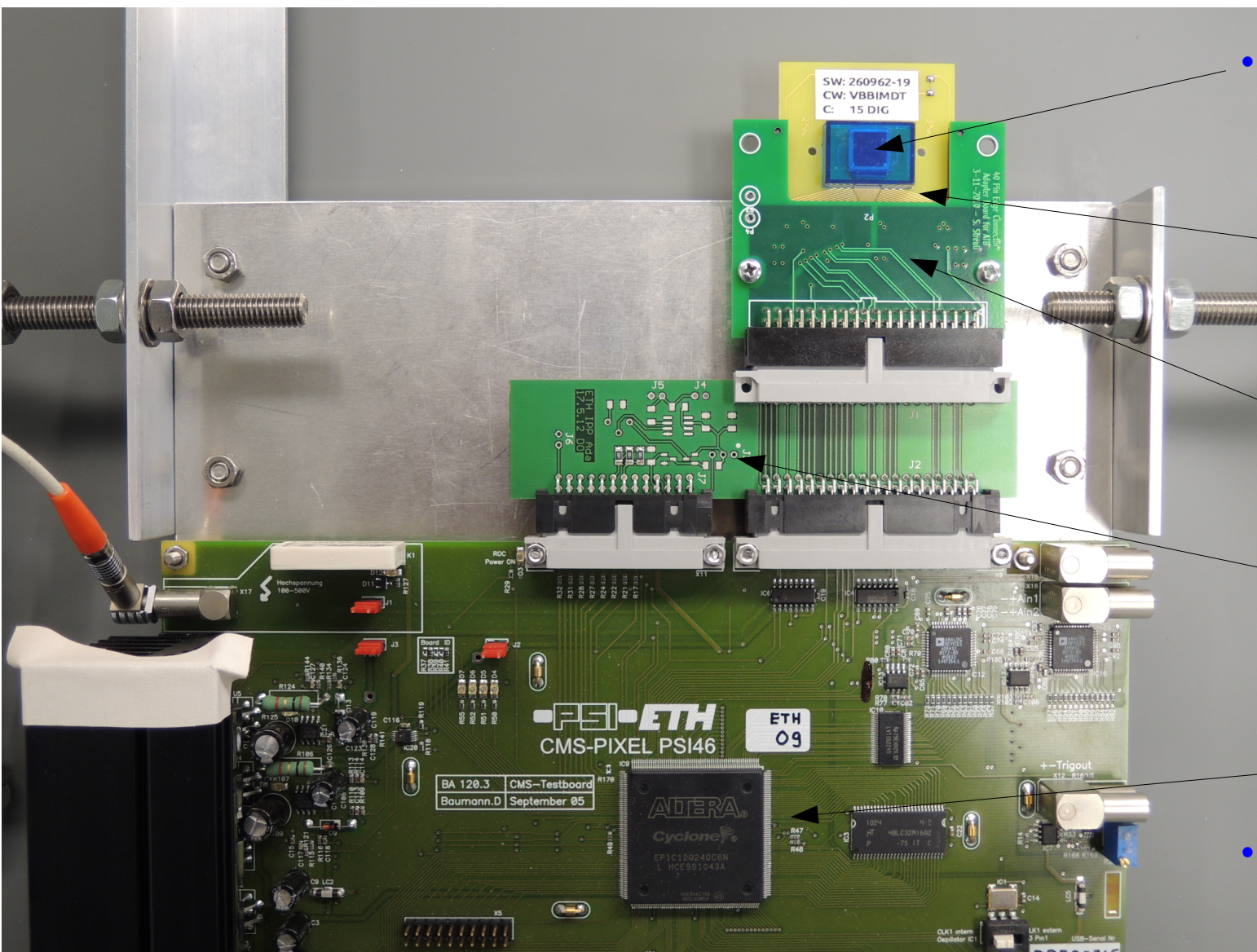
psi46dig pixel unit cell



adjustable by programmable DAC

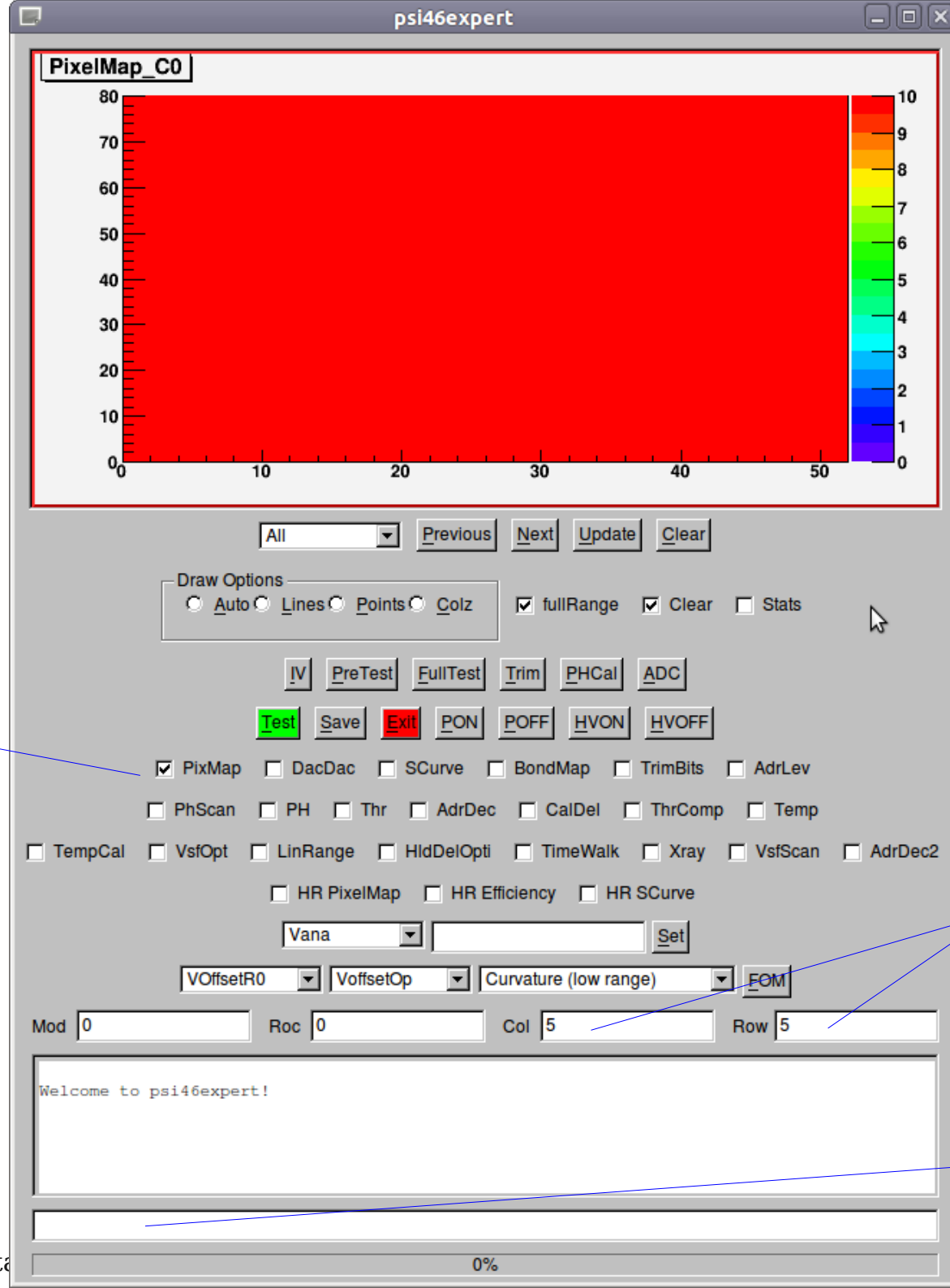
modified in psi46dig

Test setup at DESY



- Single chip module:
 - Indium bump bonded at PSI
 - Glued and wire bonded to carrier printed circuit board
 - Interface card to psi46 TB with edge connector
 - ETH adapter card for digital 160 MHz differential signal directly into FPGA (LCDS into LVDS)
- Small firmware update to select digital path as 'TBM channel 1'

Pixel Alive test



saved in
expert.root

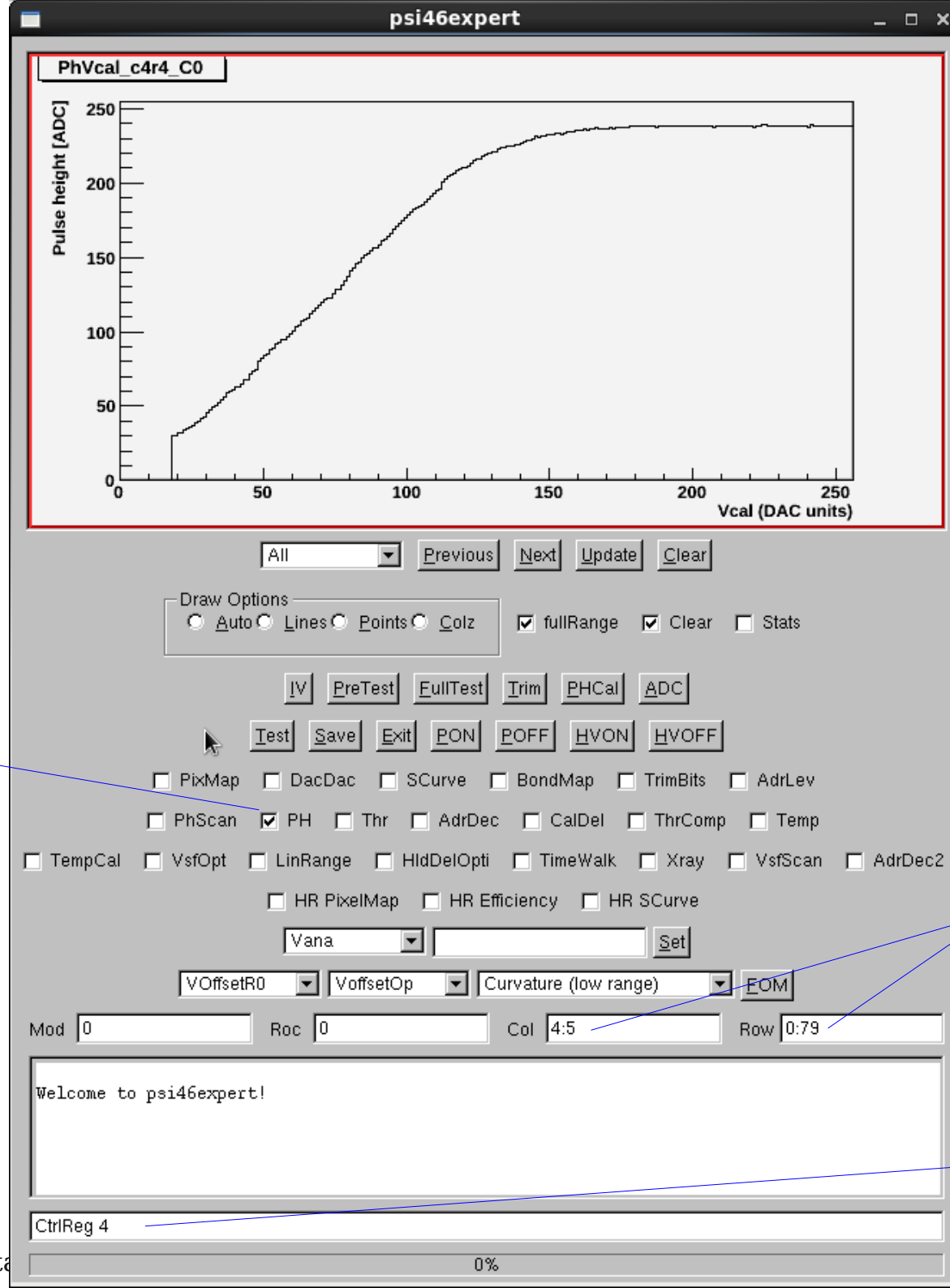
Map of pixels

PixelAlive.cc

define
pixel
range

command line
roc or tb

PH vs Vcal for gain calibration



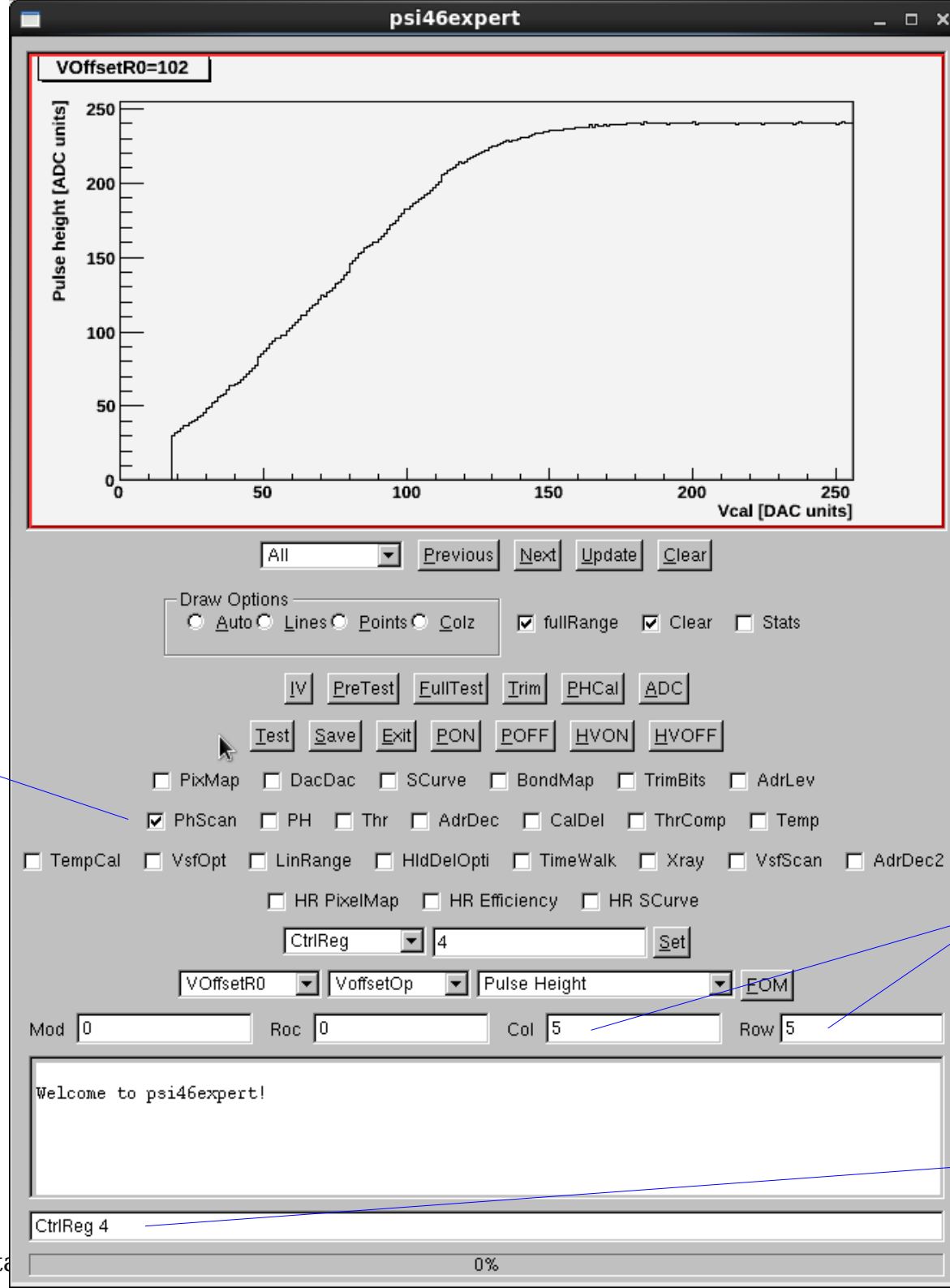
saved in
expert.root

PH vs Vcal
per pixel
PHTest.cc

define
pixel
range

command line
roc or tb

**PH vs Vcal
vs all DACs**



**saved in
expert.root**

**PH vs Vcal
vs all DACs
per pixel**

PhDacOverview.cc

**define
pixel
range**

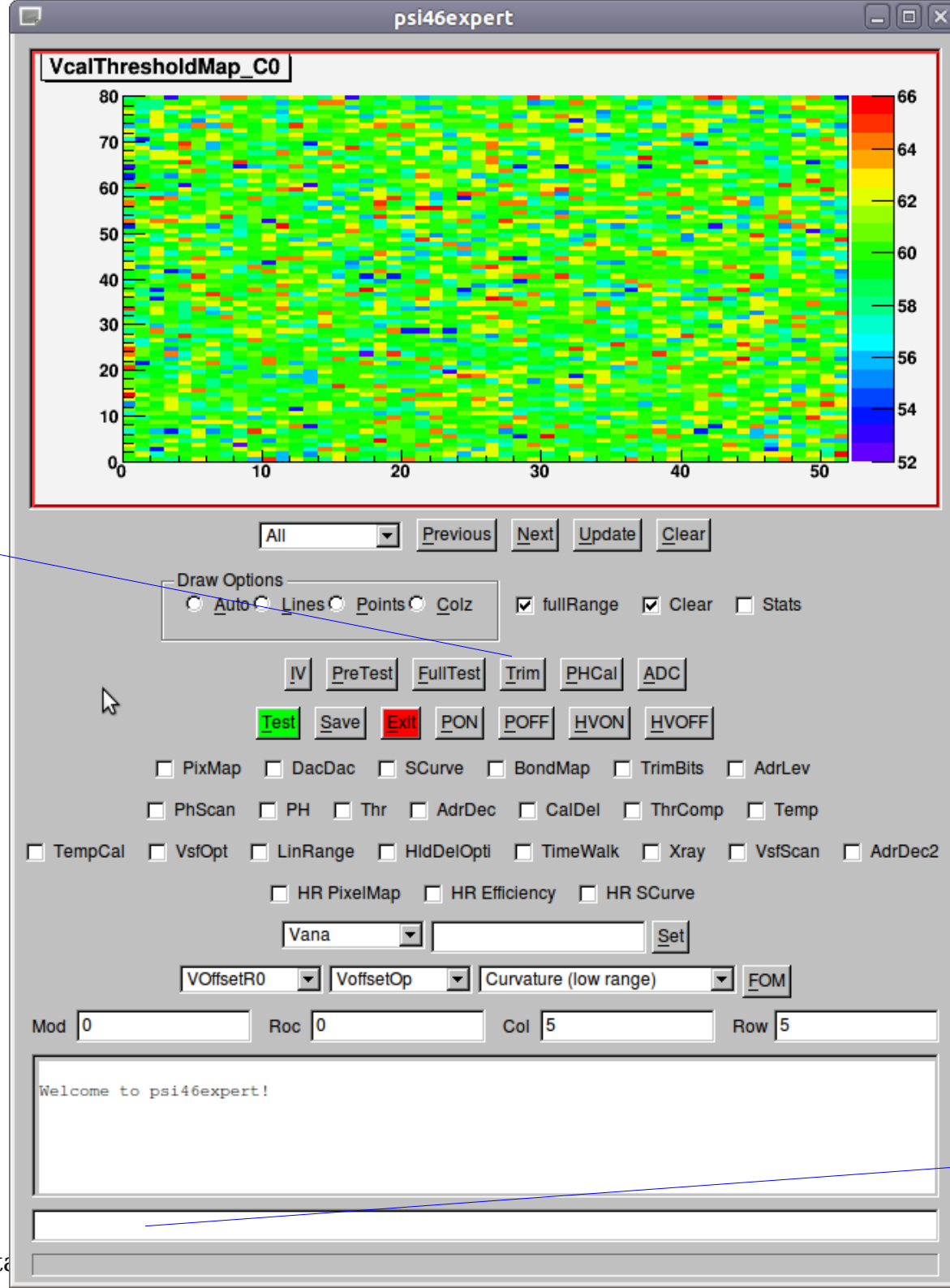
**command line
roc or tb**

**Vcal Thresh.
map after
trimming**

**Trimming
of 4160 pixels**

TrimLow.cc

**saved in
expert.root**

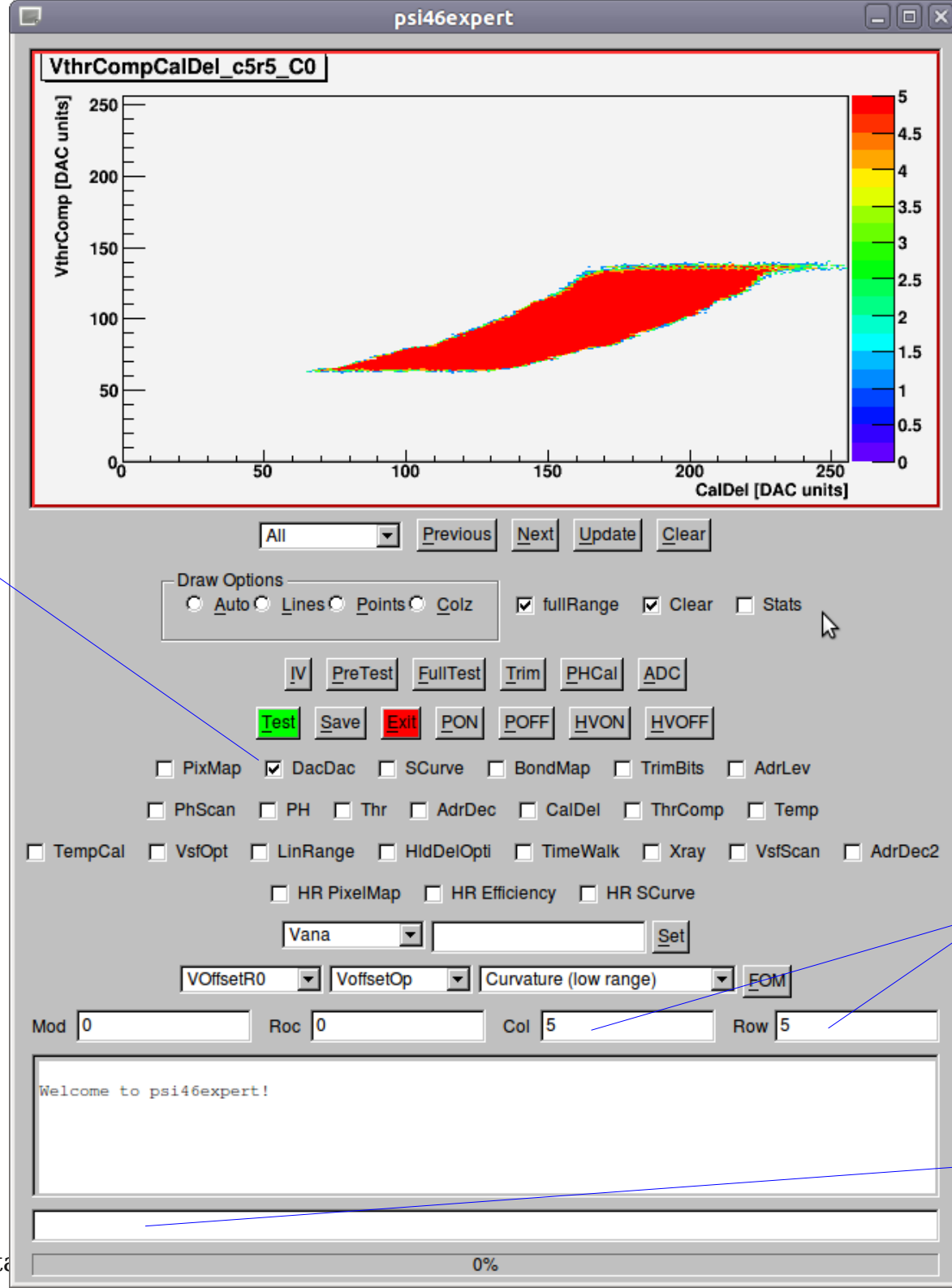


**command line
roc or tb**

VthrComp vs CalDel

DAC correlations

DacDependency.cc

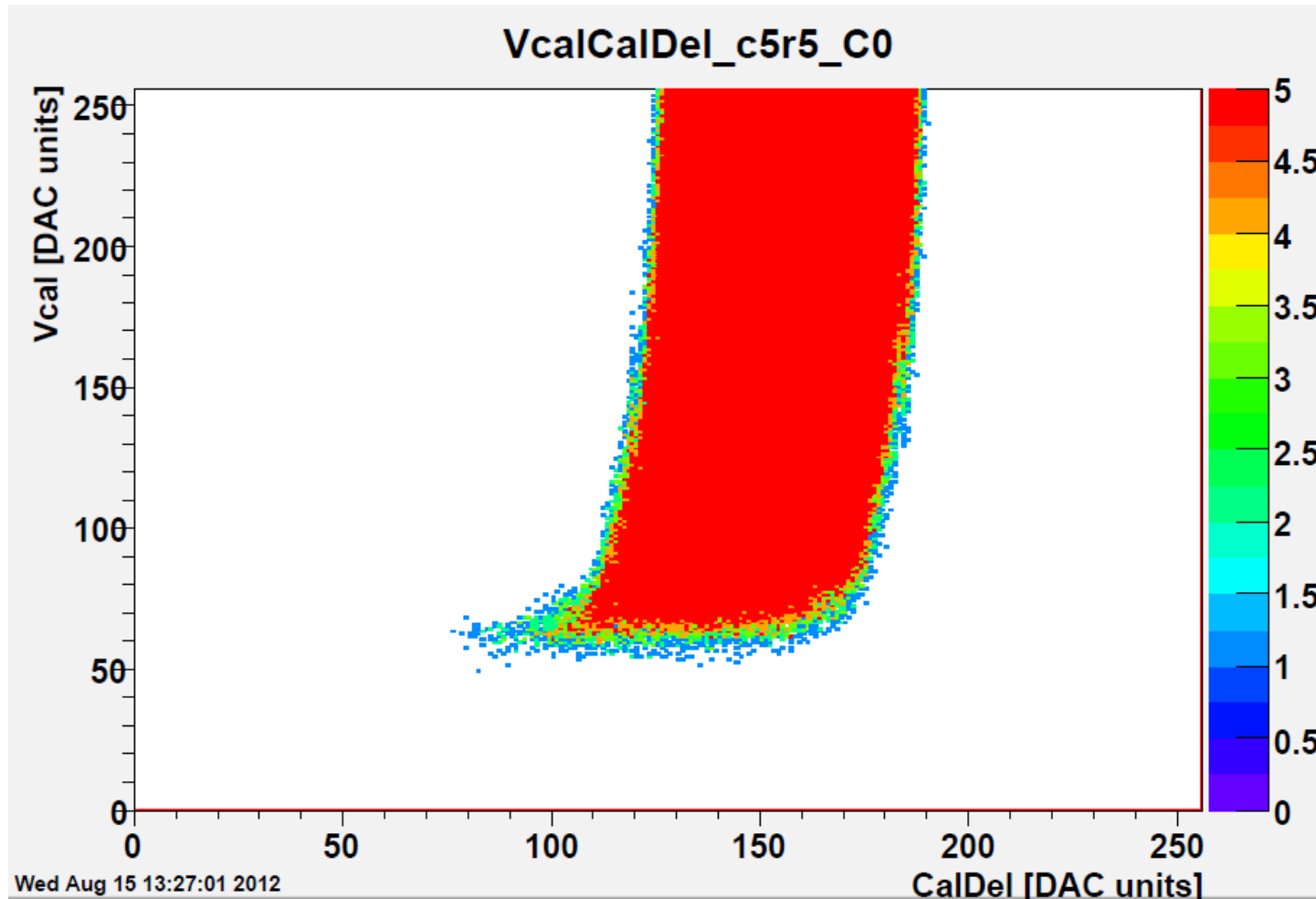


saved in
expert.root

define
pixel
range

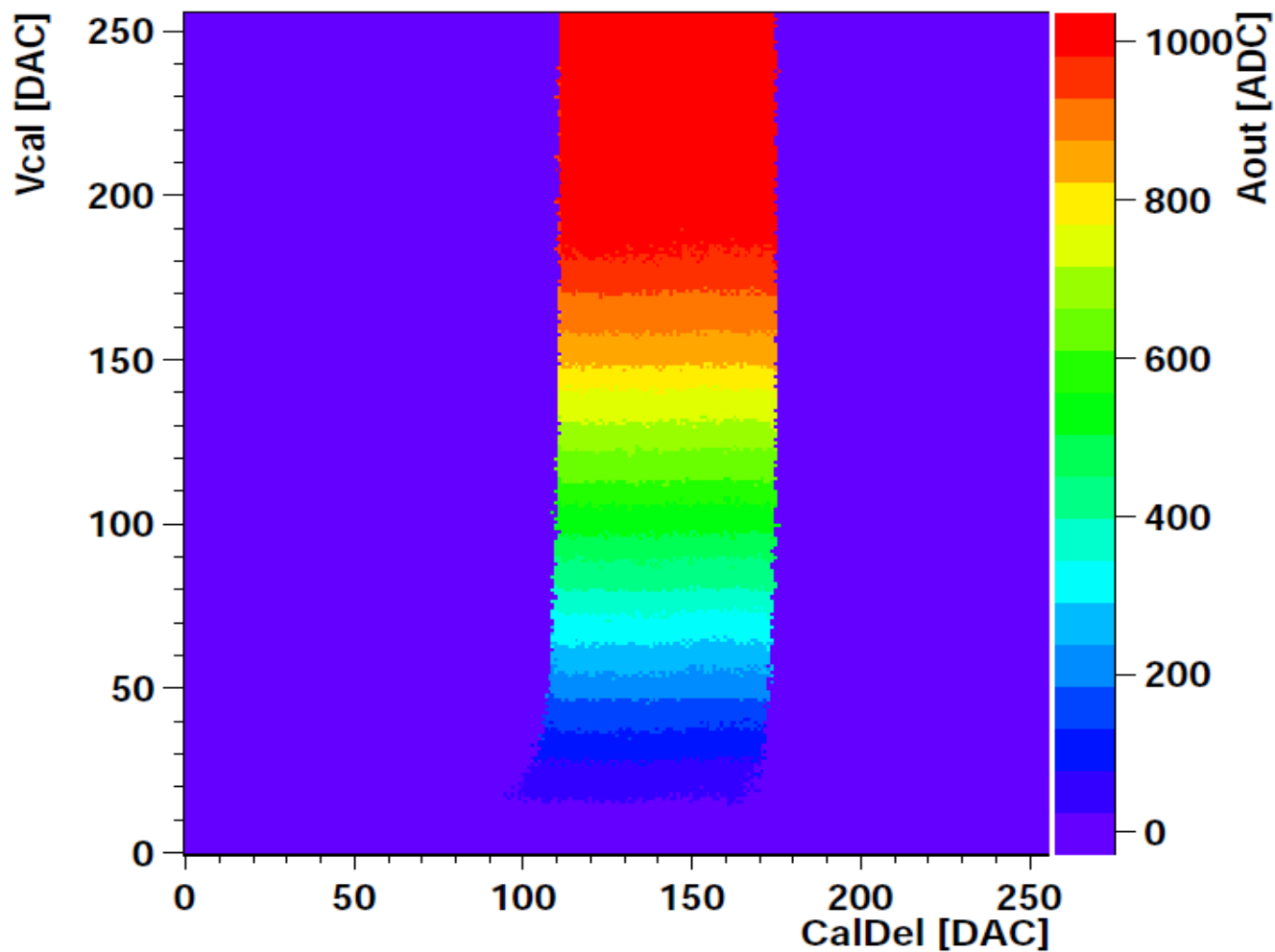
command line
roc or tb

Vcal vs CalDel digi



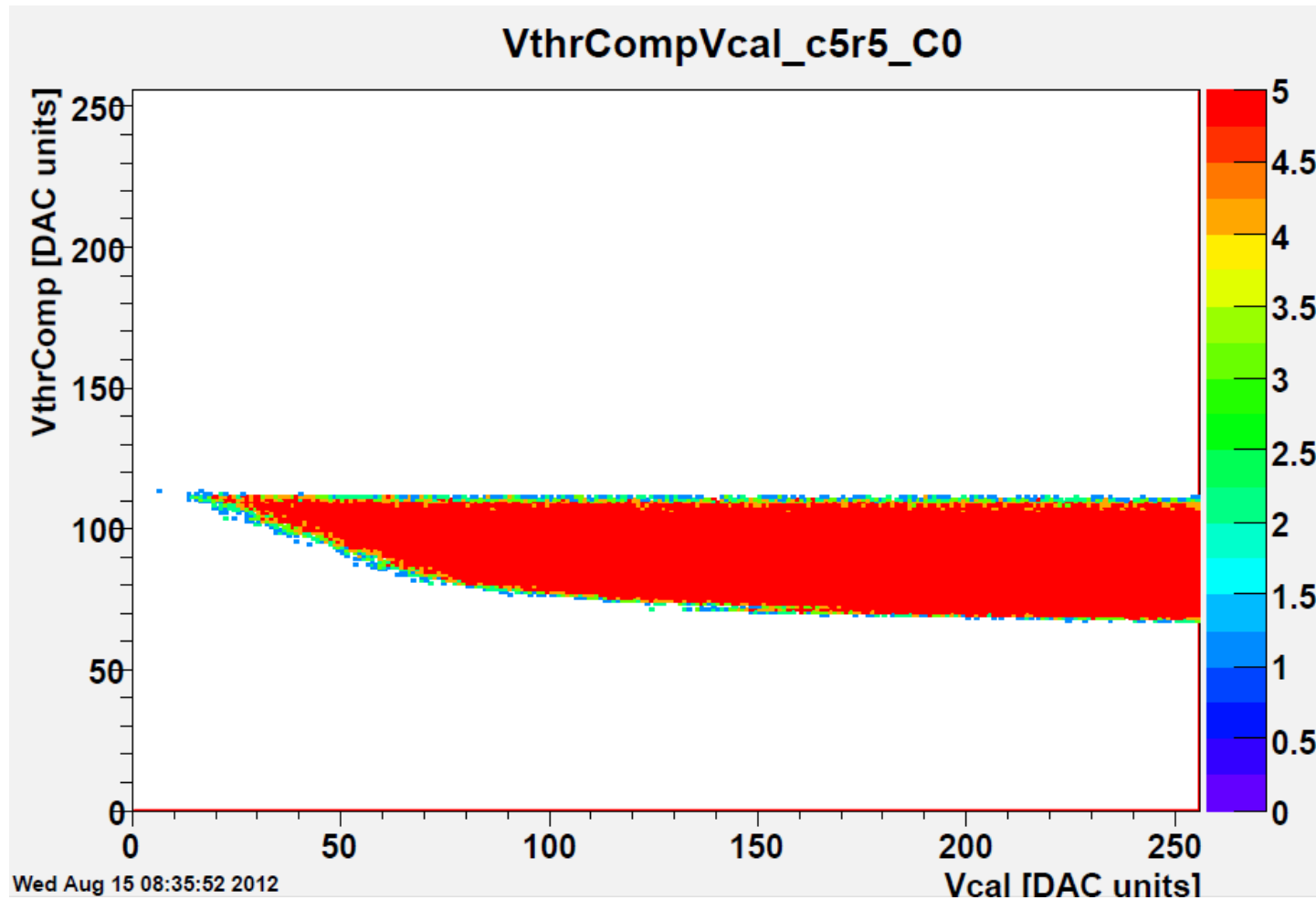
Trimmed, target Vcal = 60

Vcal vs CalDel xdb



Smaller time walk?

VthrComp vs Vcal



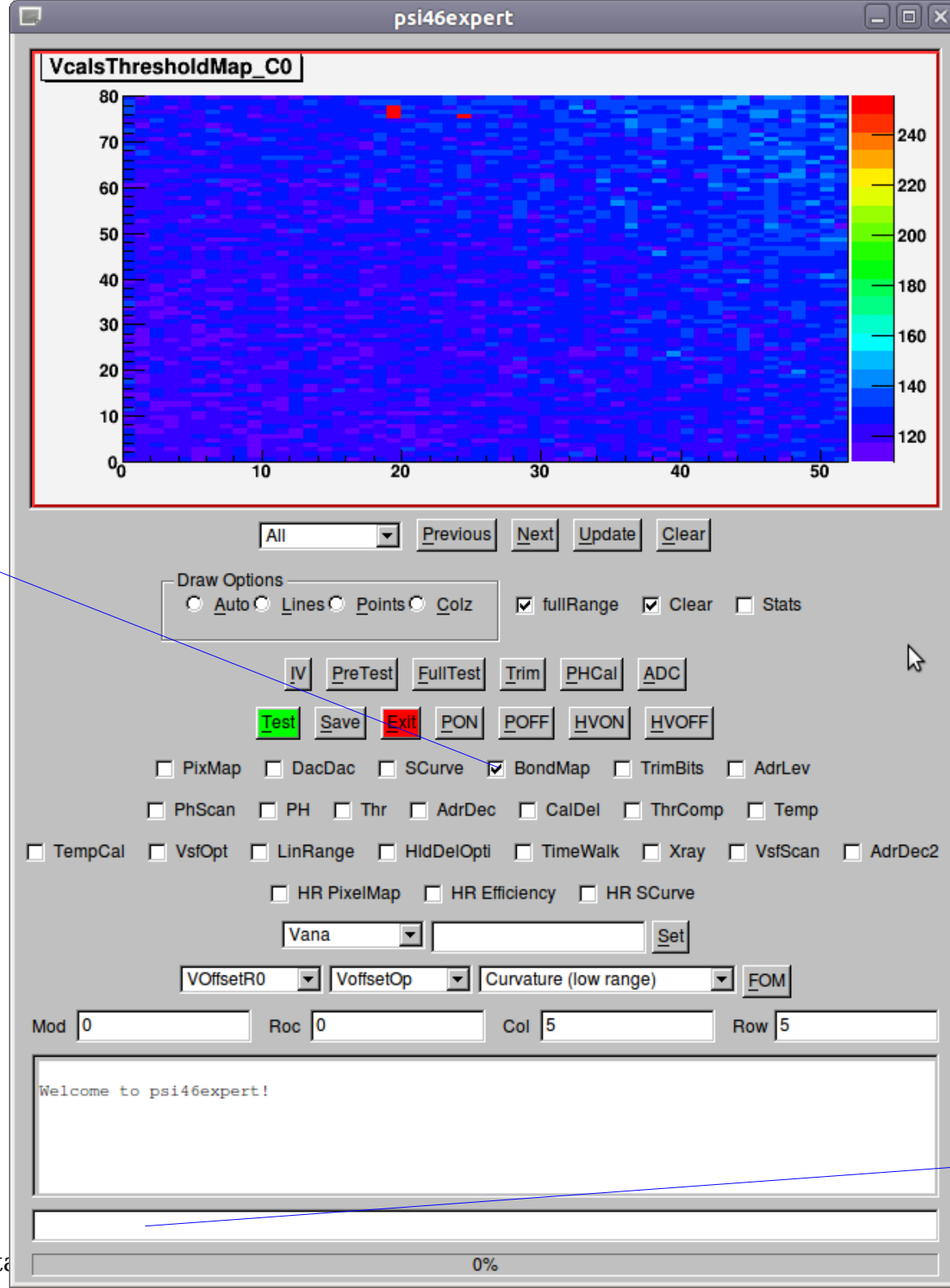
Trimmed, target Vcal = 60

Bump bonding check

Test 4160
bump bonds

BumpBonding.cc

saved in
expert.root



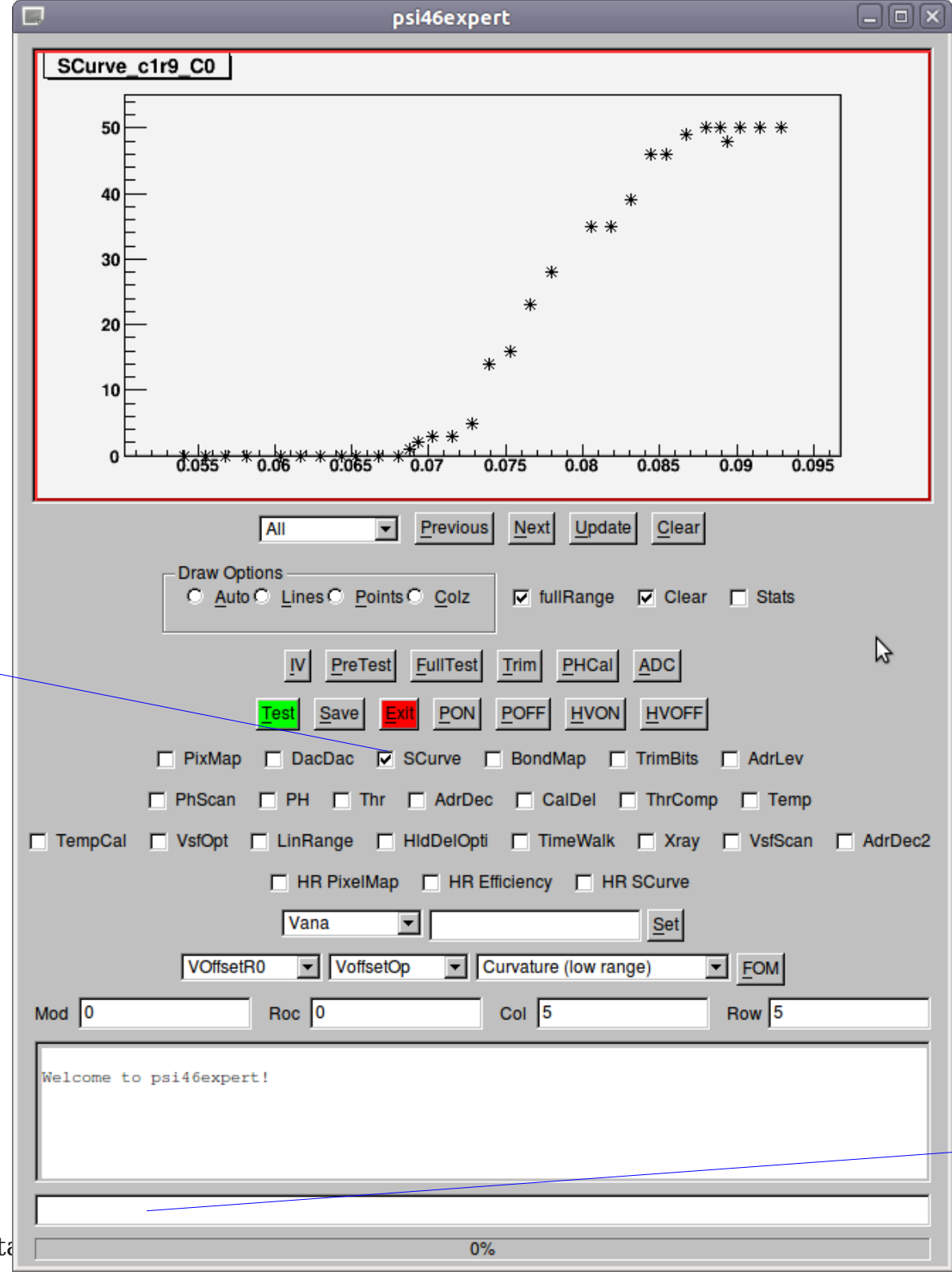
command line
roc or tb

**Threshold
curves: number
of readouts
vs calibration V**

**Count valid
readouts for
each pixel**

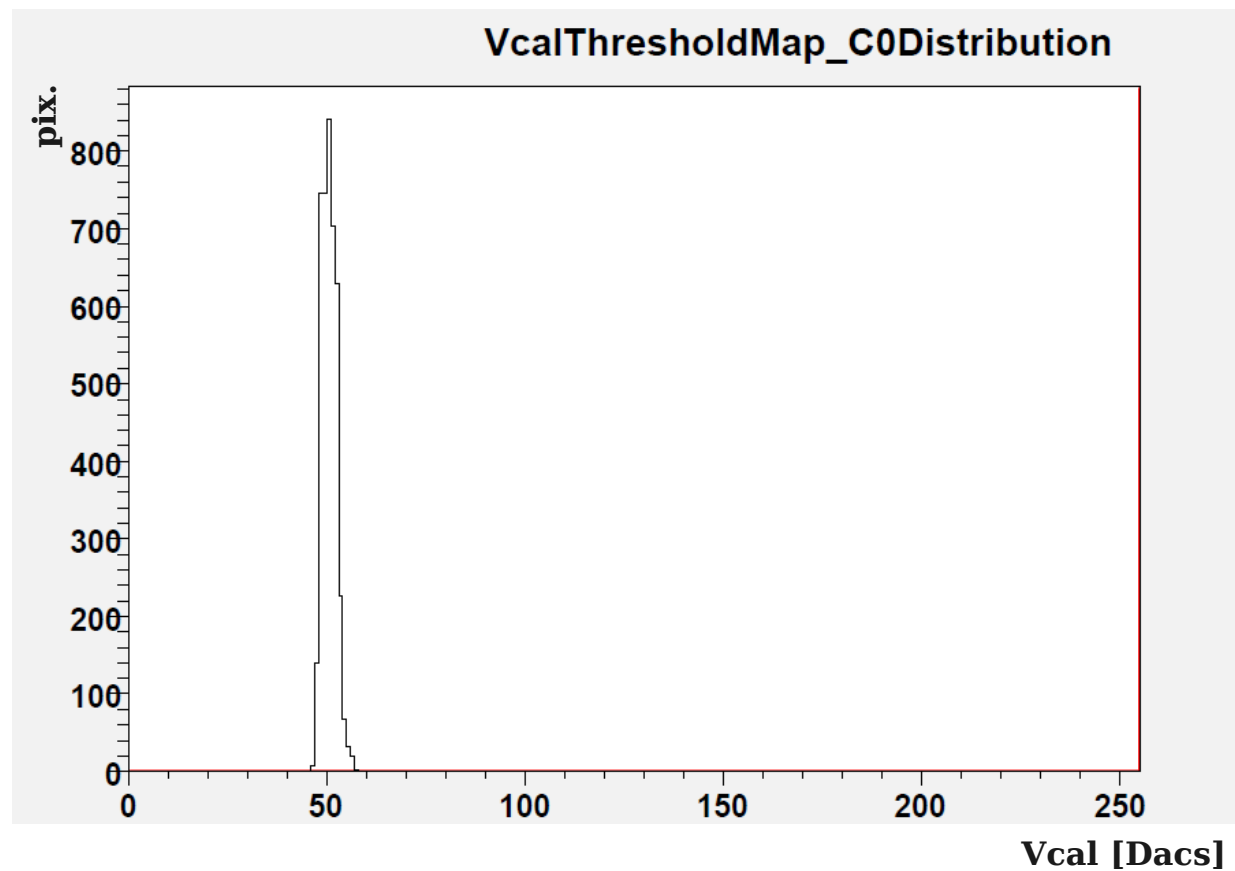
SCurveTest.cc

**saved in
expert.root**



**command line
roc or tb**

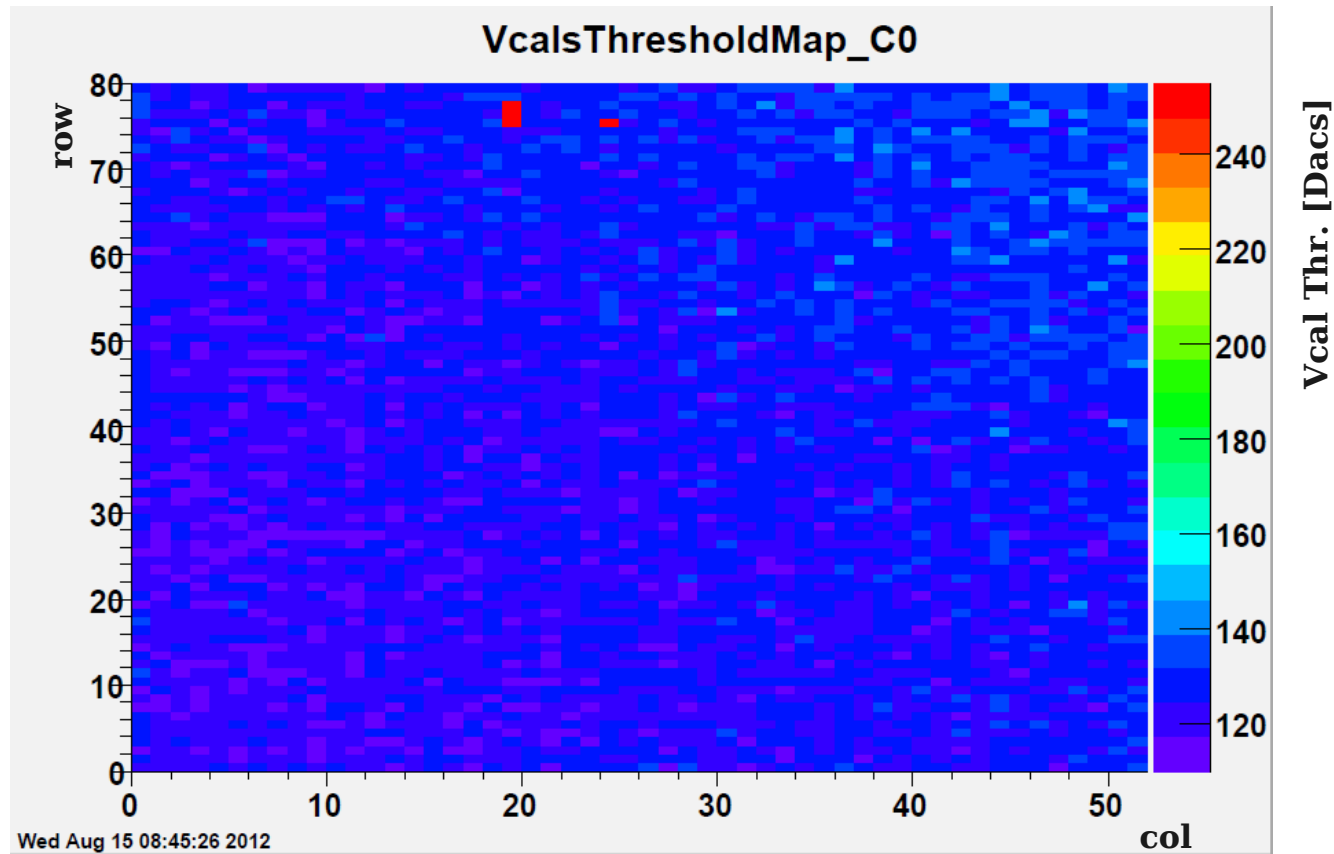
Vcal Thresholds



Target Vcal = 50 for trimming

Bump bonding test

digital
chip 202



ETH procedure used:

The calibration signal injected to a pad on the ROC surface.

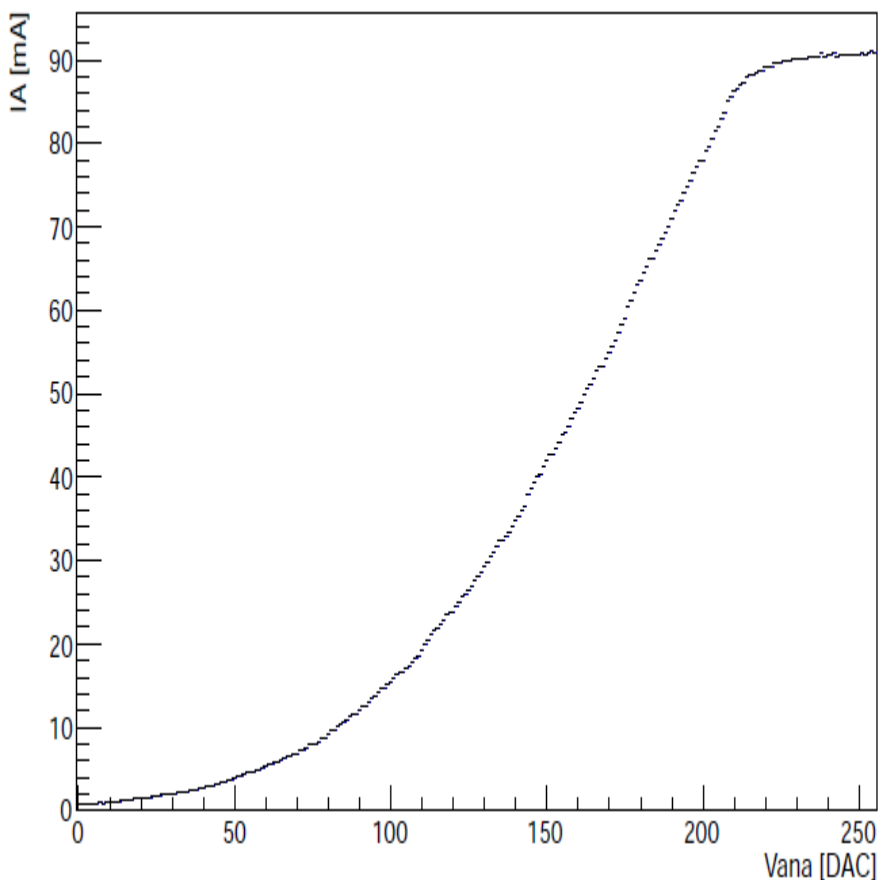
It induces a charge in the sensor, which mimics a hit.

Hit is detected if bump bond is present.

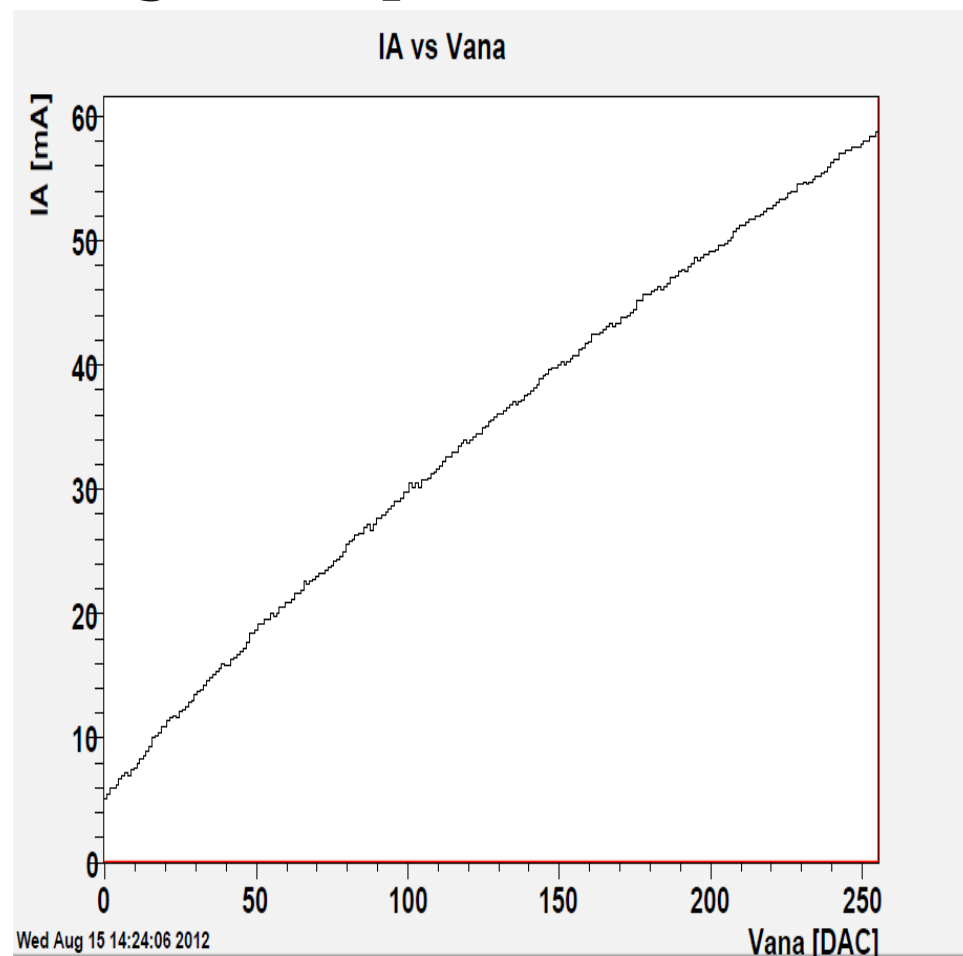
Vcal - thresholds are measured in the high Vcal range.

Power: Ia vs Vana

**psi46
chip 5**



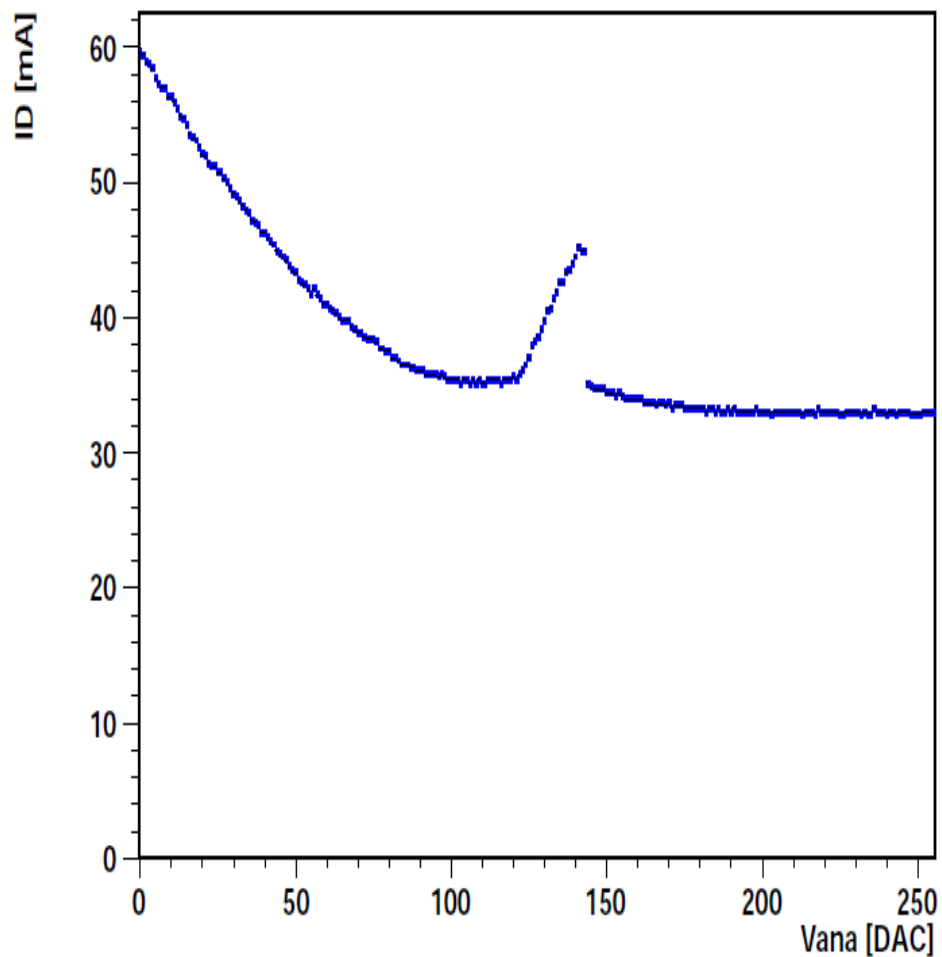
digital chip 202



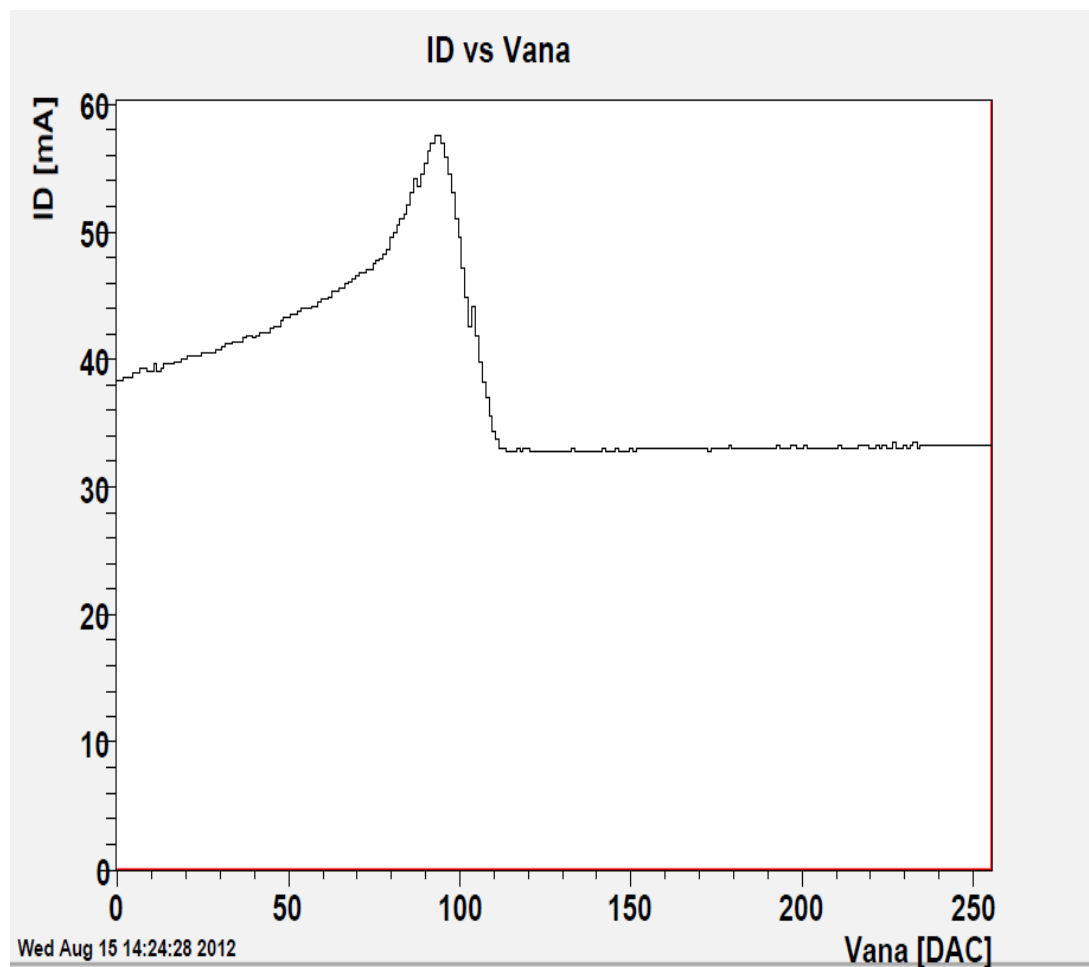
IA is almost linear (and smaller range)

ID vs Vana

**psi46
chip 5**



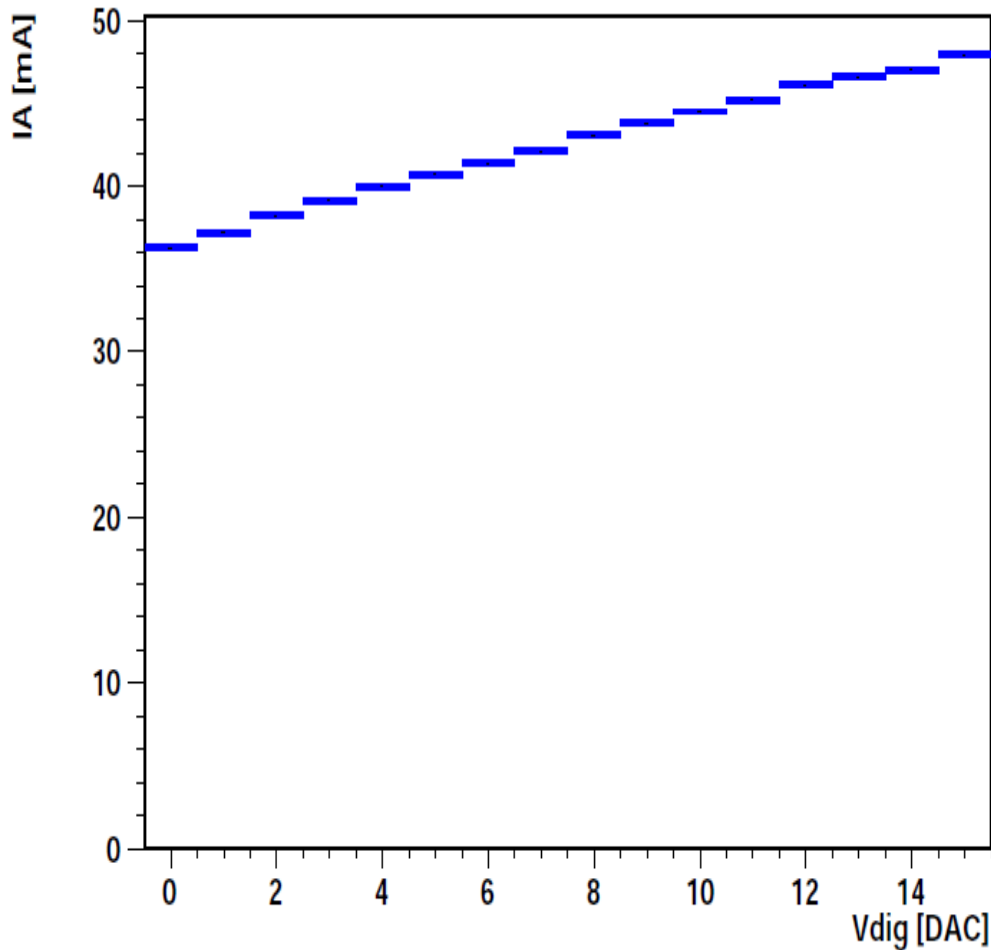
digital chip 202



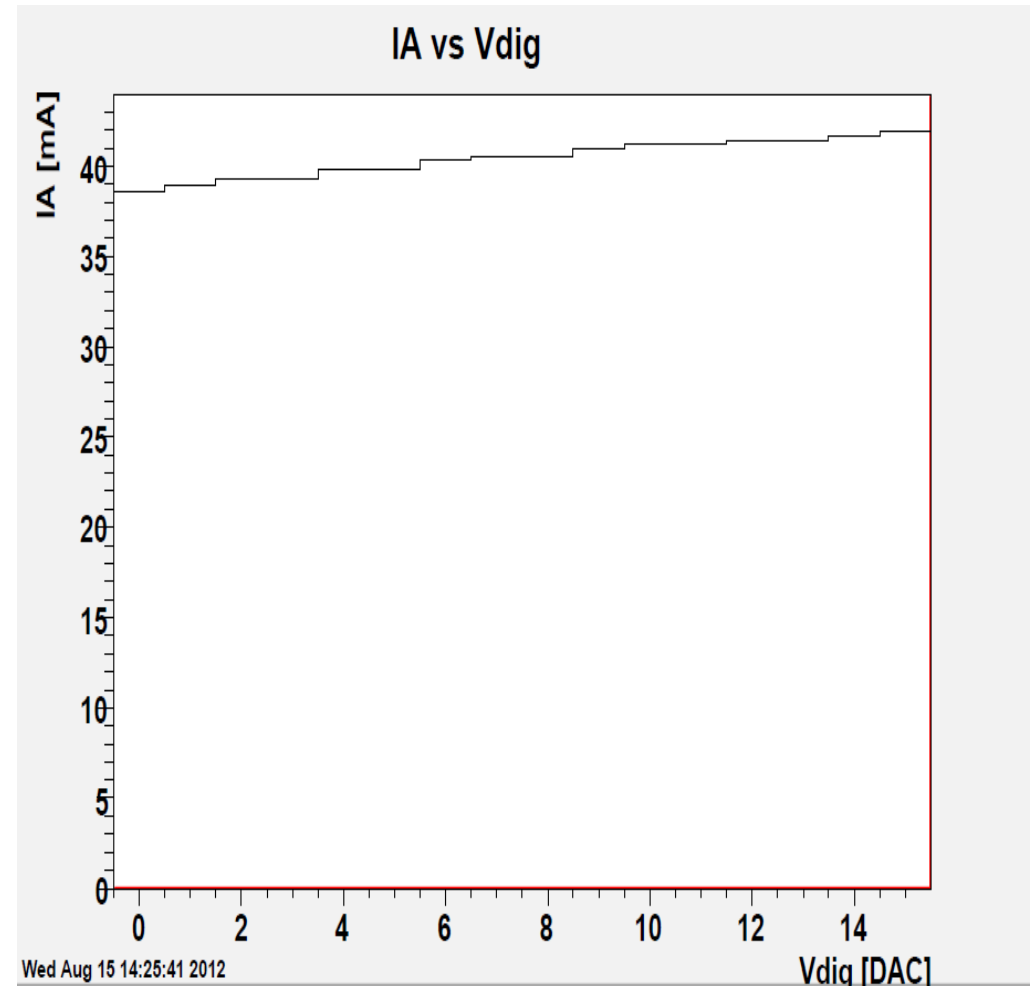
Different ID behavior with Vana

IA vs Vdig

**psi46
chip 5**



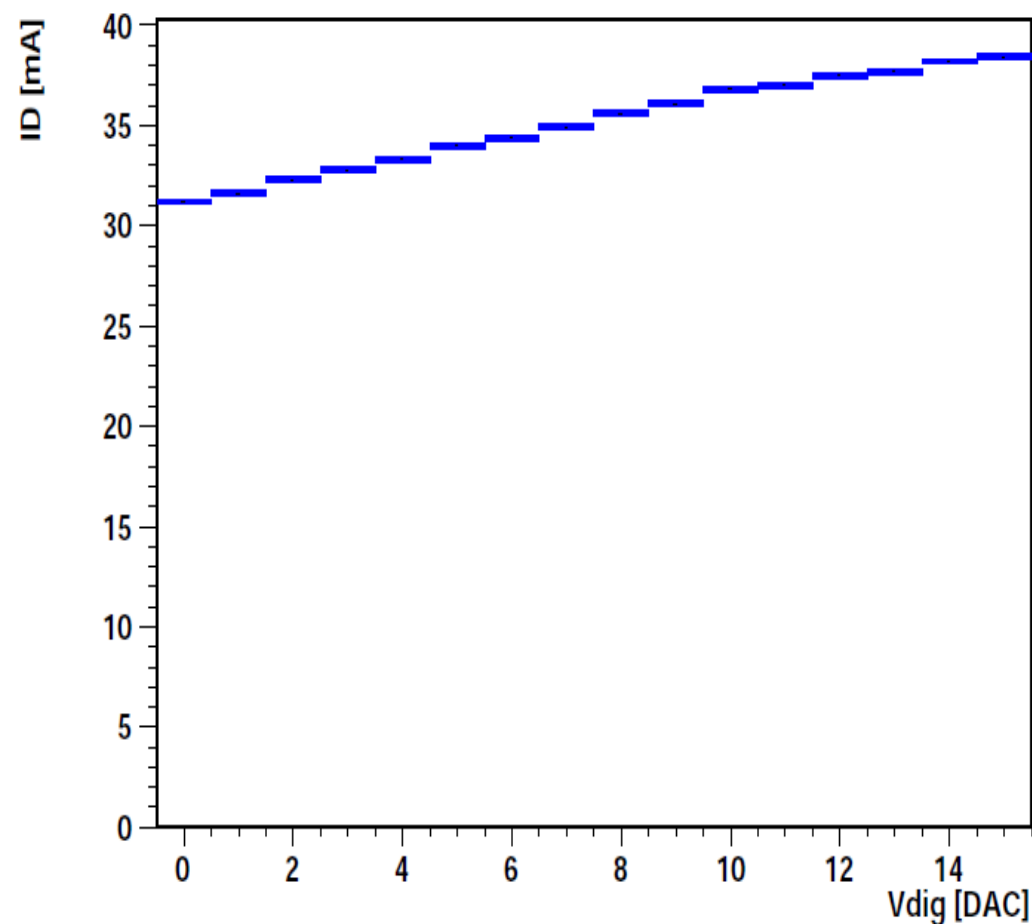
digital chip 202



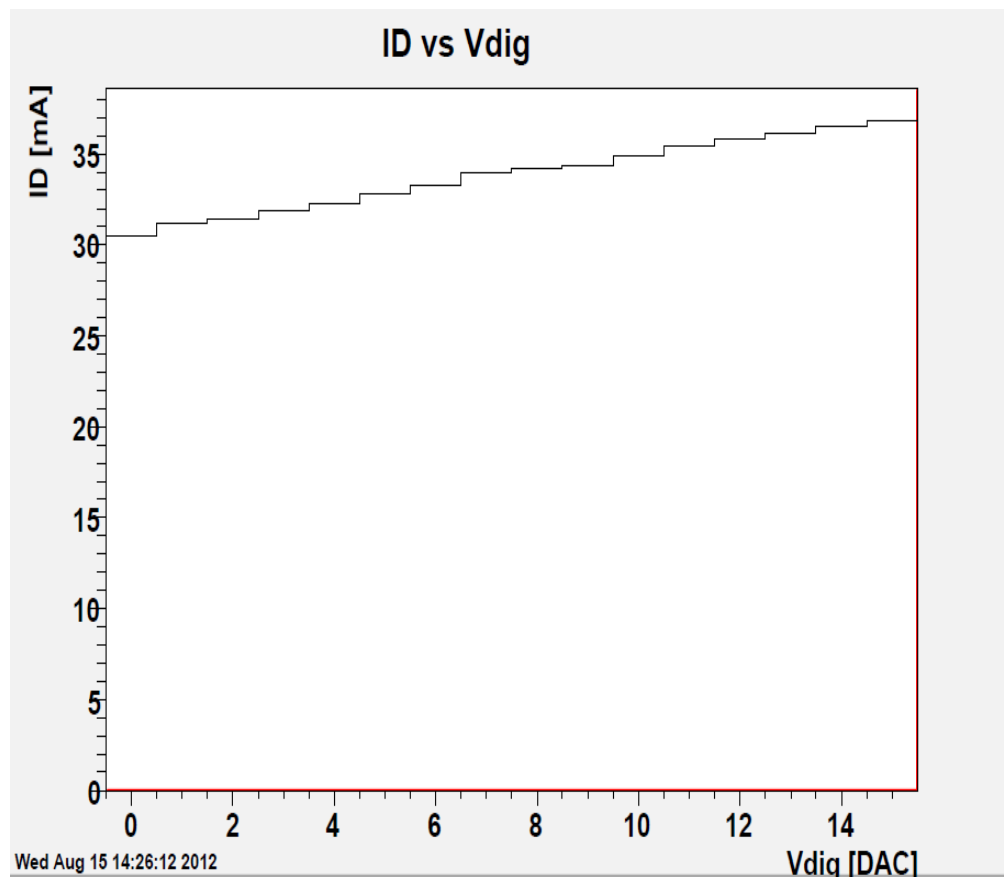
More flat dependence on Vdig

ID vs Vdig

**psi46
chip 5**



digital chip 202



Similar to old ROC