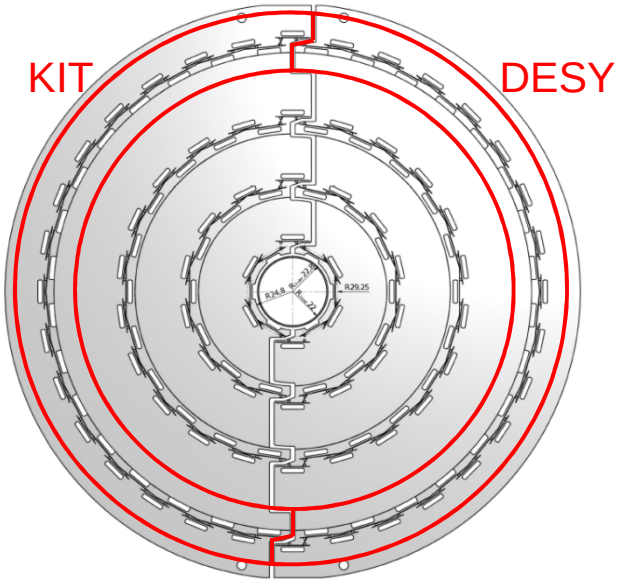
CMS DPIX
Bump Bonding Activities.

Facility Test Results and Plans



DPIX volume
- 512 modules (~42% BPIX)
- ~ 12k ROC to be bonded
- ~53M bump bonds

Jan Hampe, Karsten Hansen (DESY)
Michele Caselle, Thomas Blank (KIT)

Phase I Pixel Upgrade Workshop
Grindelwald, August 28th, 2012

HELMHOLTZ ASSOCIATION

Karlsruher Institut für Technologie

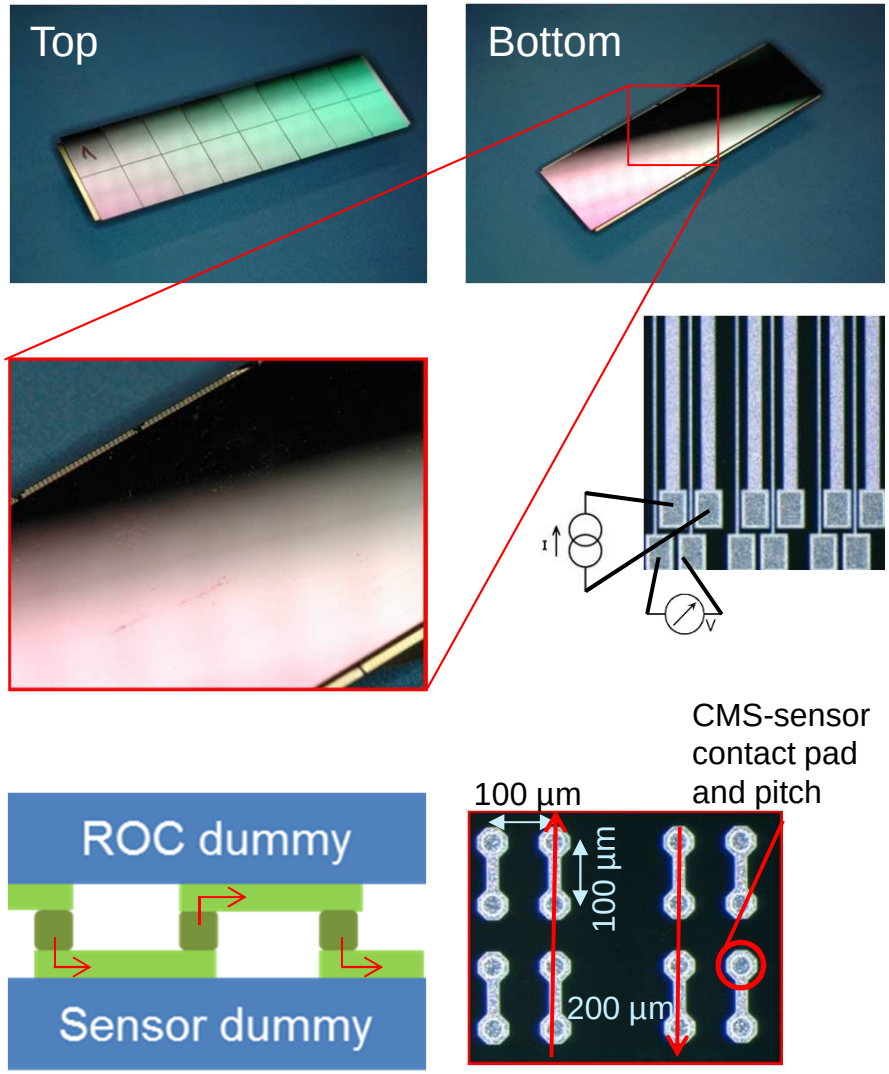
DESY

Outline

- Evaluation of Bumping Methods
- Flip-Chip Bonder Test Results

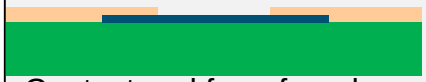
BPIX module dummies

- 4-wire resistance measurements
  - 66560 bumps / module
  - 416 double columns (dc) / module
  - 26 dc / ROC
  - 160 bumps / dc
  - 4 probe pads / dc
  - 104 probe pads / ROC
  - 30 µm passivation opening
  - single „dead pixel“ → open circuit
- Future tests also with
  - 15 µm opening (real ROC like)
  - 285 µm silicon thickness



Pac Tech‘s electroless UBM & solder jetting

Step 1:UBM Process

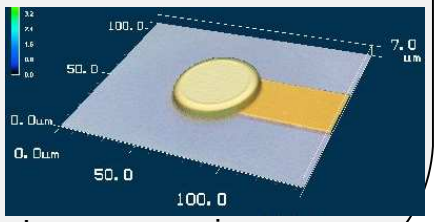


Contact pad from foundry

UBM-line

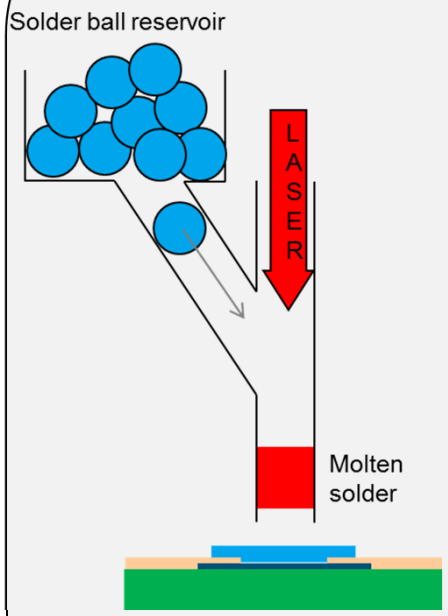
ENEPIG
e-less Ni 5µm,
e-less Pd 200 nm,
immersion Au 50 nm

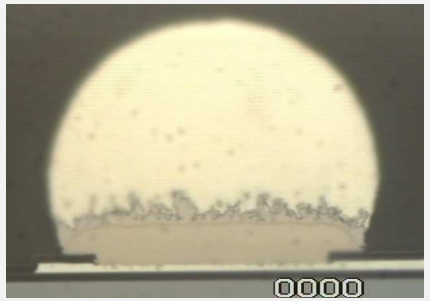
Pad after ENEPIG deposition



Laser scan microscopy

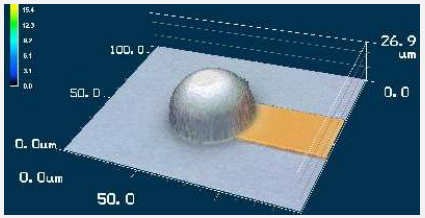
Step 2: Jetting Process





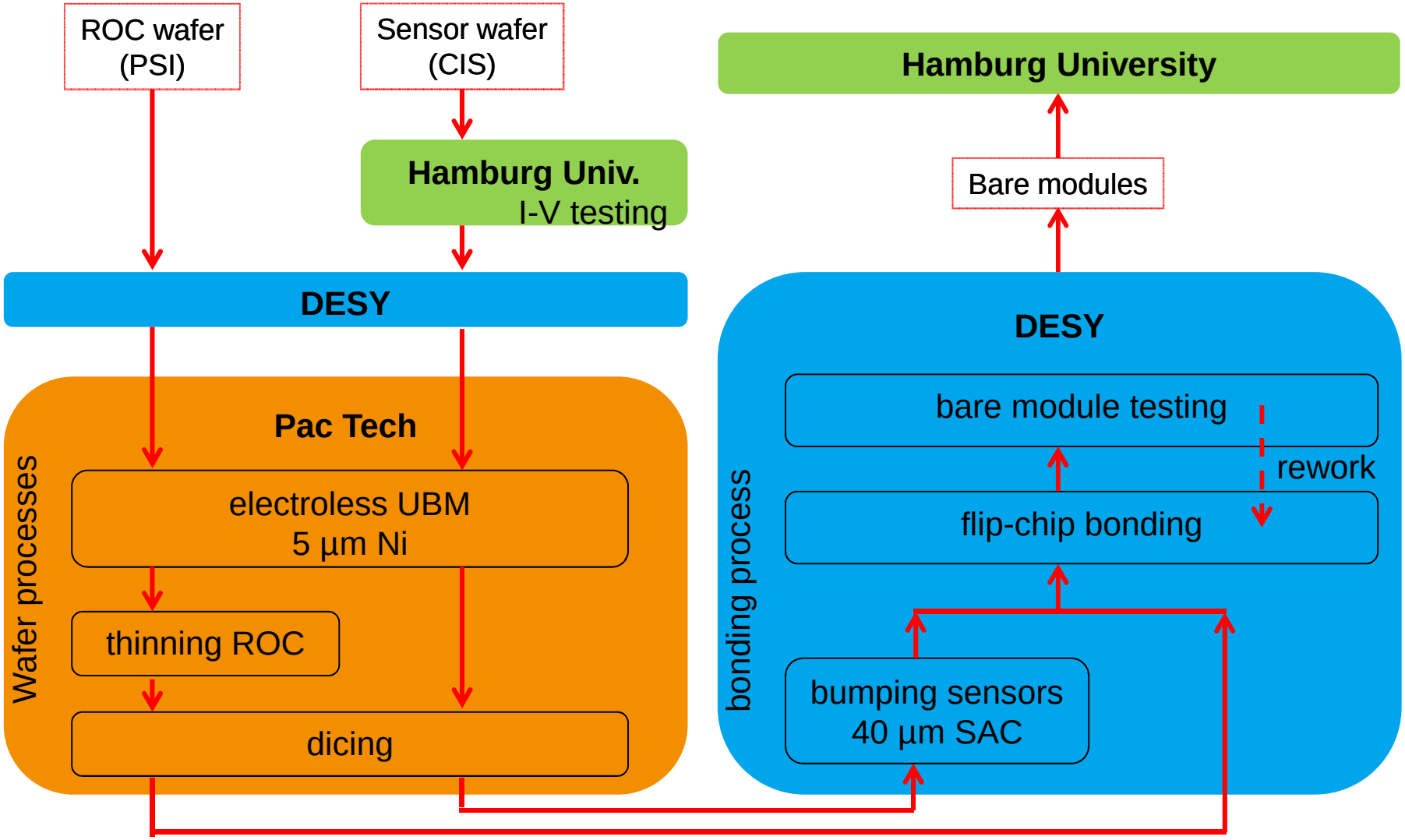
Cross section micrograph

DESY
40 µm,
5 Hz

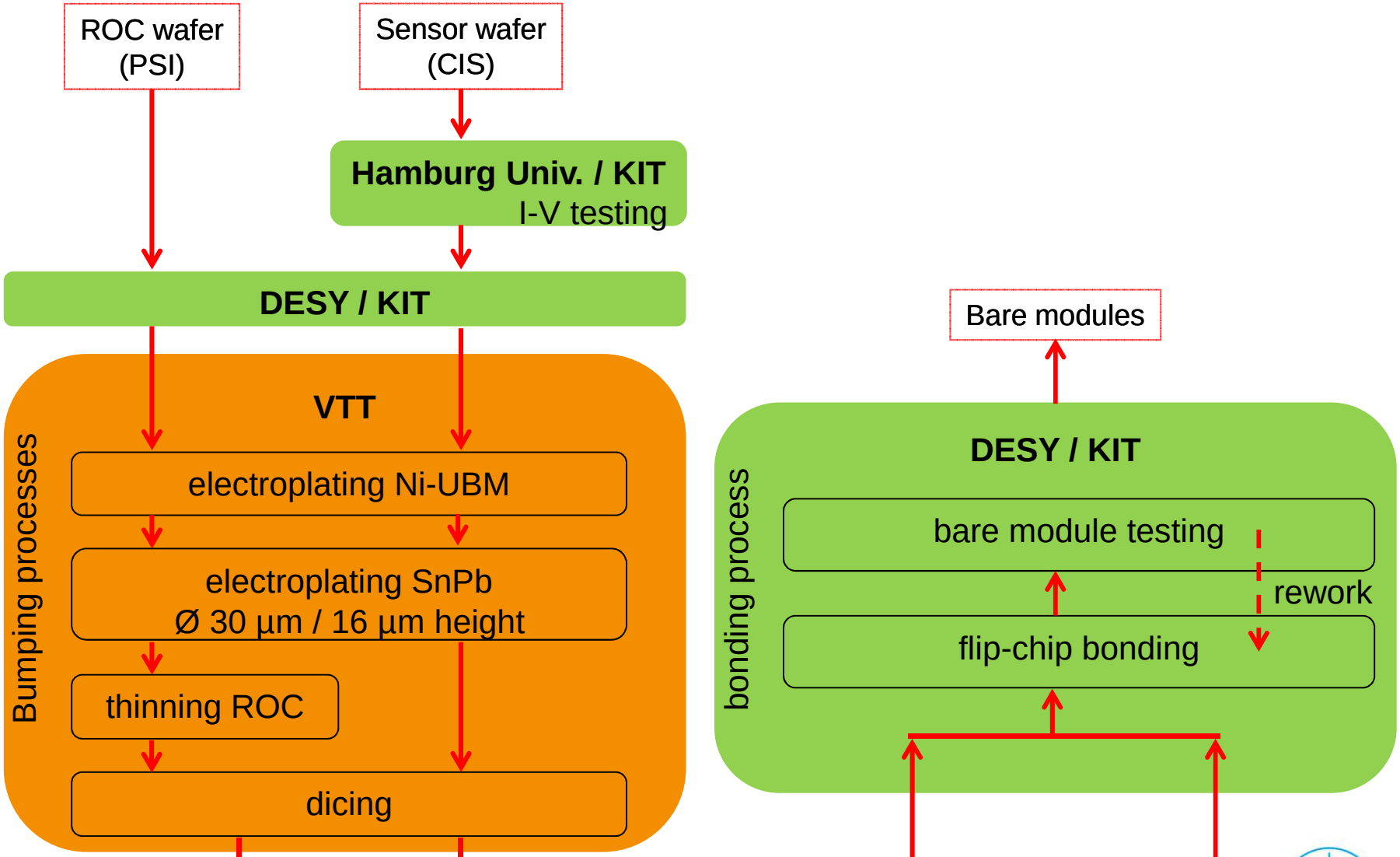


Laser scan image of pad with SAC solder bump

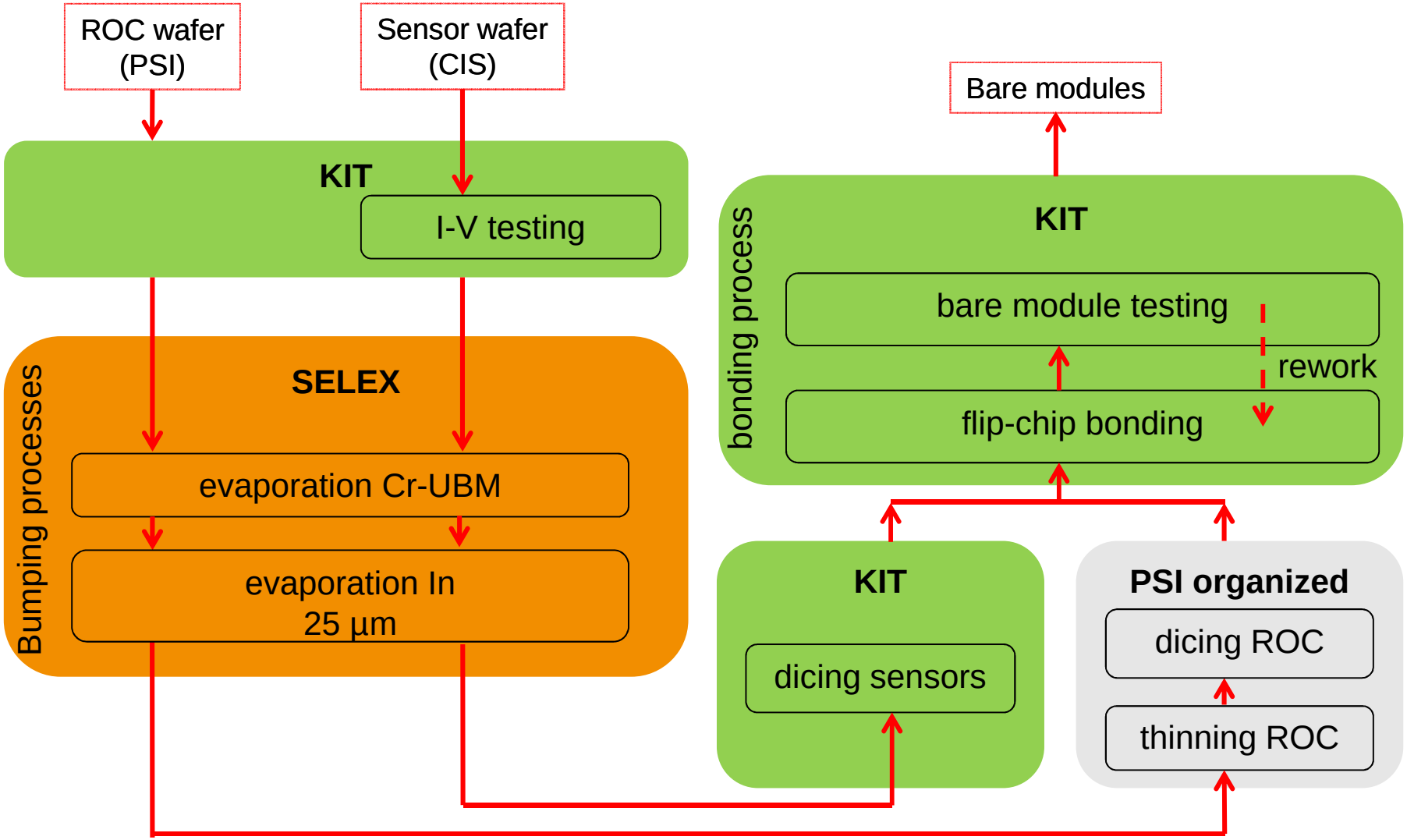
Bump Bonding plan at DESY



Alternative bumping (VTT)



Alternative bumping (SELEX)



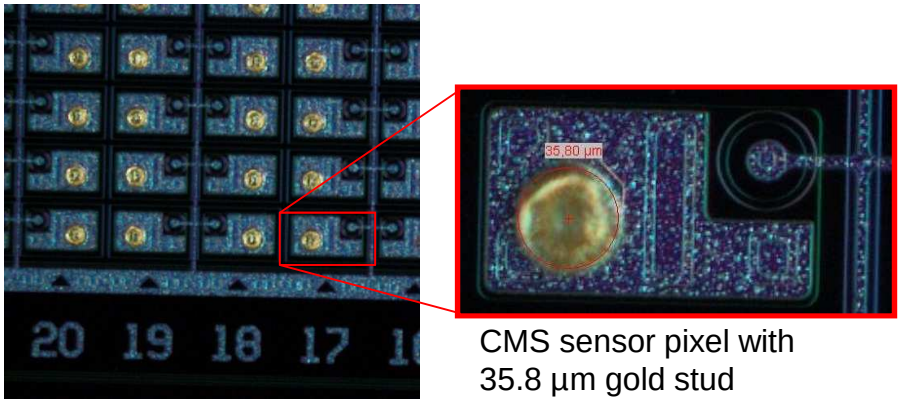
Alternative bumping development @ KIT: gold studs

- Not for Phase I
- Tests on CMS sensor samples:
  - conventional ball–wedge bonder
  - ~ 20 bumps / s
  - in development:

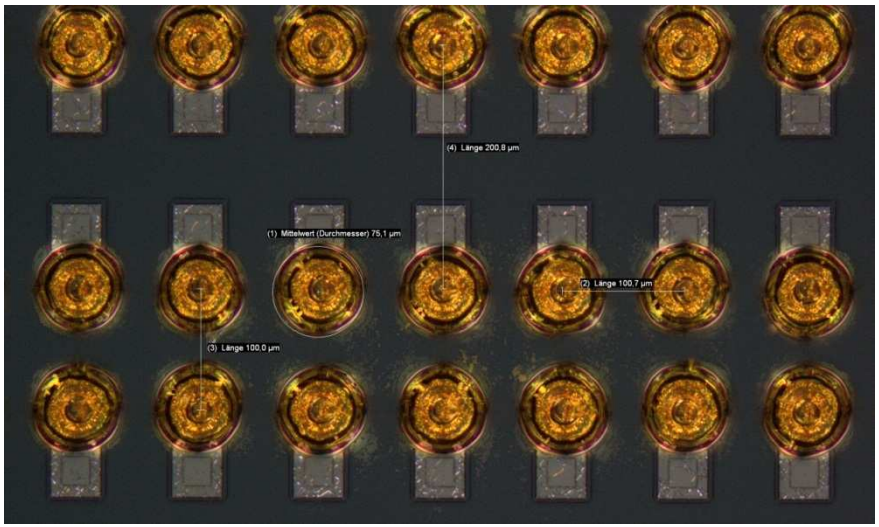
    ~35 µm bumps (15 µm gold wire)

  - envisaged:

    ~ 25 µm bumps (12.5 µm wire)



CMS sensor pixel with
35.8 µm gold stud



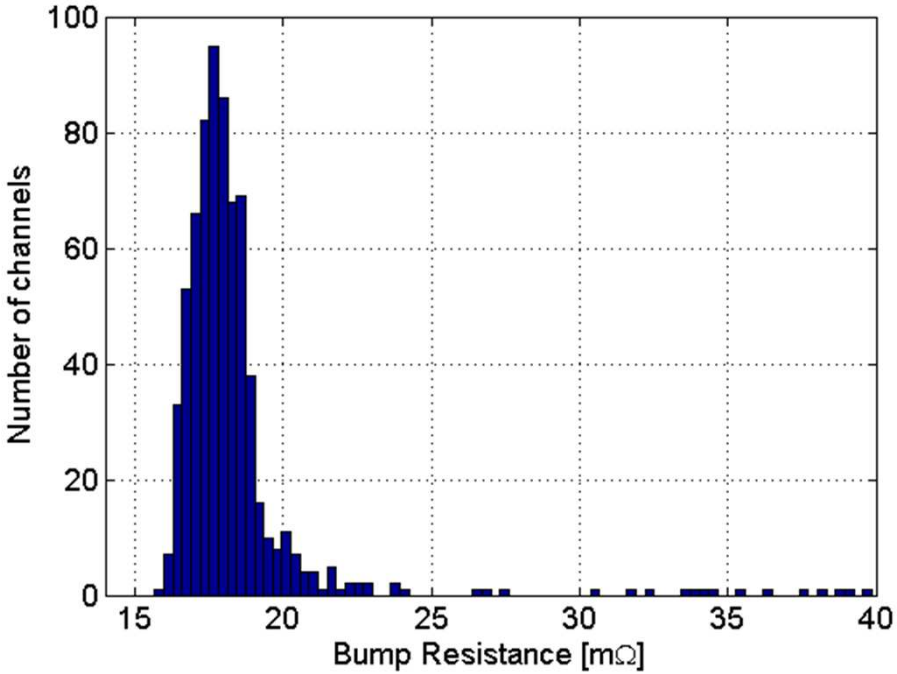
by Stefan Heitz

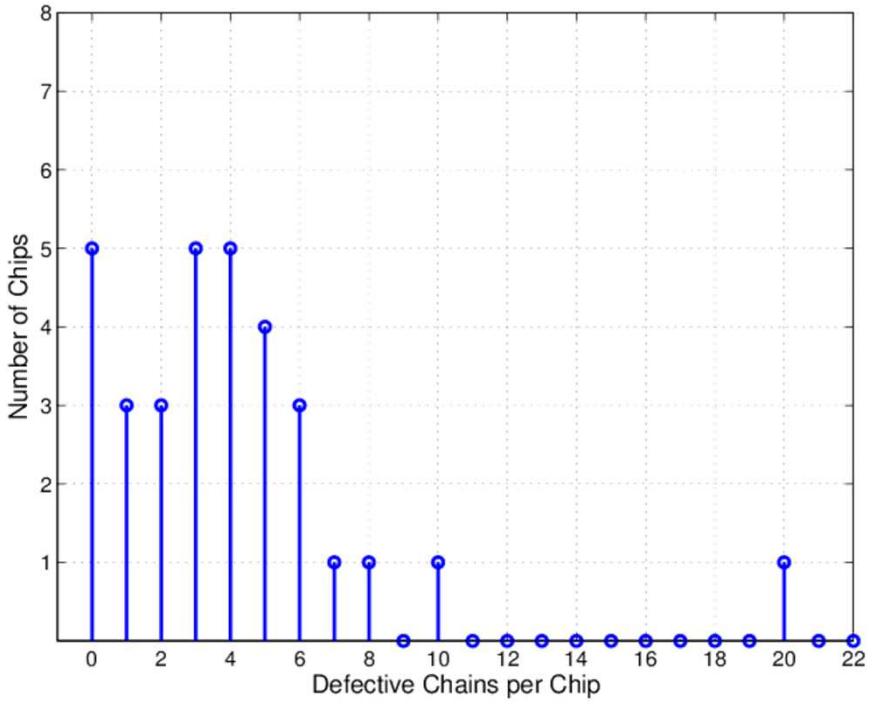
DPIX Flip-Chip bonding

- Finetech‘s automated fineplacer FEMTO
  - accuracy < 1 µm
  - KGD probing before bonding
  - formic-acid ambient chamber
  - complete process parameter monitoring
- Process parameter status
  - SAC solder (melting point 217℃)
  - ~ 1 min./chip (without KGD probing)
  - tacking: 100℃ hot plate, 210℃ Chip, 200 N)
  - reflow: ~3 min., formic-acid, max. 240℃ HP
  - in development

DESY sample characterization

- Results
  - 84.7% double columns with finite resistance
  - residual dc have ≥ 1 bad bump → 0.09% module bump yield
  - shear result: 21 g/bump
  - Bump resistance ~ 17.5 mΩ



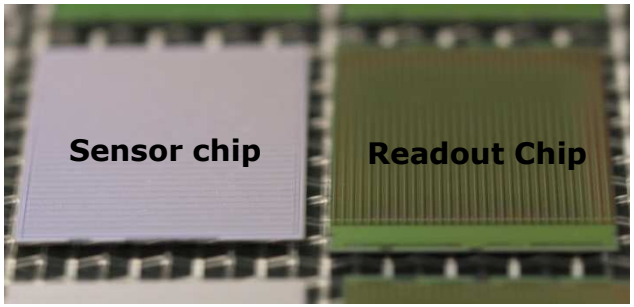


KIT sample characterization

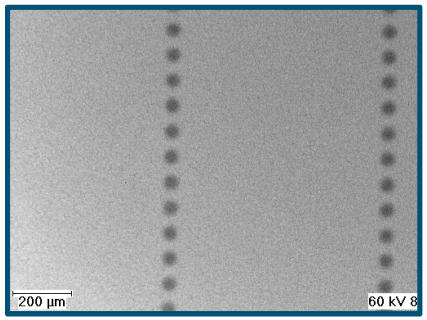
- ALICE1 spares
  - VTT processed (plated SnPb bumps)
  - 8192 bumps/sample
  - 425 µm / 50 µm pitch
  - 30 µm diameter
  - 2.5 g/bump in pull tests
- CMS FPIX spares
  - KIT Au-studs (35 µm)
  - current placing parameter:

    380°C hot plate and chip

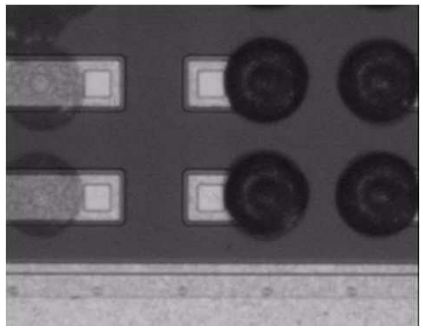
    400 N



ALICE1 pixel detector ROC and sensor after VTT bumping



X-ray of ALICE1 sample bonded with Femto



X-ray of FPIX sample bonded with Femto

Summary

- Test structures copying the critical properties of the real modules
  - top metal, passivation
  - pad pitch, pad size, pad count
- Solder bumping processes
  - DESY inhouse SAC solder jetting (selected)
  - KIT external service (evaluation ongoing)
  - second source services (evaluation ongoing)
- FC-Bonding machine selected
  - for both sites KIT and DESY
  - automated high accuracy bonder: Femto
  - special features: in-situ reflow and KGD probing prior to attach

Acknowledgments

For their patience, useful comments, supporting work & cooperative attitude

- Equipment vendor
  - Pac Tech
  - Finetech
- Bumping vendor
  - VTT
  - SELEX
- DESY people
  - Inge Diehl
  - Alexander Titze
  - Dominik Belzer
  - Marco Sessa
- KIT people
  - Stefan Heitz
- ALICE collaboration for provision of test samples

Backup

Timetable

> Bonding machines installed	end of 2012
> DESY‘s solder jet machine installed	mid of 2013 (tendering (20 weeks) and production (20 weeks))
> KIT/SELEX In-bump test samples	Nov. 2012
> DESY/KIT/VTT SnPb-bump test samples	Nov. 2012
> First real bare module produced	summer 2013

Summary

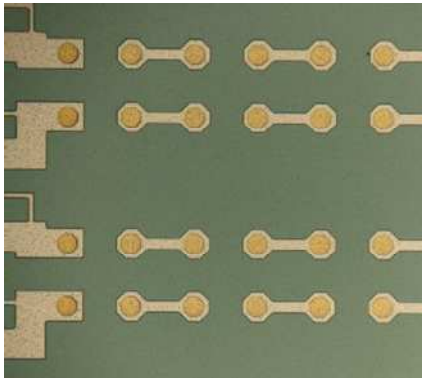
- Test structures copying the critical properties of the real modules
  - top metal, passivation
  - pad pitch, pad size, pad count

Solder Bumping				
Site	**UBM**	**Conducted at**	**Bumping**	**Conducted at**
DESY	e-less	Pac Tech	jetting 40 µm, 5 Hz	DESY
KIT	plating / evaporation	VTT / SELEX	plating / evaporation 25 µm	VTT / SELEX

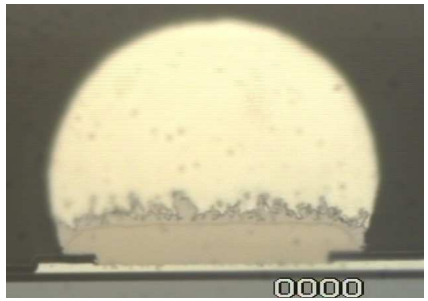
Flip-Chip Bonding				
Site	**Bonder**	**Conducted at**	**Comments**	
DESY	Femto	DESY		
KIT	Femto	KIT	Collaboration with INFN & CERN & SELEX	

DESY bumping processes overview

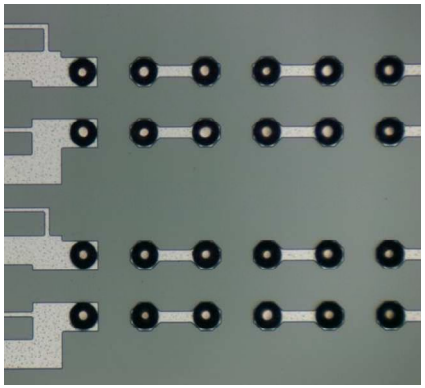
- DESY ENEPIG UBM:
  - conducted at Pac Tech
  - 5 µm e-less Nickel
  - 200 nm e-less Palladium
  - 50 nm immersion Gold
  - isotropic growth
  - mushroom like cross section
- SAC305 solder spheres
  - in future placed and reflowed at DESY
  - lead free (Sn96.5Ag3Cu0.5) ($\%_{wt}$)
  - readily alloyed by vendor
  - solder volume controlled by sphere size / vendor



Micrograph of a dummy ROC with ENEPIG UBM



Cross section micrograph of a DESY bump



Micrograph of a dummy ROC with jetted solder bumps

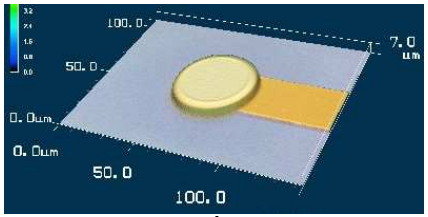
Pac Tech‘s electroless UBM

- Batch process
  - industrial standard process
  - high throughput / capacity
  - cost-efficient
- wet chemical deposition
  - grows on metal
    - ≥ 1 µm metal pad thickness
    - no pin holes
  - maskless
  - optional backside protection

Contact pad from foundry

UBM-line

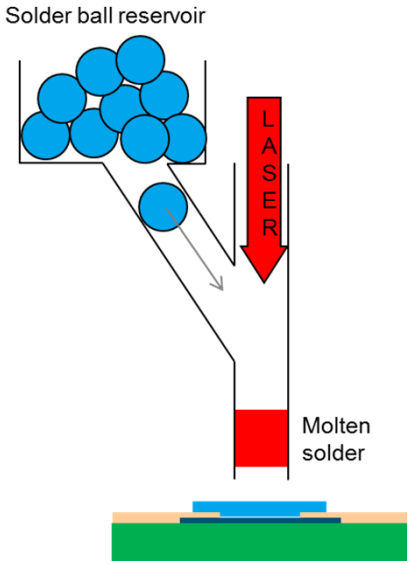
Pad after ENEPIG deposition



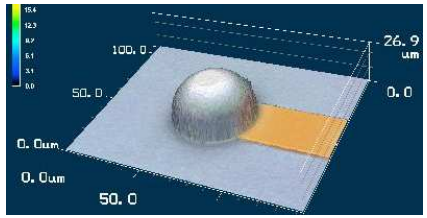
Laser scan microscopy

Pac Tech‘s solder jetting

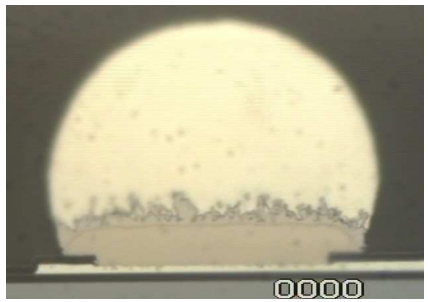
- Sequential process (≤ 5 bumps / sec)
  - singulation of sphere from reservoir
  - directing to pad through capillary with forced N_2
  - melting by laser pulse
  - jetting molten solder ball
- High flexibility in
  - solder choice
  - bump size (≥ 40 µm now ⟶ 30 µm ⟶ 10 µm)
  - bump map (no mask)
  - substrate (chip / wafer / 2.5 D …)



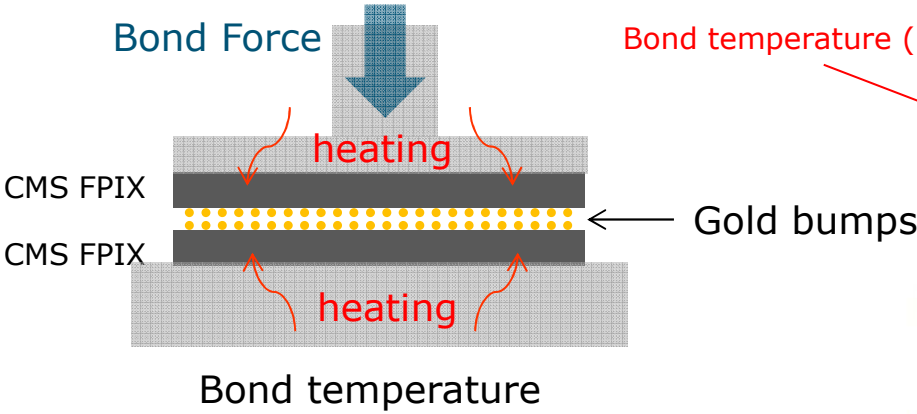
Laser enhanced solder ball jetting

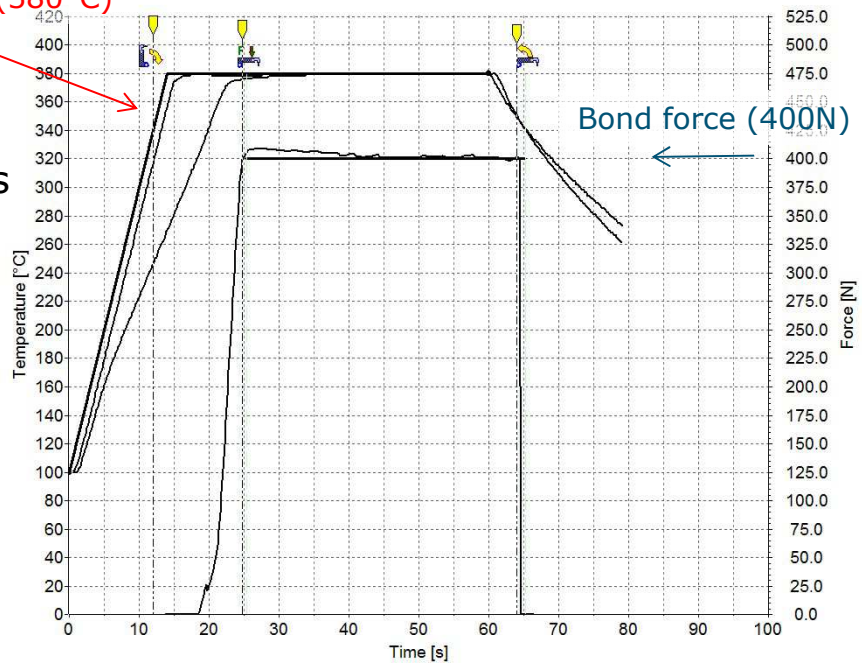


Laser scan image of pad with 40 µm SAC solder bump

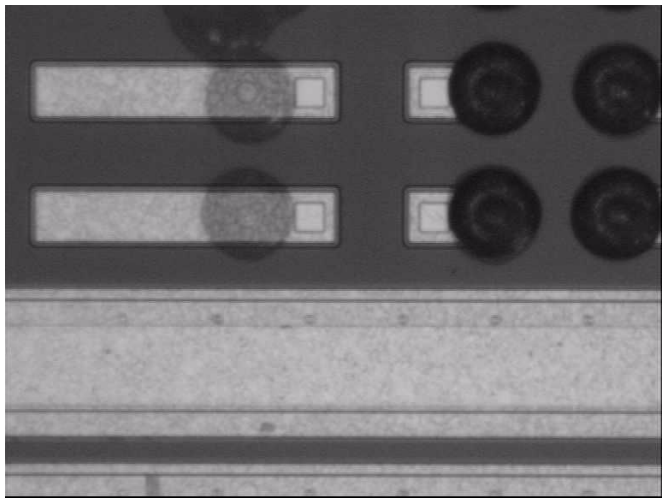

Cross section micrograph

Assembly with Au-studs by Femto

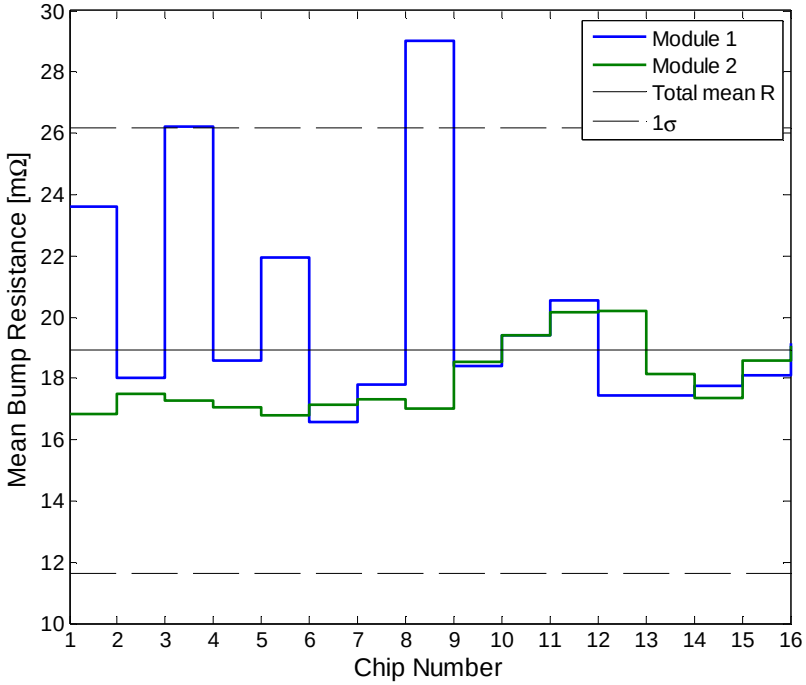


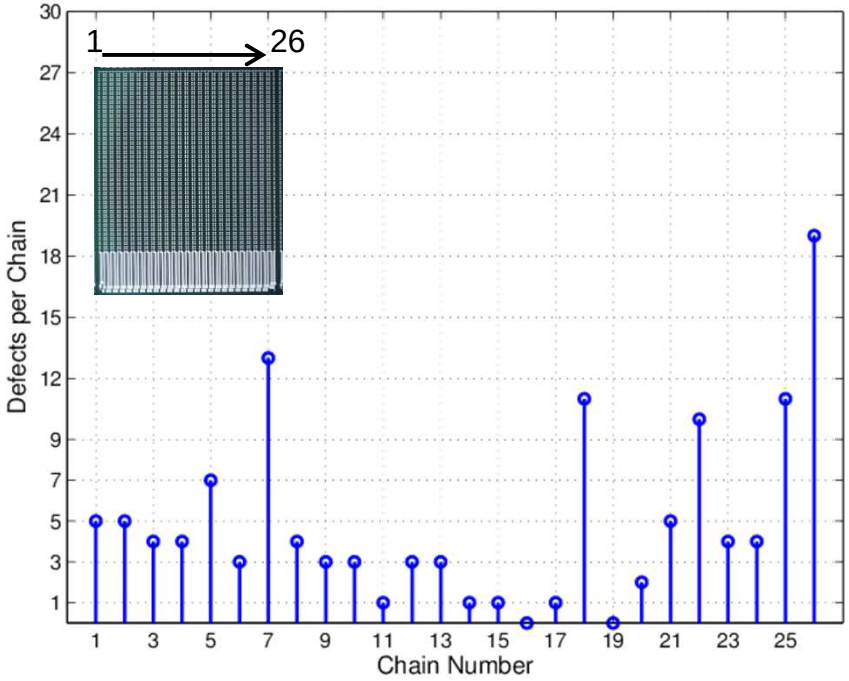


Gold stud bump bonding



Further (spatial) details in first electrical tests





- First 8 chip areas of module 1 have been used in several attempts to find correct bonding parameter
- Very low indication of leveling issues during bonding found