# Silicon Tracking for Linear Colliders

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IEEE/NSS Linear Collider Special Event

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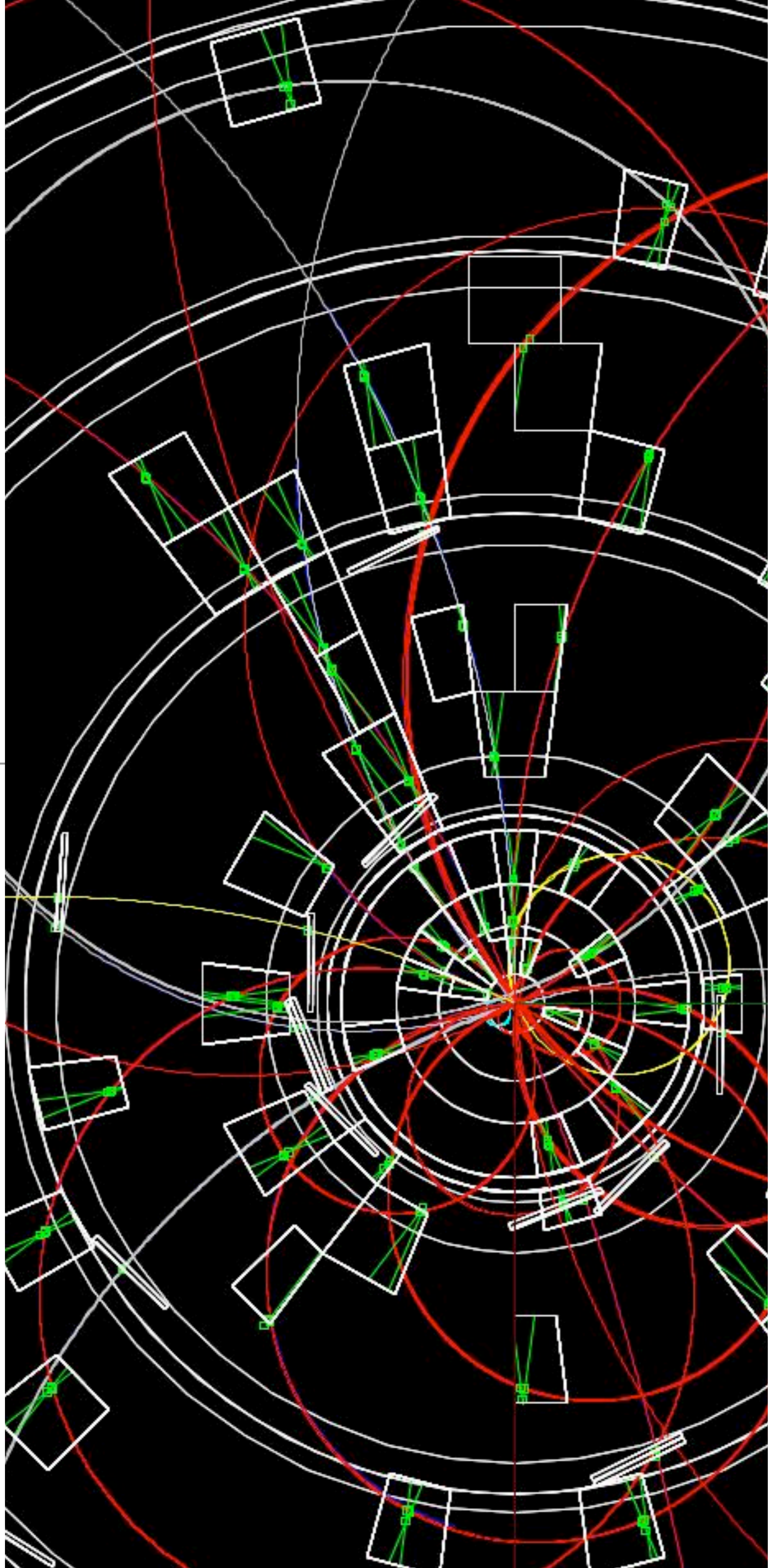


# In the mind of the tracking designer...

Uses no power so requires no cooling

Contains no material but is perfectly stable mechanically

Has infinite readout granularity in both space and time

Has perfect energy resolution and infinite dynamic range

Has infinite readout bandwidth

Is robust against radiation damage and accidents

Is simple and inexpensive to build


Then there's reality...
Uses no power so requires no cooling
Contains no material but is perfectly stable mechanically
Has infinite readout granularity in both space and time
Has perfect energy resolution and infinite dynamic range
Has infinite readout bandwidth
low occupancies
Is robust against radiation damage and accidents
low radiation doses
Is simple and inexpensive to build
A great ILC tracker!

# LC Tracking Requirements

In *all* concepts, outer Si tracking part of an integrated tracking system!

- Pattern recognition includes vertex detector (also ECal!)
- Outer silicon tracker has a primary role only in measuring $p_T$.

- Physics requires excellent resolution at all $\theta$, $p_T$. Given $B$ and $\Delta$R:
  - high $p_T$ resolution $\propto 1/\sqrt{N_{\mathrm{hits}\ (r-\phi)}} \times \sigma_{\mathrm{hit}(r-\phi)}$
  - low $p_T$ resolution $\propto \sqrt{\mathrm{material}} \propto \sqrt{N_{\mathrm{hits}}}$
  - forward tracking cannot be an afterthought.

*minimize* ⇒

$\sigma_{\mathrm{hit}(r-\phi)}$

$\frac{\mathrm{material}}{\mathrm{hit}}$

$N_{\mathrm{hits}}$ *(non r-φ)*

- Particle-flow calorimeters to measure jets with exquisite precision. Must not place material in front of ECal that jeopardizes this mission.

- Cost and complexity should not be ignored.

# Shopping List

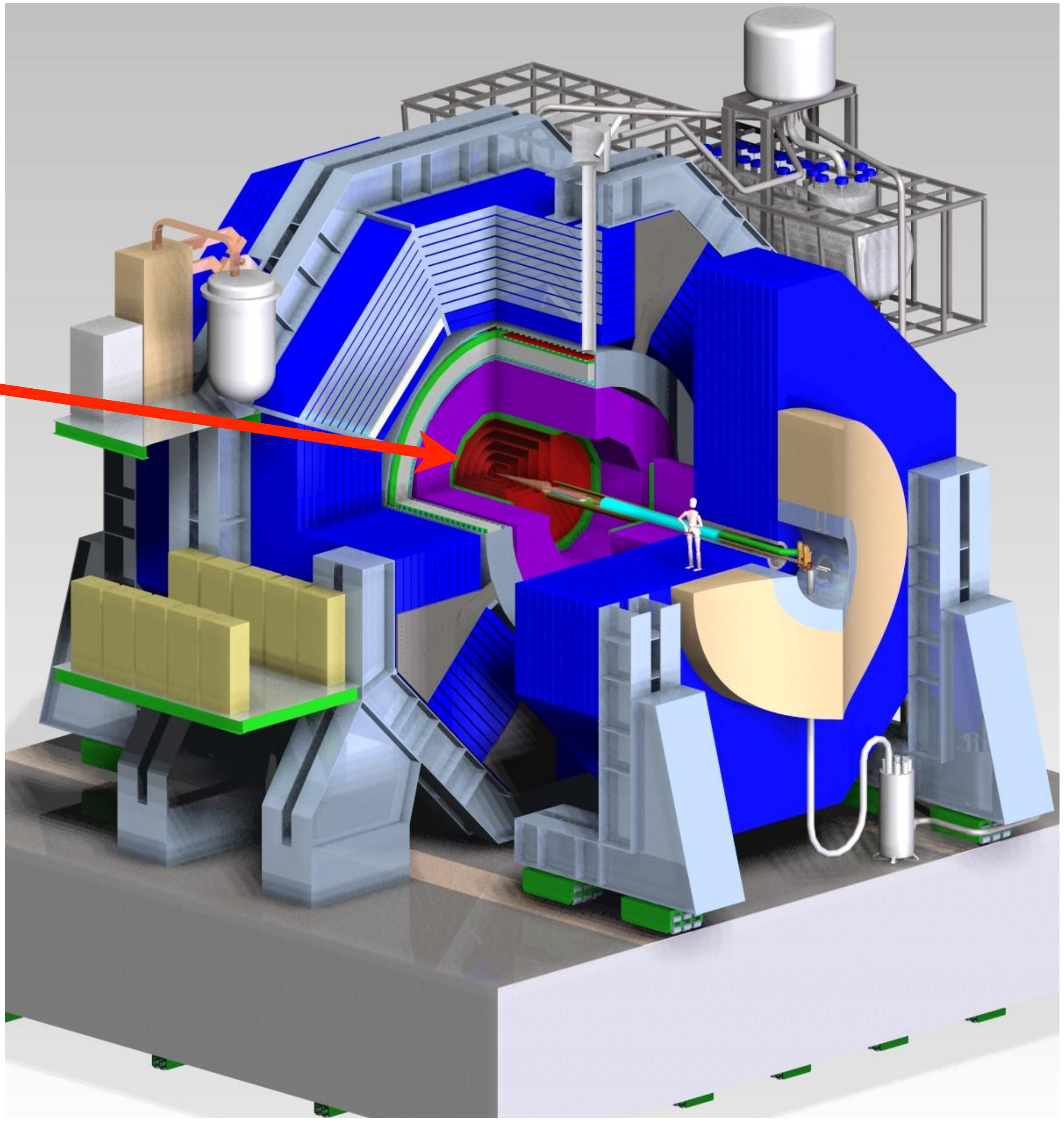
- Provide coverage as hermetic as possible
- Minimize material/hit
- Minimize single-hit resolution in r-phi
- Minimize number of hits required to achieve acceptable pattern recognition
- Employ simple, mature solutions where possible to lower risks and contain costs.

# Example: SiD for the ILC

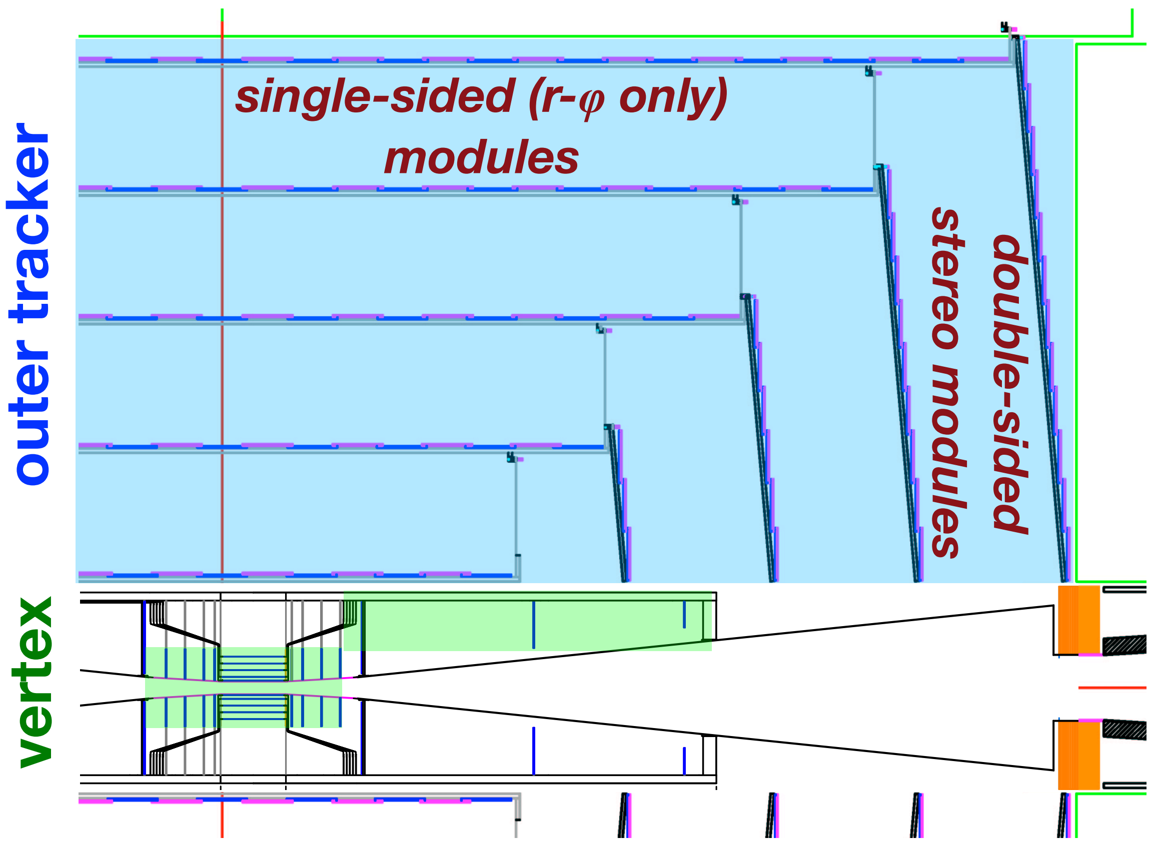
*Aggressive performance at a constrained cost*

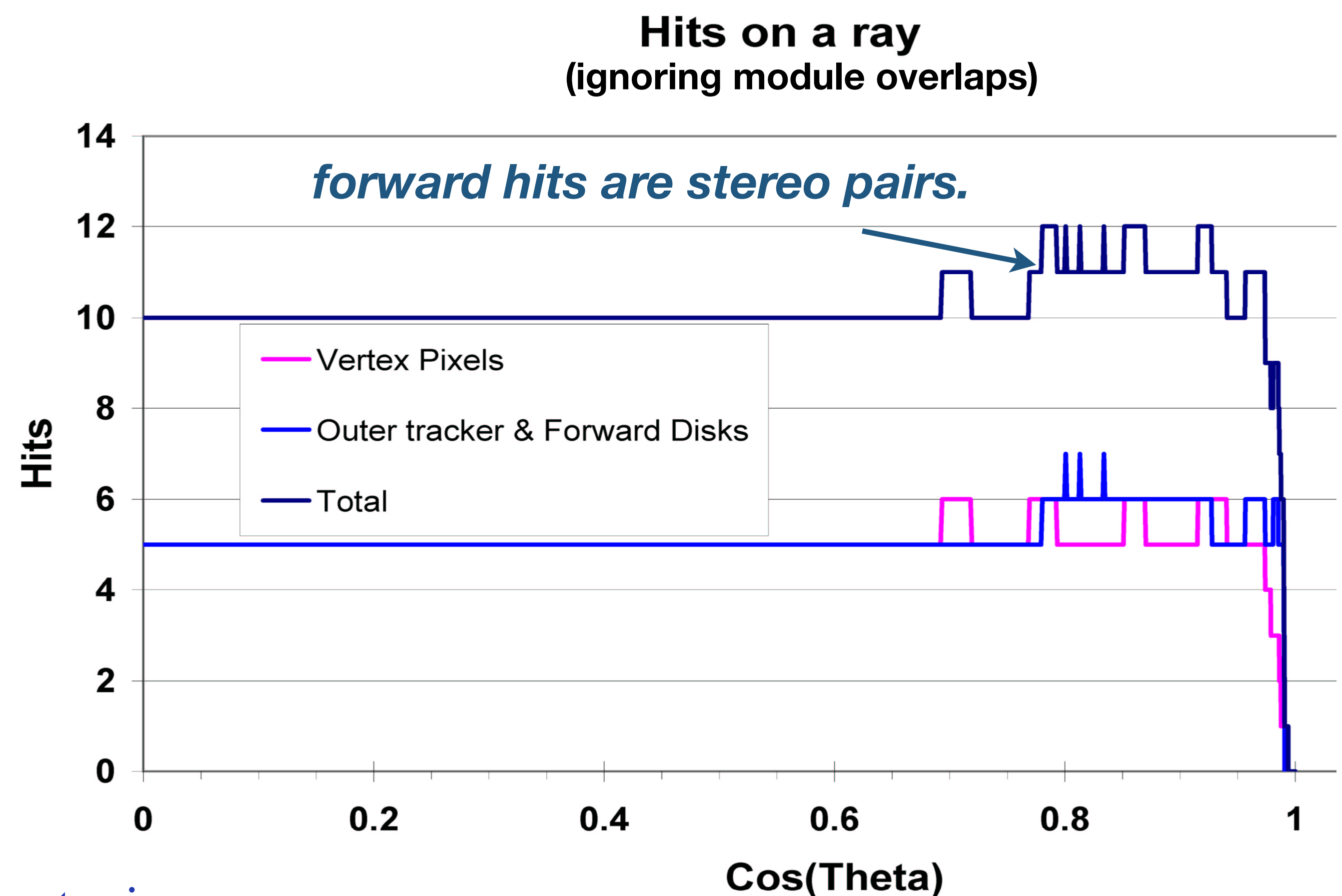
- 5-layer silicon vertexing detector ($\sim 3\times10^9$ channels)
- 5-layer silicon microstrip tracker ($\sim 3\times10^7$ channels)
- Finely segmented particle-flow calorimeter with Si-W ECal ($\sim 2\times10^8$ channels)
- All inside a 5 T solenoid: SiD is "small" (roughly CMS-sized)

*SiD is a "particle flow" detector: subdetectors work together to reconstruct the physics objects, including tracks*

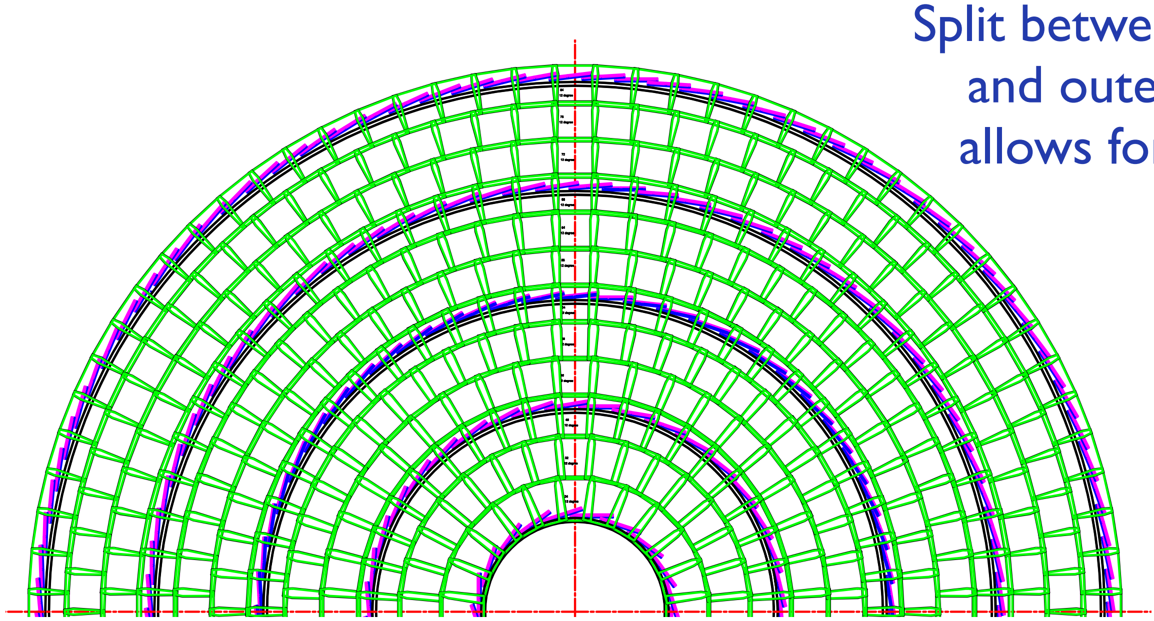


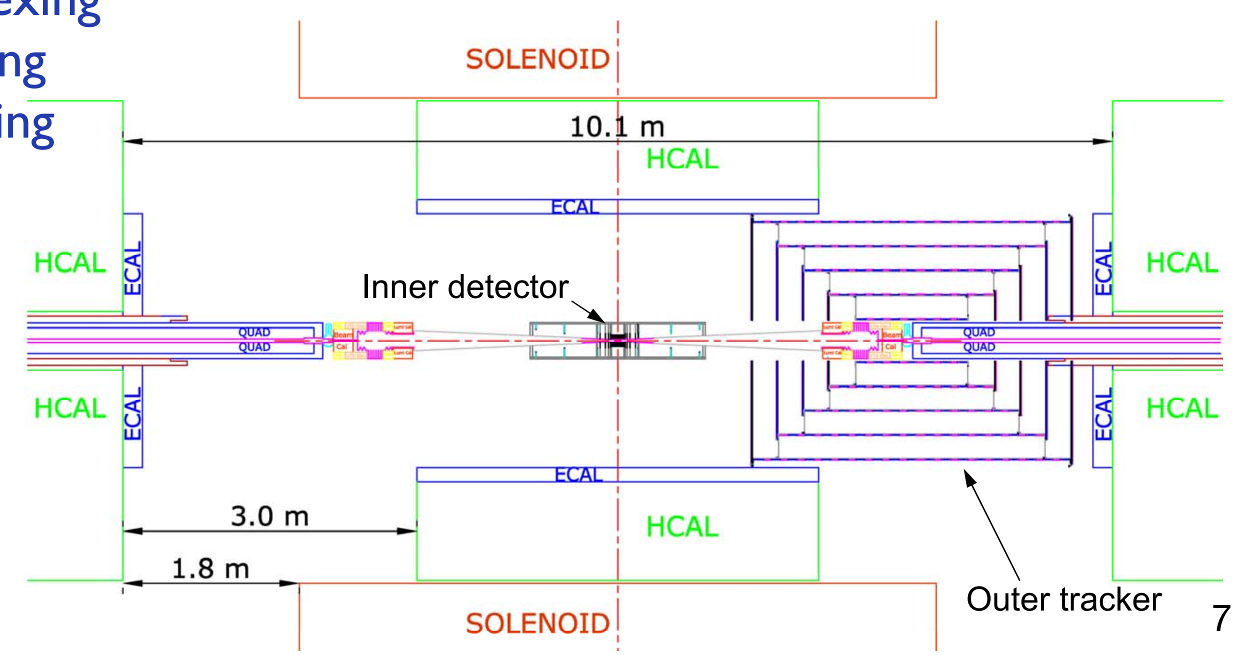
# SiD Tracker Coverage




Split between vertexing
and outer tracking
allows for servicing



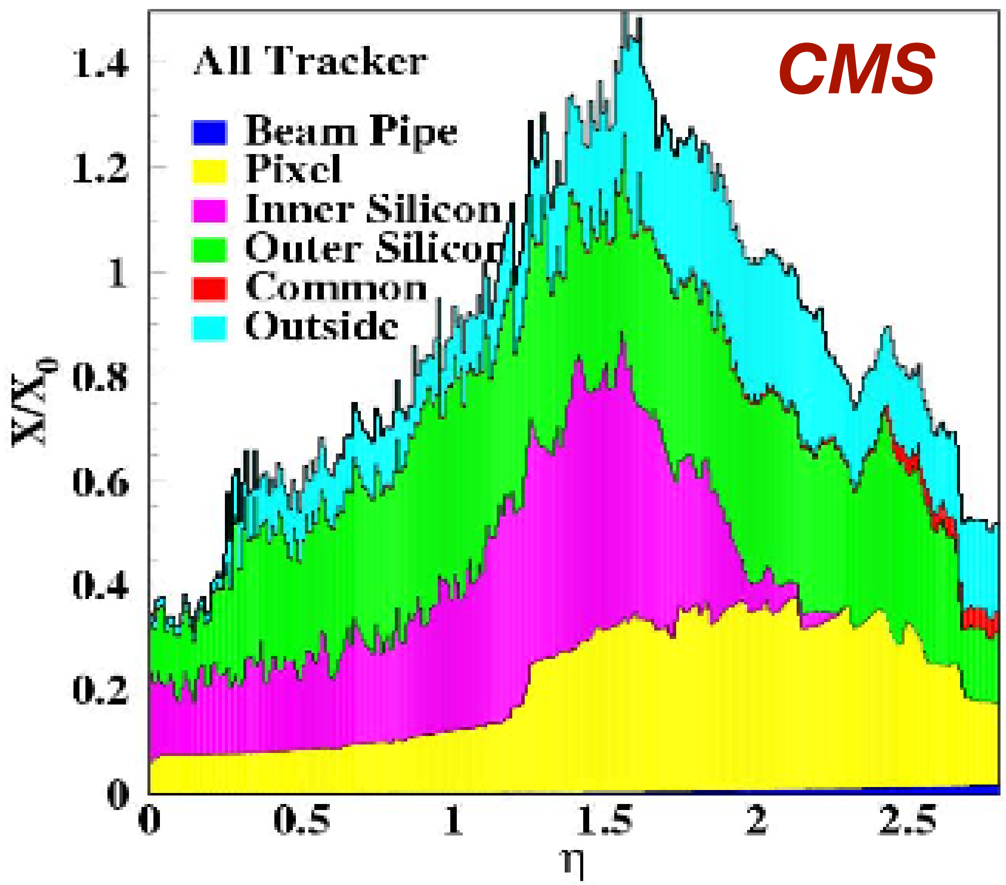


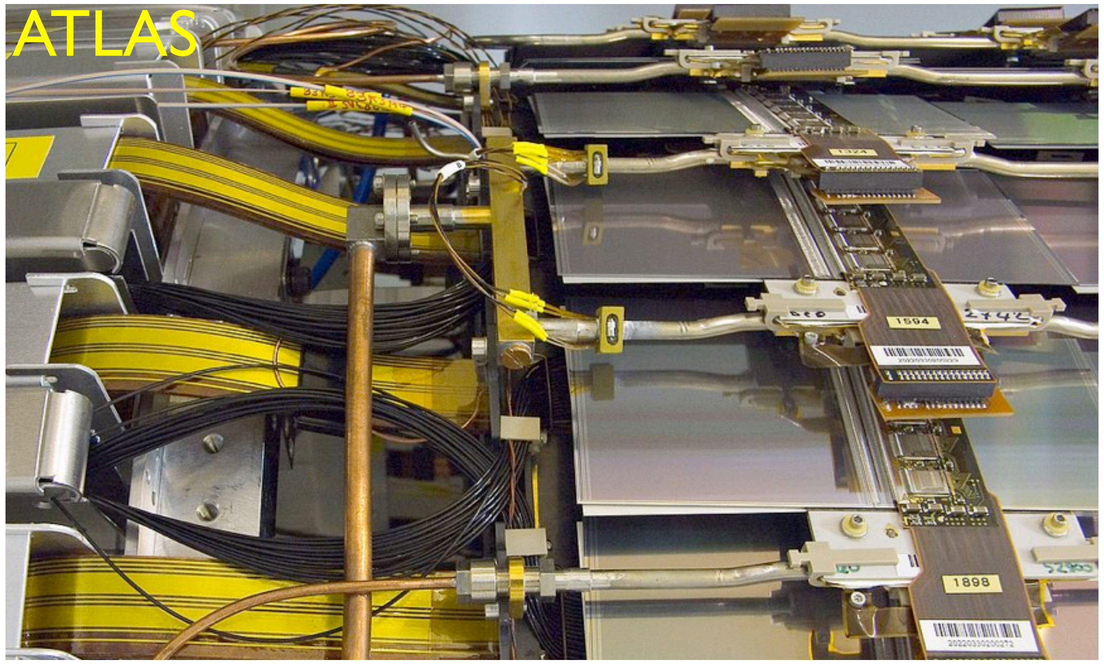
# Reducing Material/Hit

*Large silicon trackers (ATLAS, CMS) have been too massive for a LC!*

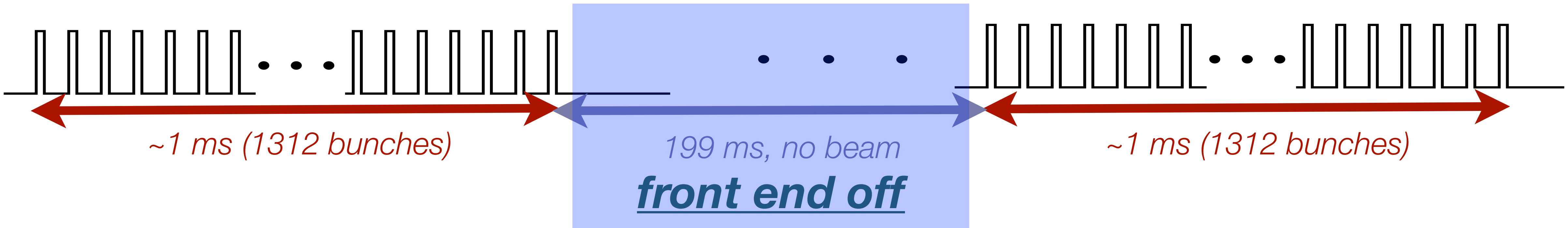
- Power
- Cooling
- Readout
- Support
- Sensors

*This is the primary challenge!*



# Reducing Power/Cooling: *ILC Timing*



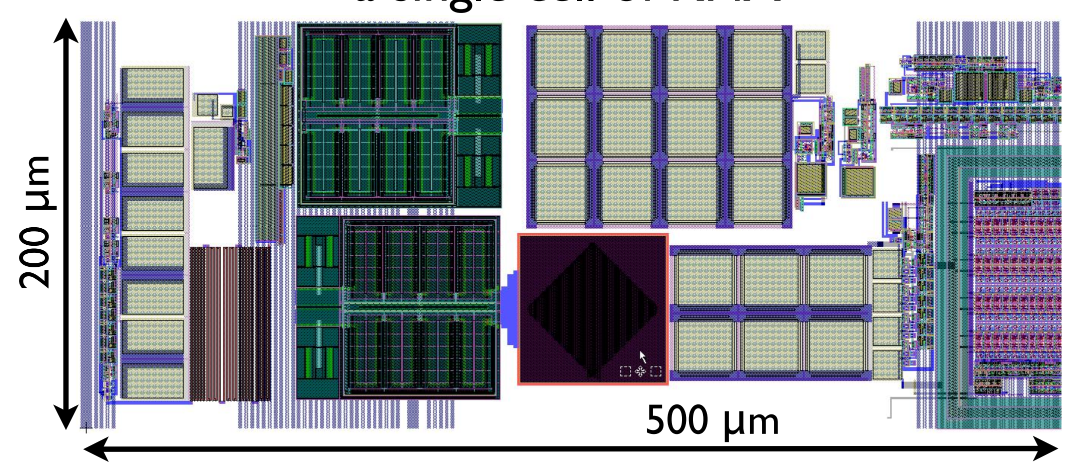

*Pulsed operation of front end results in ~100X reduction in dissipated power*

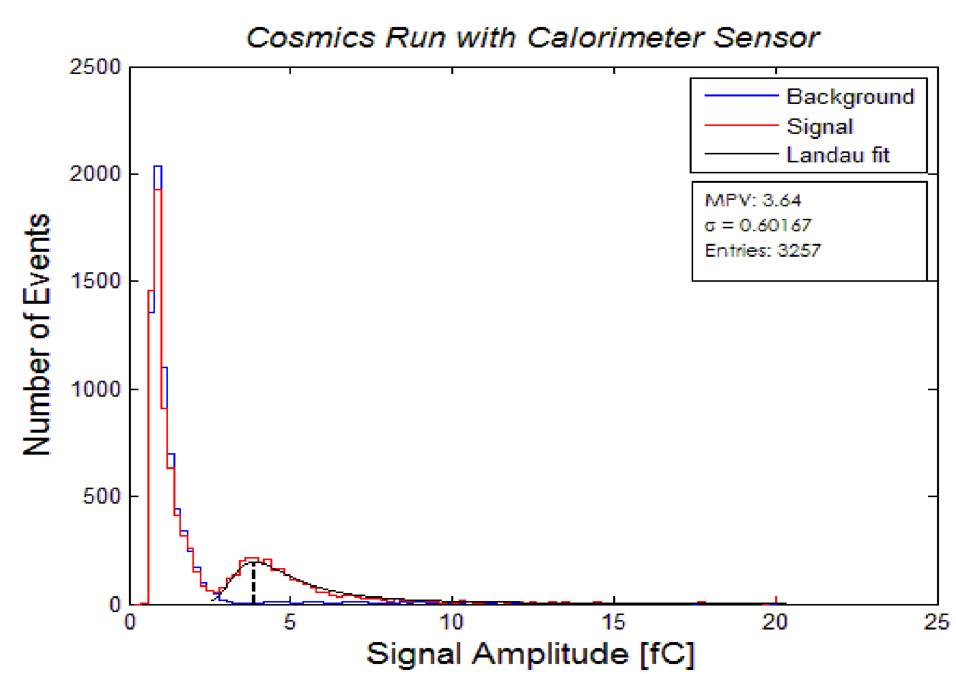
- Minimizes cable plant *and* cooling
- The SiD realization is KPiX ASIC
  - 1024 channels
  - 20 μW/channel avg. = 400 $\mu W/cm^2$

➡~600 W total for 30 million channels: tracker can be gas cooled

*KPiX used in ECal, possibly HCal, Muons also!*

a single cell of KPiX



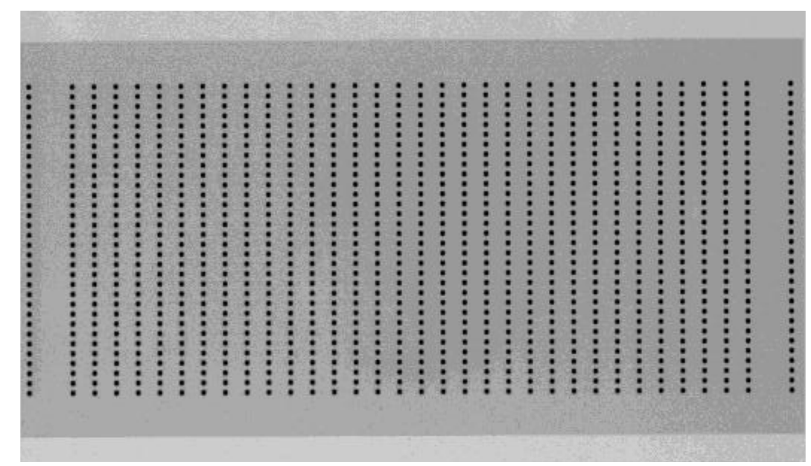
# Reducing Readout Material


*KPiX stores signals acquired during a bunch train in 4 analog buffers*

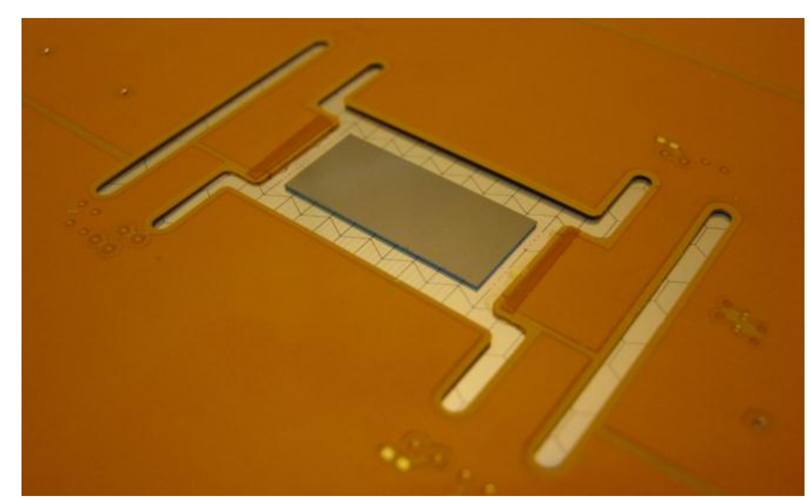
- Hits are time-stamped to individual bunch crossings, reducing background susceptibility
- Digitization and readout occur between bunch trains, minimizing potential for pickup of digital activity on analog front end.

Along with an enormous repertoire of built-in capabilities and flexibility of configuration, KPiX may be bump-bonded directly to sensors

UBM/bumping/bonding by IZM

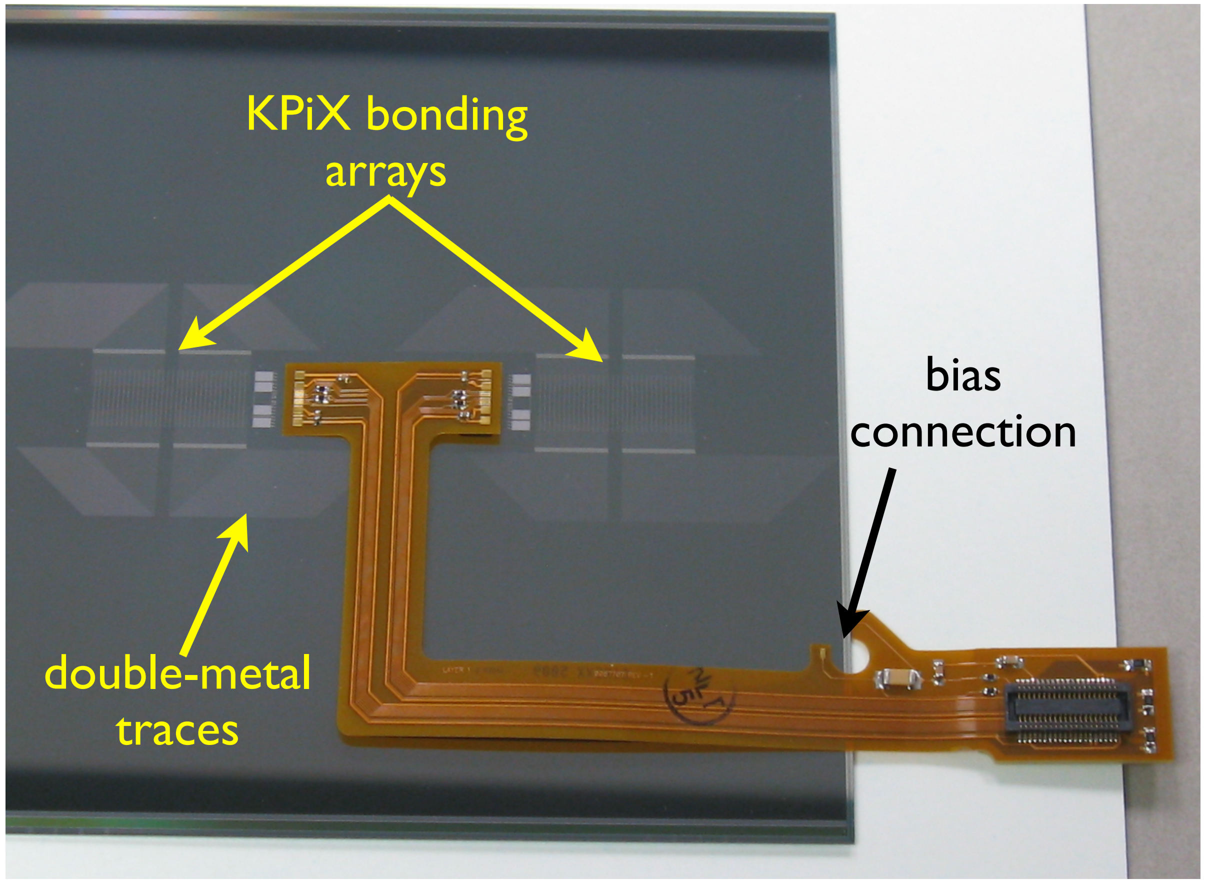


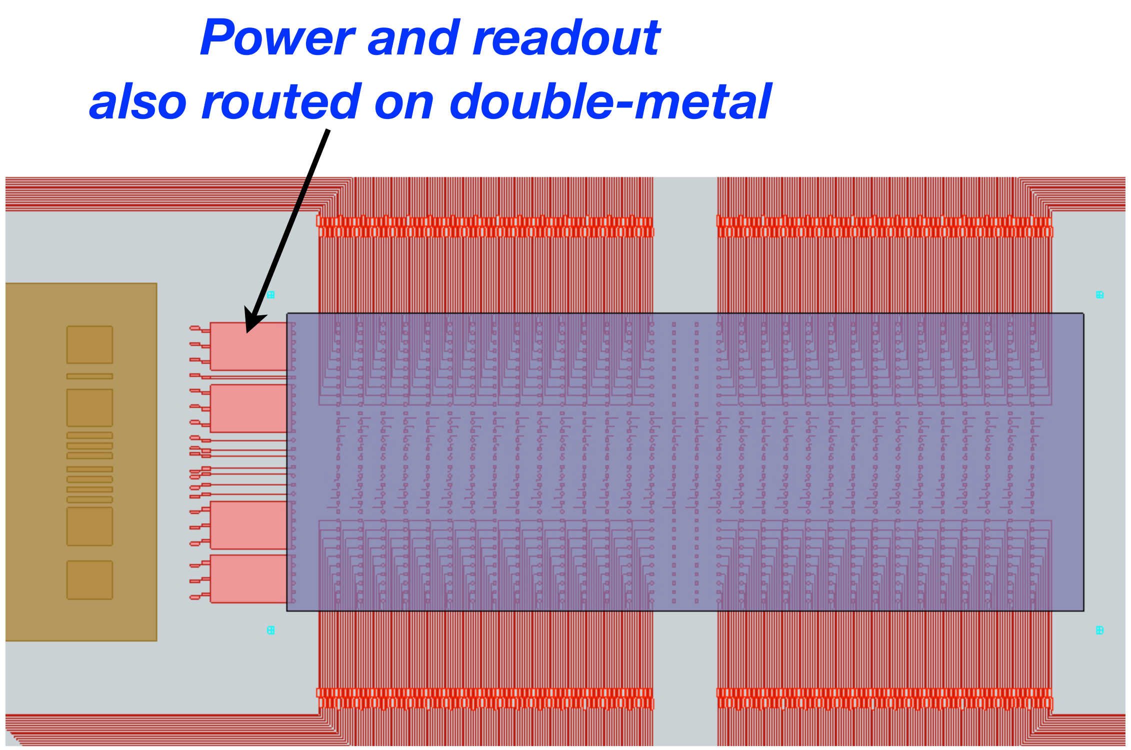
bonded to ECal sensor



# SiD Tracker Module Design

- Two bump-bonded KPiX ASICs with double-metal readout: *no hybrid circuit board!*
- Single-sensor modules ensure low capacitance ⇒ high signal/noise
  - negligible single-hit inefficiency reduces reliance upon redundancy in layout
  - excellent single-hit resolution provides best possible high-$p_T$ resolution
  - per-sensor occupancy from physics+noise is small: allows use of single-sided ($r$-$\varphi$ only) modules in barrel without compromising pattern recognition

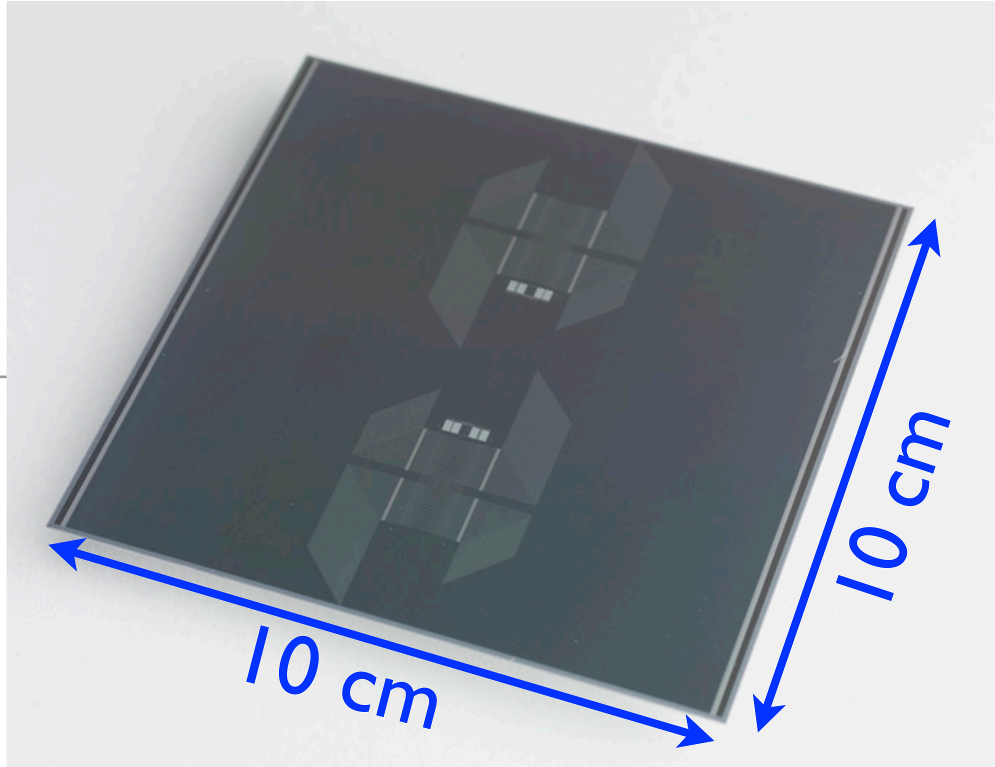


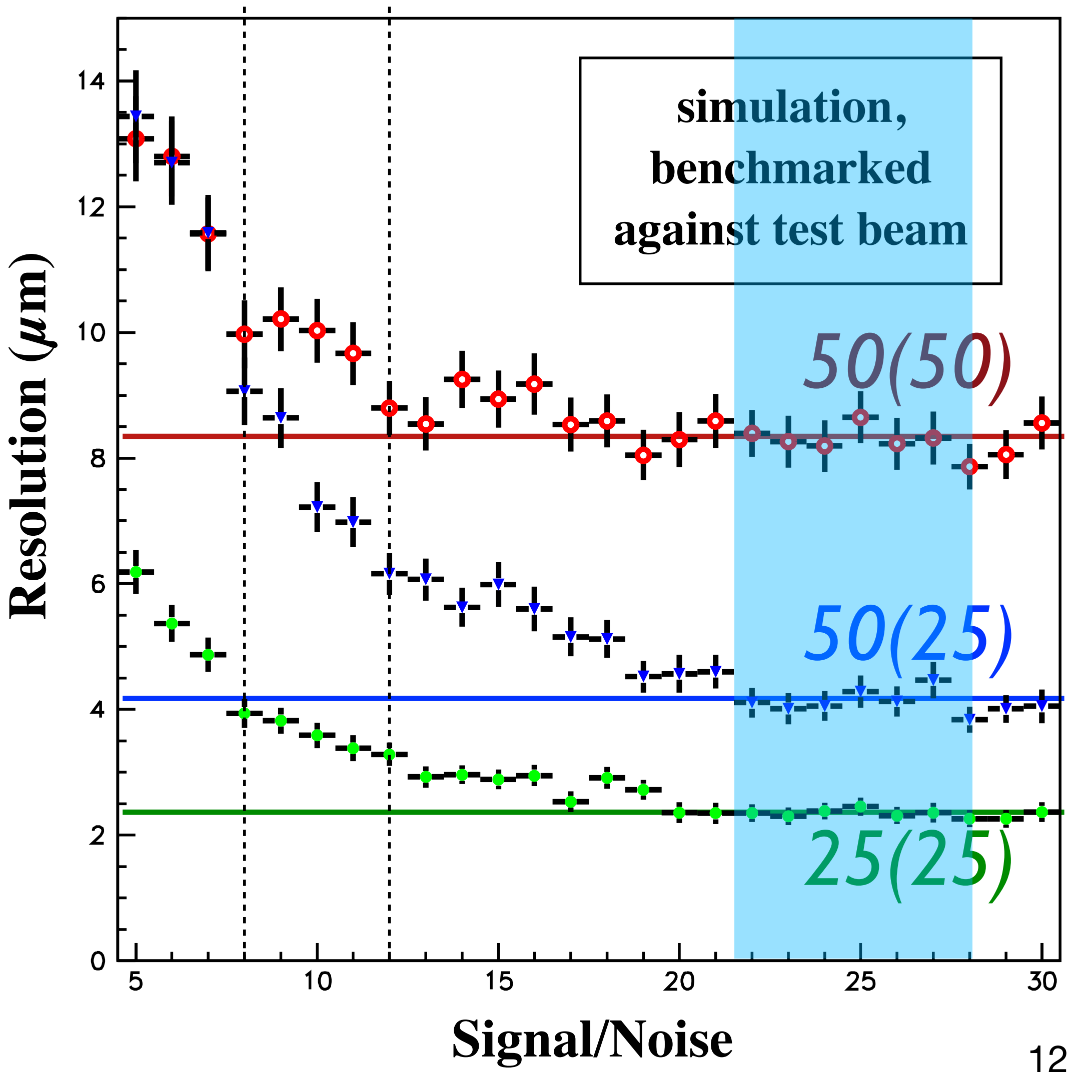
# Thinned Sensors?

*The last place to pare down material*

- High S/N is valuable!
  - efficiency
  - resolution
  - purity (rate of noise hits)
- With 14,000 sensors; keep it simple, cheap
  - 300 $\mu$m, single-sided, p$^+$ in n-bulk, <100> Si
  - Largest square sensor from 6" wafer
- Want best resolution for channel count
  - 25 micron sense pitch with 50 $\mu$m readout ⇒ 4-5 $\mu$m single-hit resolution at high S/N.

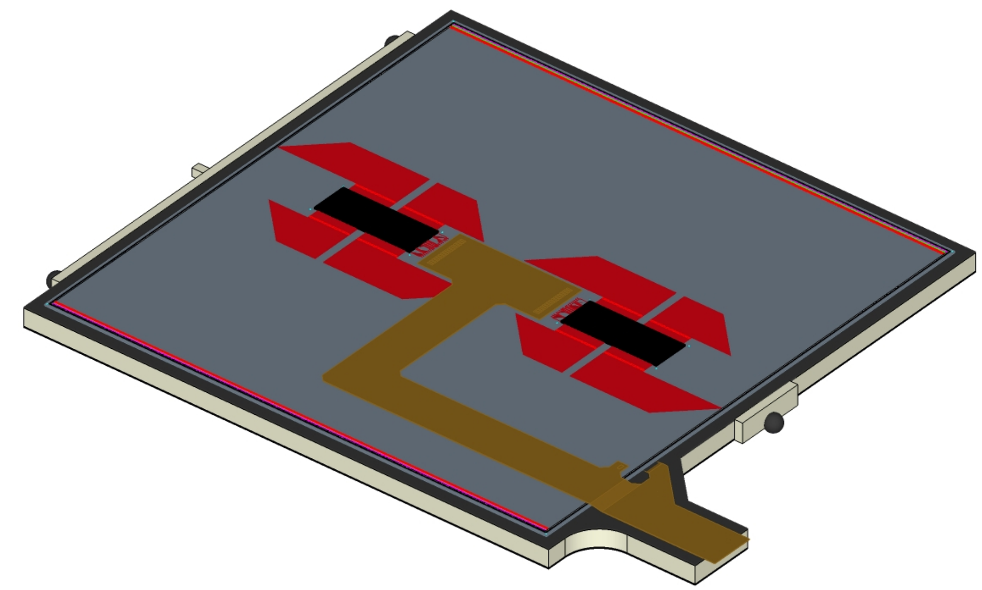



*resolution vs. readout(sense) pitch* (μm)

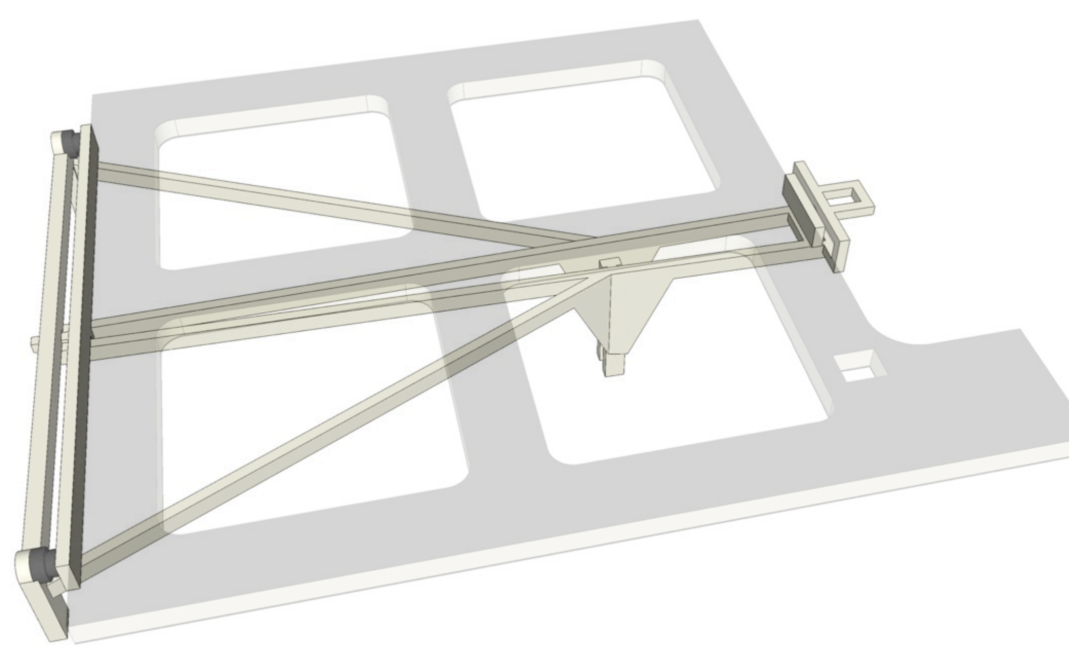


# Minimizing Support Material

*Emphasis on mass-producibility, ease of assembly, handling: conservative w.r.t. material*



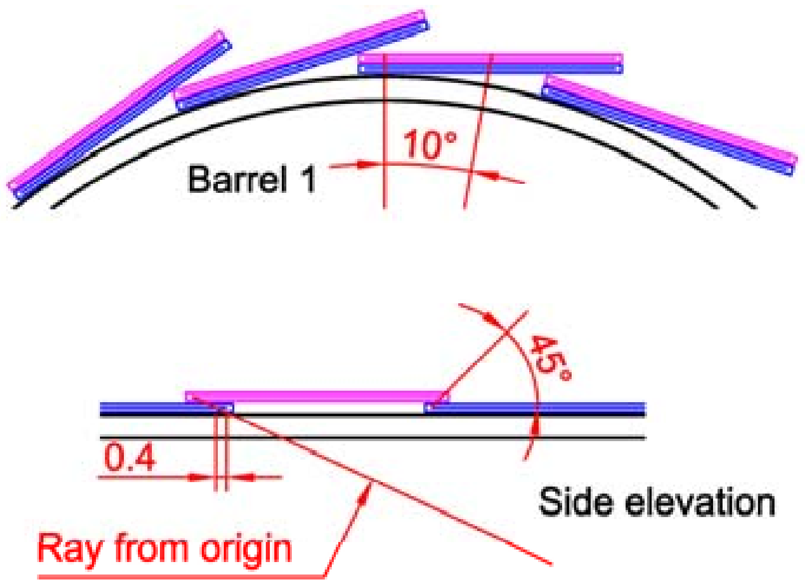
- Holds silicon flat; provides stable, repeatable mount
- Double-sided with addition of silicon on back side: forward concept differs only in shape
- Pair of high-modulus carbon-fiber composite sheets around Rohacell 31 foam
- 0.10% $X_0$ average w/o mounting hardware
- Carbon-fiber reinforced PEEK mounting clips glue to large-scale supports

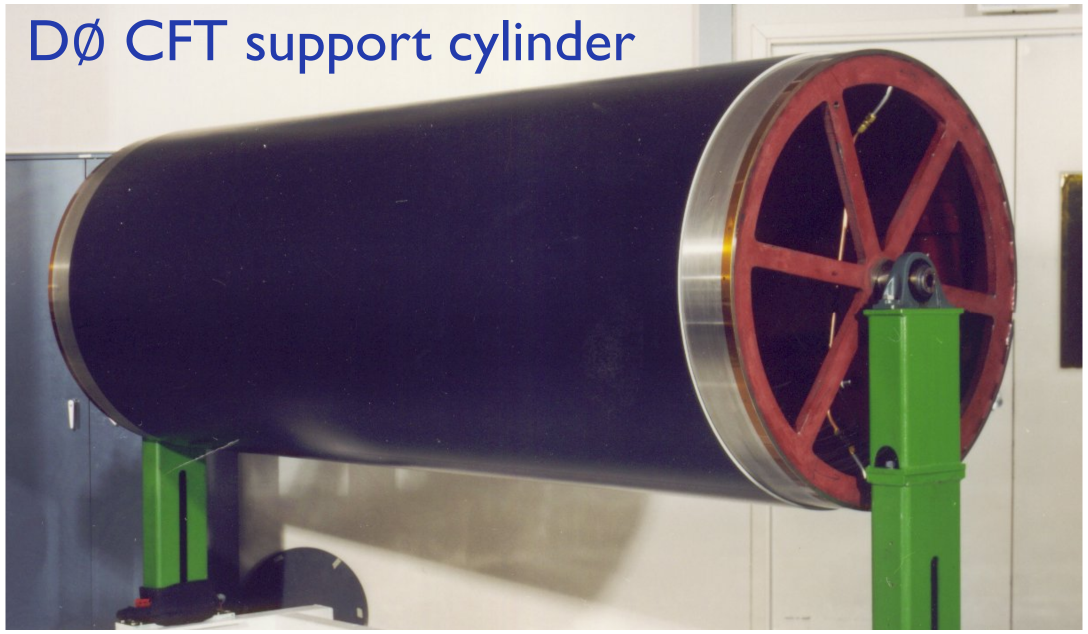


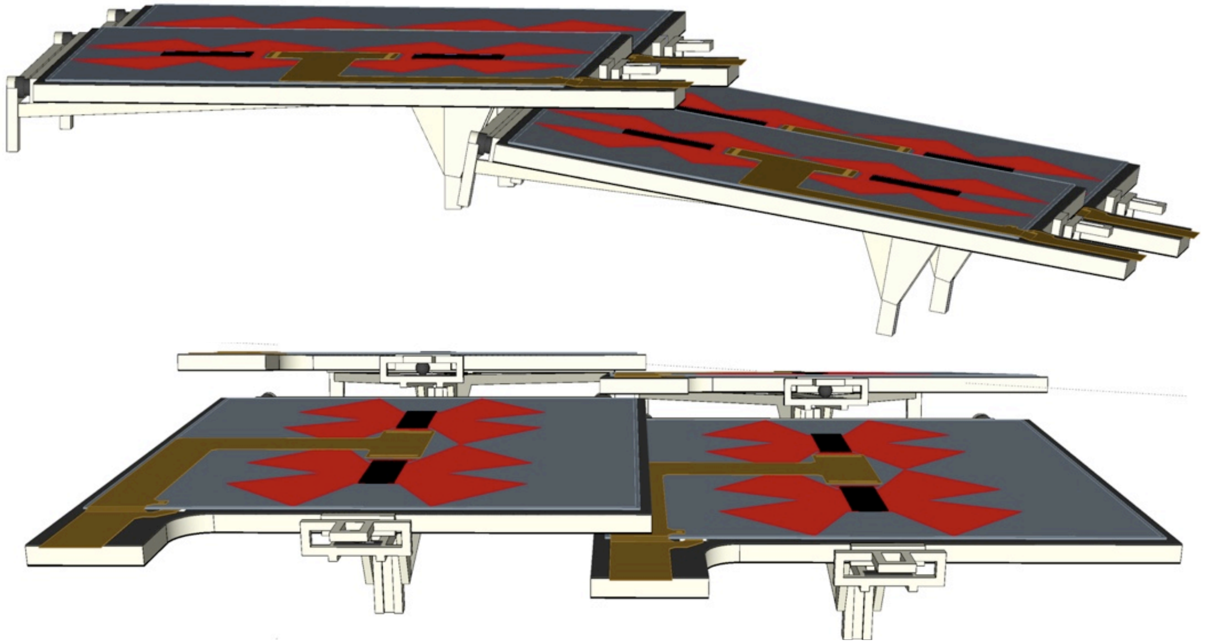
# Minimizing Support Material

*Modules tile CF/Rohacell cylinders (like DØ, ATLAS): minimizes material for given rigidity*

- Module tilt corrects for Lorentz drift
- FEA results: 7 μm static deflection, fully loaded
- 0.3% $X_0$ for solid cylinders: could be ~50% void
- Endcap disks are of similar construction

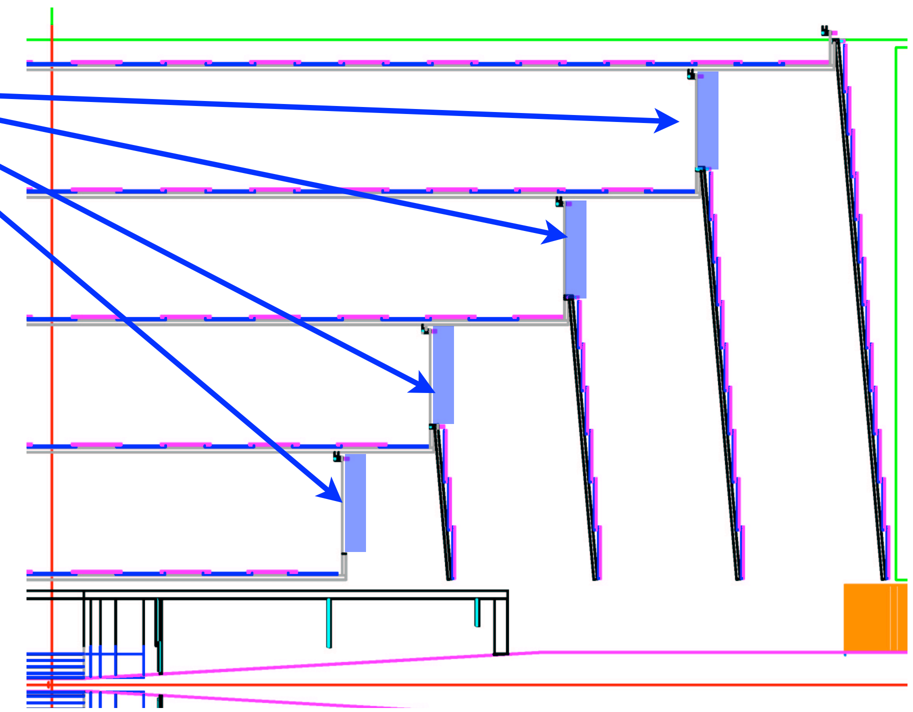


# Power and Readout Services

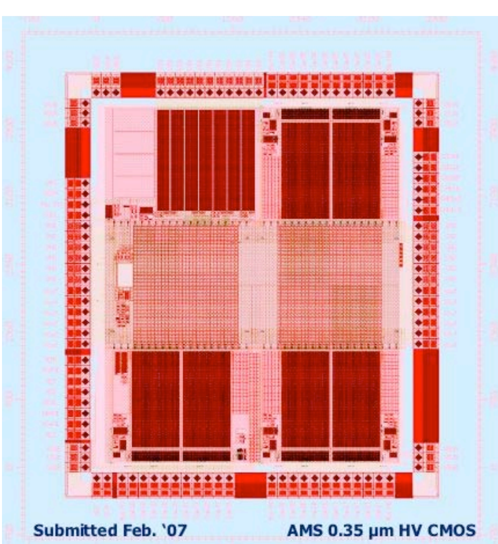
*Spoked support rings host power and data concentrators*

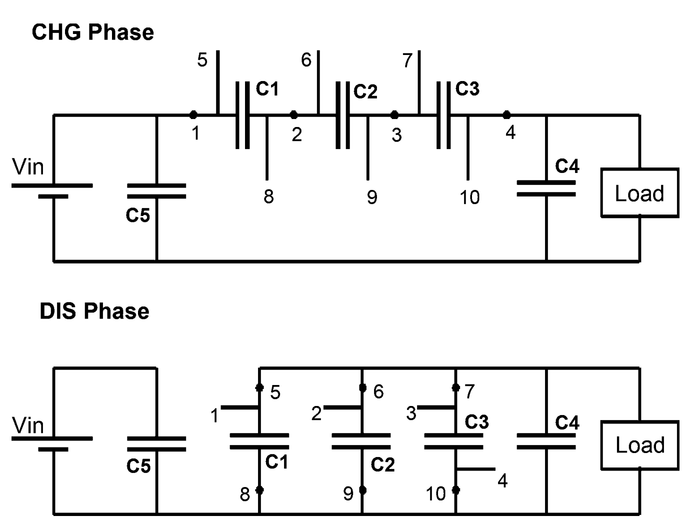


- Commercial optical transceivers work fine here for data
- DC/DC conversion reduces cable plant for power, but... peak current for tracker during pulses is ~10000 A!
  - Store charge for each pulse (~10 mC) locally on capacitors
  - Carefully balance Lorentz forces in remaining cables

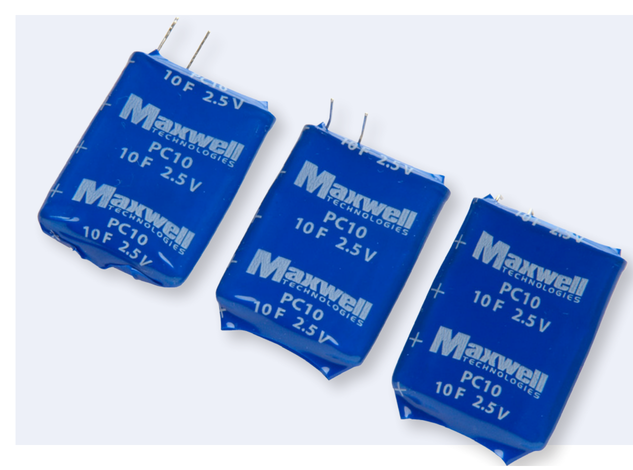
*Technology here is rapidly evolving.*

Example: DC/DC charge-pump ASIC (LBNL)




Example: Maxwell PC10 Ultracapacitor




$$C = 10\ F$$
$$V_{\text{max}} = 2.5\ V$$
$$E_{\text{max}} = 32\ W \cdot \text{sec}$$
$$I_{\text{max}} = 4.5\ A$$
$$\text{Mass} = 6.8\ g$$

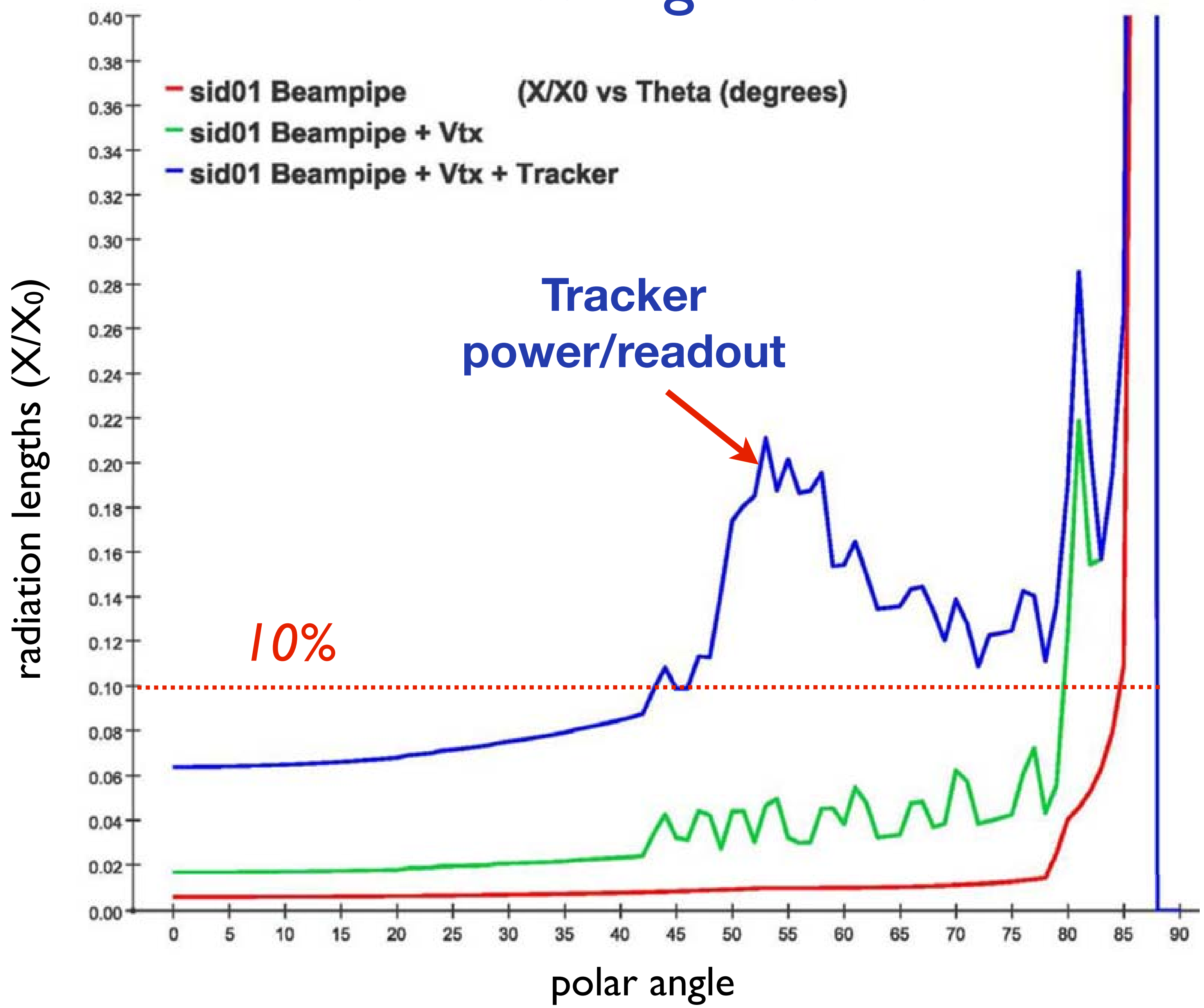
only 1 mV droop during train but adds 0.3% $X_0$ / layer

# SiD Simulation

*Scrupulous accounting of material is critical!*

- Included in GEANT: sensors, chips, cables, connectors, bypassing, glue, module supports, module mounts, overlaps, power distribution boards, DAQ
- Goal 0.8%/layer, currently 0.92%/layer
- *Simulation includes overlaid backgrounds*

## SiD Tracking Material



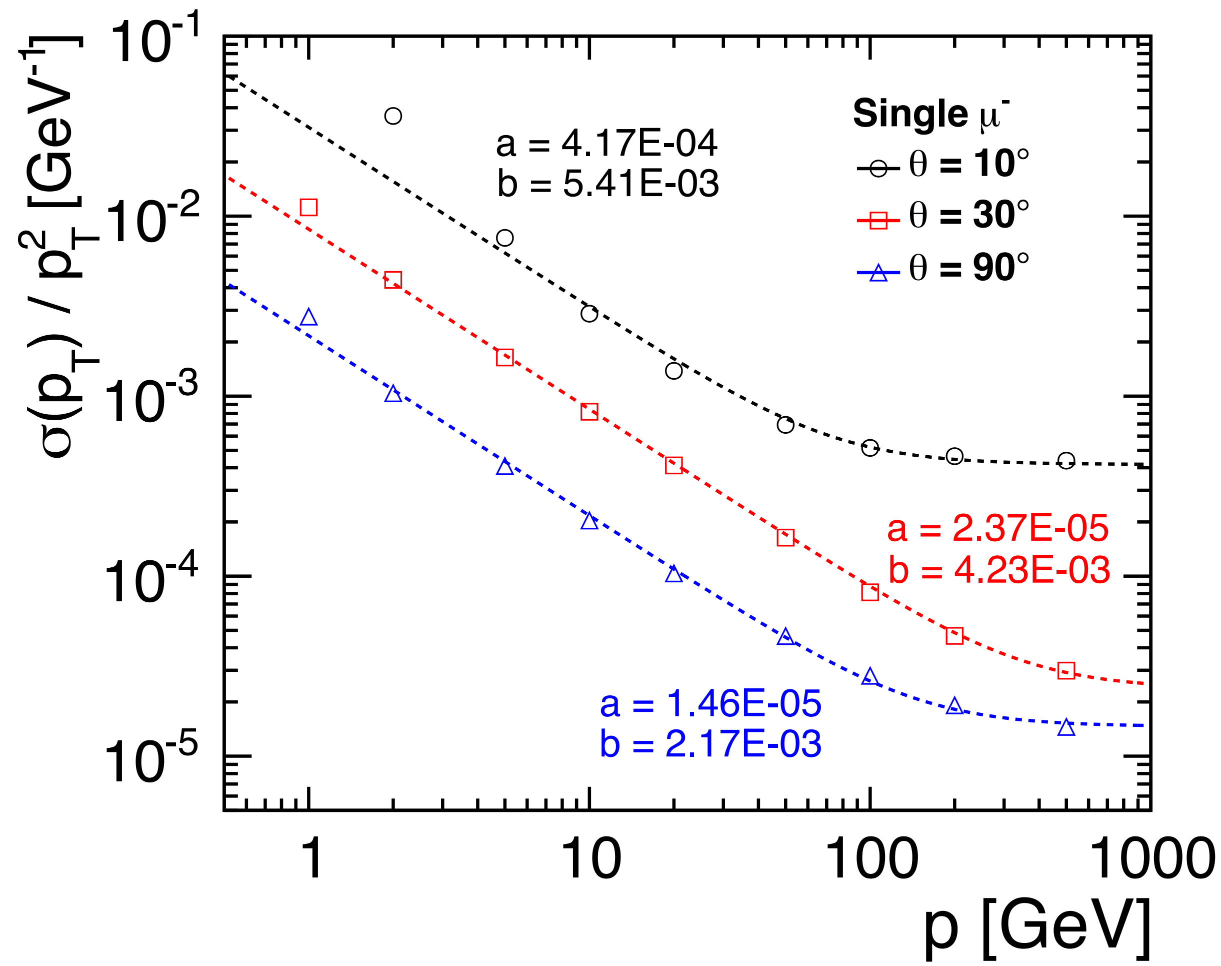
# Momentum Resolution

*High $p_T$ resolution is excellent:*

- 1 TeV tracks to 15-25 GeV for $\theta$<30°
- Degrades significantly as $\theta \to 0°$
- Multiple scattering still dominates below ~100 GeV

*Low $p_T$ resolution is excellent:*

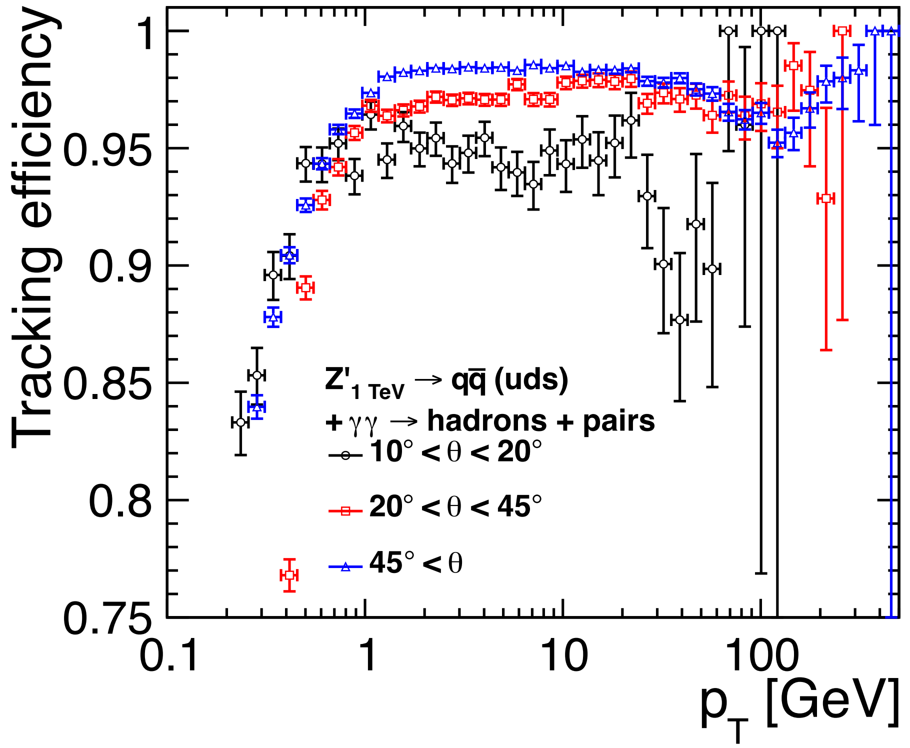
- 10 GeV tracks measured to 20-200 MeV
- 1 GeV measured to 2-20 MeV
- Would still benefit from less material!

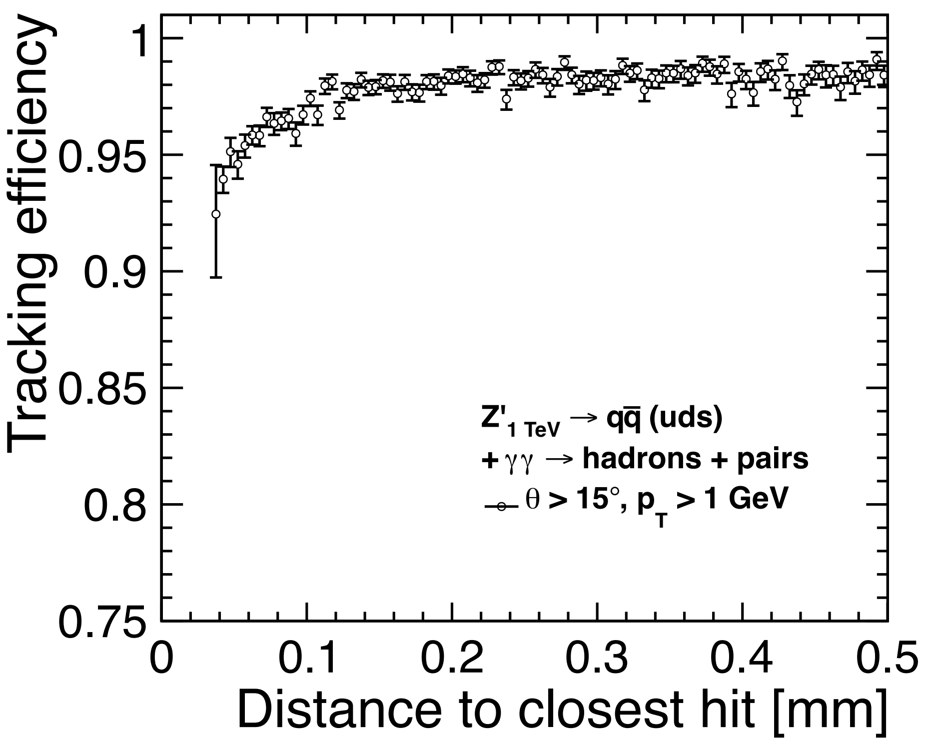


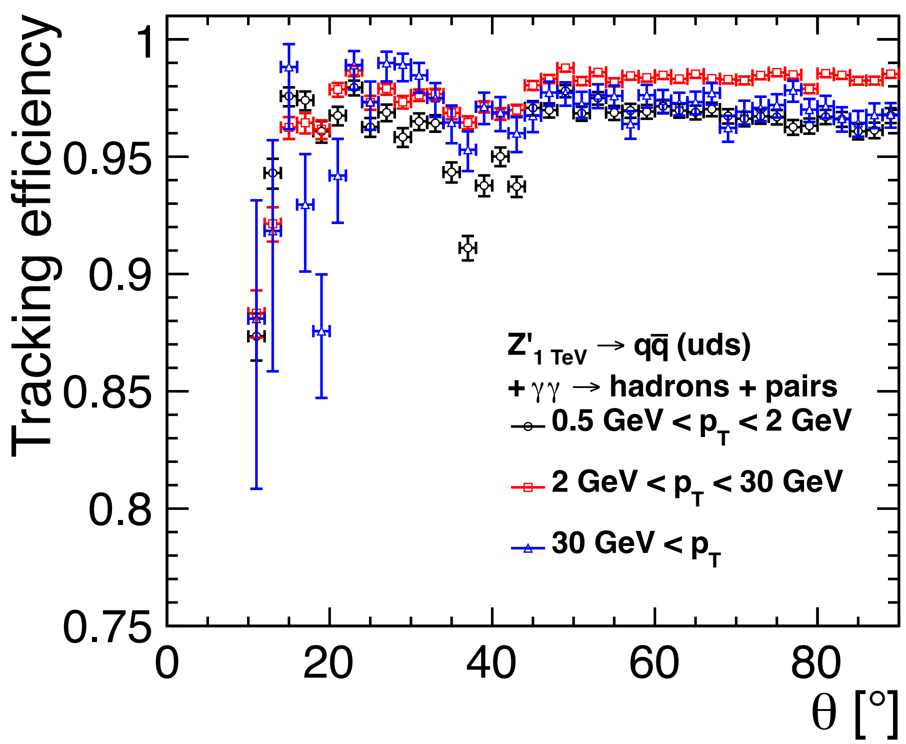

$$\sigma(p_\mathrm{T})/p_\mathrm{T}^2 = a \oplus \frac{b}{p\sin\theta}$$

# Tracking Efficiency $Z'_{1\ \mathrm{TeV}} \rightarrow q\bar{q}\ (uds)$

- Efficiency is excellent for $p_T$ > 1 GeV, reasonably good down to 200 MeV.
- Performance extends to forward region: small modules, high S/N minimize ghost hits
- $p_T$ < 200 MeV (VTX-only) is very difficult, especially in presence of full backgrounds

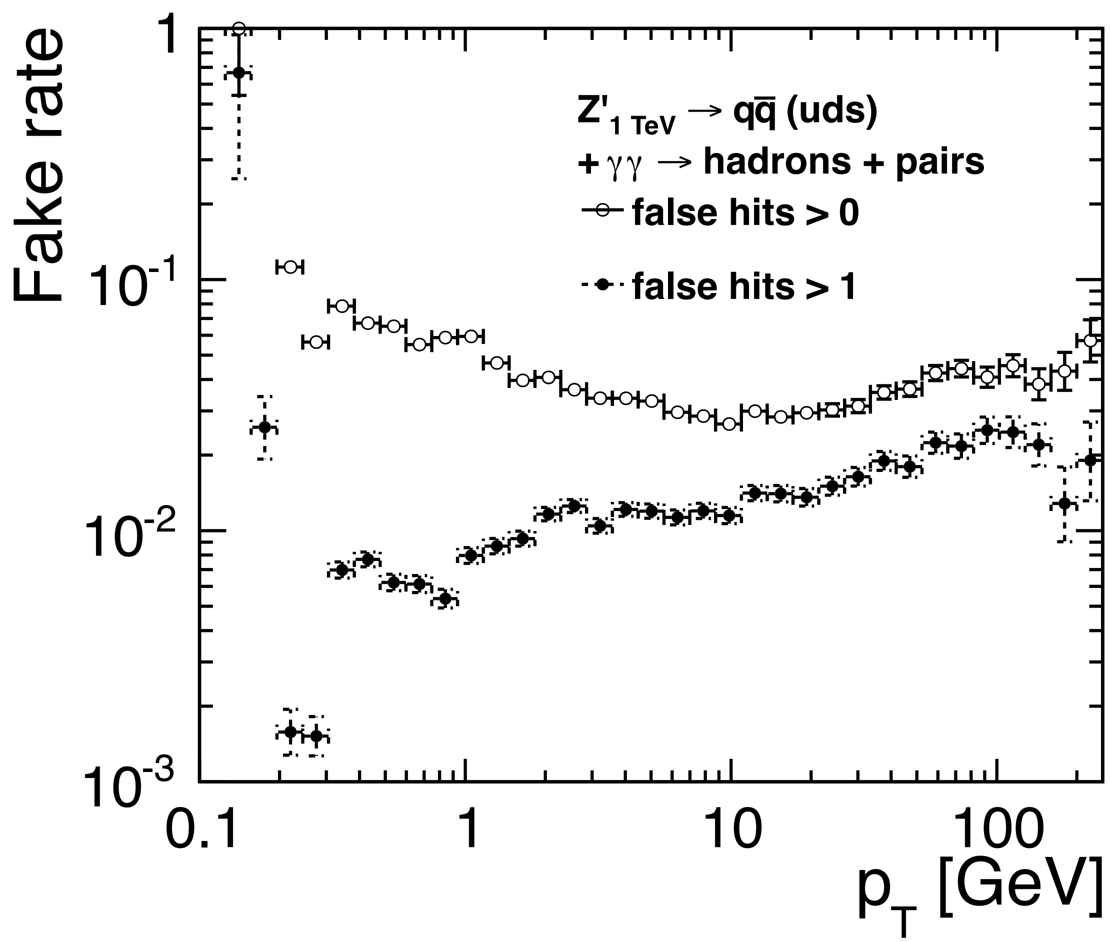


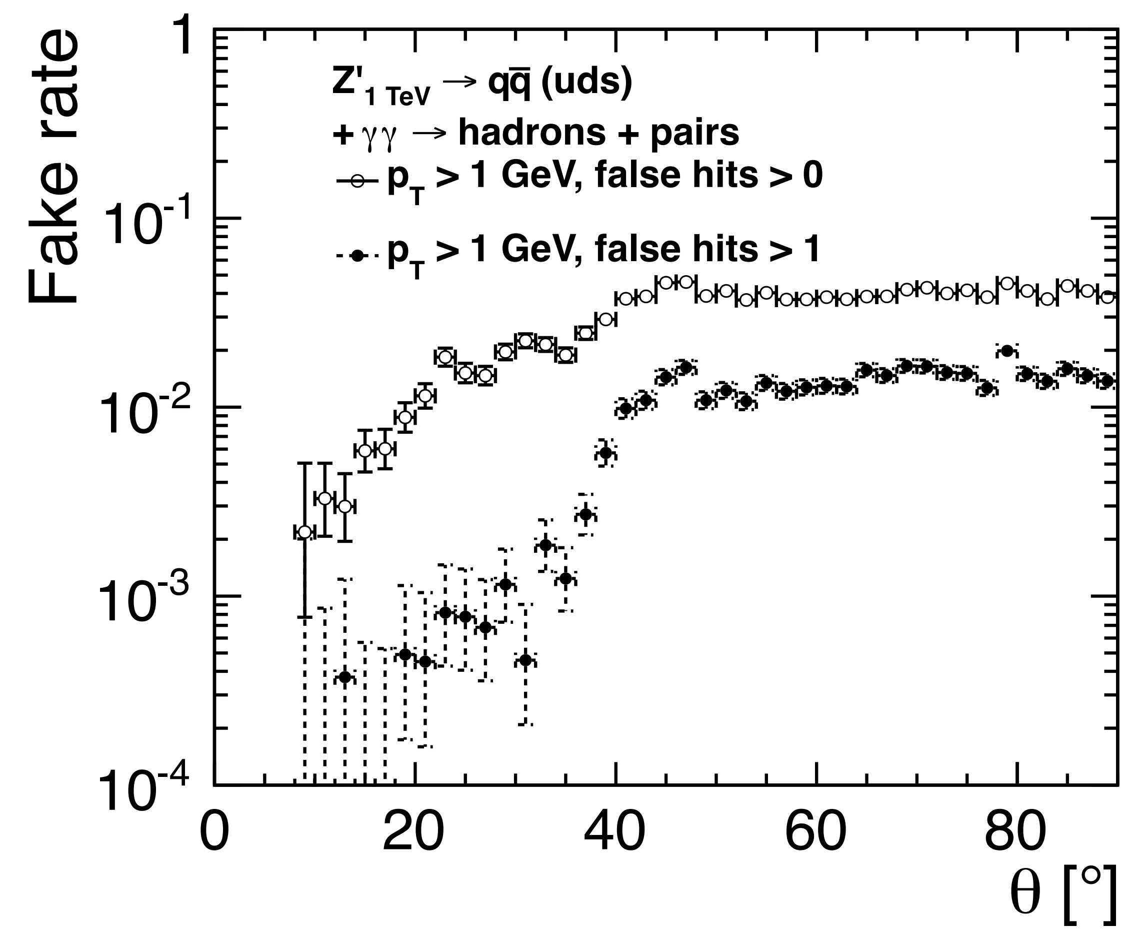



# Tracking Purity $Z'_{1\ \text{TeV}} \rightarrow q\bar{q}\ (uds)$

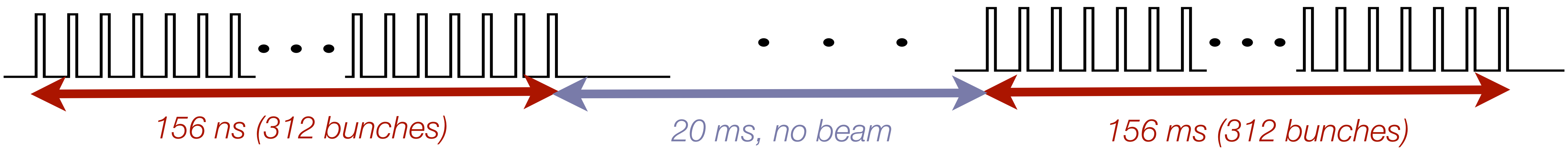
## Rates of incorrectly assigned hits on tracks



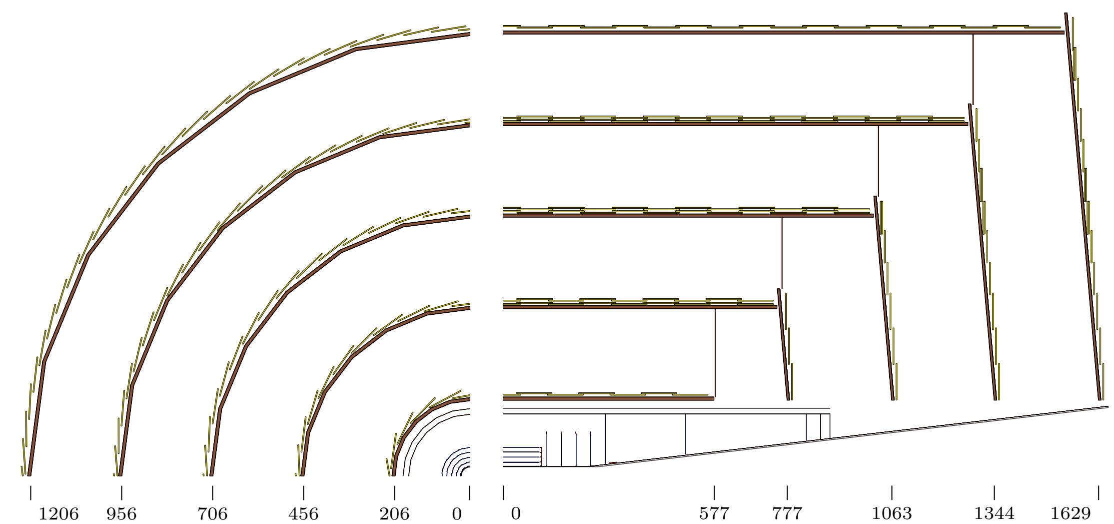

- Rate of tracks with incorrect hits is low for $p_T$ > 200 MeV
- Stereo information not necessary in barrel, but helpful forward

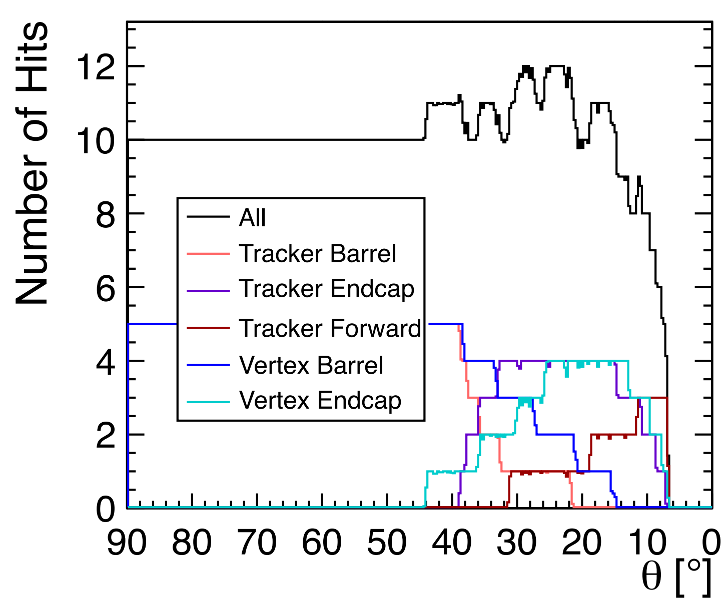
# How Does the Solution Differ for CLIC?

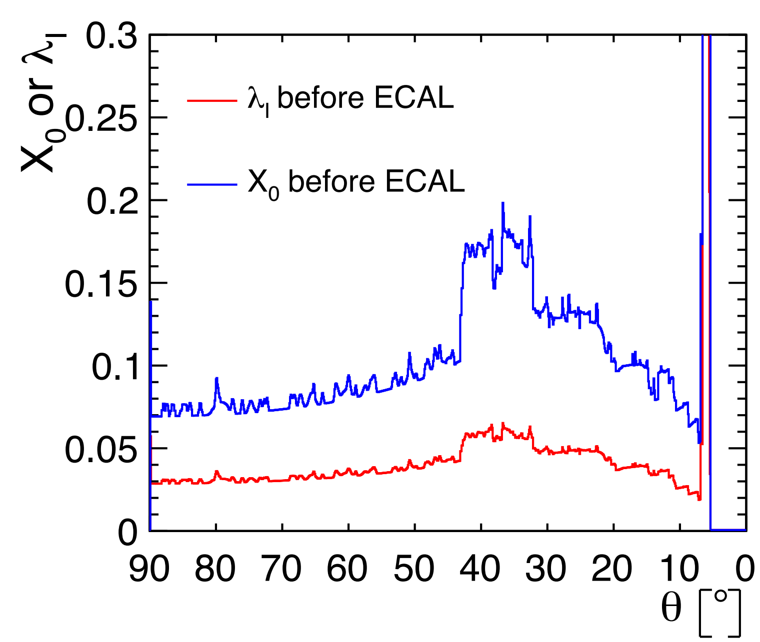



*"CLIC-SiD" is nearly identical to SiD:*

- More aggressive timing for pulsed power
- Believe KPiX scales to 10 ns hit timing (20 bunches)
- Believe a similar power envelope is achievable (still air cooled)
- Storing charge for bunch train at module is easier, if anything.



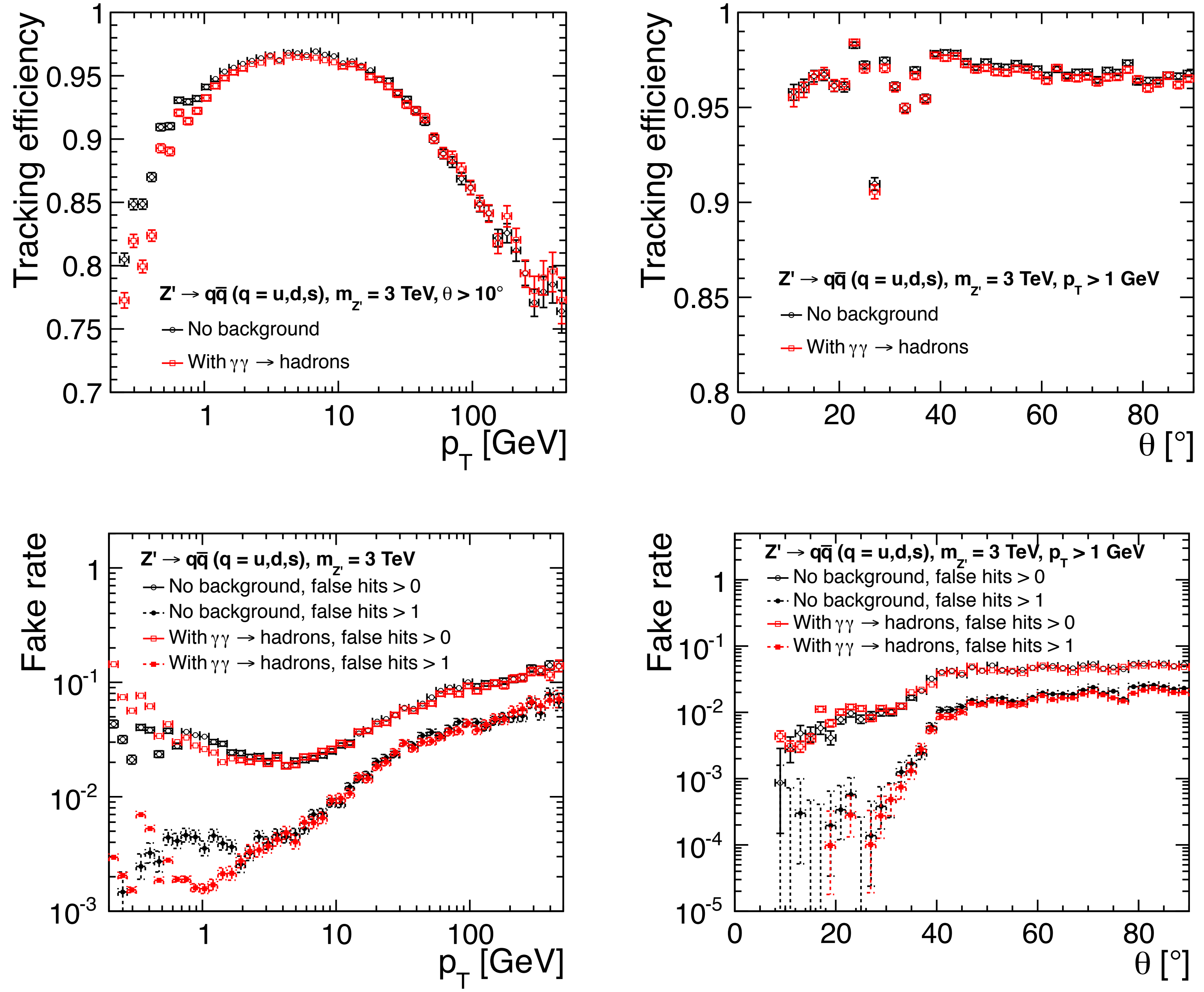



# CLIC-SiD Efficiency/Purity

$Z'_{3\ \mathrm{TeV}} \rightarrow q\bar{q}\ (uds)$

- Efficiency and purity are similar to SiD under same conditions
- Most challenging processes at 3 TeV definitely stretch the limits of the SiD design
- Background immunity demonstrates safety factor in time stamping assumptions



# Pixel Trackers?

*Some serious challenges to overcome...*

- Power:
  - pixels must be small in phi for high-$p_T$ resolution, small in z to improve tracking performance
  - Small pixels × large area = huge channel counts
  - ➡ $P_{TOT}$ = 100 kW at 0.1 W/cm$^2$ = an LHC-sized power and cooling problem (CMS is 30 kW)
- Assembly:
  - Full tracker requires 250000 4 cm$^2$ sensors
  - ➡ Even modest processing on each part incurs costs that dwarf cost of sensors themselves.

*... but in N years many more things will be possible!*

STAR HFT "ultimate"

4 cm$^2$ @ 0.17 W/cm$^2$

# Summary

- The fact that silicon systems have either been low-mass (e.g. B-factory vertex detectors) or large (hadron colliders) does not mean that large-scale, low-mass silicon tracking detectors cannot be built
- The experimental environment at energy frontier e+e- colliders lends itself particularly well to low-mass silicon tracking.
- The outer silicon tracker of the SiD detector concept embodies a set of solutions for which most of the technical challenges have already been overcome
- We hope to have the problem of needing to complete remaining R&D on an aggressive timescale.
- While the baseline uses "mature" silicon technologies, commercial process development fuels rapid changes that will open up additional options in the future.