ROC inefficiency at low threshold?

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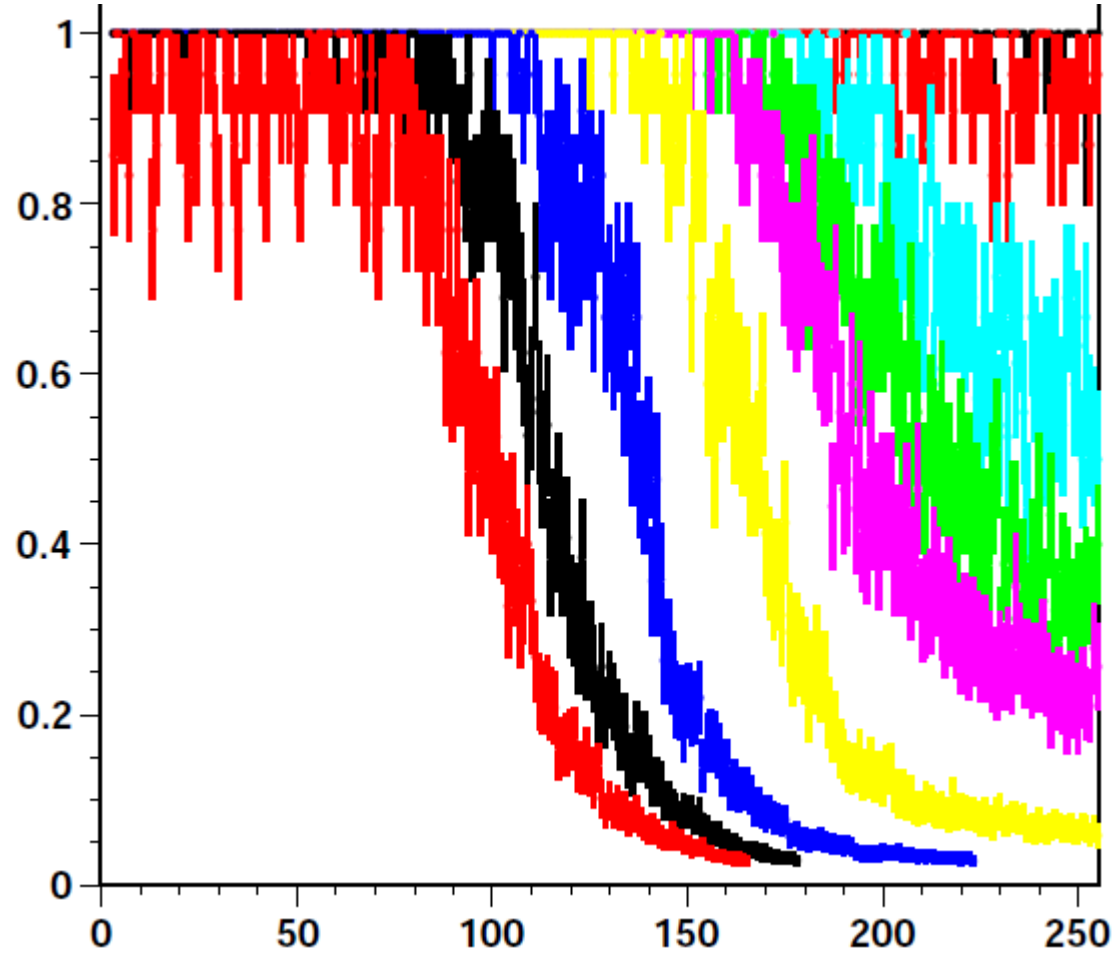
Phase I pixel upgrade, 5.10.2012



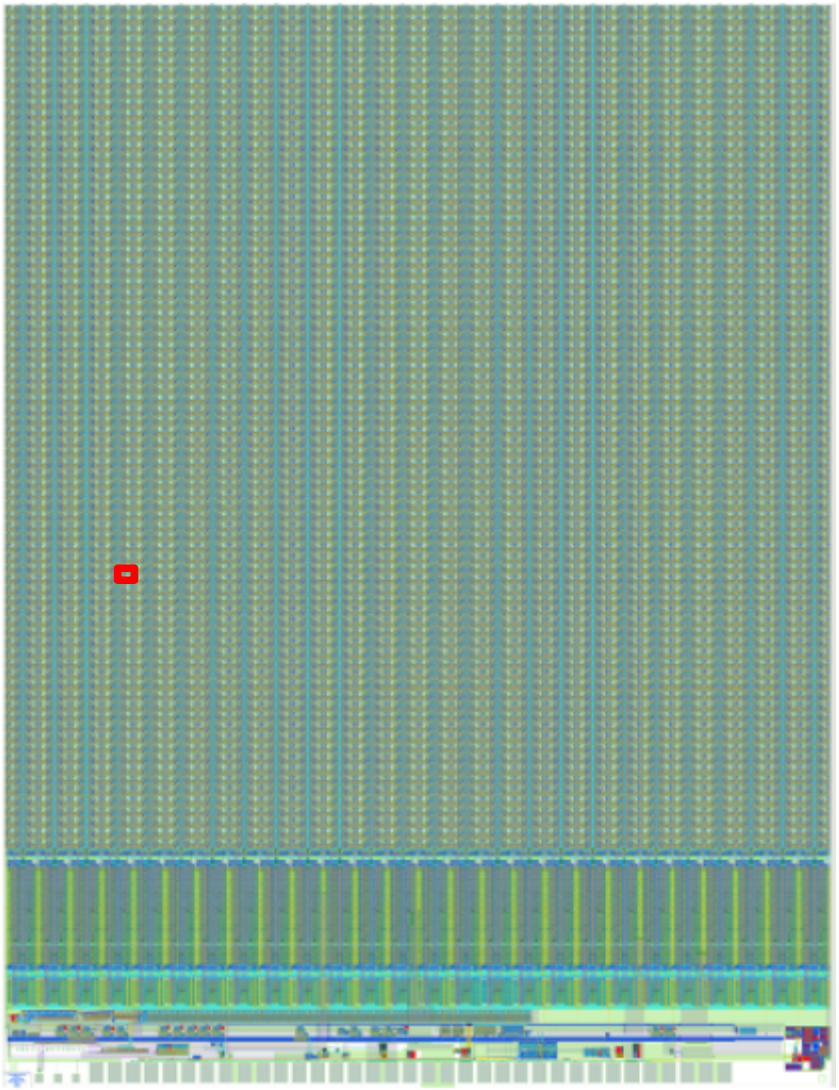
- lowest thresholds
- ROC operation:
  - lab vs beam
- test pulse efficiency
- beam test maps

The problem

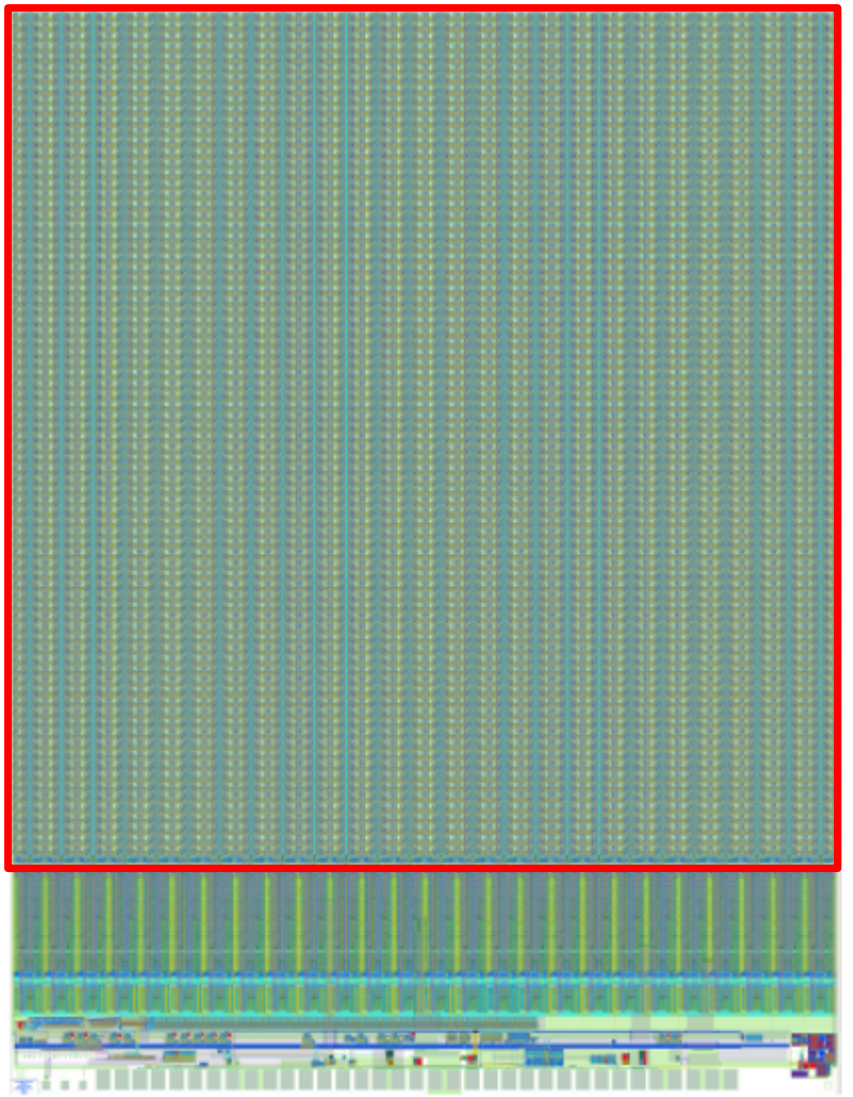
- In the lab:
  - activate ('arm') one pixel at a time, pulse, and read out
  - all other 4159 pixels are masked out
  - setting of very low thresholds (800 e) is possible
- In the test beam:
  - all 4160 are enabled
  - chip becomes noisy and inefficient for thresholds below 1.8 ke (new psi46dig) or 2.9 ke (old psi46v2)
- Why?
  - what's going on?
- The approach:
  - activate all pixels in lab tests

psi46dig

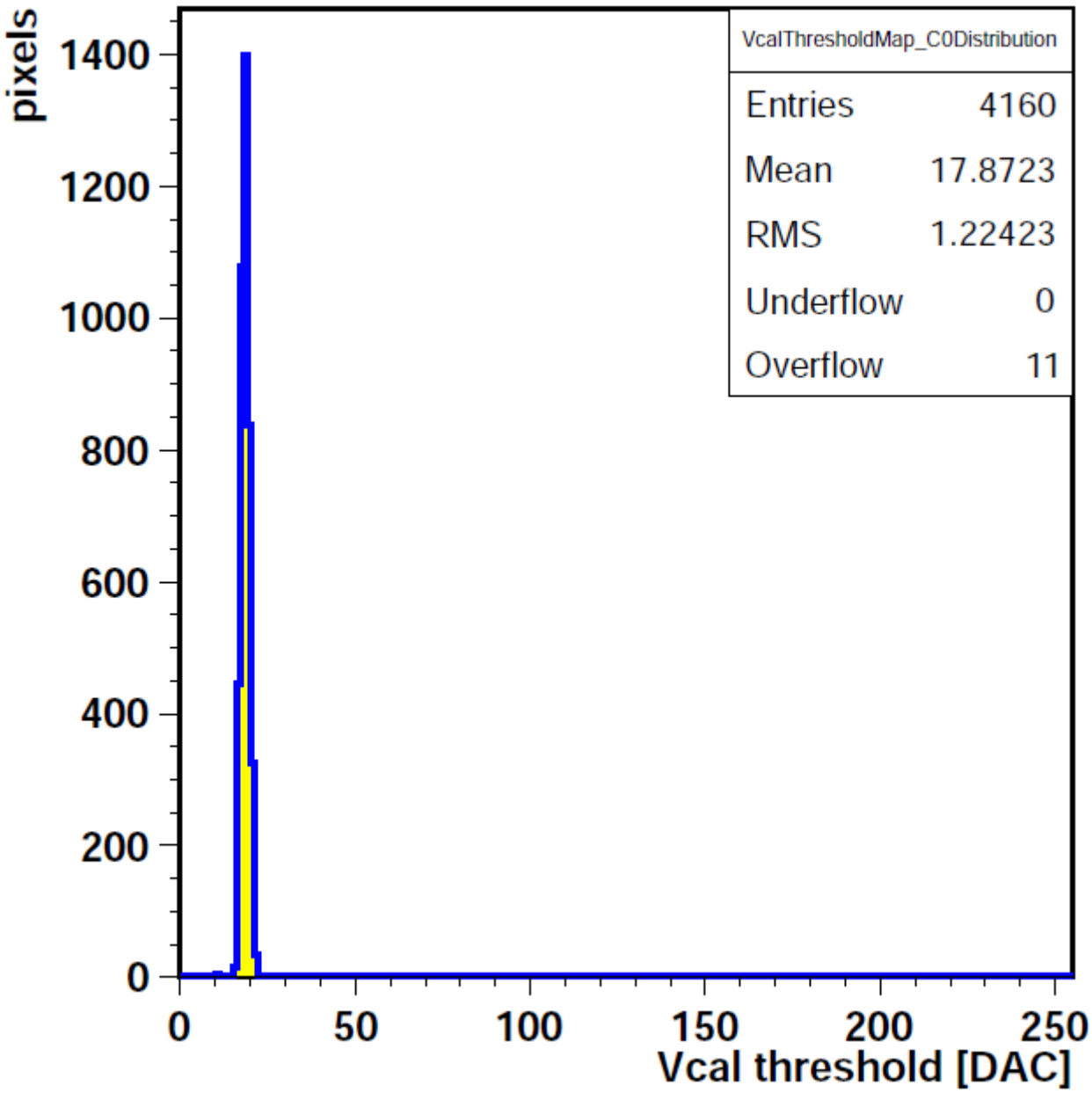
lab: one pixel active



beam: all pixels active

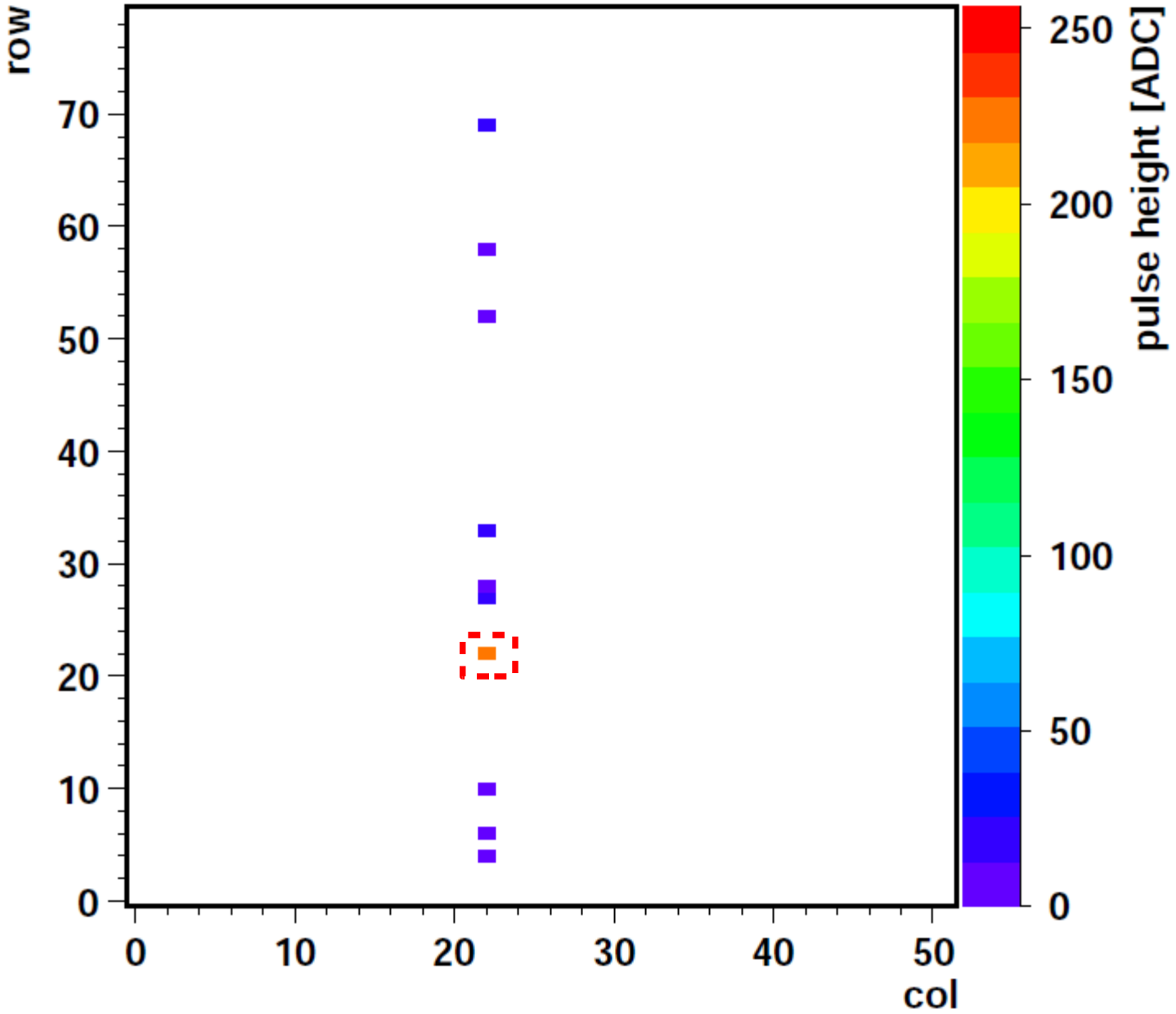


thresholds after trimming



- run pretest:
  - analog current 35 mA
- trim:
  - target Vcal threshold 18 (~900e)
- nice:
  - when activating one pixel at a time...

event display

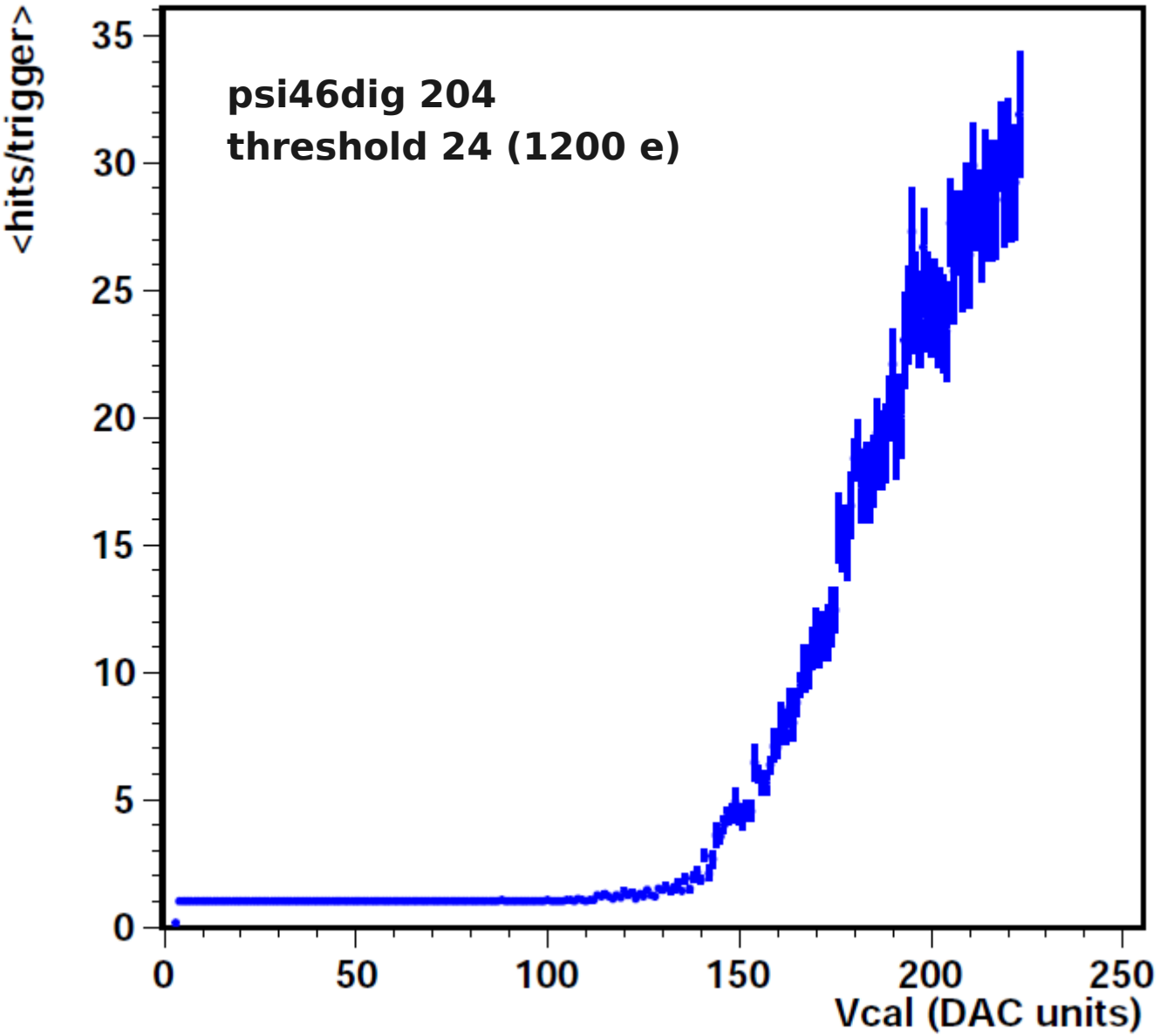


- Digital Chip 204
  - Ia 35 mA
  - trimmed to Vcal threshold 24 (1200 e)
  - high range (CtrlReg 4)
  - **enable all: pixe 0:51 0:79**
  - pulse one: arm 22 22
  - readout out: adc
- **several other pixels in the same column respond.**

Column cross talk?

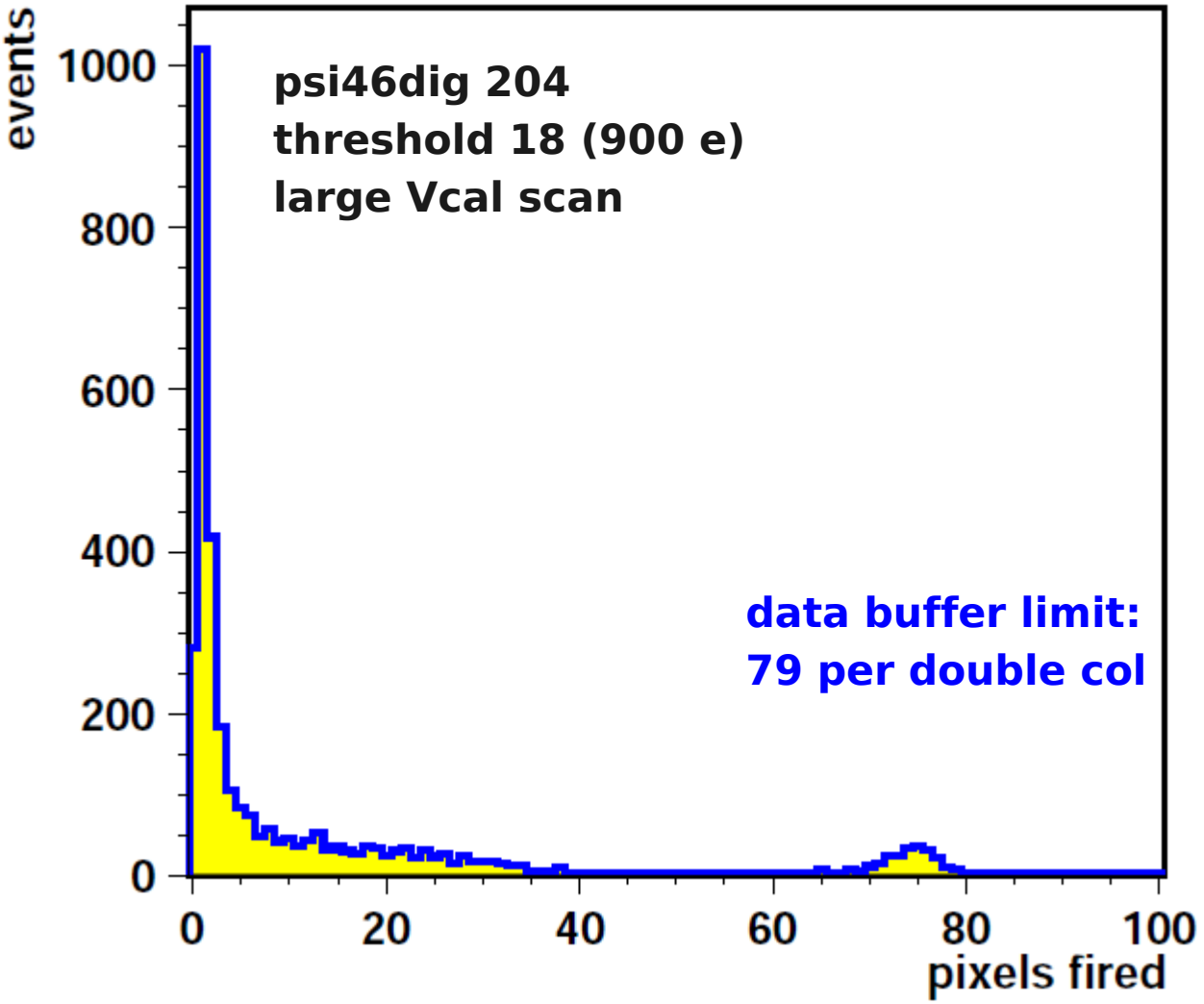
- The effect depends on:
  - amplitude of the test pulse
  - threshold and trim setting
- Data buffer overflow:
  - psi46dig has 80 data buffers per double column
  - data buffer is automatically cleared when full
  - maximum occupancy is 79
  - mean values will be smaller…

Pixel multiplicity vs amplitude



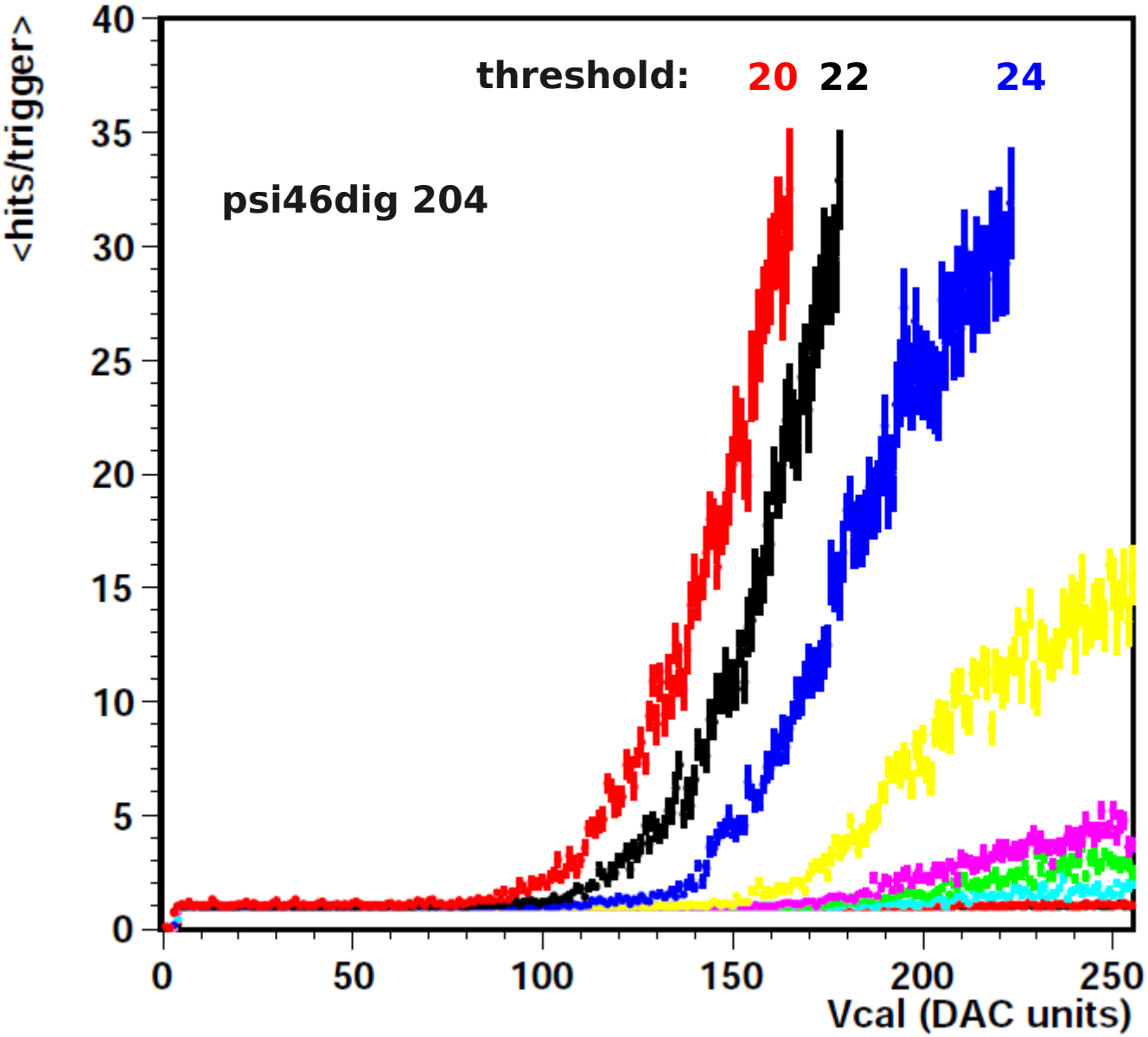
- Digital Chip 204
  - Ia 35 mA
  - trimmed to Vcal threshold 24 (1200 e)
  - high range (CtrlReg 4)
  - **enable all: pixe 0:51 0:79**
  - pulse one: arm 22 22
  - readout out: adc
- **pixel multiplicity increases with test pulse amplitude**
  - **threshold at 135 DAC (2 mip)**

Pixel multiplicity distribution in Vcal scan



- Digital Chip 204
  - Ia 35 mA
  - trimmed to Vcal threshold 18 (900 e)
  - scan Vcal in high range (CtrlReg 4)
  - **enable all: pixe 0:51 0:79**
  - pulse one: arm 22 22
  - readout out: adc
- **pixel multiplicity:**
  - **data buffer limit 79**

Multiplicity vs amplitude and threshold



Vcal threshold:
20 DAC = 1000 e

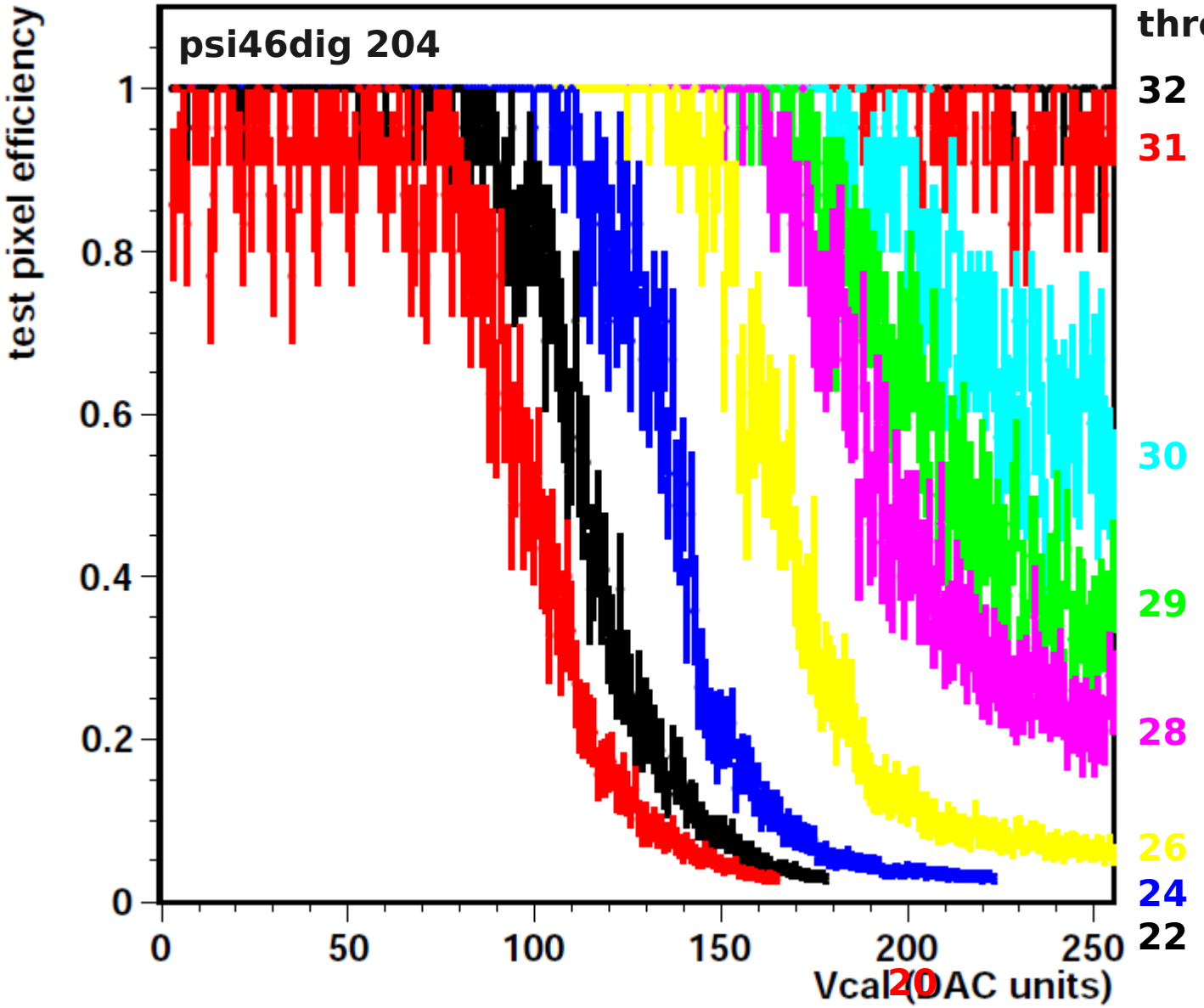
no cross talk for thresholds > 1600 e

Efficiency for test pulses

- Method:
  - Inject a test pulse to a selected pixel
  - read out entire chip
  - check for column and row of the selected pixel
  - repeat 100 times

efficiency = selected pixel responds / test pulse events

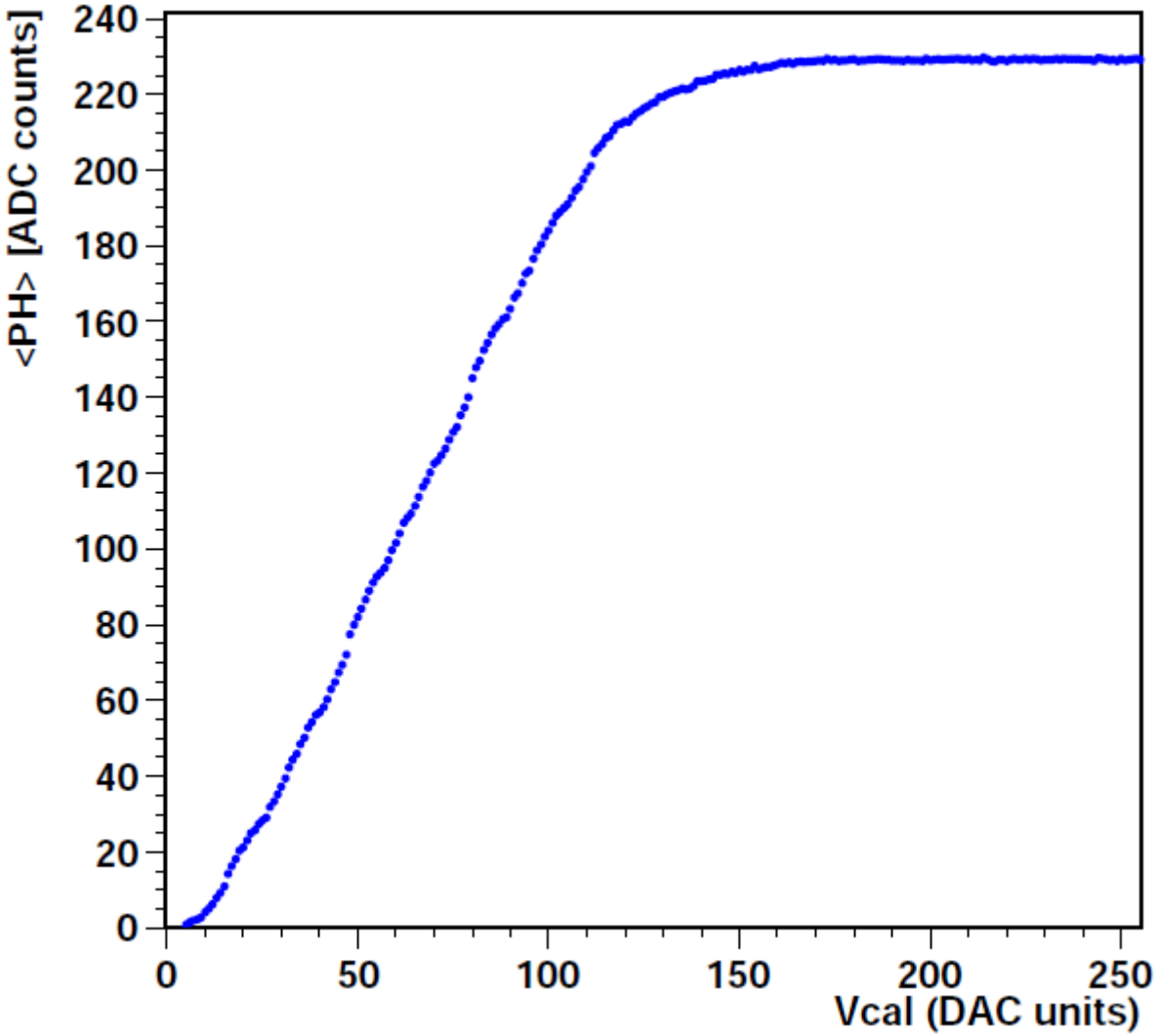
TP efficiency vs amplitude and threshold



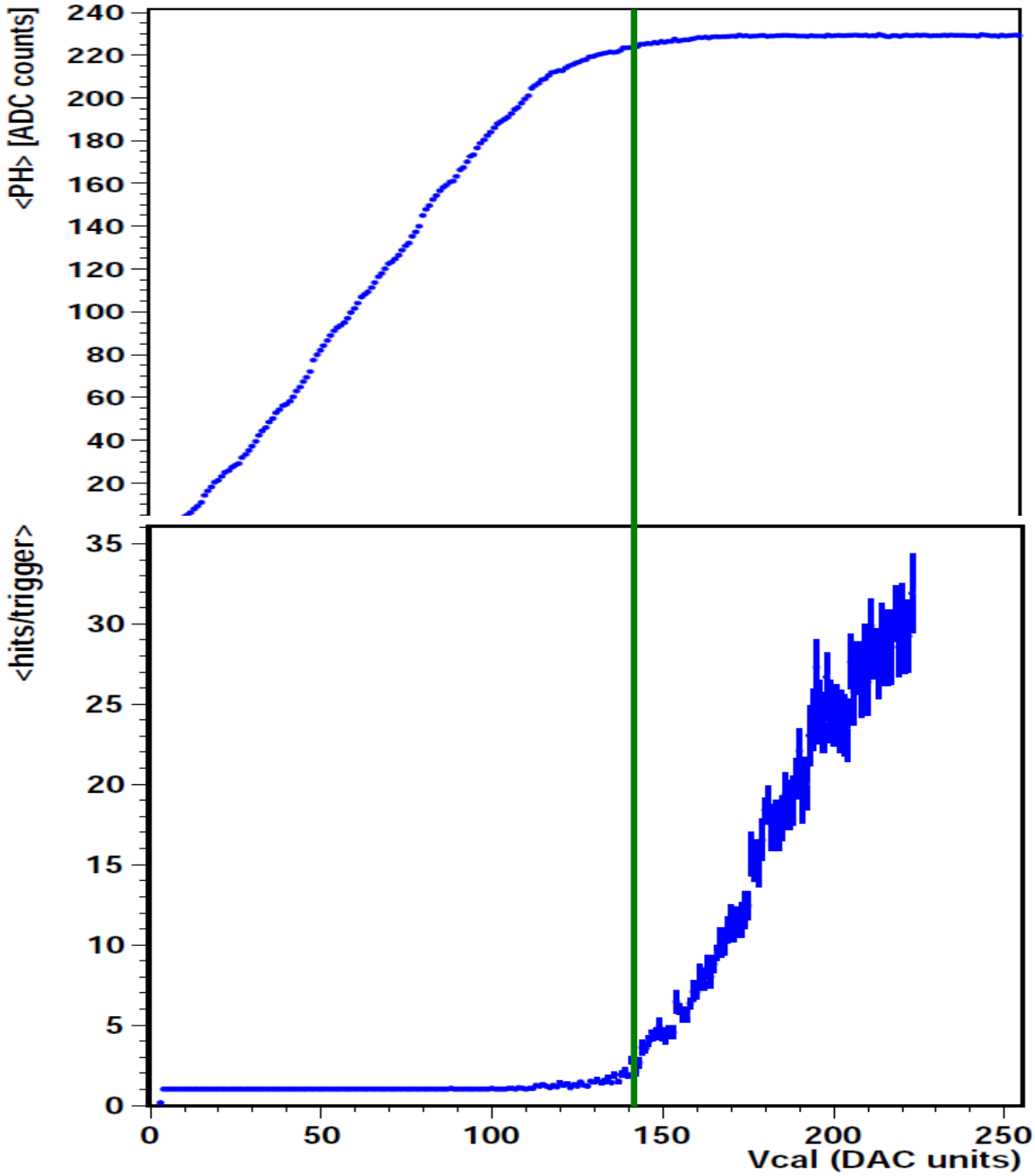
Vcal threshold:
20 DAC = 1000 e

fully efficient for thresholds > 1600 e

Column cross talk induced by injected calibrate pulse or by analog pixel pulse?



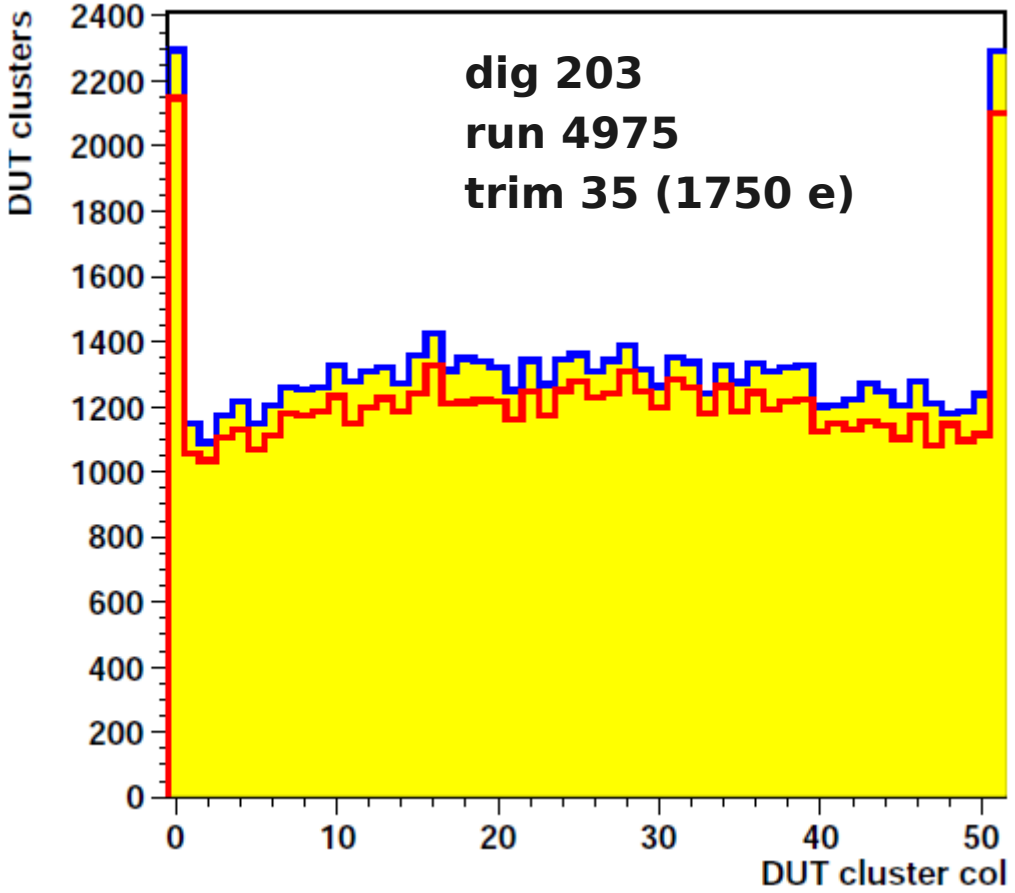
pulse height and noise vs Vcal

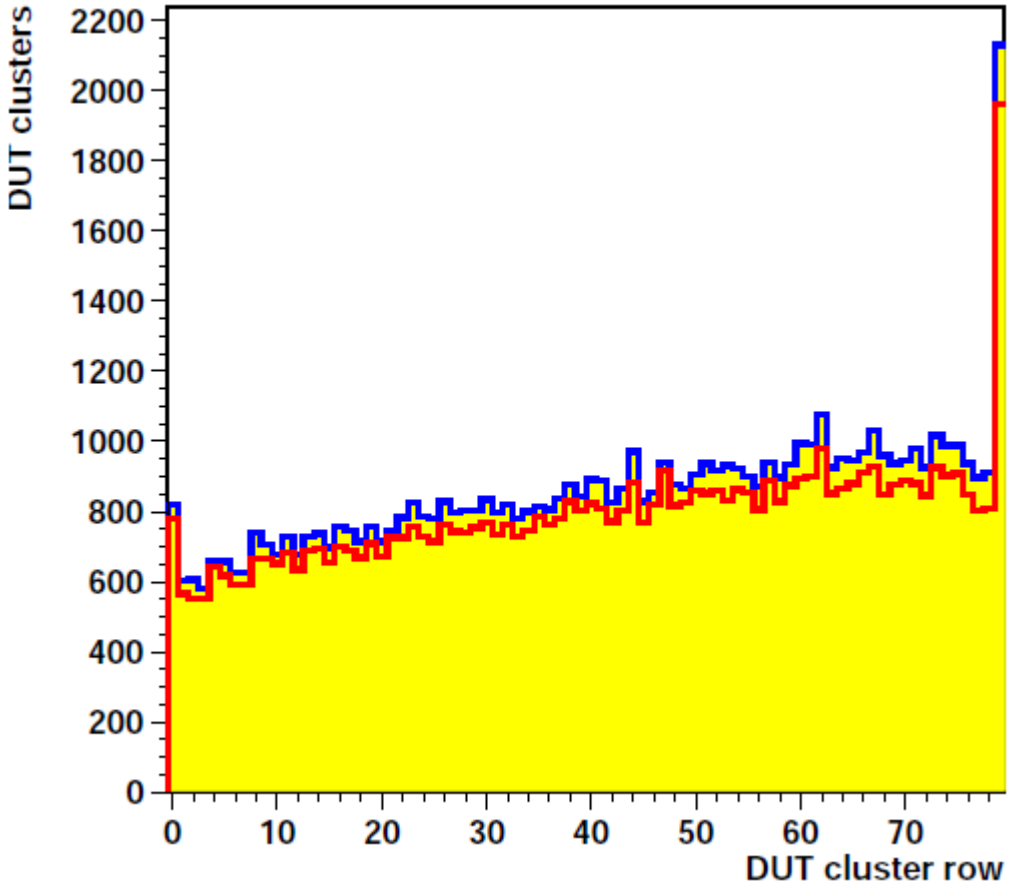


- Pixel pulse height saturates where noise just starts:
  - suggests that Vcal is the source of the noise (crosstalk)

Beam test data at trim 35

- Occupancy maps:
  - all clusters
  - clusters linked to tracks

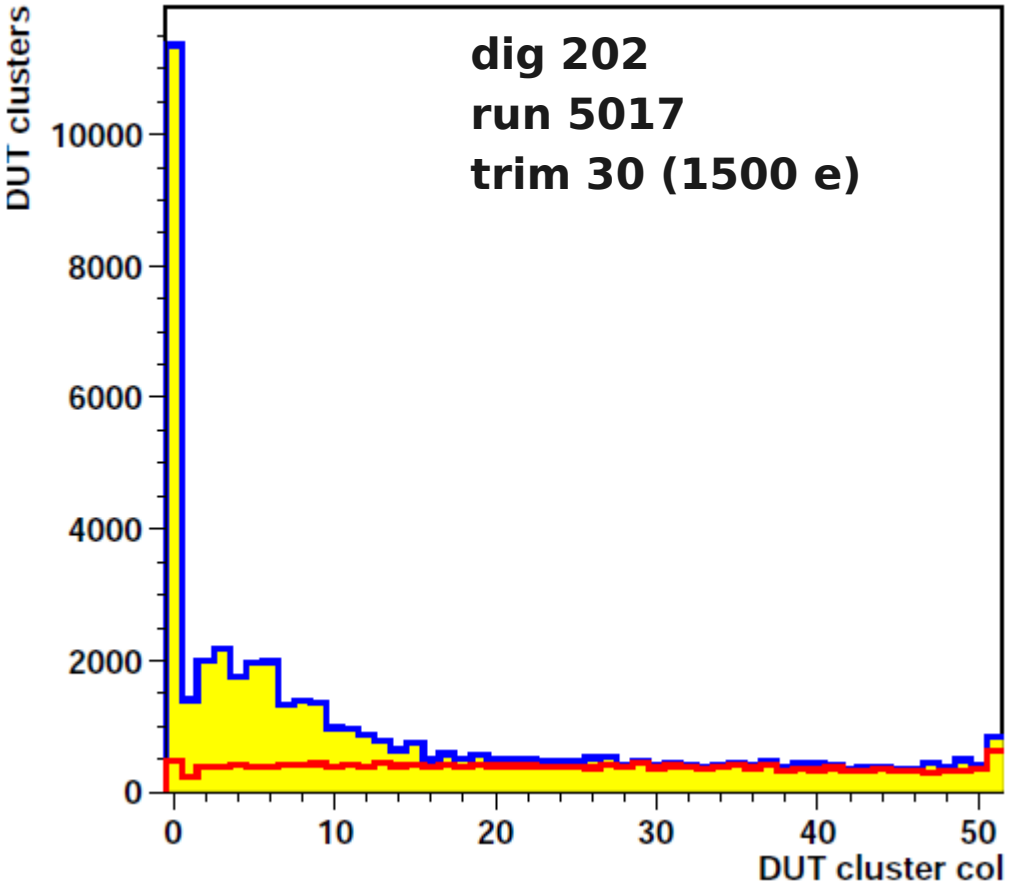


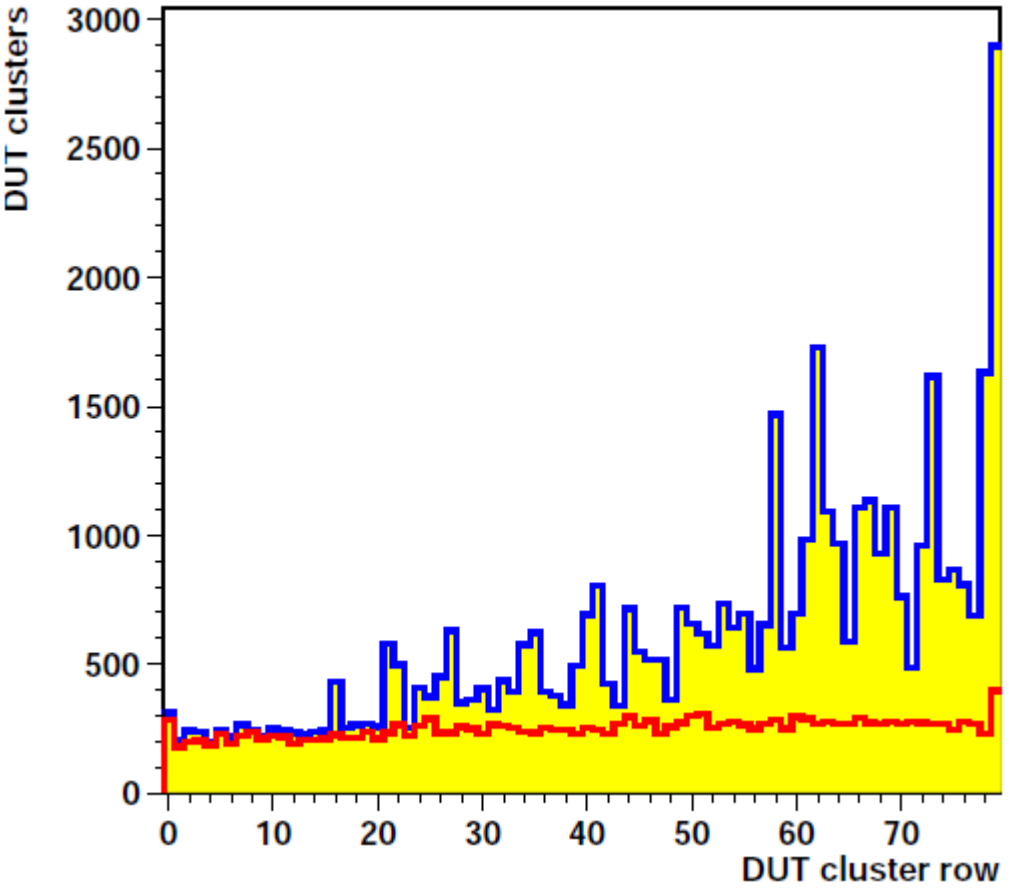


all fine

Beam test data at trim 30

- Occupancy maps:
  - all clusters
  - clusters linked to tracks

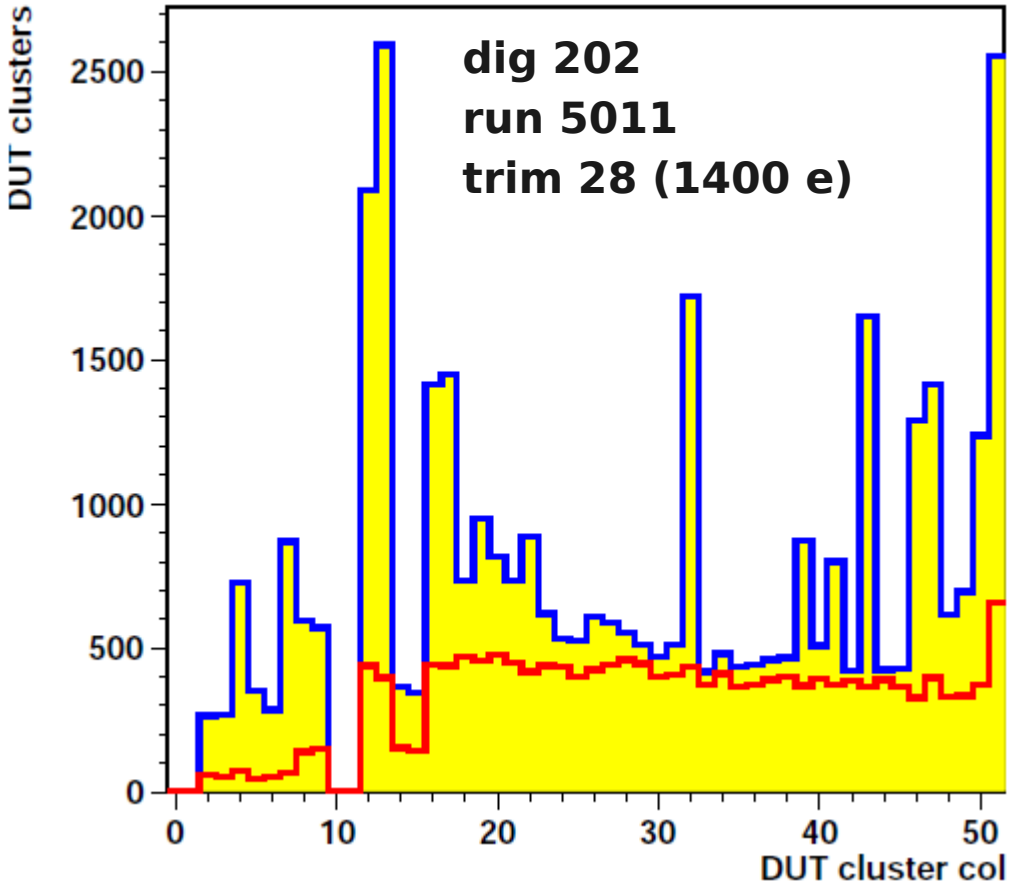


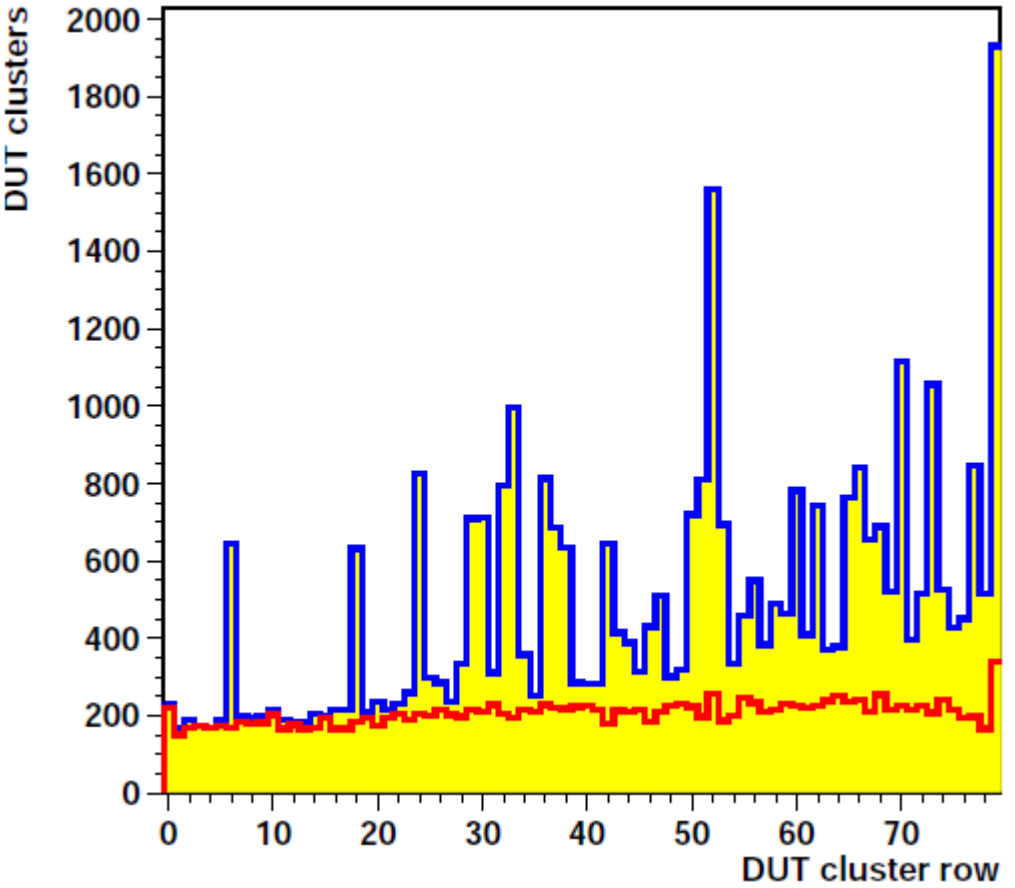


noisy region appears

Beam test data at trim 28

- Occupancy maps:
  - all clusters
  - clusters linked to tracks

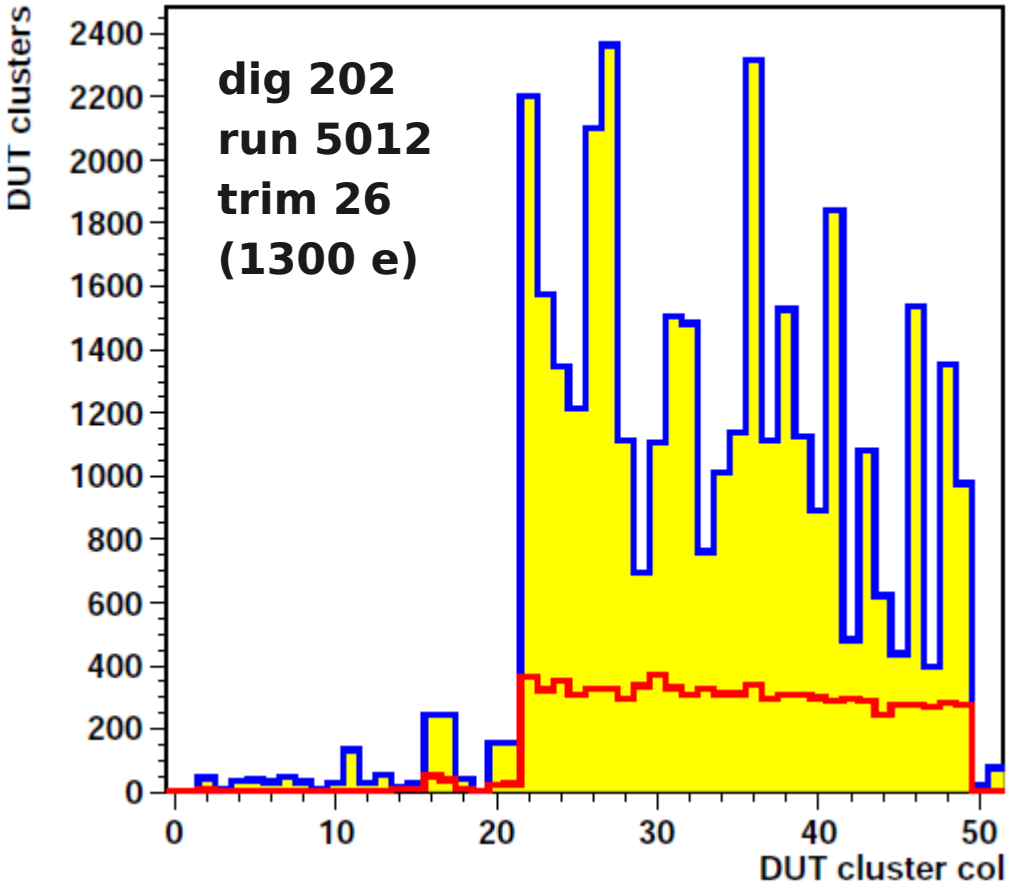


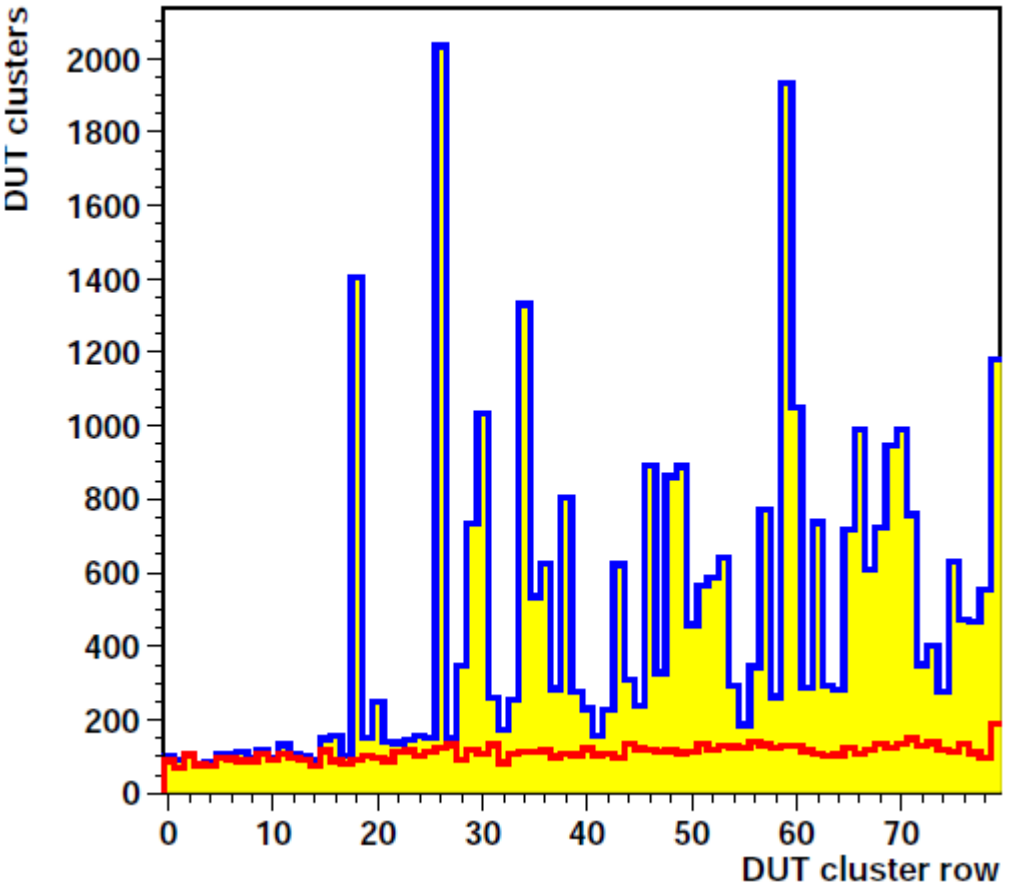


4 dead columns: saturated by noise?

Beam test data at trim 26

- Occupancy maps (columns and rows):
  - all clusters
  - clusters linked to tracks





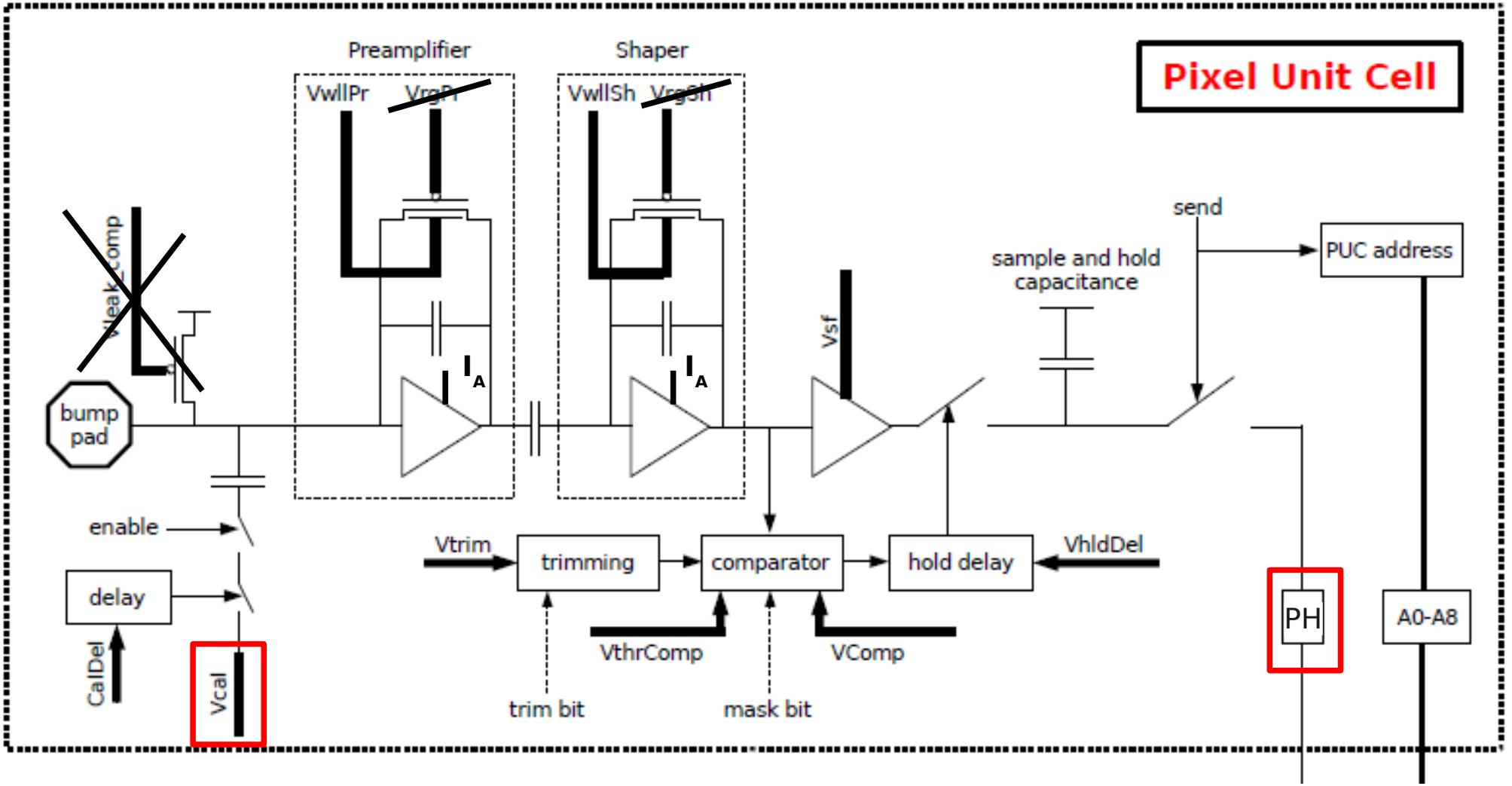
22 dead columns: saturated by noise?

Summary

- From beam tests:
  - pixel modules become noisy and inefficient at low thresholds
  - below trim 35 (1750 e) for psi46dig
  - below trim 45 (2900 e) for psi46v2
- try to understand this in the lab:
  - enable all pixels
  - inject one test pulse
  - observe column cross talk at low thresholds
  - probably induced by the test pulse signal, not the pixel response
- Next step:
  - take random trigger data in the lab
  - vary conditions: threshold, rate, run duration, ...

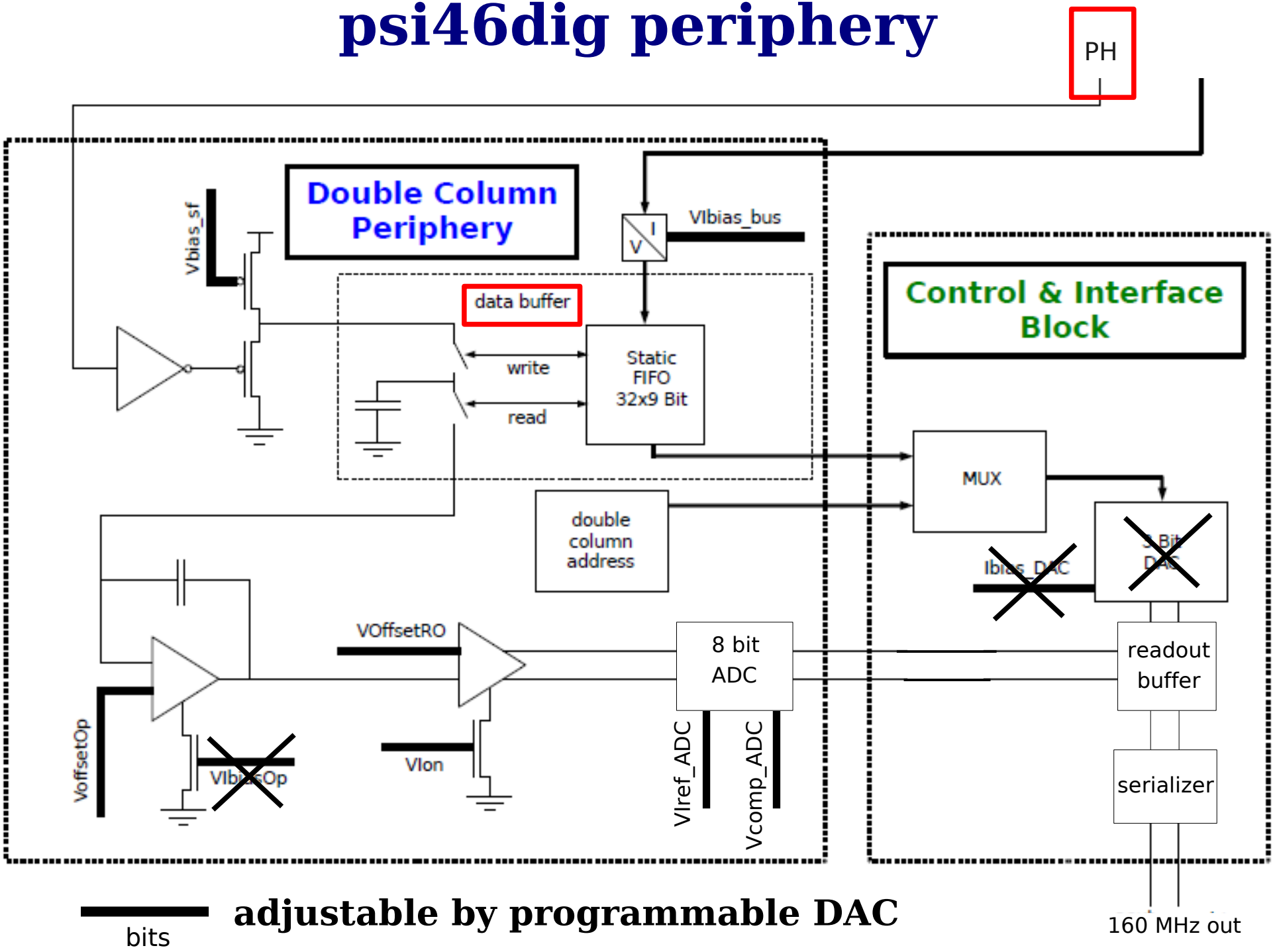
Back up

psi46dig pixel unit cell

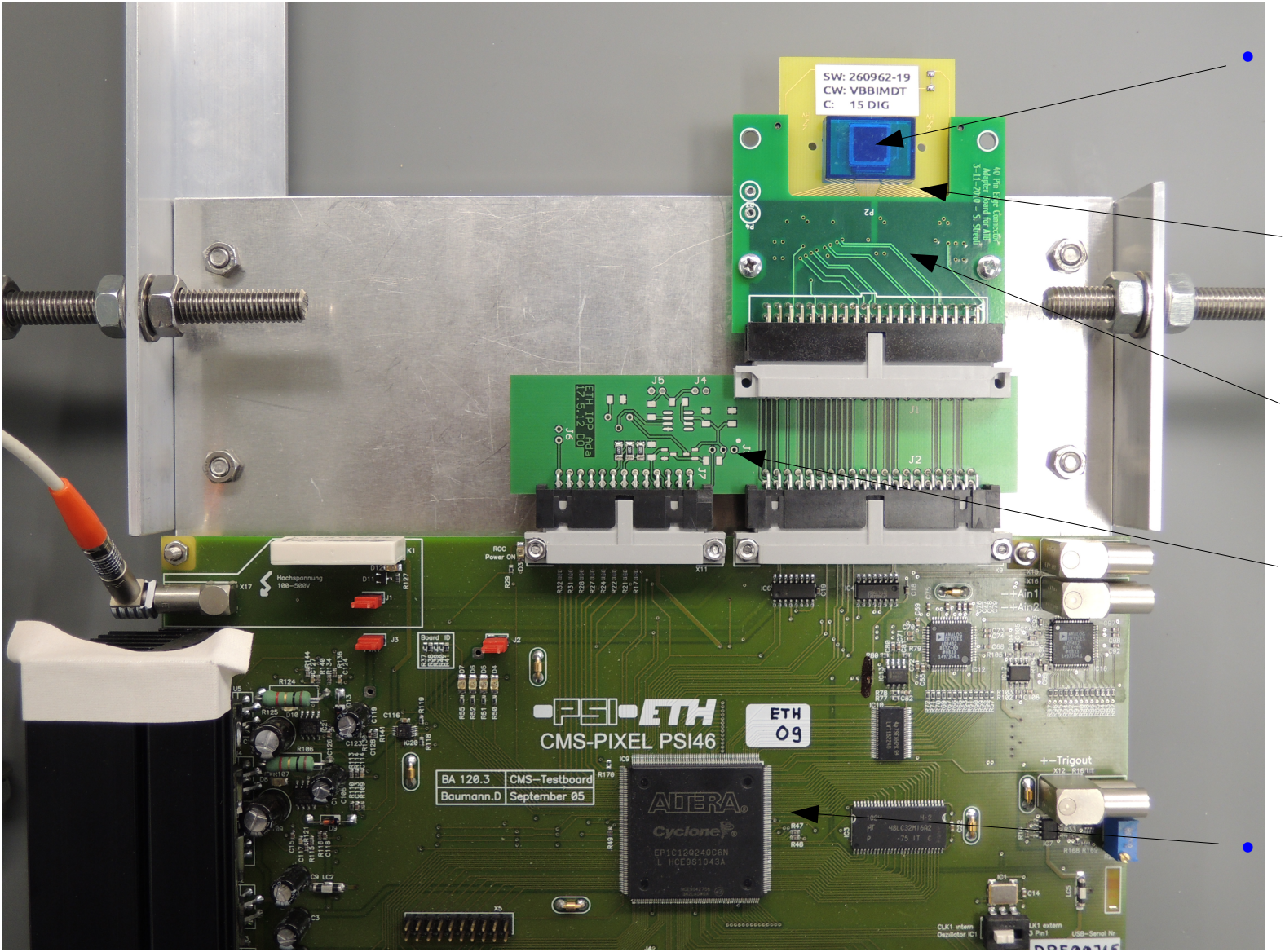


adjustable by programmable DAC

psi46dig periphery



Test setup at DESY



- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
  - ETH adapter card for digital 160 MHz differential signal directly into FPGA (LCDS into LVDS)
- FPGA firmware update to select digital path as 'TBM channel 1'

psi46dig DACs (Vcal threshold 18)

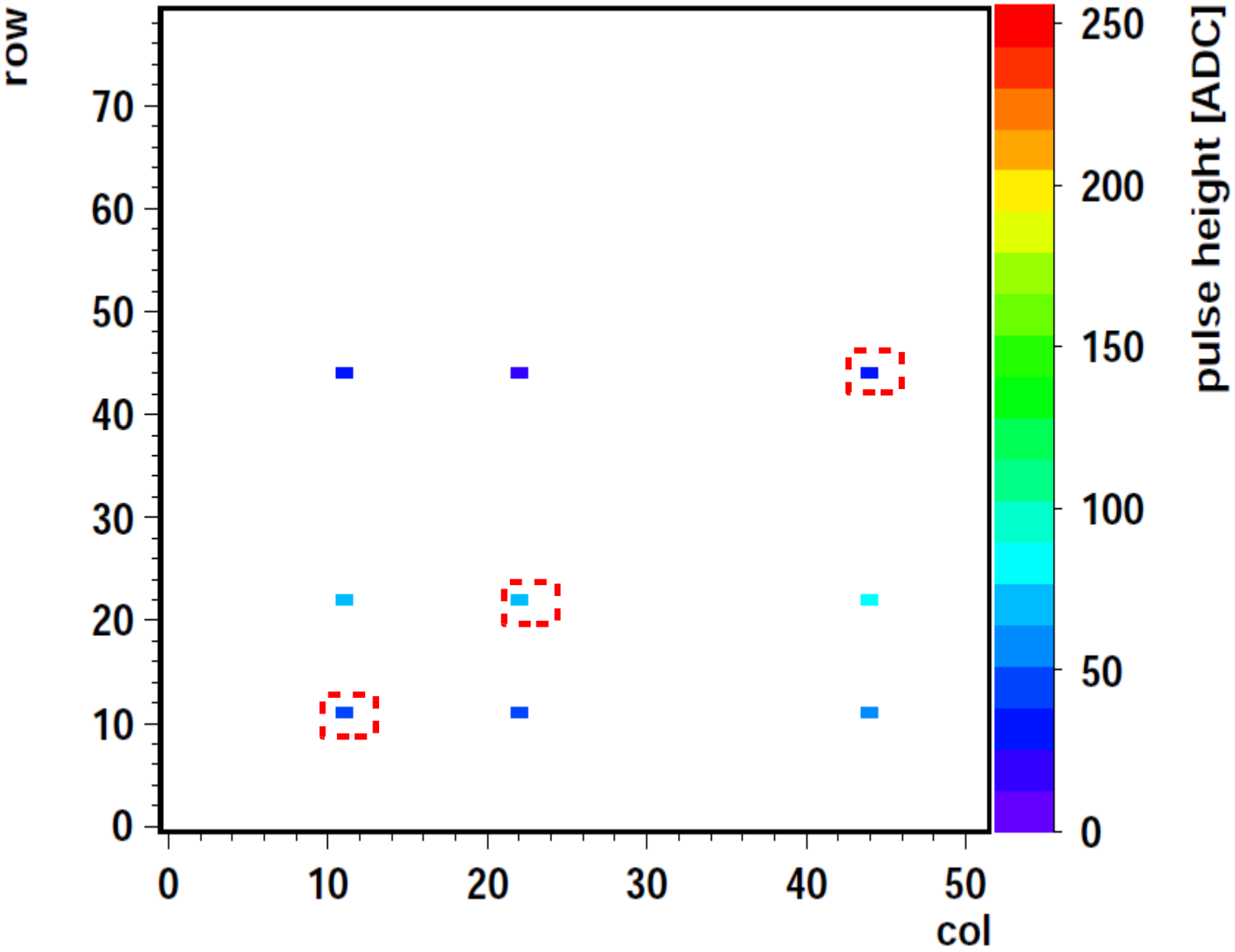
1	Vdig	6
2	Vana	159
3	Vsf	30
4	Vcomp	12
7	VwllPr	60
9	VwllSh	60
10	VhldDel	252
11	Vtrim	116
12	VthrComp	129

13	VIBias_Bus	20
14	Vbias_sf	10
15	VoffsetOp	30
17	VOffsetR0	110
18	VIon	115
19	Vcomp_ADC	120
20	VIref_ADC	70
22	VIColOr	100
25	Vcal	55
26	CalDel	152
253	CtrlReg	4
254	WBC	100

psi46expert procedure

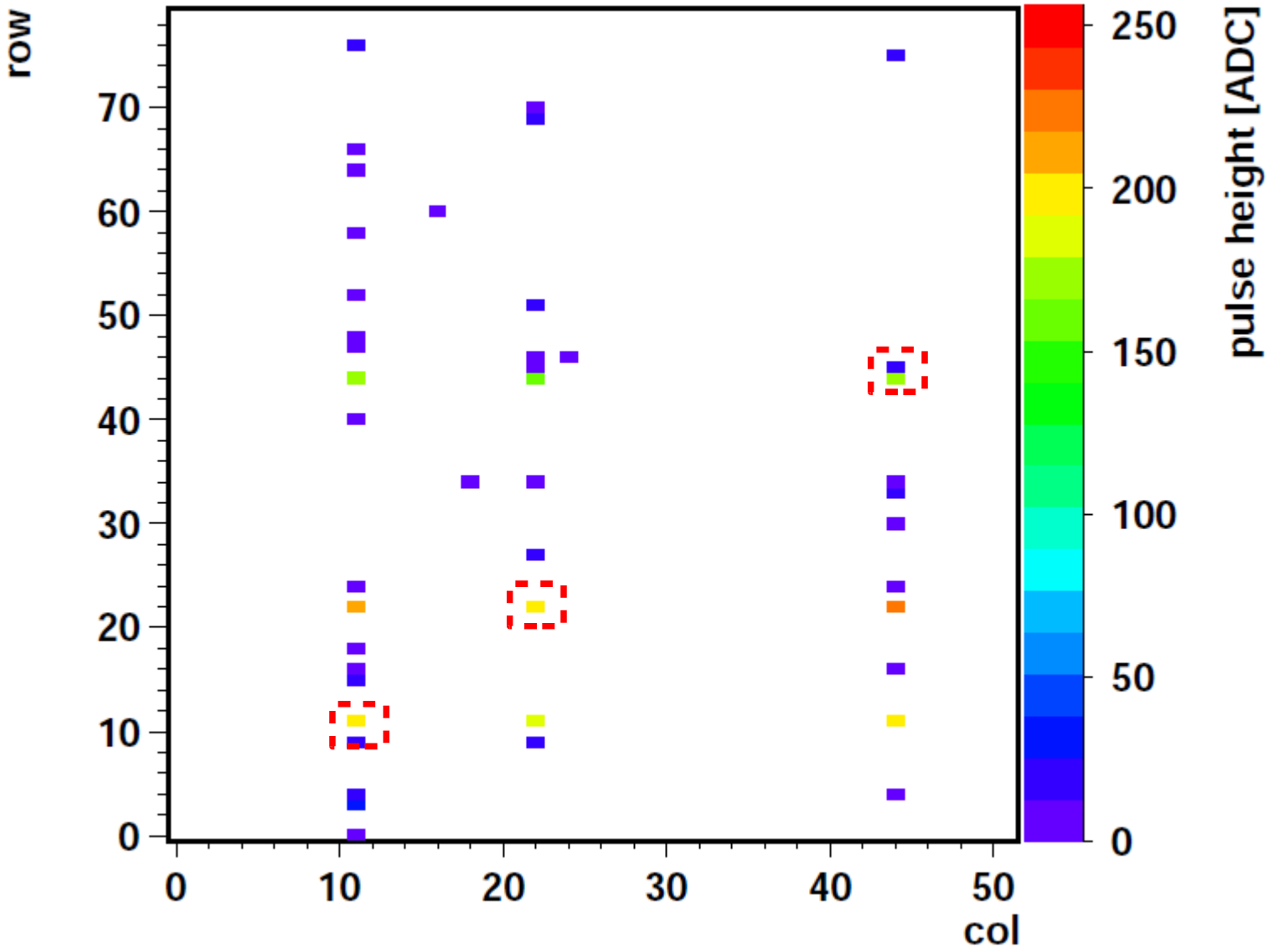
- run pretest:
  - analog current 35 mA
- trim:
  - target Vcal threshold 18 (~900e)
- enable all pixels
- give calibrate to 3 pixels
  - in different double columns
- vary Vcal in high range (CtrlReg 4)
- give RES|CAL|TRG|TOK and read data

test pulsing 3 pixels



- Digital Chip 204
  - enable all: pixe 0:51 0:79
  - arm 11 11
  - arm 22 22
  - arm 44 44
  - adc
- off-diagonal pixels respond:
  - ROC feature
  - 'arm' selects entire column
  - pulse injected in one row

event display Vcal 122



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  - Ia 35 mA
  - trimmed to Vcal threshold 18
  - high range (CtrlReg 4)
  - pixe 0:51 0:79
  - arm 11 11
  - arm 22 22
  - arm 44 44
  - adc
- in-column cross talk?