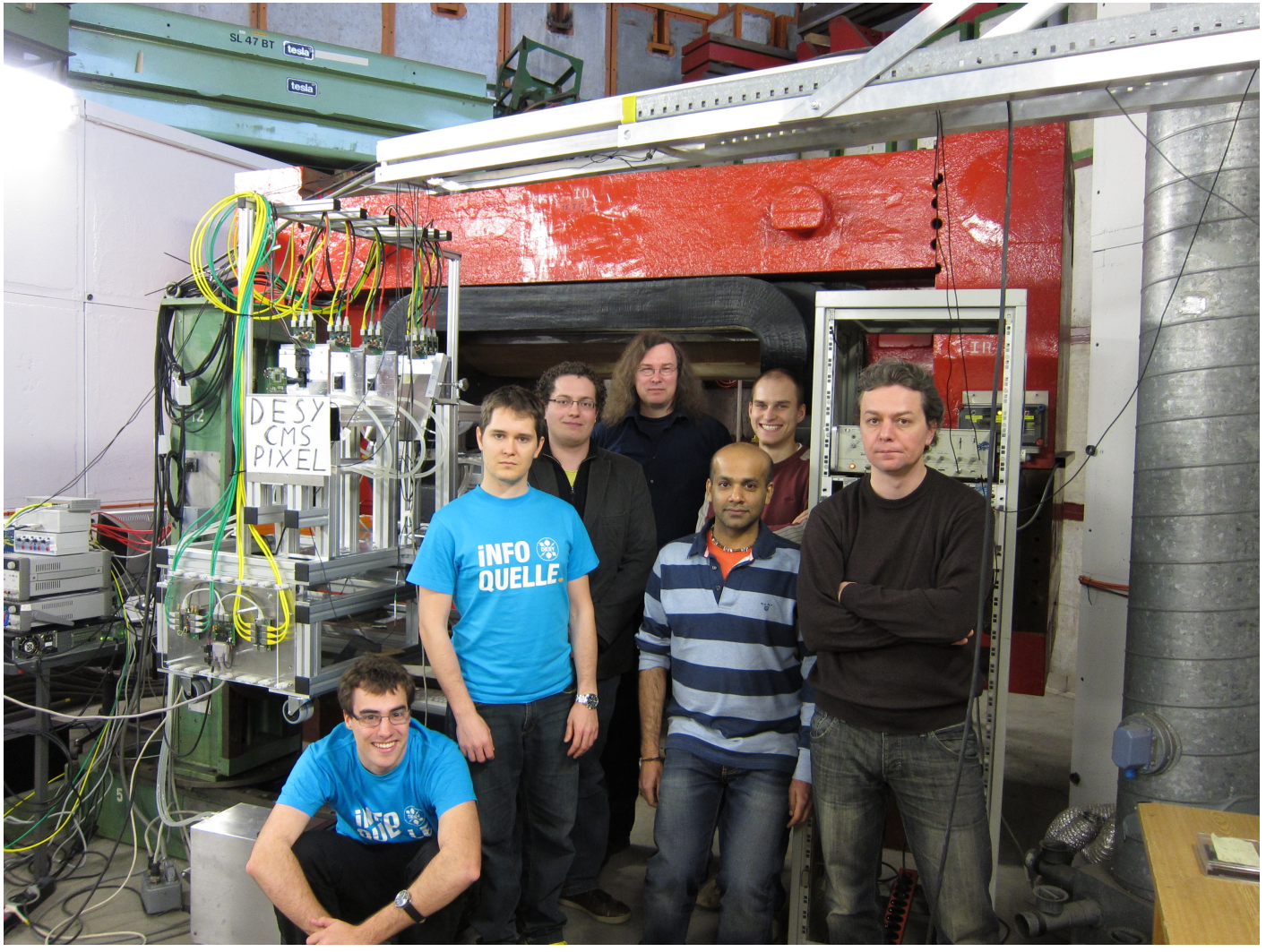
Bias scan results from the April/May 2012 beam test

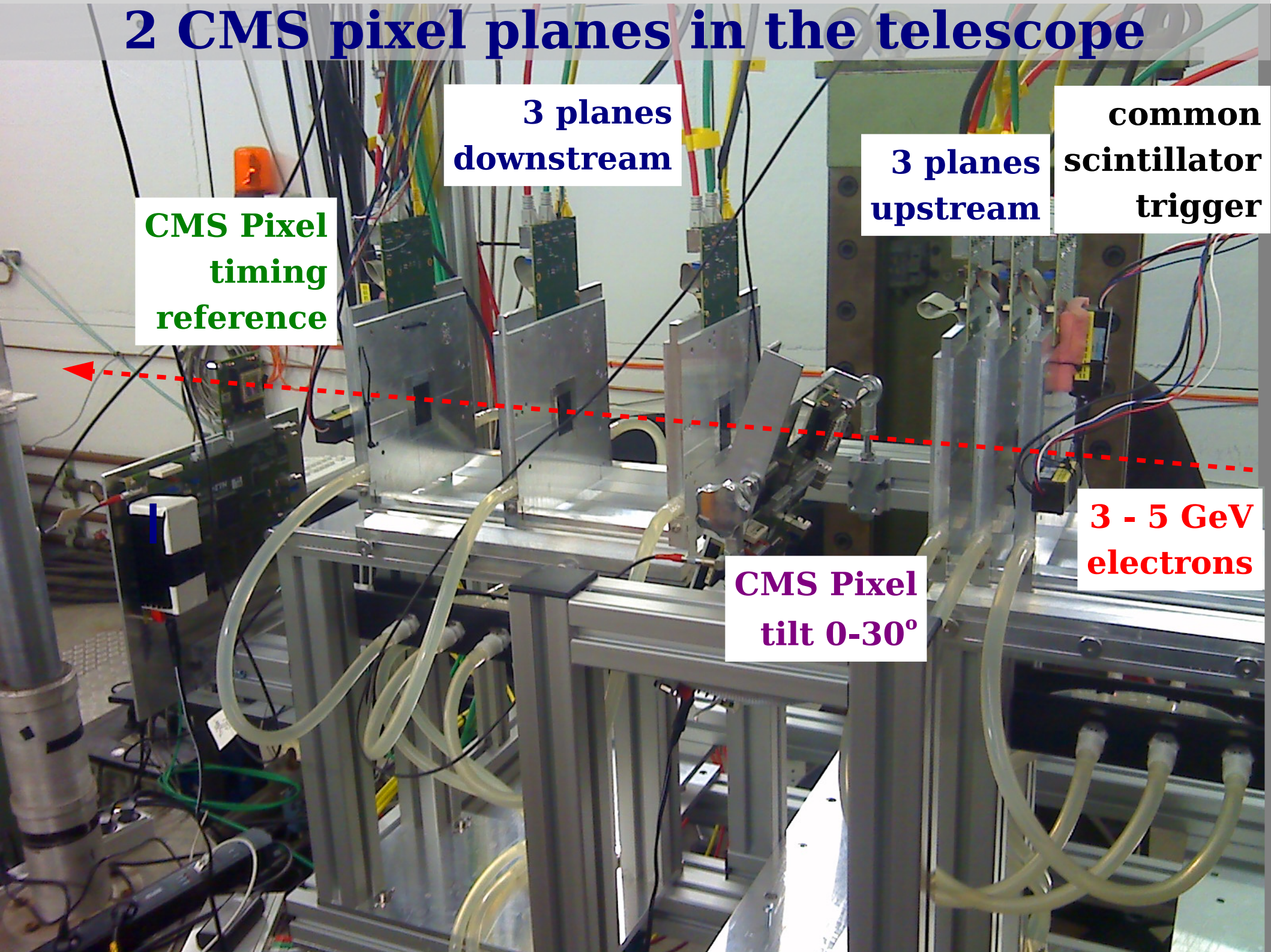
Armin Burgmeier, Luigi Calligaris, Thomas Eichhorn, Shiraz Habib, Hanno Perrey, Alexey Petrukhin, Daniel Pitzl

CMS Phase I pixel upgrade, 5.10.2012

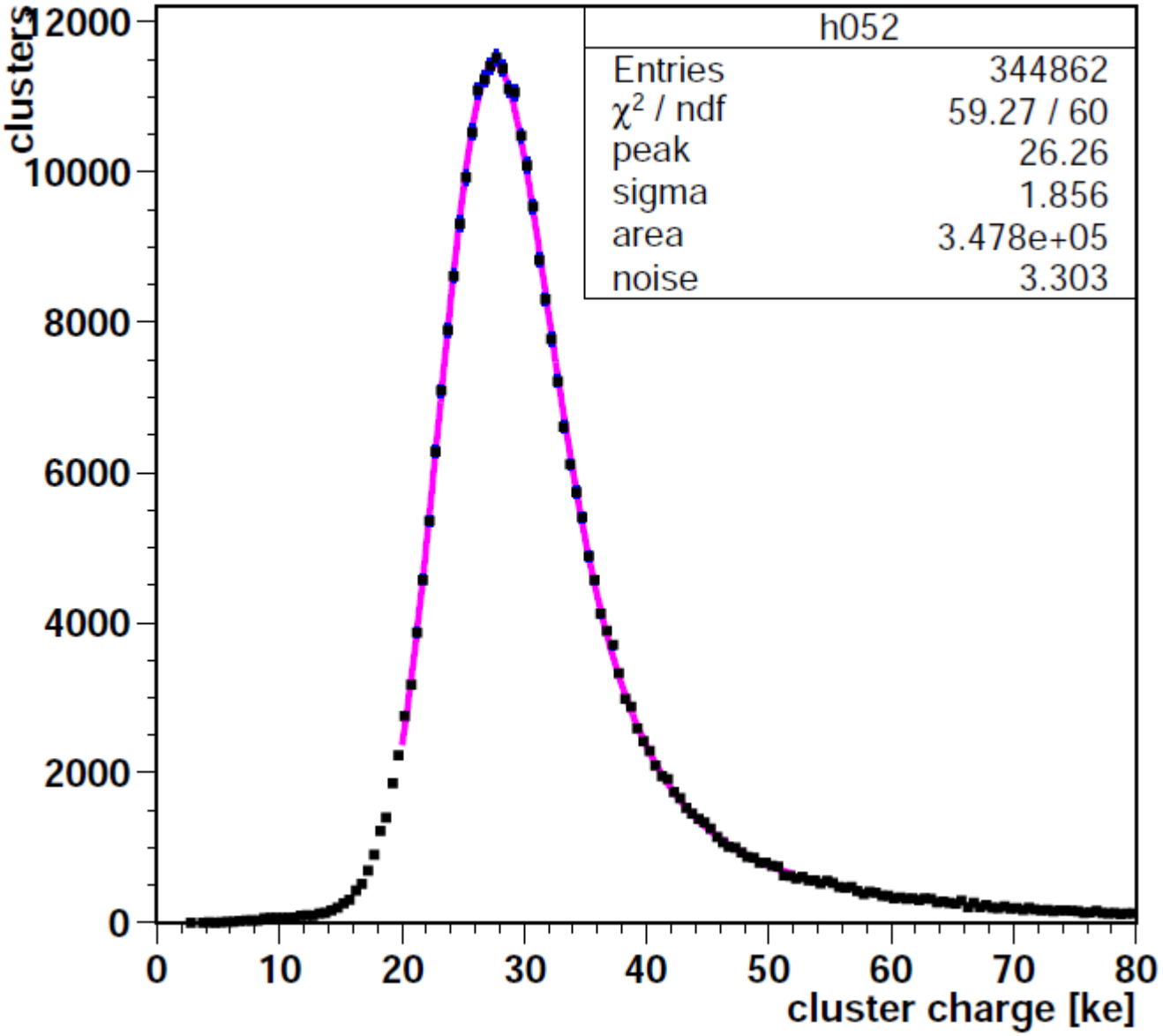


- motivated by sensor C-V curves shown 21.9.2012: drop between 130 and 150 V bias
- beam test setup
- bias scan results

2 CMS pixel planes in the telescope

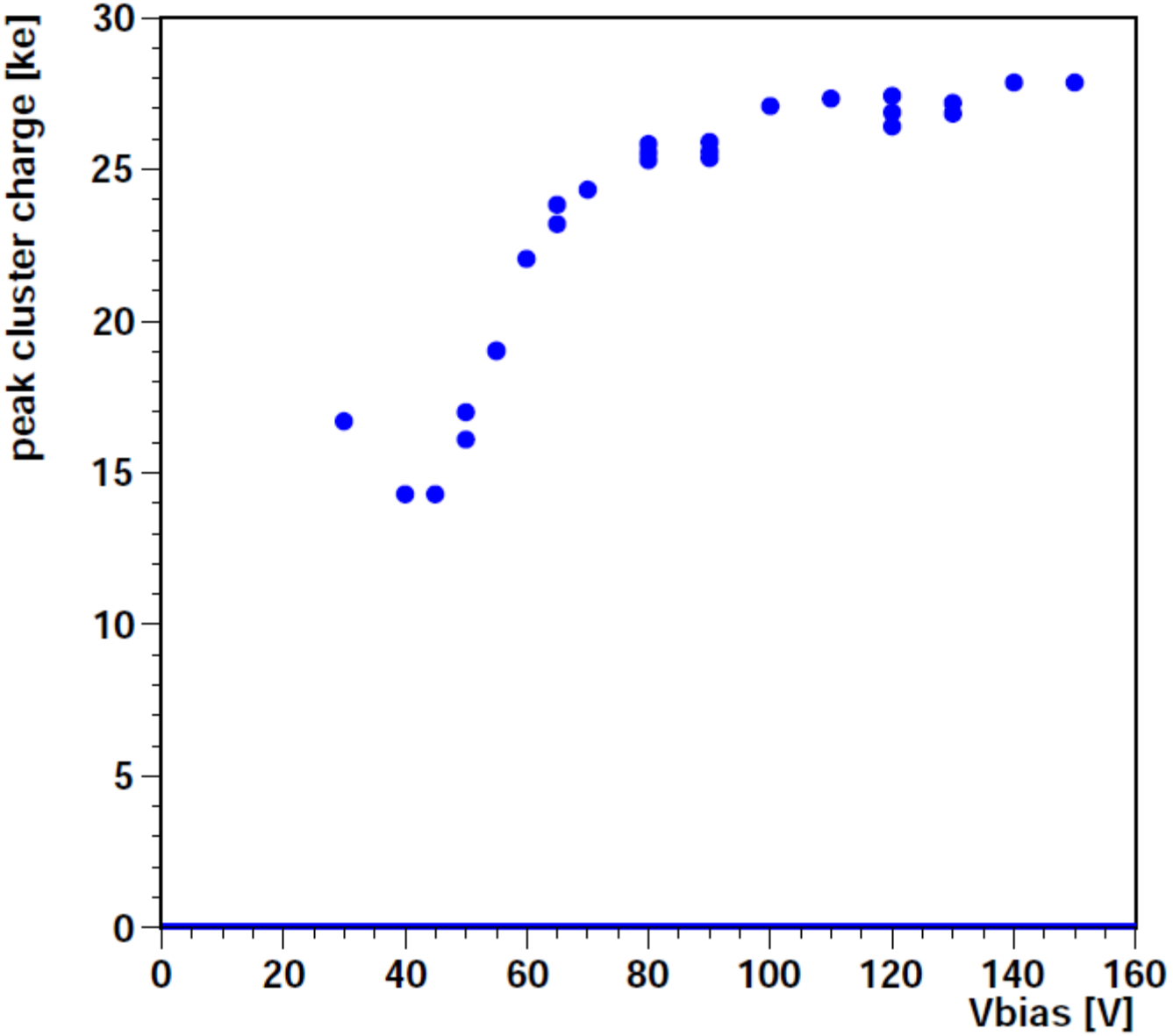


Pulse height distribution



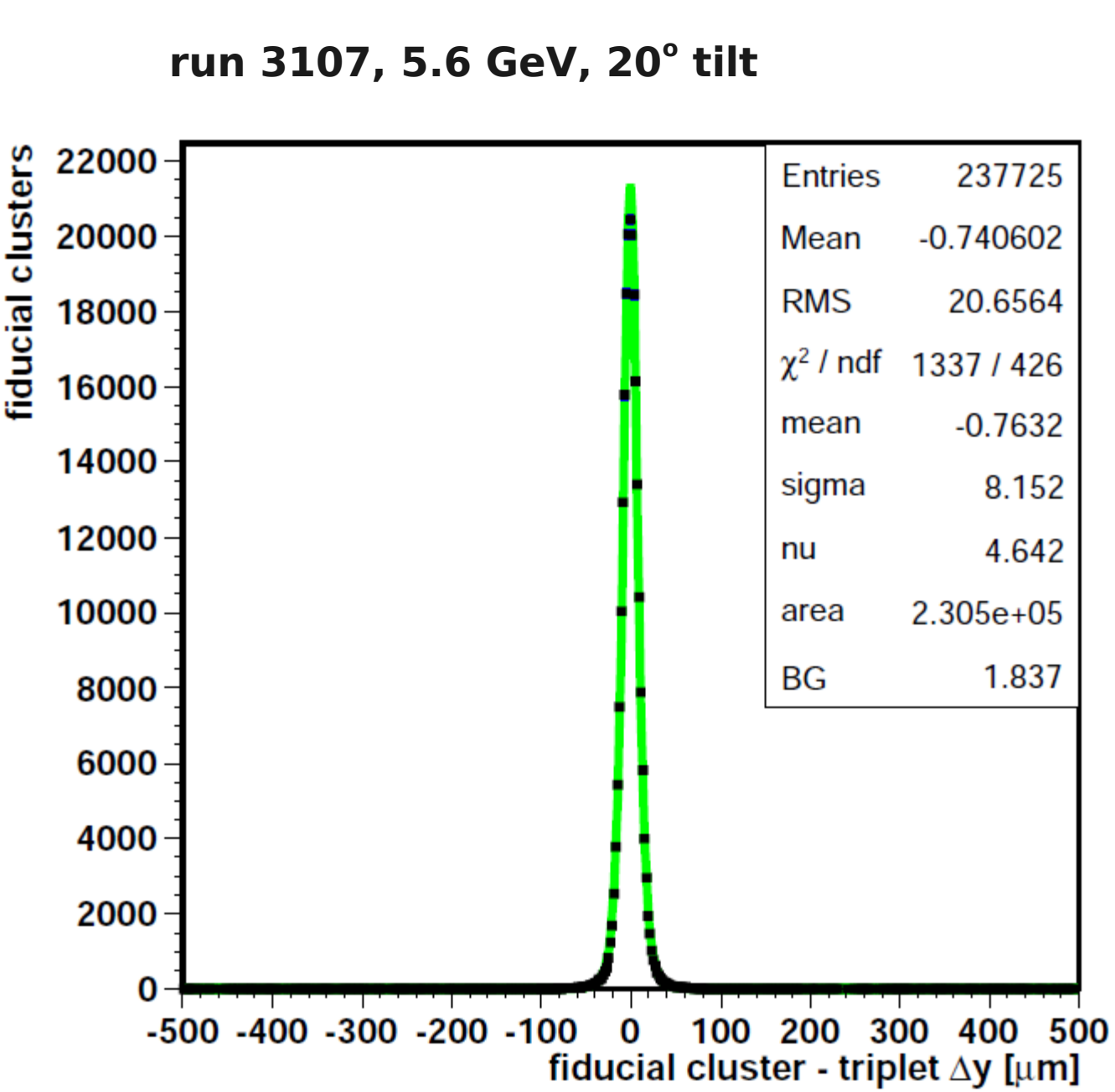
- Chip 10 at 20° tilt.
- Gain calibration from Shiraz.
- fiducial cuts:
  - edge pixels avoided.
- Landau ⊗ Gauss:
  - perfect fit,
  - peak position and width OK for 285 µm silicon,
  - Gaussian smearing too large: non-uniformities?

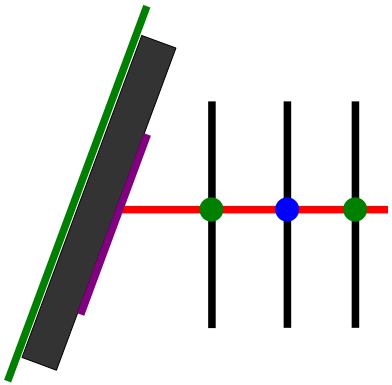
Cluster charge vs bias voltage



- Chip 10, 5.6 GeV, 20°
- Position of the Landau peak.
- slowly reaching plateau:
  - not a good indicator of full depletion

CMS pixel row resolution





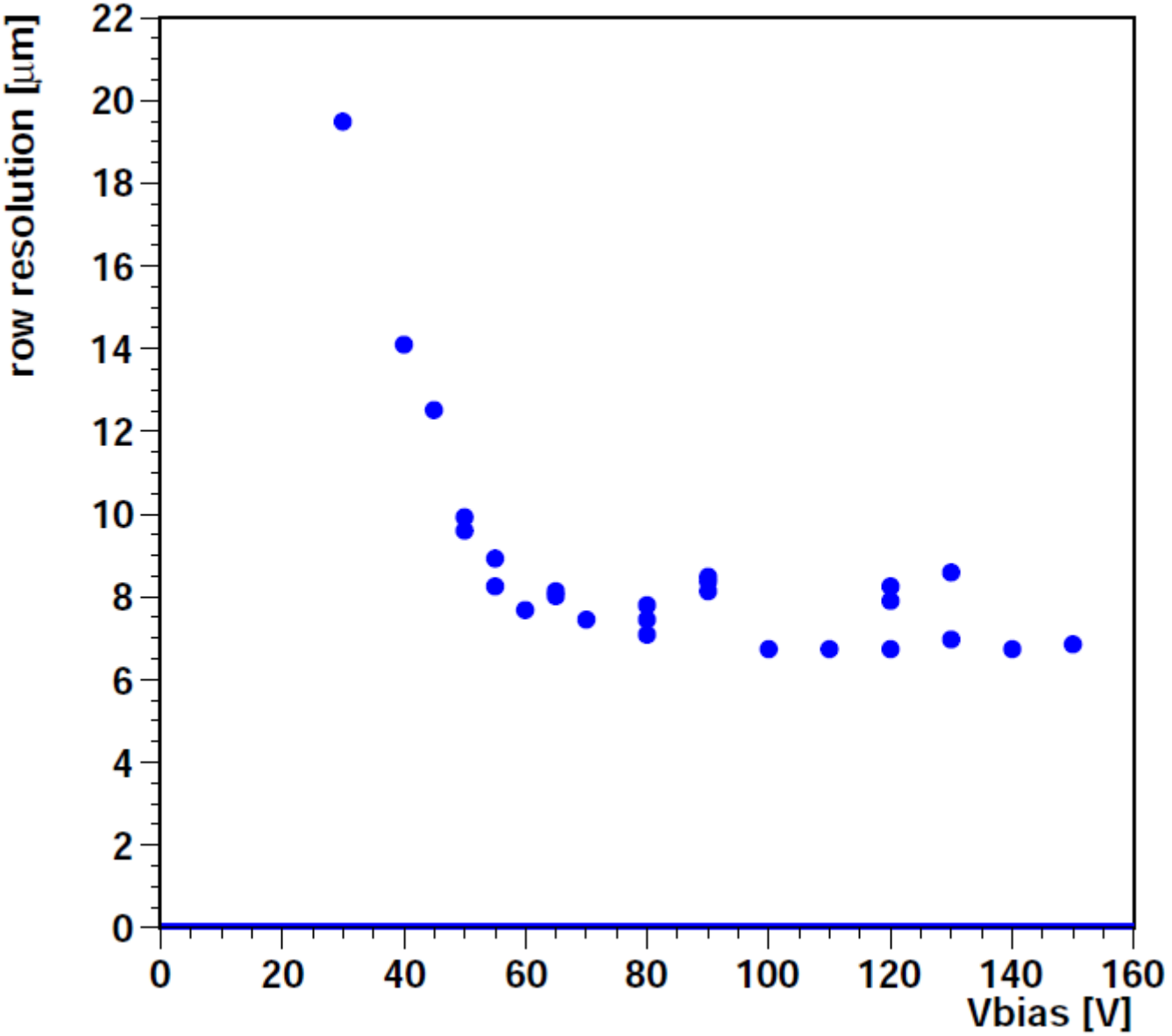
Vertical = rows

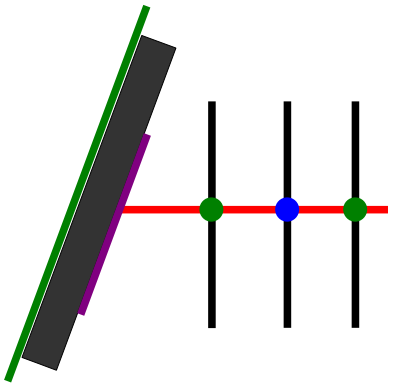
- CMS pixel = 100 µm.

Residual:

- σ = 8.2 µm,
- telescope extrapolation: 4.5 µm,
- **CMS resolution: 7 µm.**

CMS pixel row resolution vs bias voltage

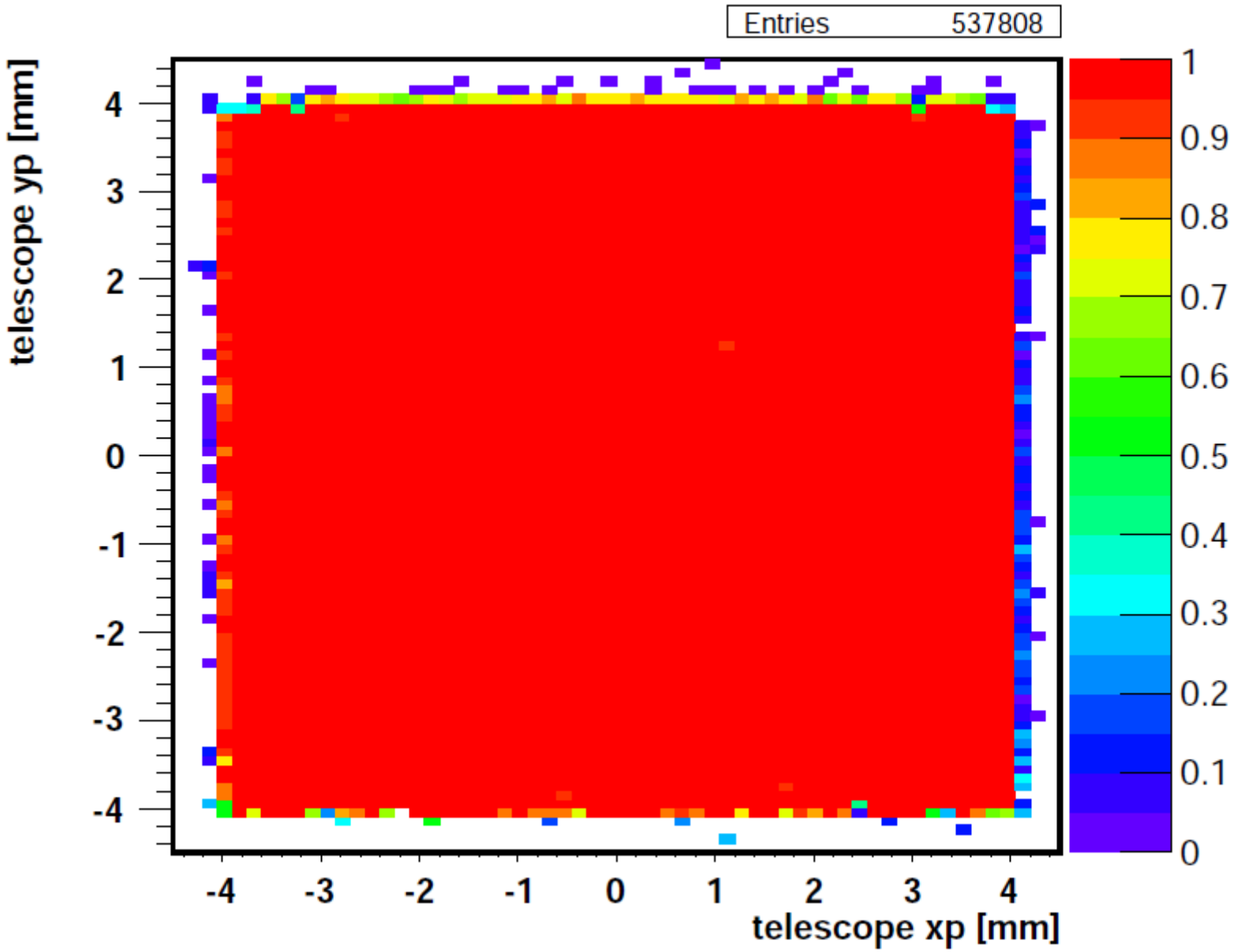




- Chip 10, 5.6 GeV, 20° telescope extrapolation uncertainty subtracted.
- best:
  - 7 µm above 80 V (full depletion)
- outliers:
  - bad timing = worse resolution

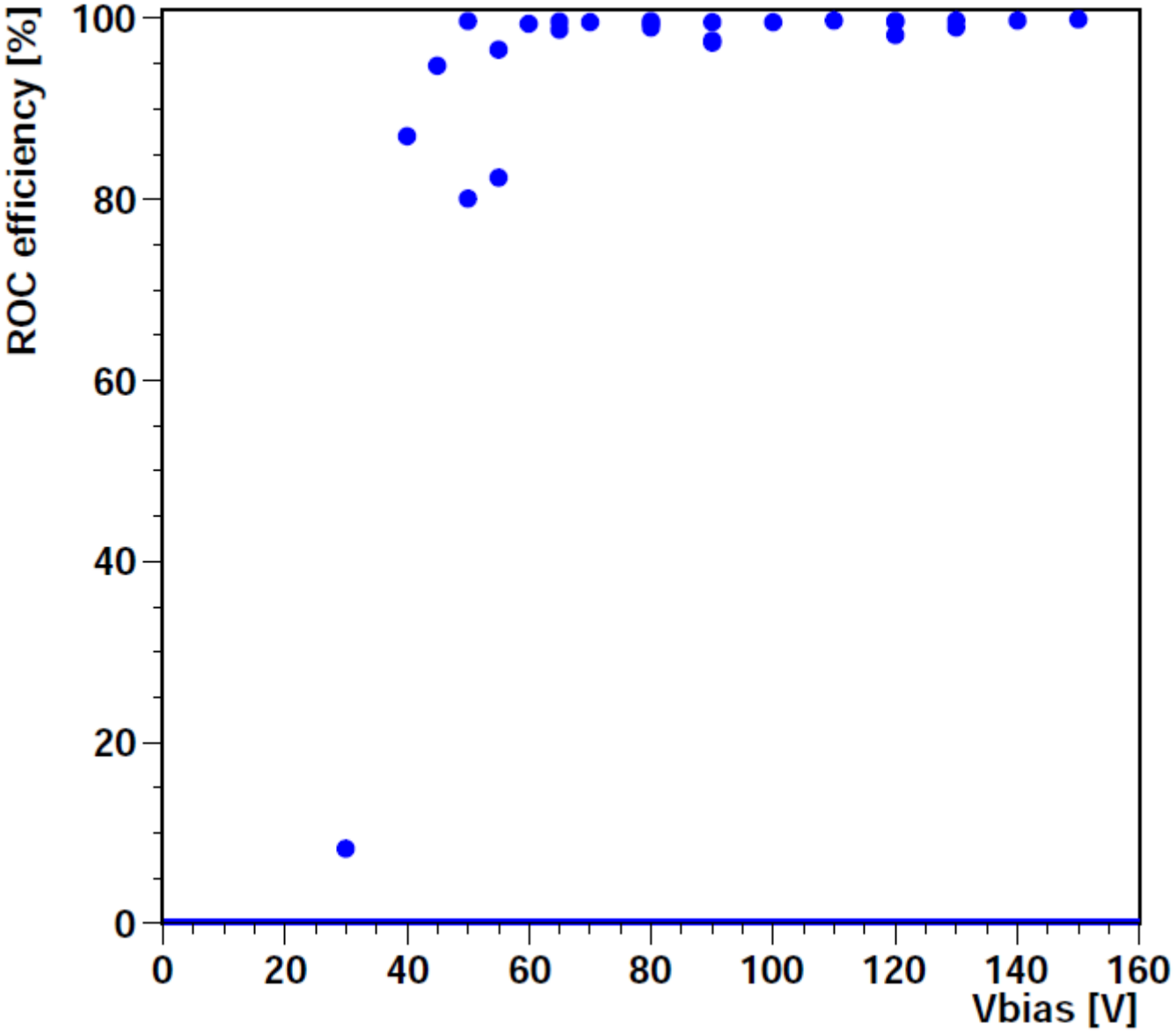
Efficiency map

efficiency = tracks with CMS hit / telescope tracks



- run 3096
  - 2800 s
- 5.6 GeV
- chip 10
- tilt 20°

Efficiency vs bias voltage

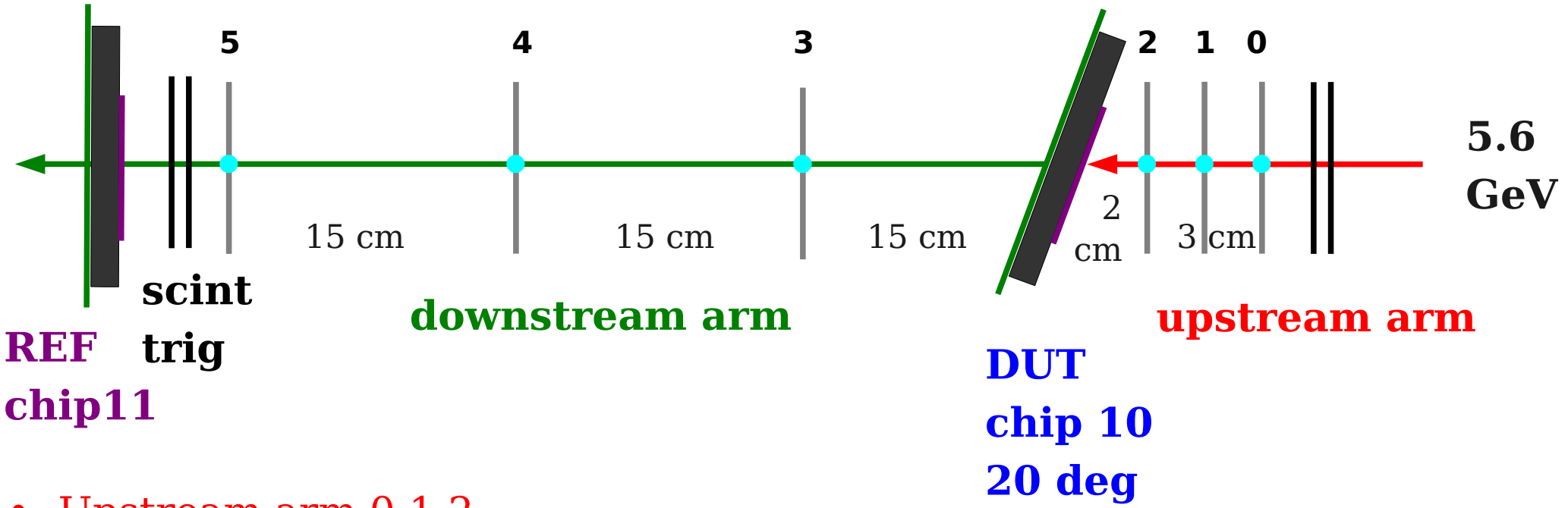


- Chip 10, 5.6 GeV, 20°
- fully efficient above 50 V: full depletion.
- some outliers with lower efficiency: timing problem.

Summary

- Beam test data with various bias voltages up to 150 V:
  - nothing special happens between 120 and 150 V:
  - in terms of resolution, efficiency, pulse height, cluster size...

Default set up



- Upstream arm 0-1-2:
  - as close as possible to DUT, but allow for tilting (open for insertion)
- DUT = single chip module, tilted by up to 30°,
- Downstream arm 3-4-5:
  - equally spaced between DUT and REF, allow for DUT tilting
- REF = single chip module for timing, as close as possible behind scint
- trigger: 2-fold coincidence (config: TLU AndMask 12)