Pixel test plans for Winter 2012/13

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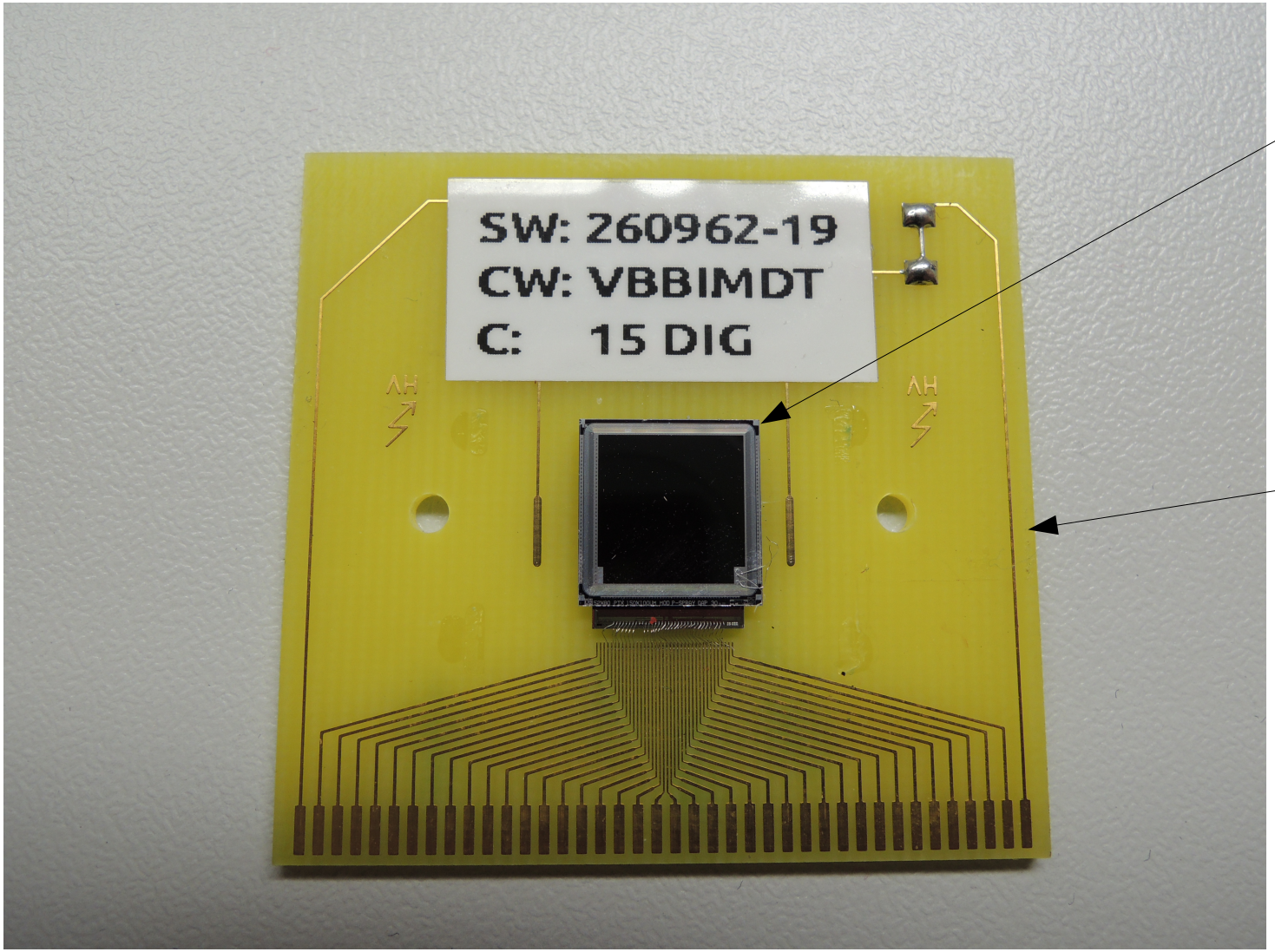
Hamburg Pixel Upgrade meeting, 2.11.2012

- Focus on digital ROC
  - use-up all samples until April 2013 when the next chip arrives
- X-ray tests (Uni)
- irradiation test (DESY)

X-ray (Uni HH)

- Got 2 single chip modules with psi46dig from PSI — 30.10.2012
  - establish DAC and trim parameters — Nov 2012
  - operate in X-ray box
- Clock stretch with digital ROC:
  - possible after all (B. Meier, U. Langenegger) — try it!
  - requires ~50 clock delay between stretch and trigger
- X-ray gain calibration at low temperature:
  - still an open issue (KIT studies on-going)
  - cooling and dry air set-up under preparation — on-going
  - avoid condensation and ice!

CMS pixel single chip module



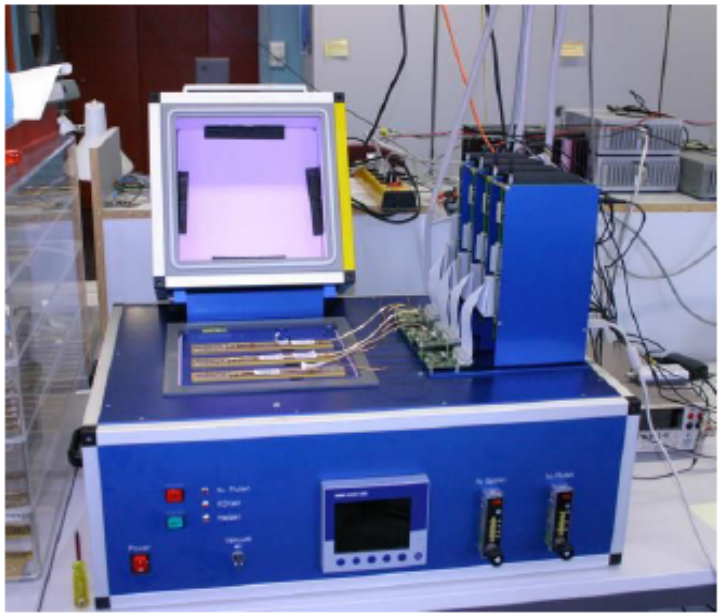
- **Single chip module:**
  - **Si: 10×10 mm²**
  - **Indium bump bonded at PSI**
  - **Glued and wire bonded to carrier printed circuit board**
  - **PCB: 40×40 mm²**

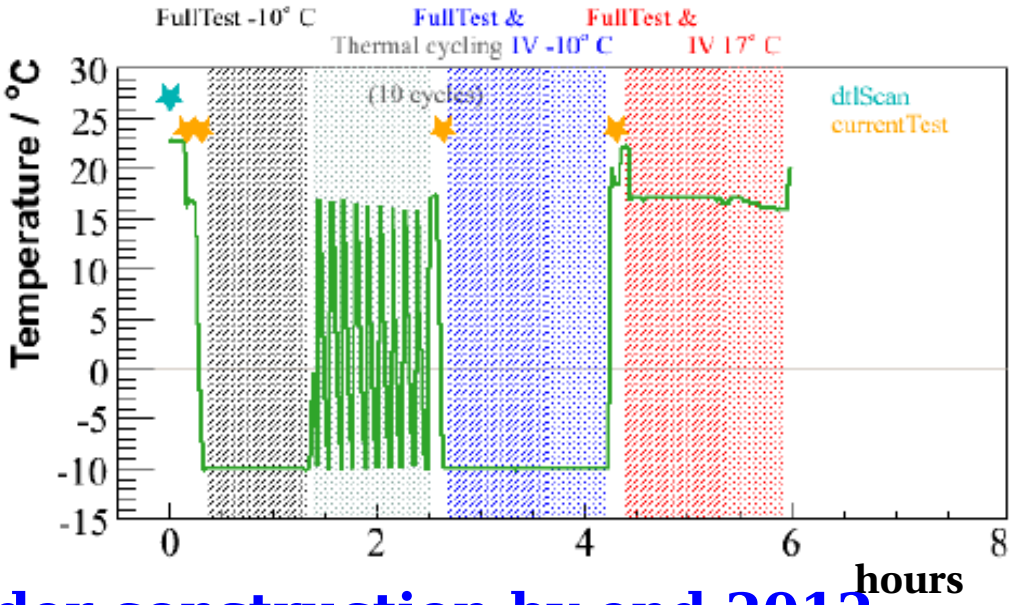
irradiation tests (DESY)

- Irradiated 2 single chip modules with psi46dig at CERN PS — Oct 2012
  - They were fully measured in the test beam — Sep 2012
  - 26 GeV protons
  - 1.5 and 4 10^{14} p/cm^2 (5 and 13 MRad)
  - cooling-off at CERN — shipping not before mid Nov '12
  - first measurements at CERN? — Nov 2012?
- Got two more digital ROCs from PSI
  - pre-irradiation measurements to be done — Nov 2012
  - Al mask for PCB around ROC made in workshop — Oct 2012
  - send to Karlsruhe Zyklotron (23 MeV protons) — Nov 2012
  - re-measure at DESY — Dec 2012

Box for module cold calibration

- Challenges
  - Huge number of channels: $5 \div 6 \times 10^7$
  - Multy-dimensional parameter space: 29 DACs/ROC
  - Temperature dependence: tests done at -10°C and +17°C **upgrade: -20°C**
- Test set up
  - Programmable cooling box
  - 4 modules at a time
  - Castom built test-boards with FPGA
- Procedure
  - Start-up adjustments
  - Full Test at -10°C
  - 10 thermal cycles
  - Full Tests and IV at -10°C and +17°C

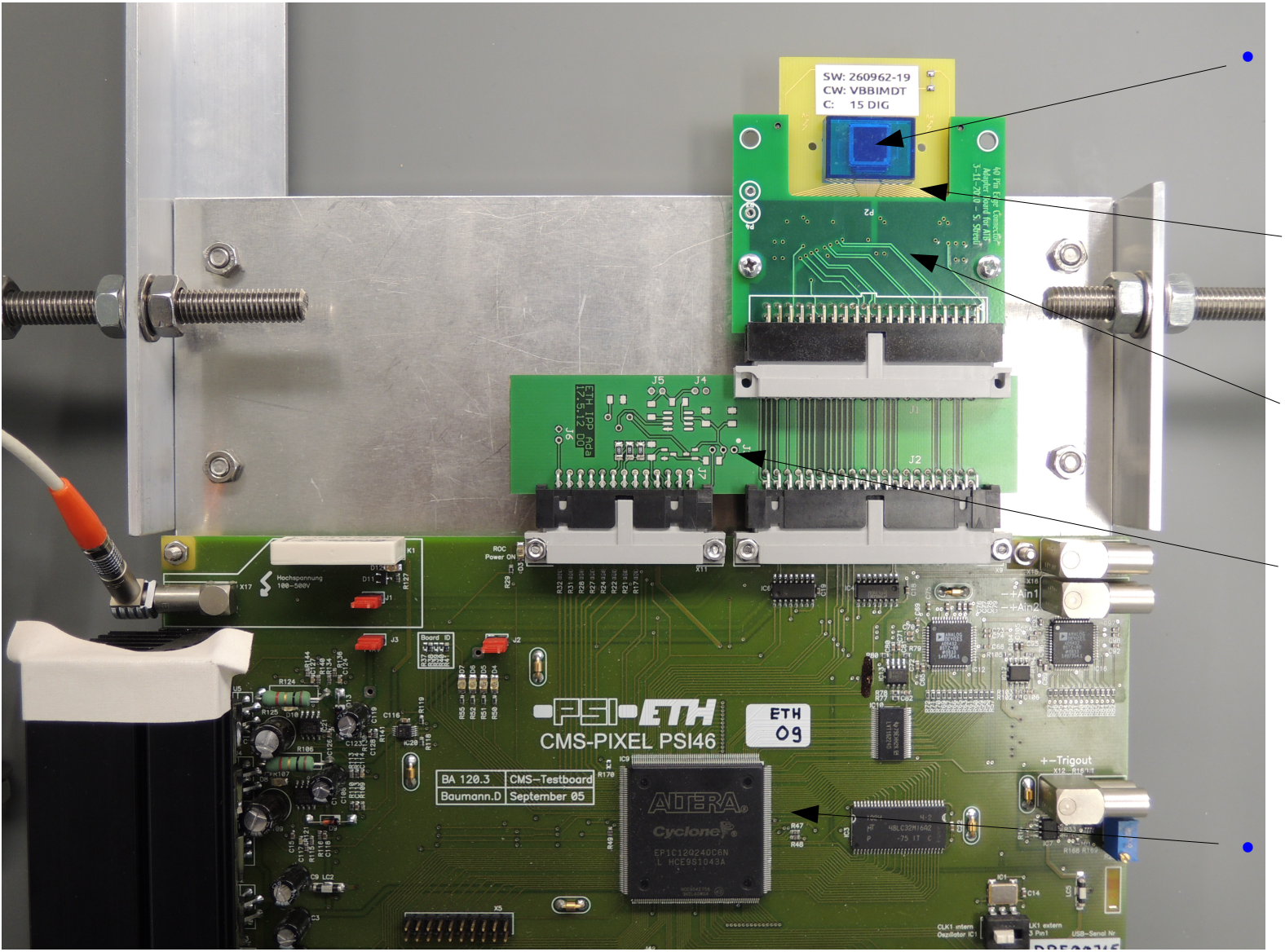




DESY box designed by C. Muhl, under construction by end 2012

Back up

Test setup at DESY



- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
  - ETH adapter card for digital 160 MHz differential signal directly into FPGA (LCDS into LVDS)
- FPGA firmware update to select digital path as 'TBM channel 1'