Future Directions in Track Triggering

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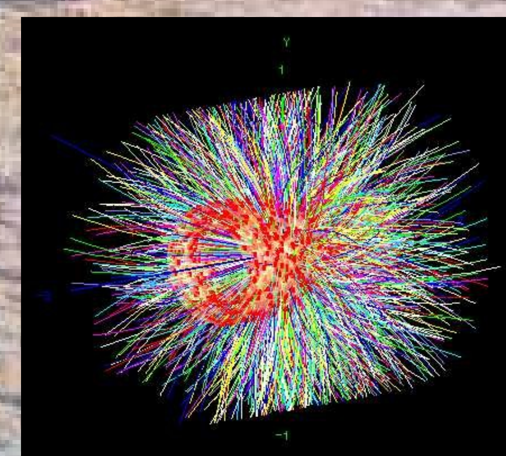
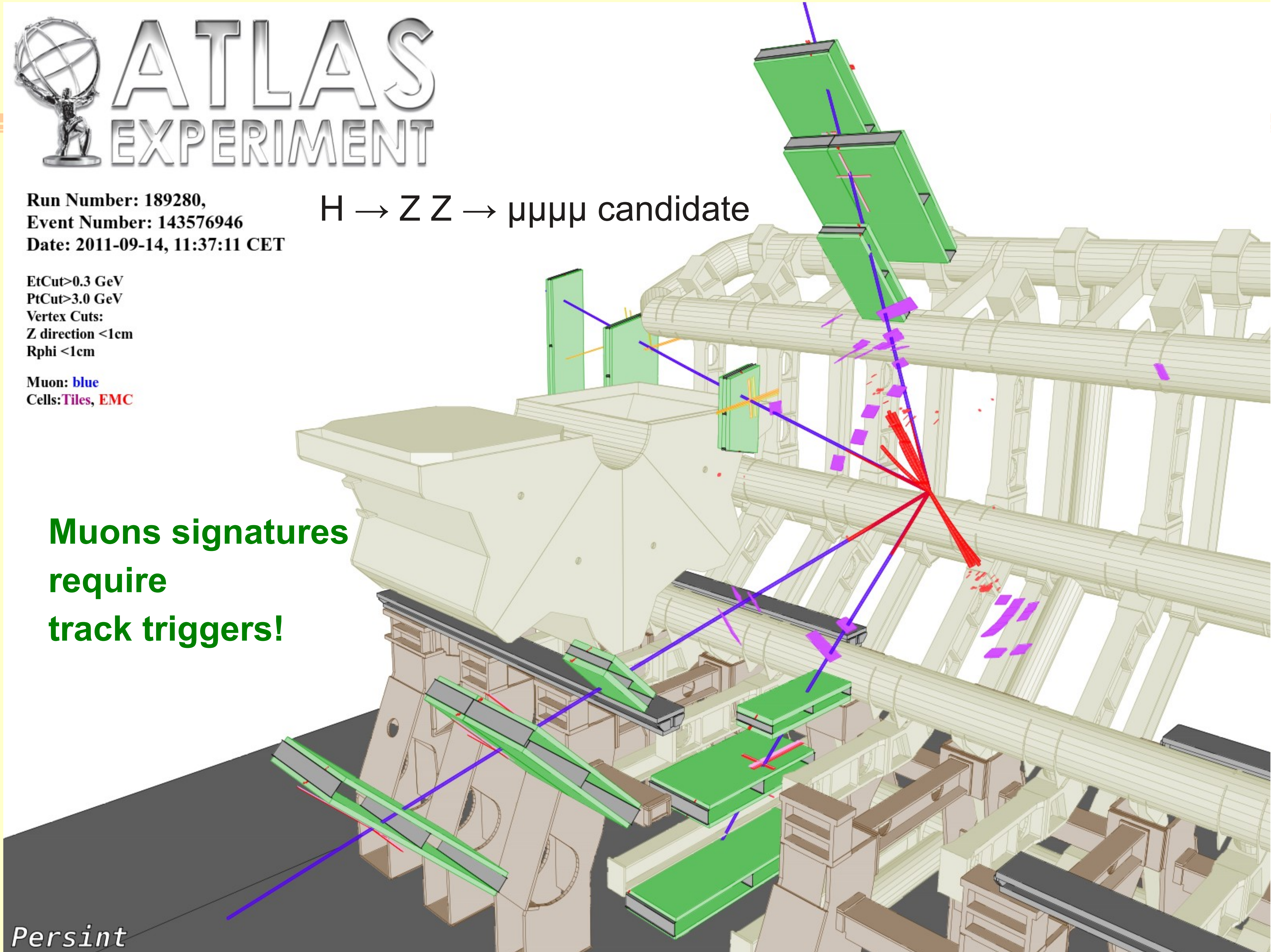
PHYSICS AT THE TERA SCALE

Helmholtz Alliance

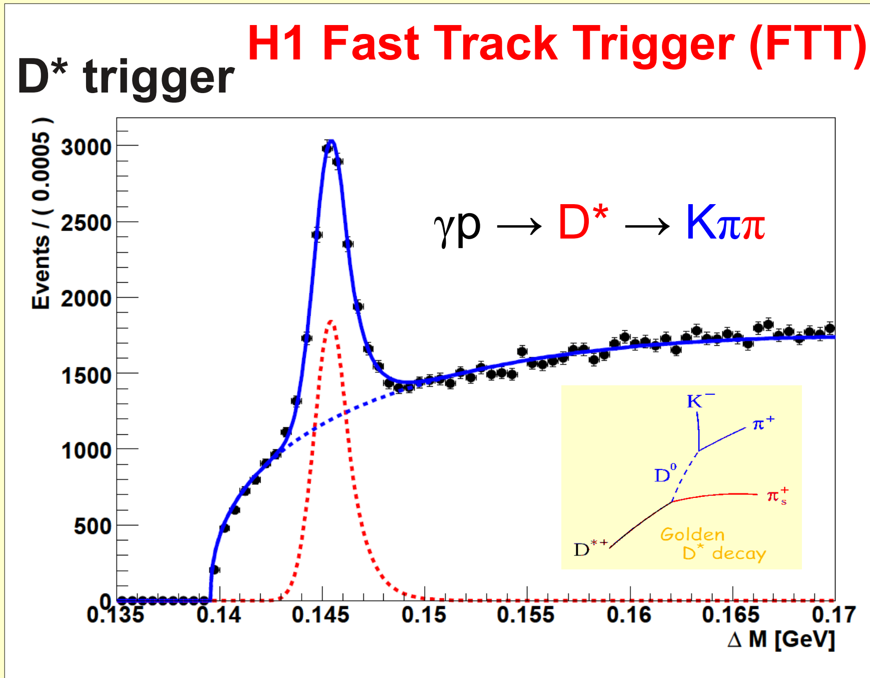


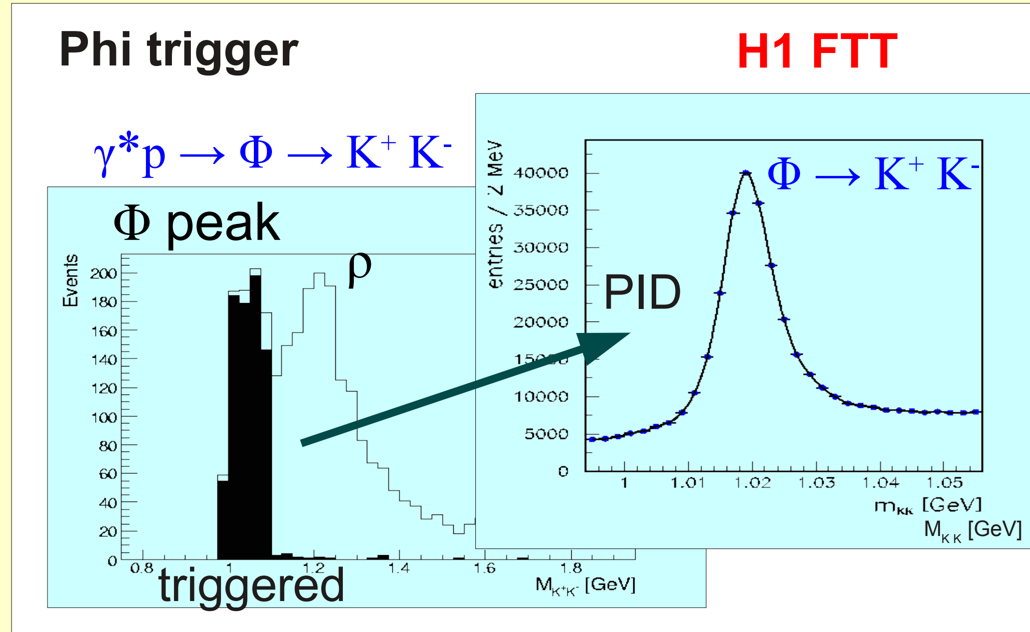
H → Z Z → μμμμ candidate

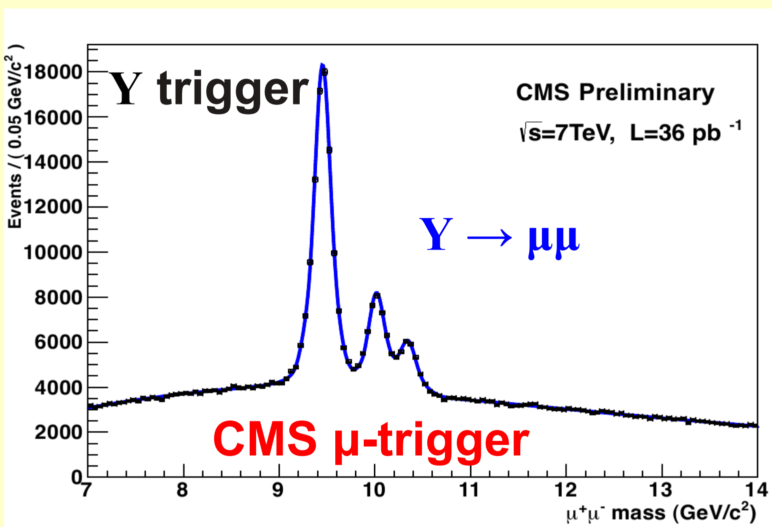


Muons signatures require track triggers!

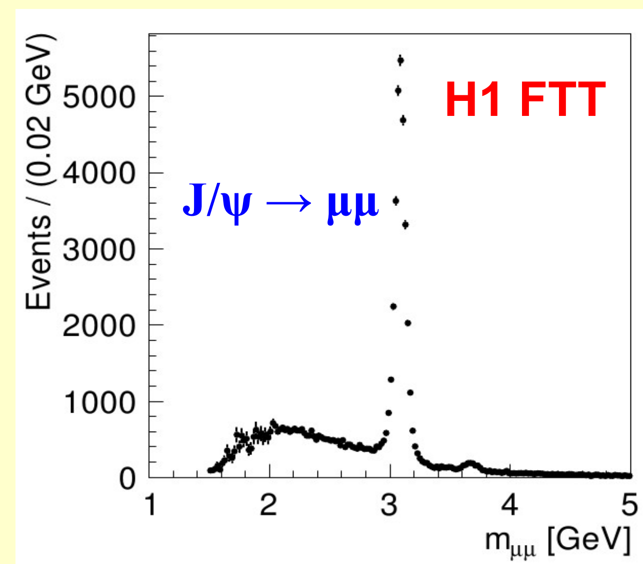
Highly Selective Track Triggers







Track Triggers
- exclusive final states
- low momentum
- lepton identification

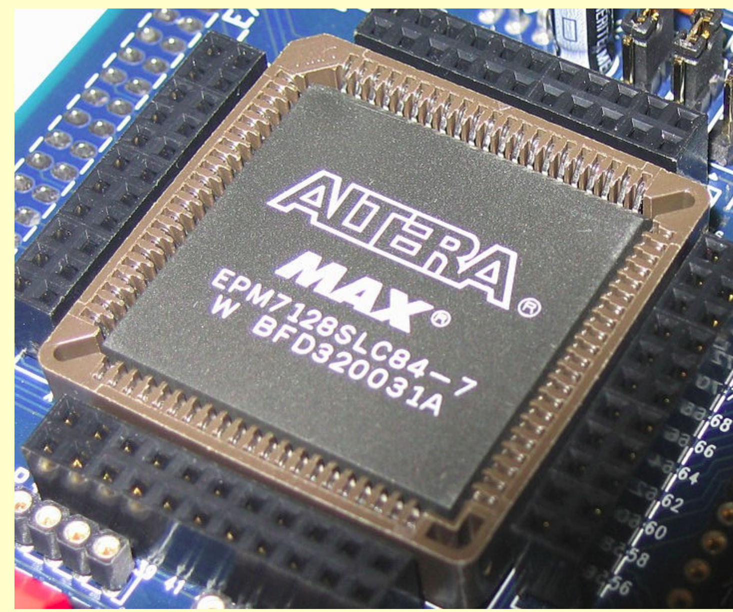


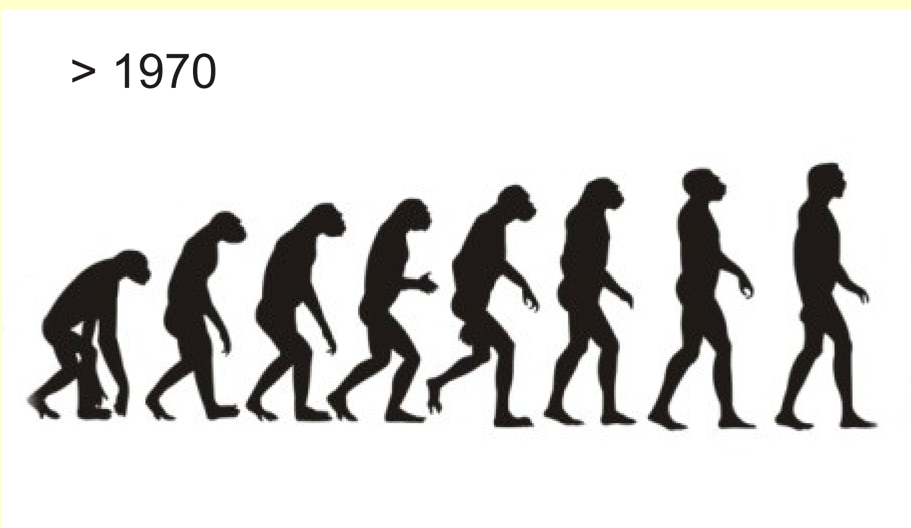
Track Trigger Generations

The birth and evolution of track triggers was and is closely related to the progress in higly integrated circuitry

- Programmable Logic Devices (PLD)
- Gate Array Logic (GAL)
- Complex Programmable Logic Device (CPLD)
- Field Programmable Gate Arrays (FPGA)

Altera CPLD





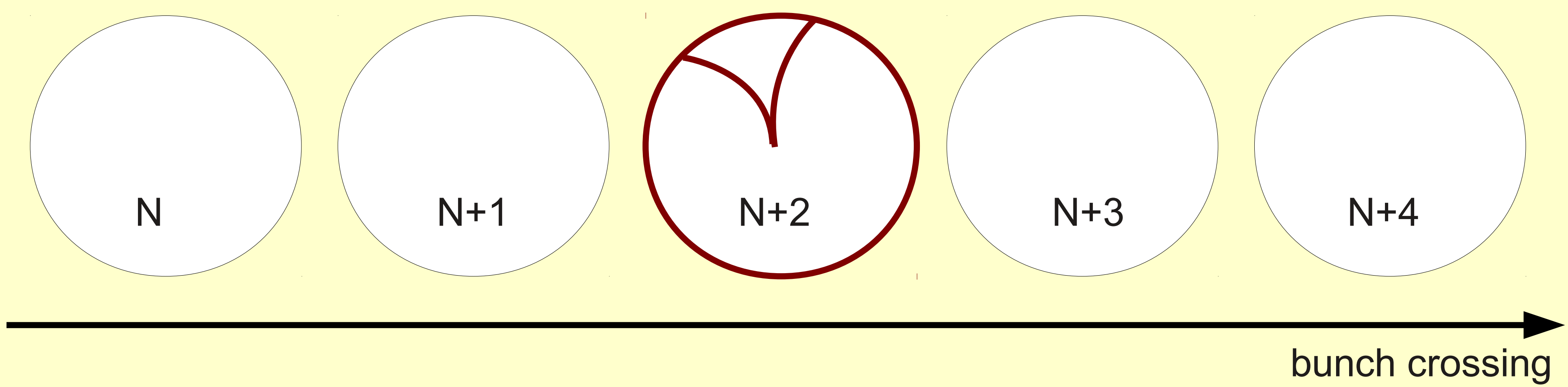
First Generation Track Triggers

IS THERE TRACK?

First Generation Track Triggers

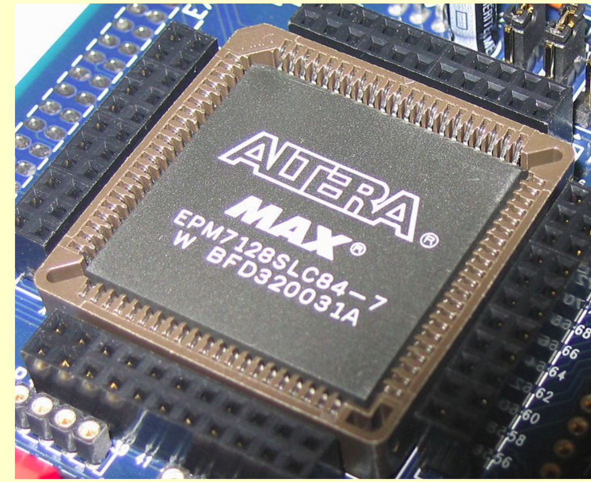
IS THERE TRACK?

Note: early “low” luminosity colliders (e.g. **PETRA**, **LEP**, **HERA**) with mostly **empty collisions**



First Generation Track Triggers

Early track triggers
- **only in two-dimensions (2D)**
- **low track multiplicity**
- **coarse resolution**
- **based on programmable gate arrays**
- **already quite fast (~1 μs)**



Complex Programmable Logic Device

hit pattern →

LUT=Look Up Table

address	result
0x00	0
0x01	0
0x02	0
0x03	1
...	...

track →

trigger information:
- how many tracks
- momentum
- direction (vertex)
- timing
- even topology (back to back)

Next Generation of Track Triggers

ARE THERE GOOD TRACKS?

Next Generation of Track Triggers

ARE THERE GOOD TRACKS?

Paradigm:

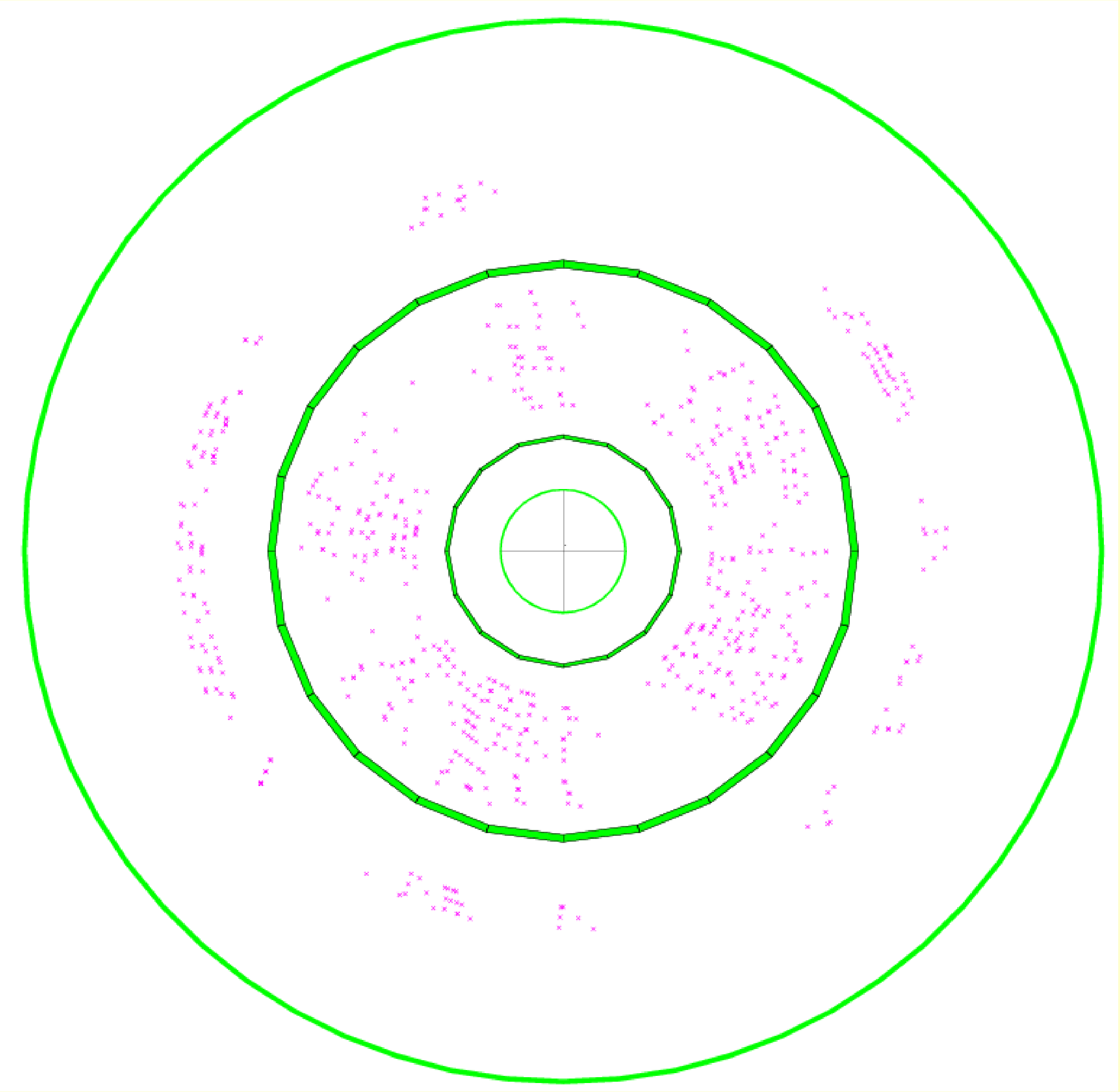
- **good tracks** as signal for **collision events**
- **bad tracks** or unmatched hits indicate **background events**

➨ **Track Quality** and **Quantity**

→ **good resolution required!**

Good or bad event?

Hits as seen in the central H1 drift chambers at HERA



Good or bad event?

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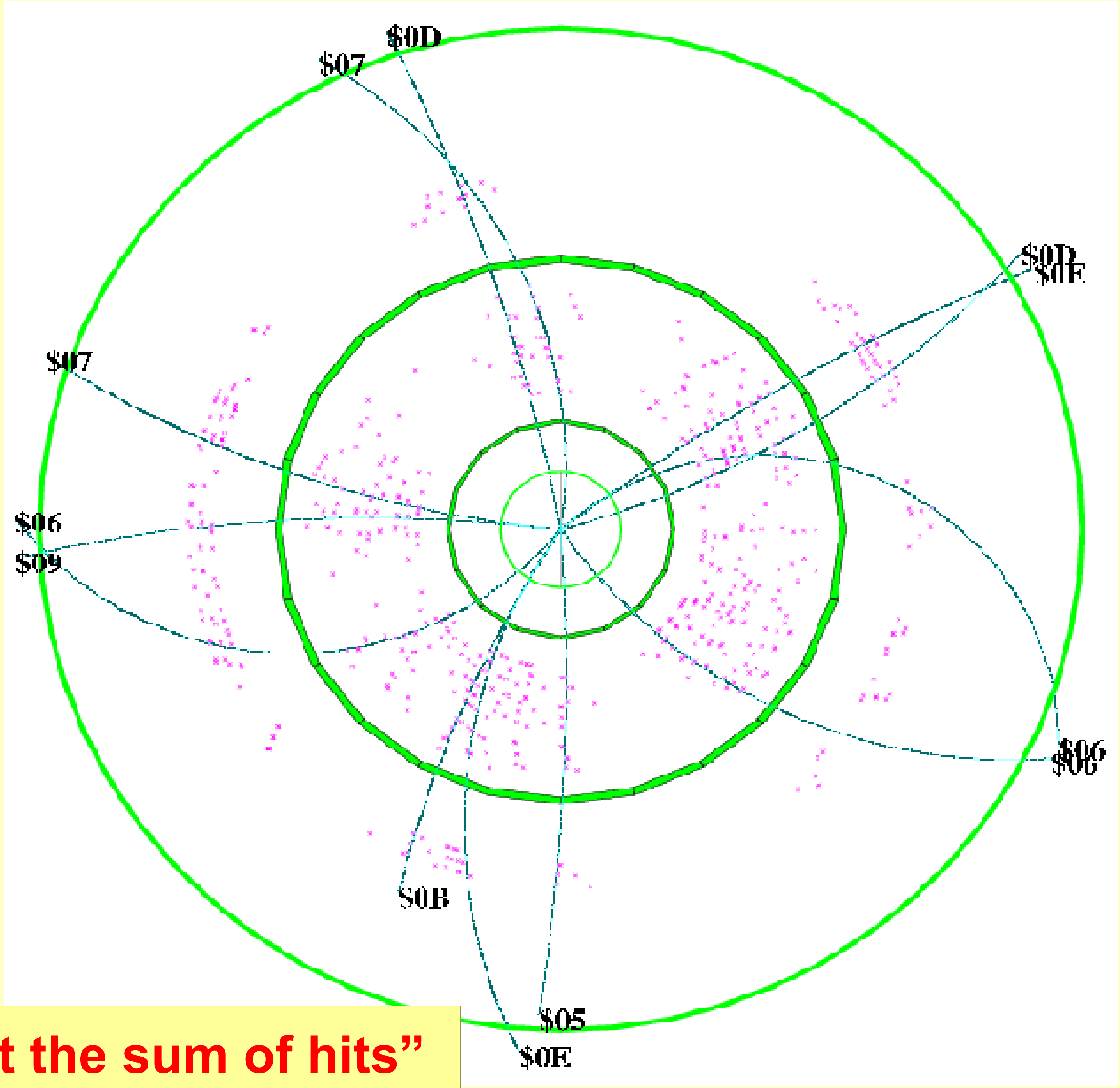


“tracks are more than just the sum of hits”

2nd Generation of Track Triggers

Tight requirements:
- high multiplicity environment
- good resolution
- ➔ high parallelism

Implementation:
- large size FPGAs

FPGA Manufacturers:
- **Altera**
- **Xilinx**
- Atmel
- Actel
- Lattice (AT&T/Lucent)

H1 track trigger system with **>2800 FPGAs**
- L1 latency ~ 2 μs

3rd Generation of Track Triggers

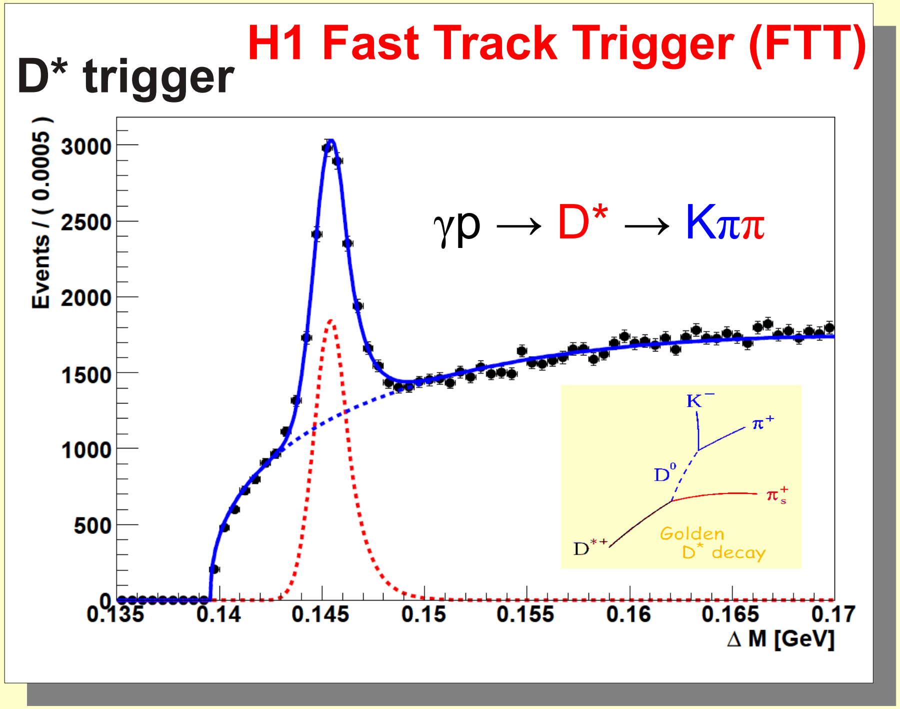
High Precision Track Triggers

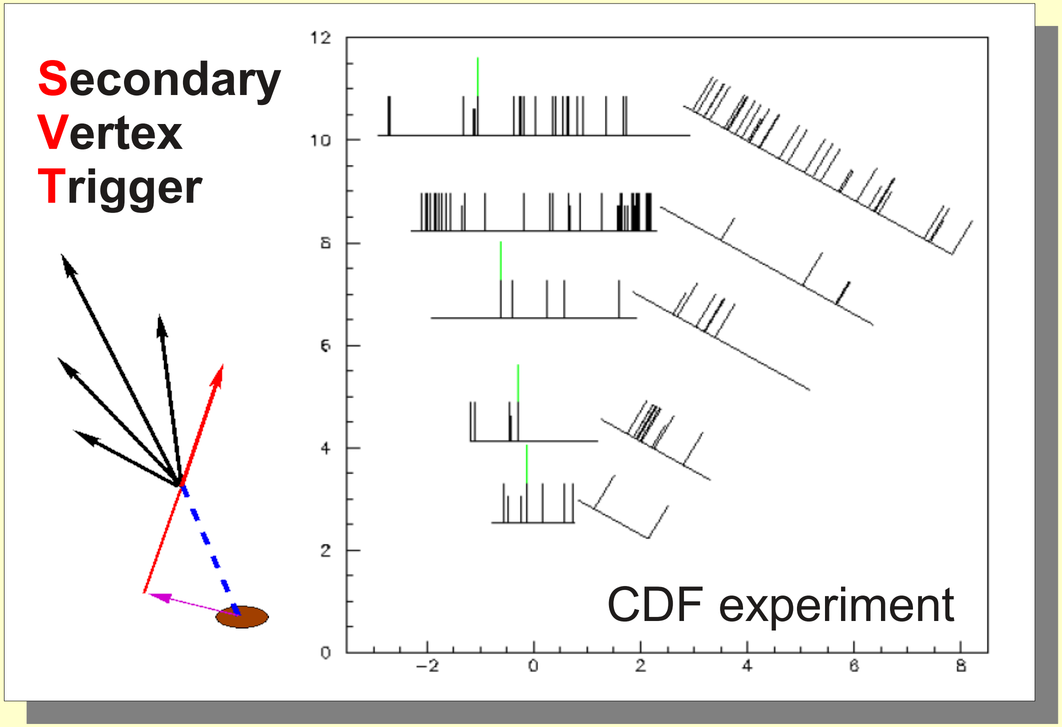
- close to offline reconstruction (3D, precision, PID)

Implementation:

- Content Addressable Memories (CAM)
- Signal Processors (DSPs)
- modernst FPGAs

- hit combinatorics
- fast track fits
- multi-purpose (memory, CAM, DSP)





Why are Track Triggers so fast?

Reconstruction time per track:

- offline (CPU based) ~ O(1 ms)
- trigger (special HW) ~ O(1 μs)

➜ track triggers are about 1000 times faster than offline reco!

Answer:

- dedicated hardware ➜ solve combinatorics
- high parallism ➜ high multiplicities
- simplifications ➜ bandwidth reduction

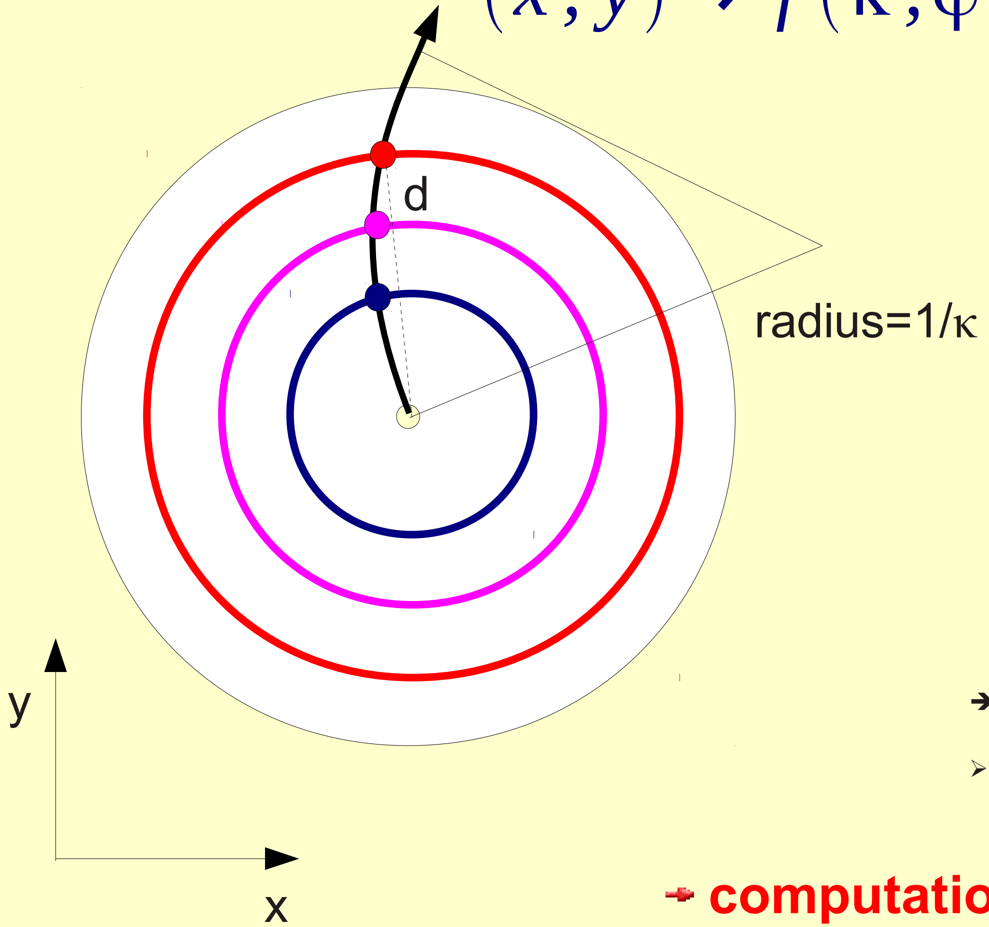
➜ and use of “clever” reconstruction methods

Hough Transformation

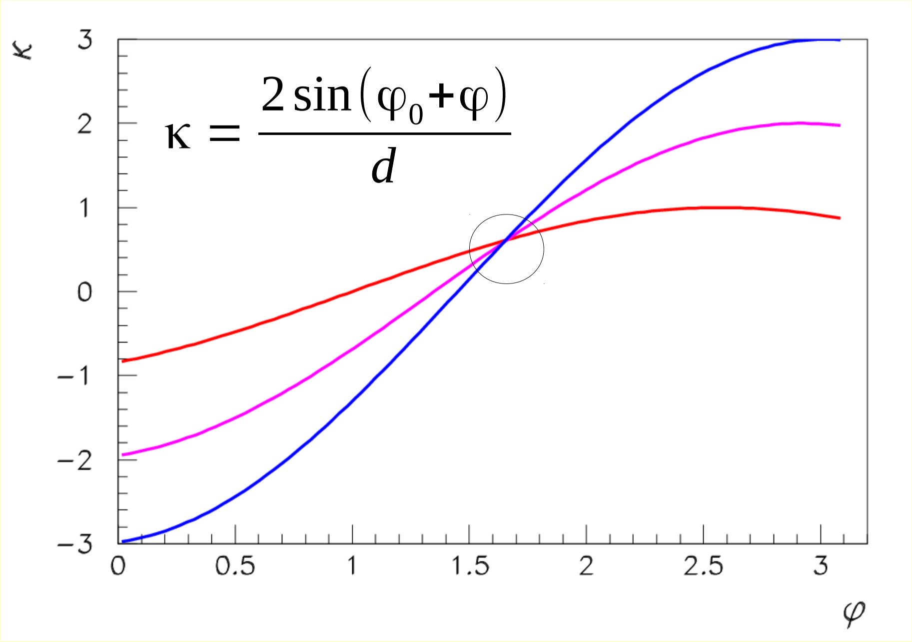
P.V.C Hough, Method and means for recognizing complex patterns, US Patent 3069654.

Transformation from cartesian coordinates to track parameters using primary vertex constraint

$$\left(x, y\right) \rightarrow f\left(\kappa, \varphi\right)$$



Functional relation:



$$\kappa = \frac{2\sin\left(\varphi_0+\varphi\right)}{d}$$

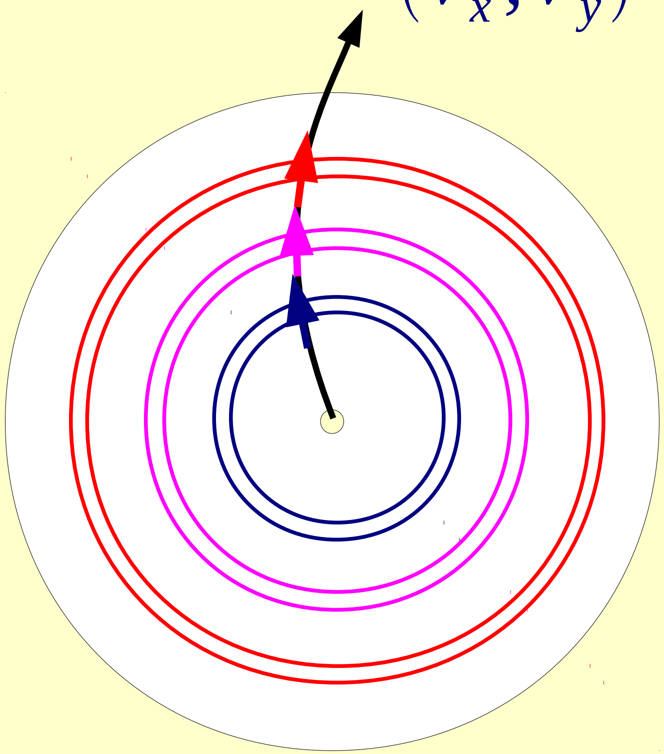
- → intersection point defines track parameters
- ➢ possible implementation: histogram

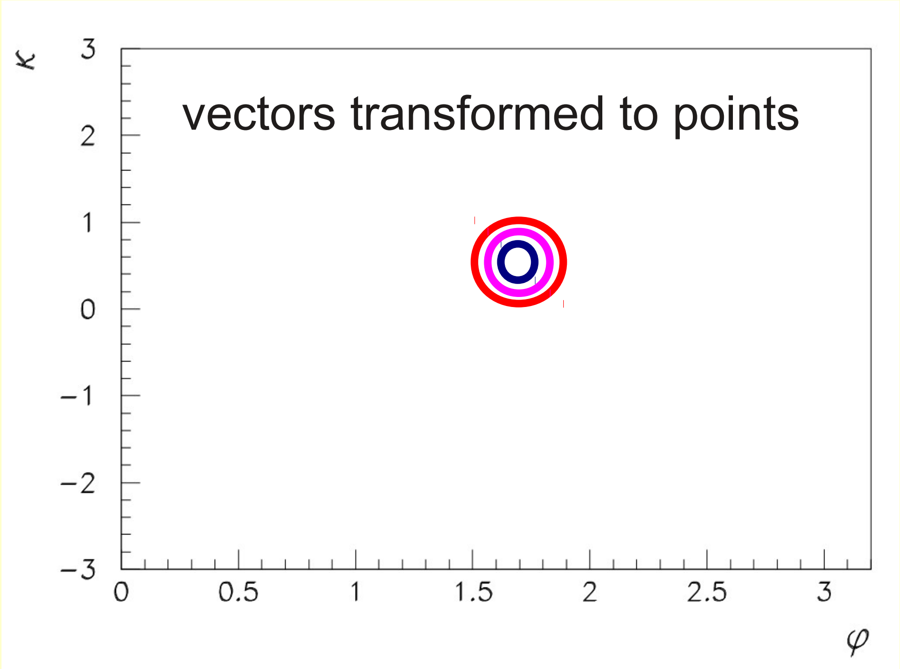
→ **computationally expensive!**

Vector Tracking

Hough transformation of **vectors** to track parameters
using primary vertex constraint

$$(v_x, v_y) \rightarrow (\kappa, \varphi)$$



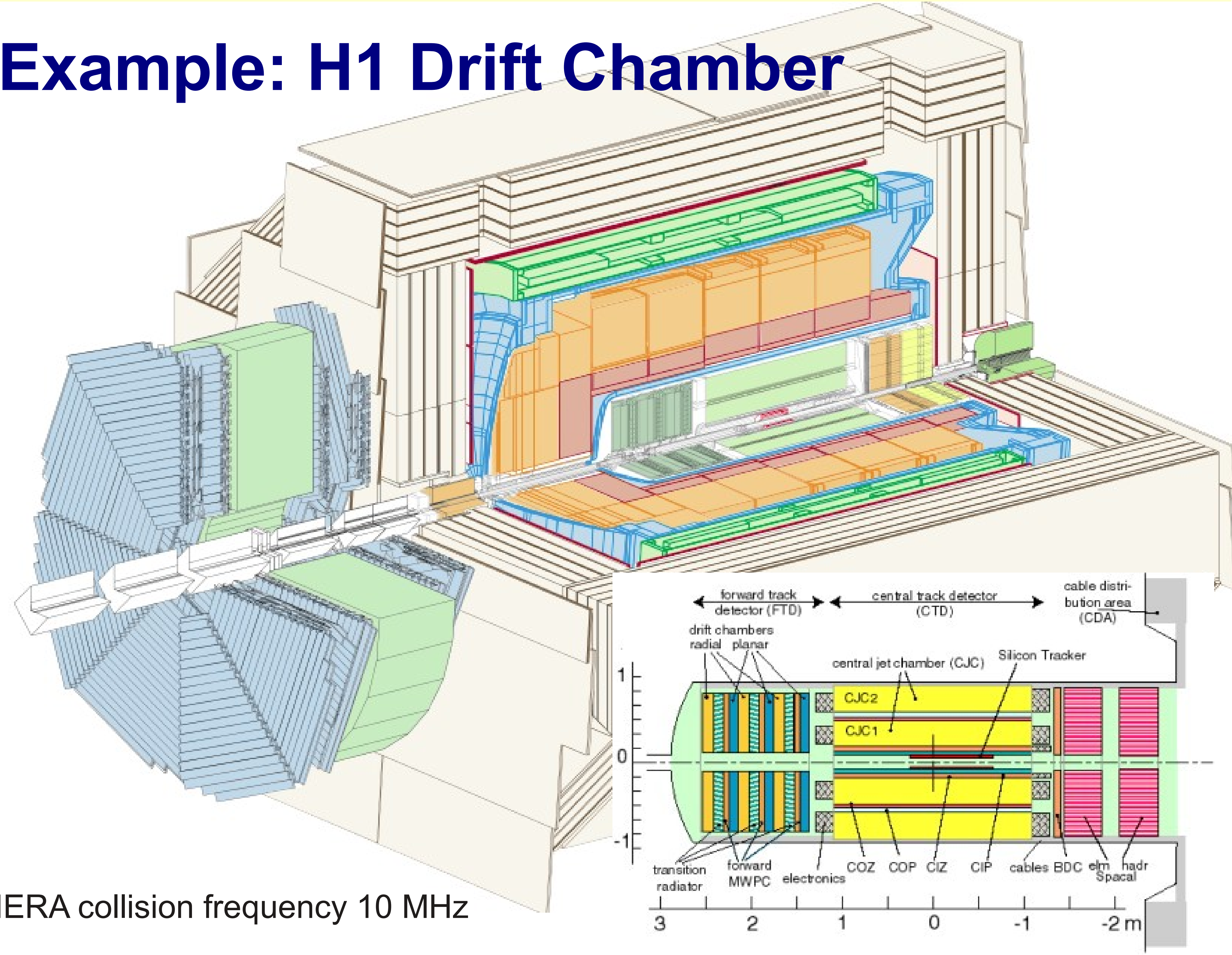


➔ cluster position defines track parameters

vectors obtained from coincidences
in e.g. double layers

computationally easy (e.g. sliding window)
and can be parallised!

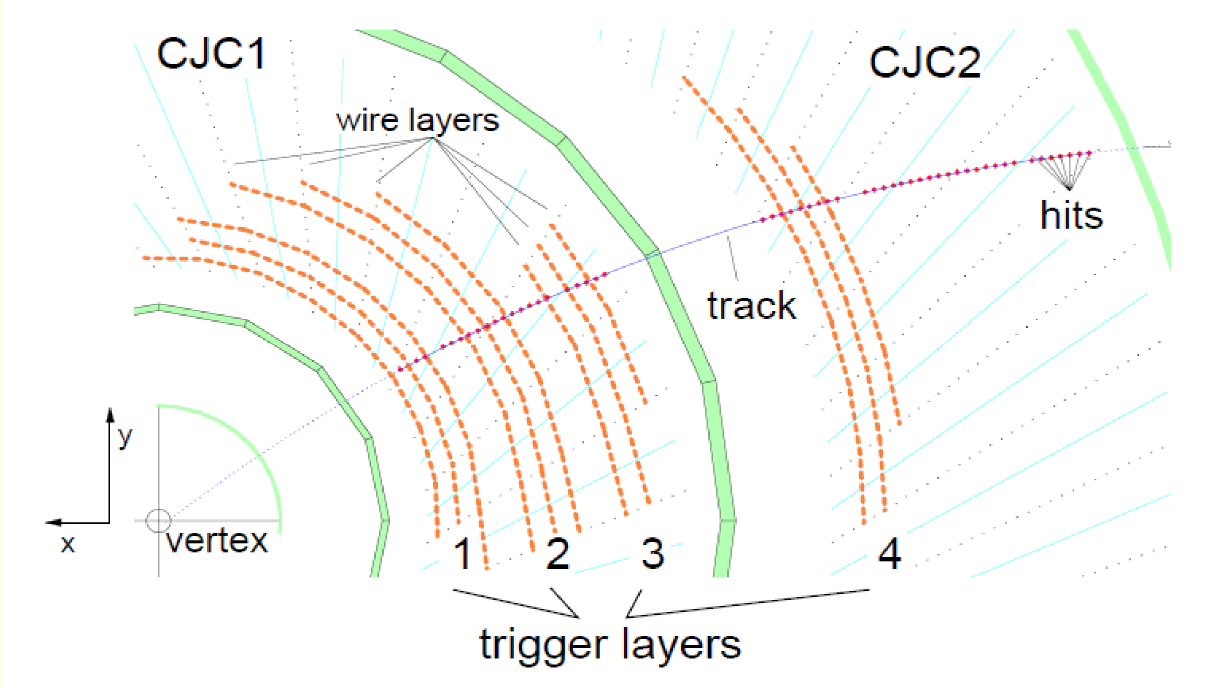
Example: H1 Drift Chamber



HERA collision frequency 10 MHz

H1 Fast Track Trigger (2004-2007)

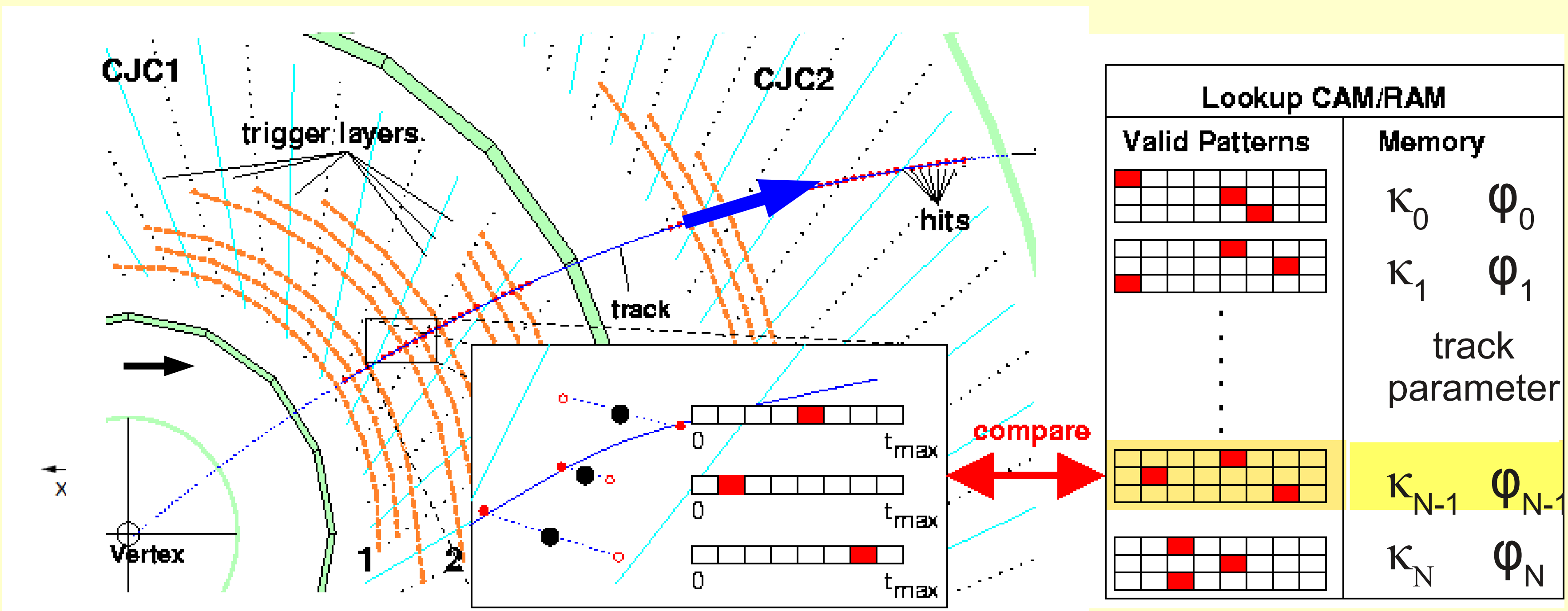
L1 bandwidth is limited → use only subsample of drift chamber layers 12/56



H1 Fast Track Trigger (2004-2007)

L1 bandwidth is limited → use only subsample of drift chamber layers 12/56

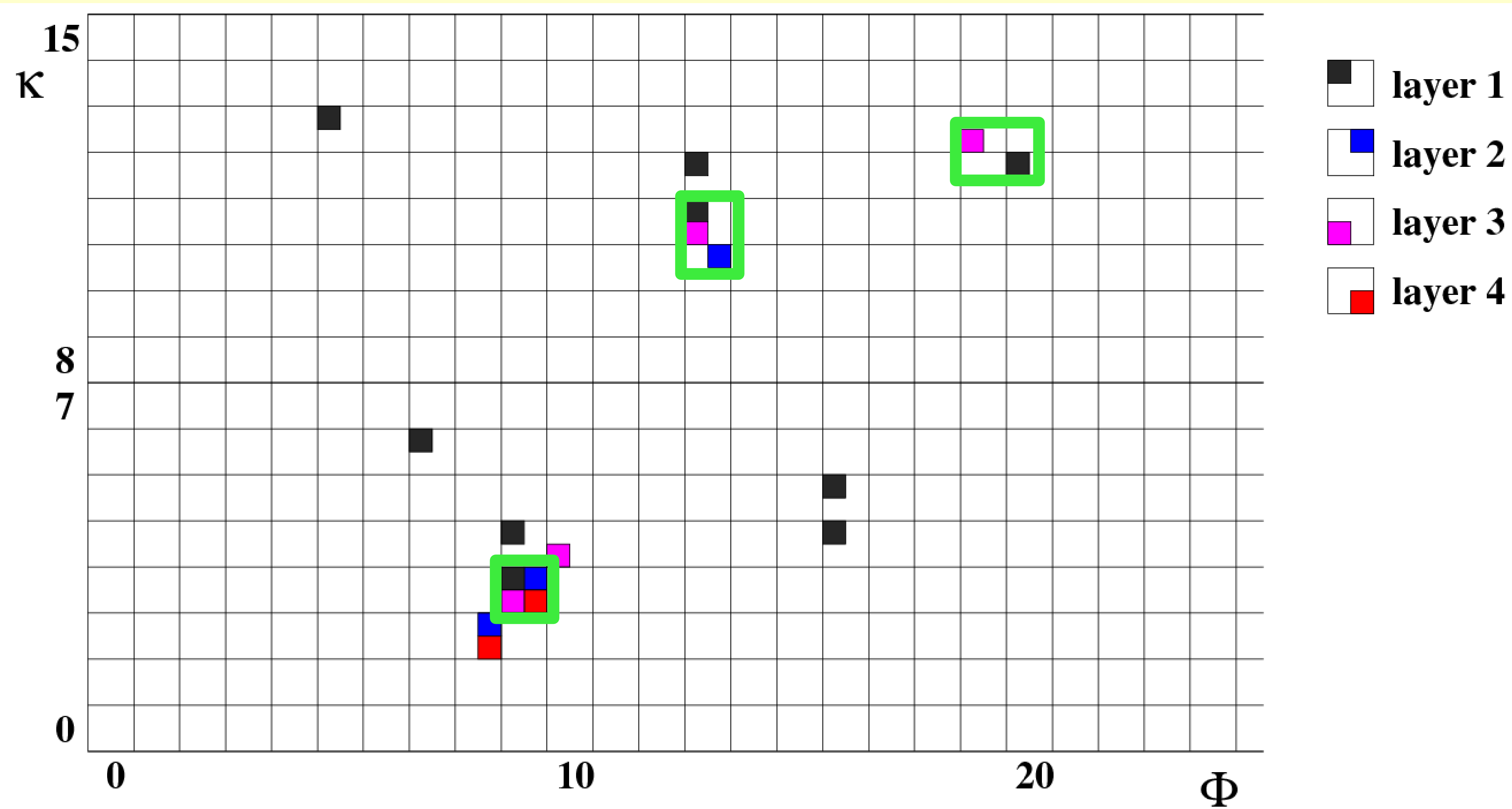
Search for **hit combinations** (track segment=vector) using **Content Addressable Memories** and get associated track parameters (**κ,φ**) (<< 1μs)



FTT: $4 \cdot 10^{12}$ pattern comparisons / second!

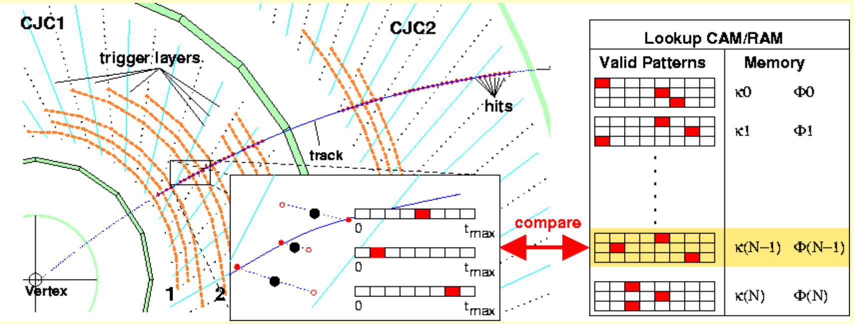
H1 Fast Track Trigger – L1 Linker

- total histogram size 16 x 60 (<< 1μs)
- cluster search: use big FPGA to localize cluster (960 bins in parallel)

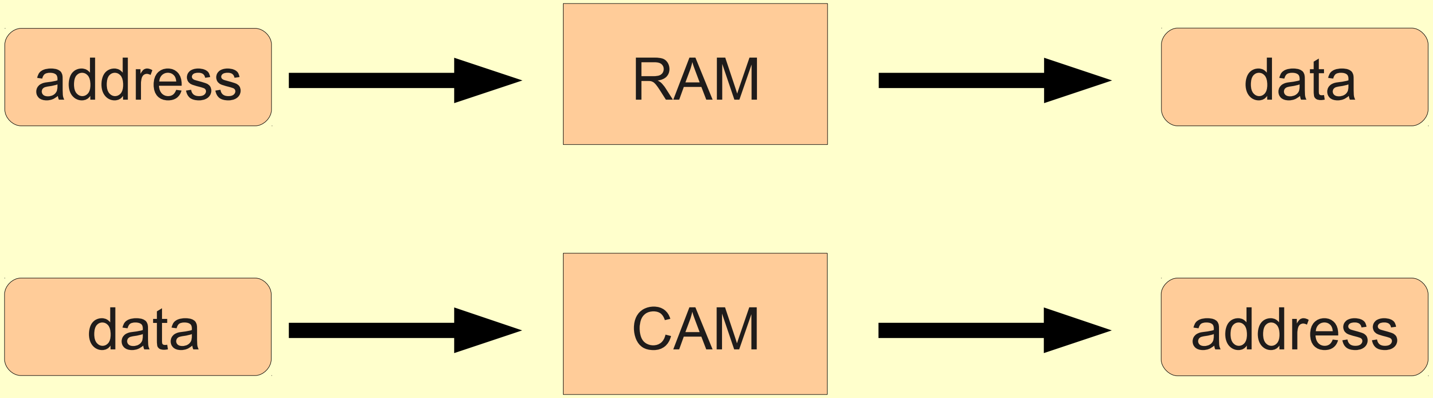


Content Addressable Memory

FTT: CAM used for fast track segment finding to solve combinatorial problem

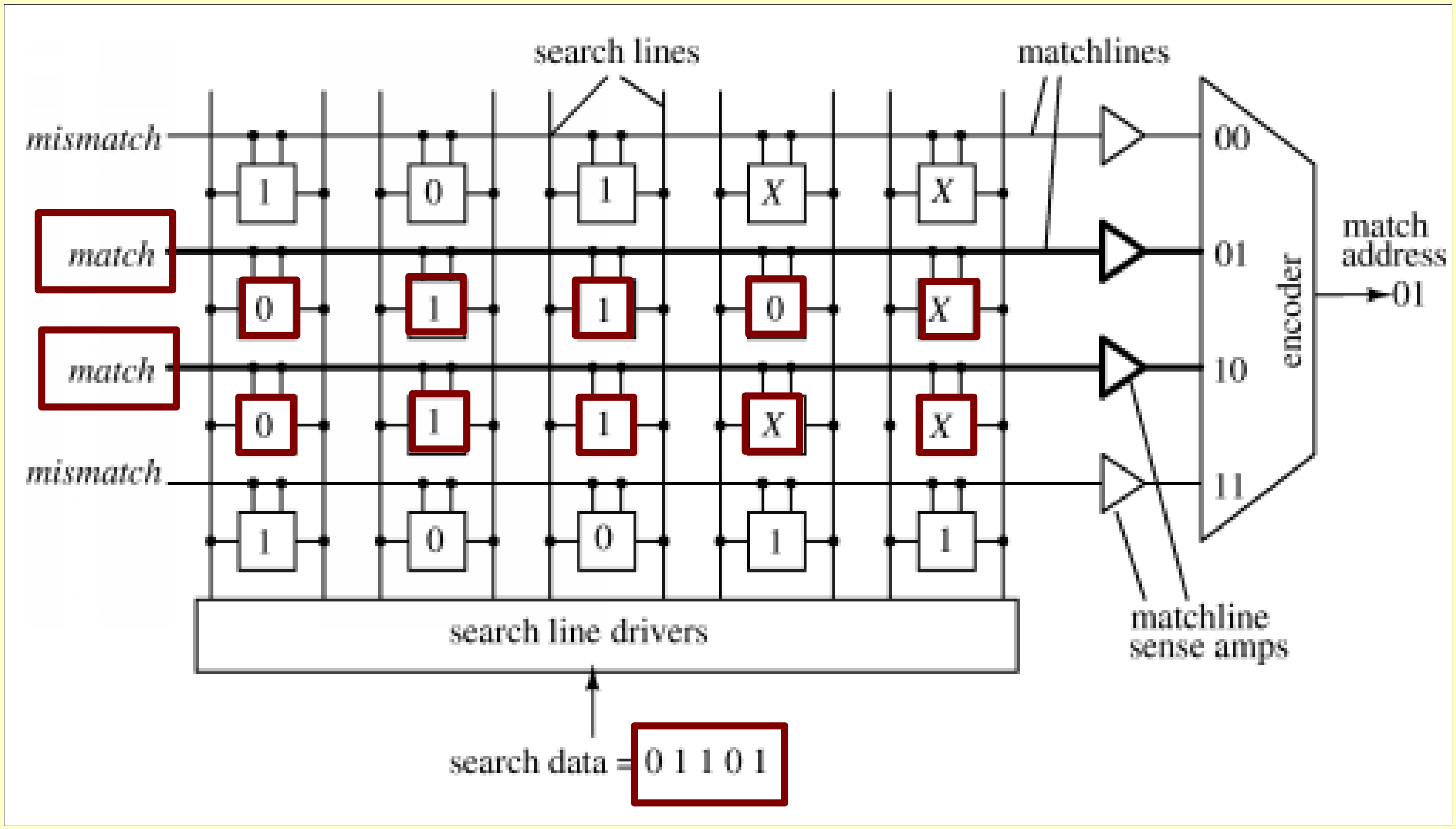


simply spoken: **a CAM is an inverse RAM**



Ternary Content Addressable Memory

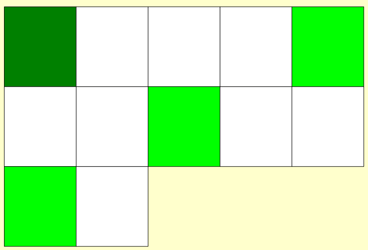
Feature: “Don't Care” Bits

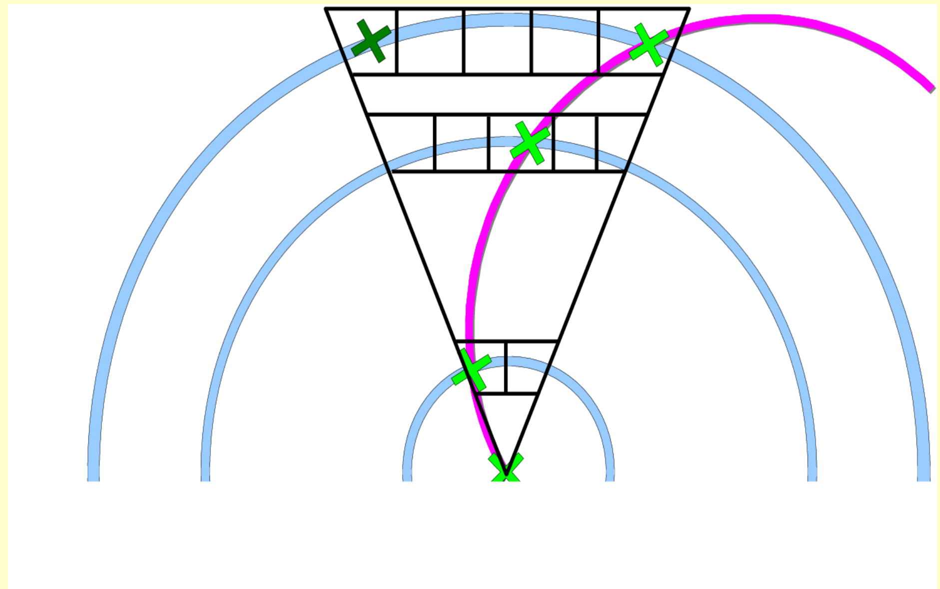


Ternary CAM Feature “Don't Care” Bits

Example:

hit pattern





CAM data: **unencoded** hit representation

X	X	X	X	1
X	X	1	X	X
1	X			

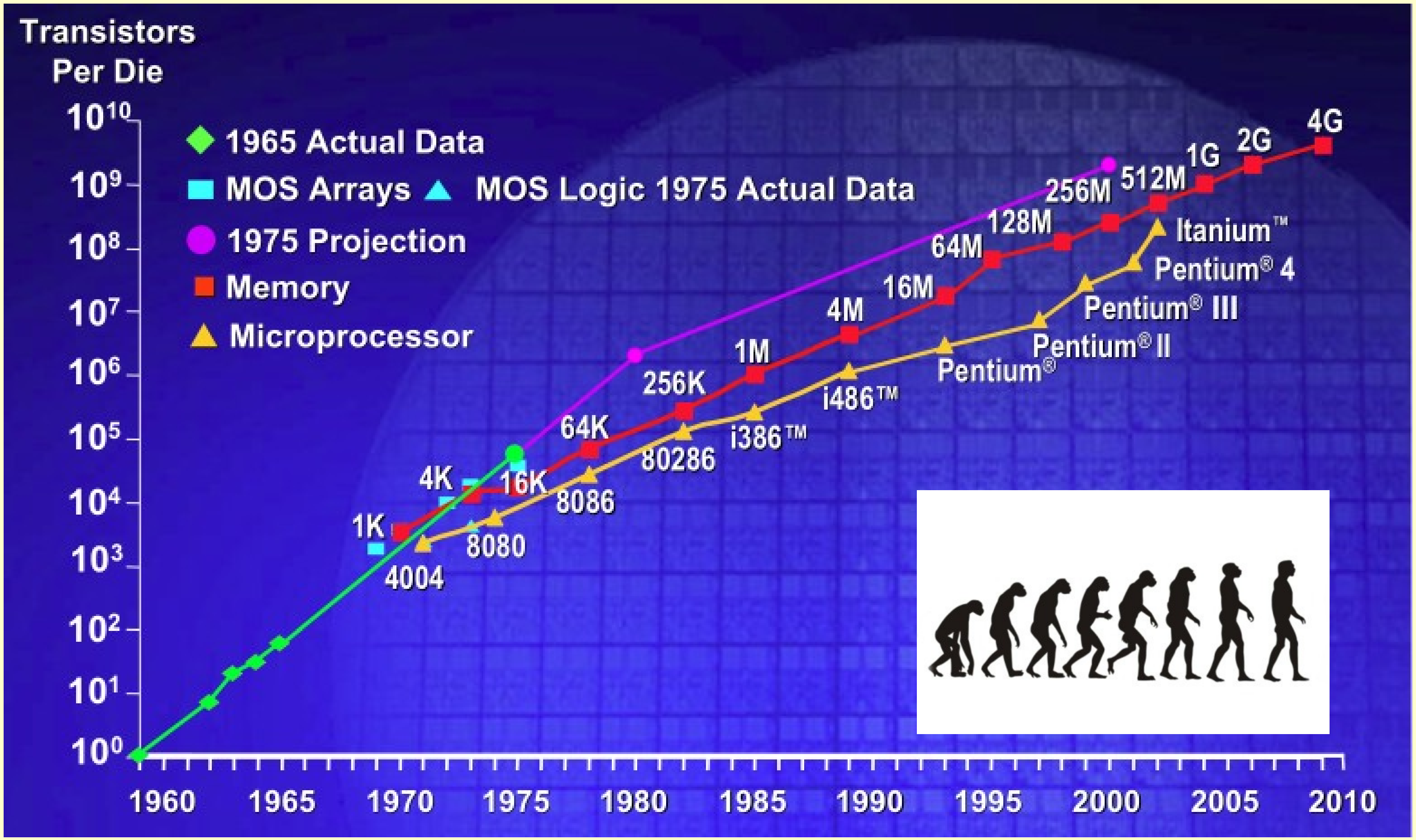
→ this pattern would match

Bonus:

X	X	X	X	1
X	1	0	X	X
1	X			

also possible to veto specific hit positions (→resolve ambiguities)

Evolution in Circuitry



Memories with more than 1 billion transistors!

Scaling of First Level Track Triggers

	CDF-XFT	H1-FTT L1	ATLAS L1TT *
Bunch Cross rate	132 ns	96 ns	25 ns
Latency	5.5 μs	2.3 μs	2.4 μs
Processing time	1.5 μs	0.5 μs	~1.0 μs
Input	16000 wires	450 wires	**25 mill. strips**
Layers used	12 x 4	3 x 4	2 x 3
Bandwidth IN	183 Gbit/s	670 Gbit/s	**900 Tbit/s**
Min p_T	1.5 GeV/c	0.1 GeV/c	**~10 GeV/c**
Max $1/p_T$	0.6 $(GeV/c)^{-1}$	10 $(GeV/c)^{-1}$	**~0.1 $(GeV/c)^{-1}$**
regions	24	30	**10000**
patterns/region	~350	3072	**~3 million**
Max. tracks	288	~50	~10000
operation	2001-2013	2004-2007	2020?

*self seeded

max. resolution

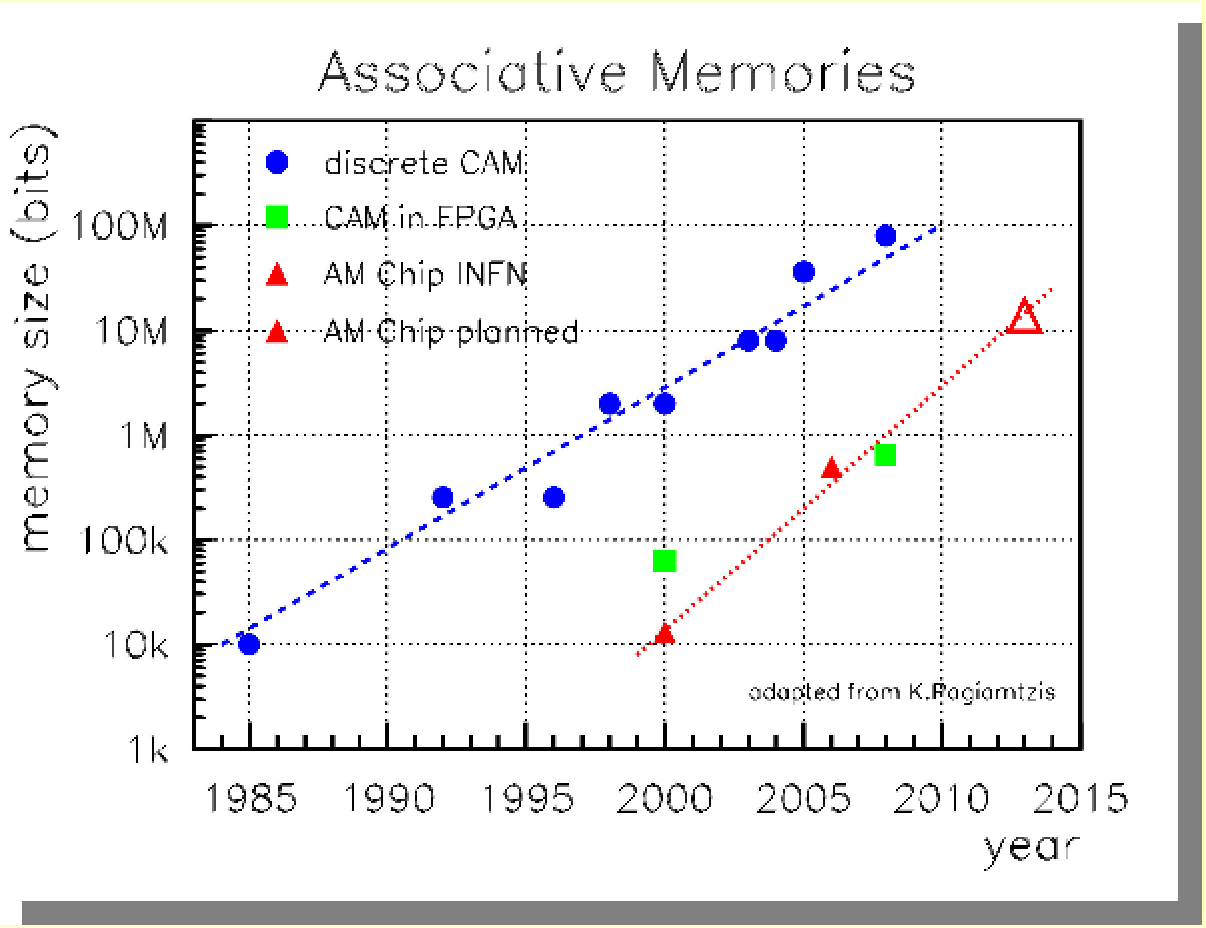
LHC: two-three orders of magnitude increase in

- number of **channels**/bandwidth
- track **multiplicities**
- number of **patterns**

Evolution of Associative Memory Chips

… this goes along with a dramatic increase in CAM memory size

CAMs mainly used for
network routing/switching



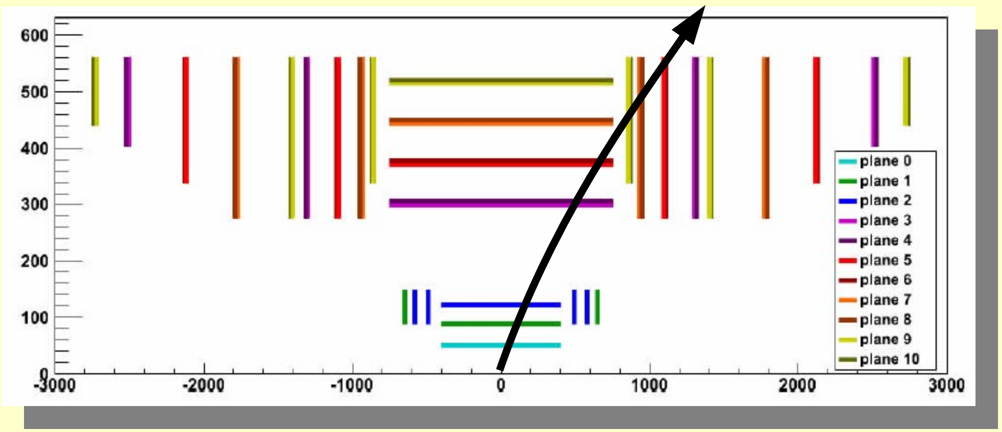
most recent:

NLA 12000 KBP
(Broadcom, 28nm)

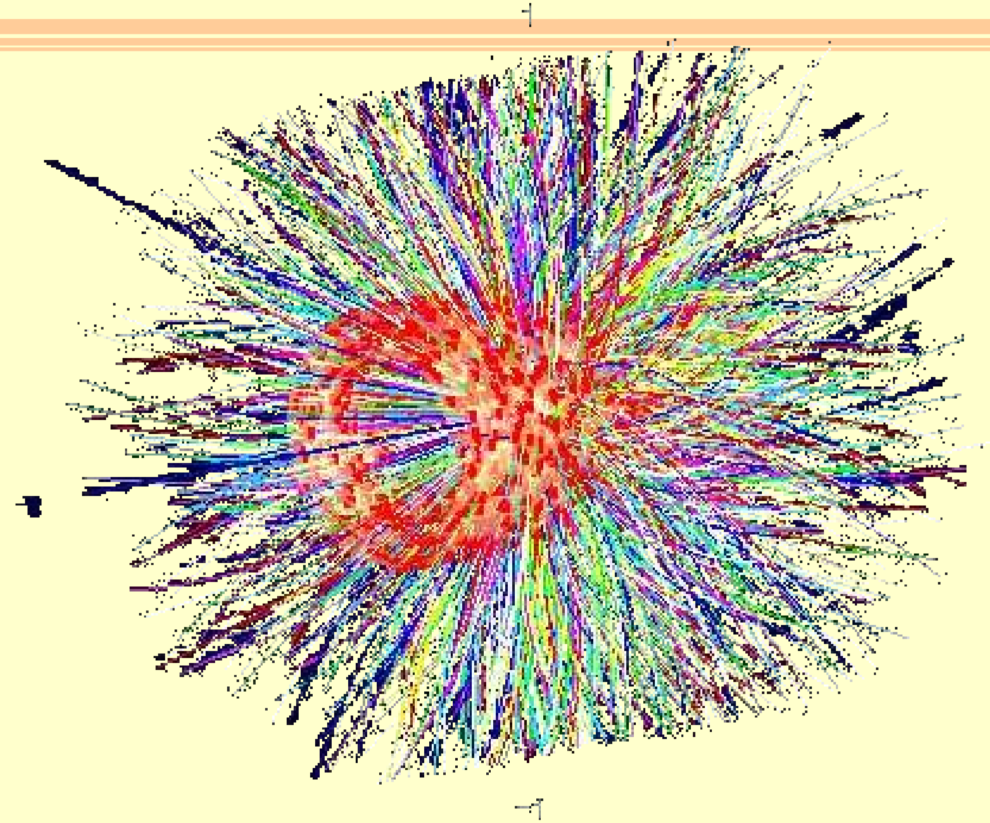
→ $2.4 \cdot 10^9$ search decisions/s
→ 2 million addresses (128 bit words)
→ aggregate bandwidth 300 Gbps

Fast Track Triggers for HL-LHC?

Brute force:
use CAMs also for global hit linking



ATLAS silicon tracker



Installion of 1000-10000 modern CAMs solves all track reconstruction problems

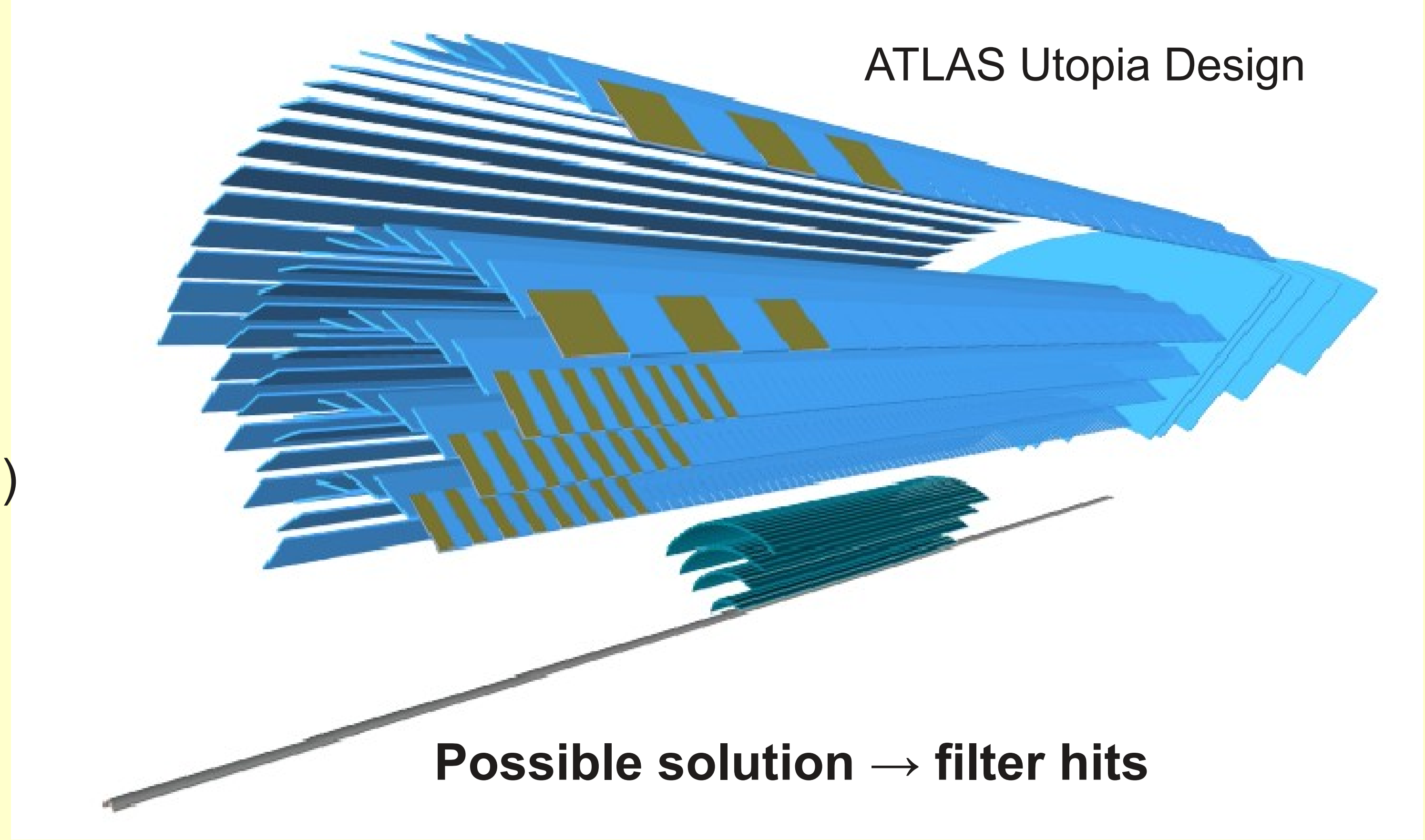
- **speed (latency)**
- **bandwidth**
- **memory size**

Fast Track Triggers for HL-LHC?

if one can get access to the data...

Data Bandwidth Problem at Hi-LHC

High luminosity LHC: L ~ 10^{35} $cm^{-2}s^{-1}$



short strips alone
(25 million channels)

→ **900 Tbit/s**

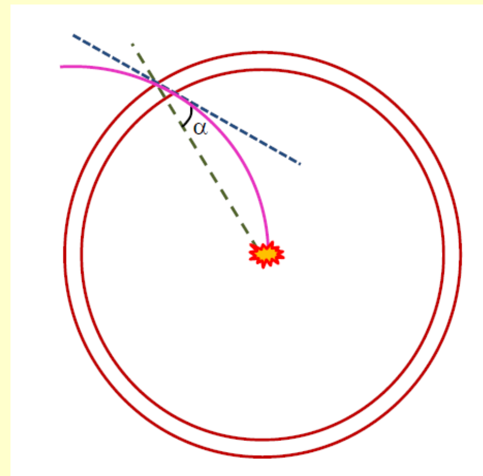
ATLAS + CMS:

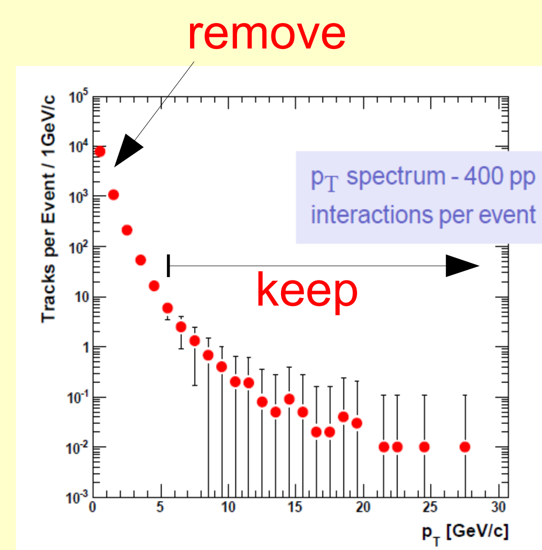
impossible to get all hit data out with nowadays readout technologies!

(without impairing detector performance)

Reduction of Tracker RO Bandwidth

Perform on-detector rate reduction (filtering):

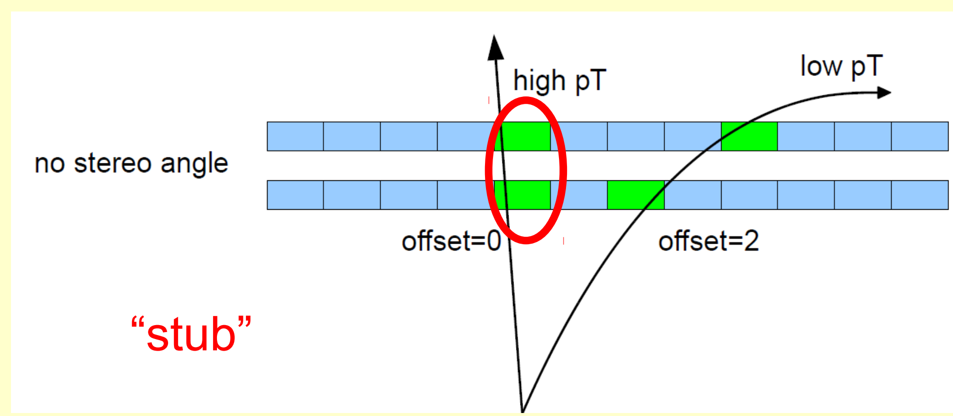




Use Vector Tracking!

+ beamline constraint

stacked layers:



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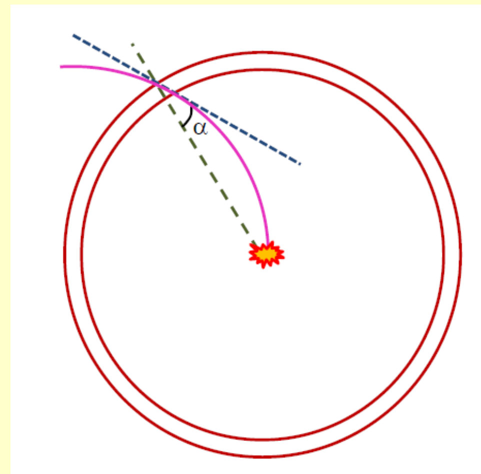
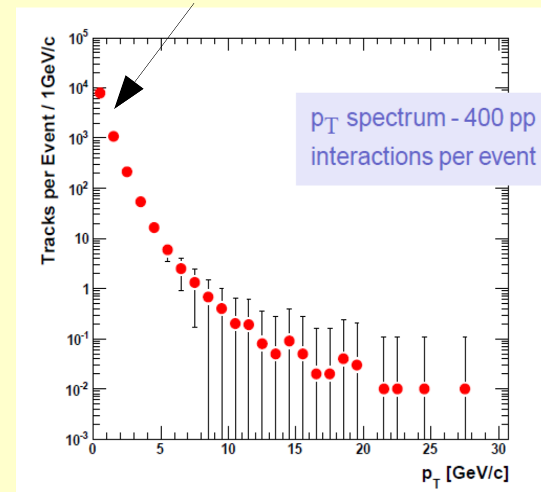
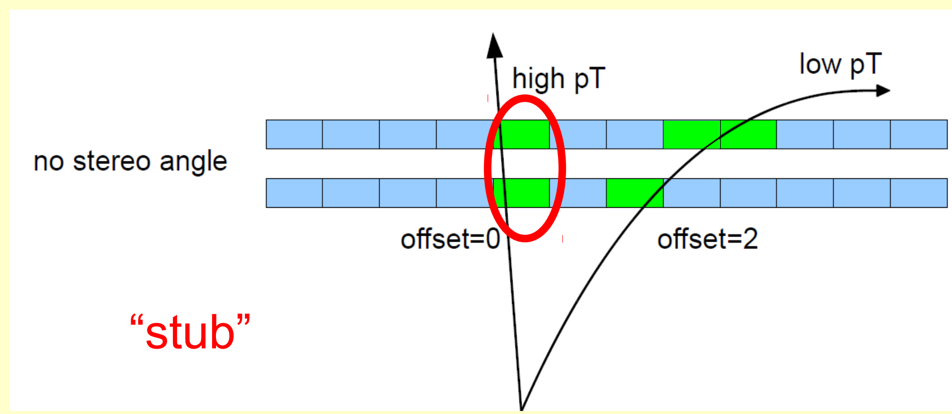


remove



stacked layers:

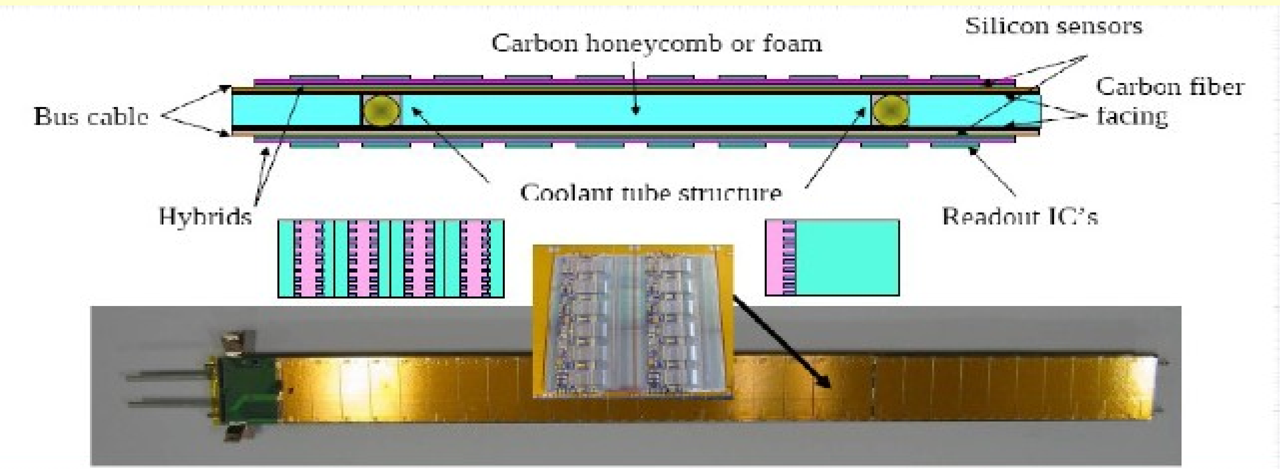


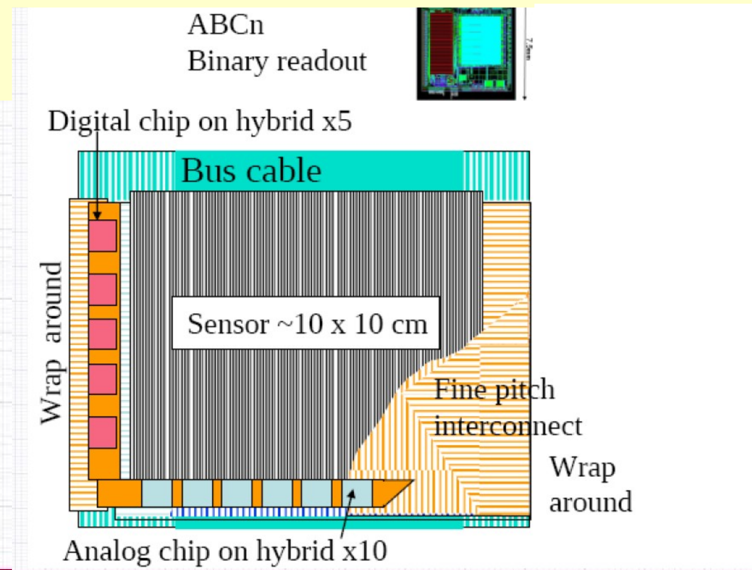
can also exploit cluster size

Local Coincidence (Stub Reco)

ATLAS

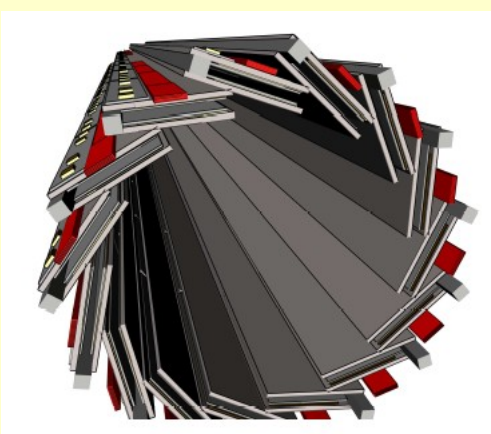
→ remove stereo angle in double strips (not baseline design)

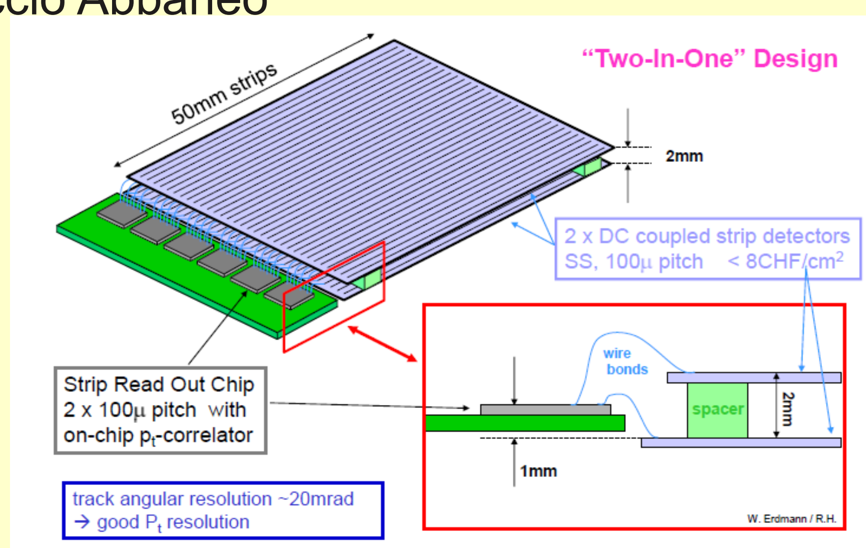


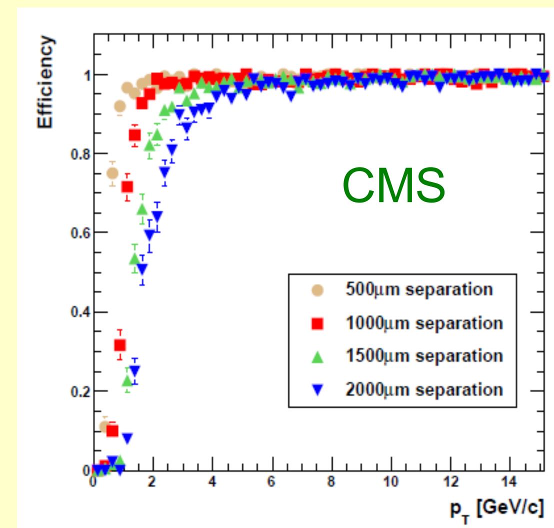


CMS

→ talk by Duccio Abbaneo



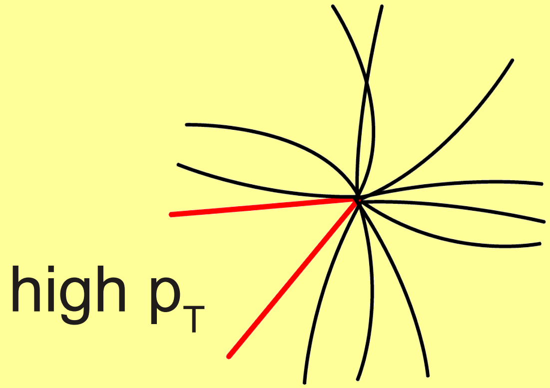




The Two Concepts for Hit Filtering

"Self Seeded Track Trigger"

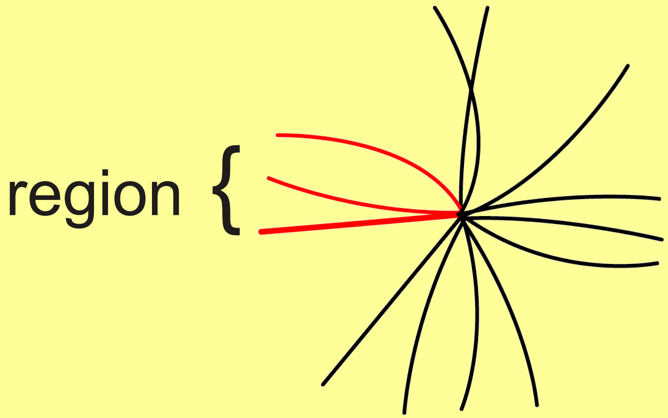
- momentum filter of clusters
- cluster size + local coincidence
- special HW design required
- all high p_T tracks



baseline for CMS (option for ATLAS)

"Region of Interest"

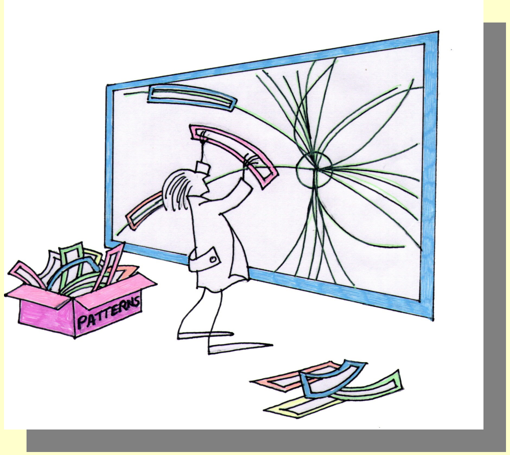
- spatial cluster filter
- external trigger information (calo, muon, ...)
- new level L0 trigger required
- all tracks in regions



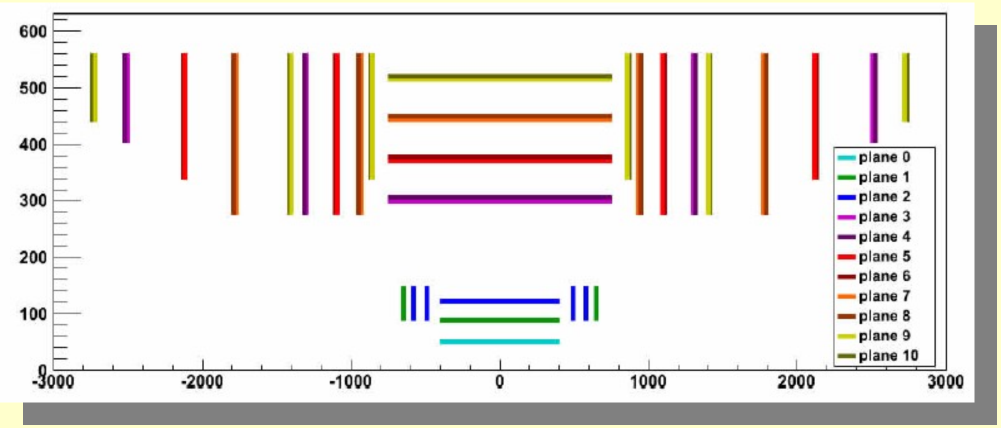
baseline for ATLAS L1 Track Trigger

ATLAS Fast TracKer Project (FTK)

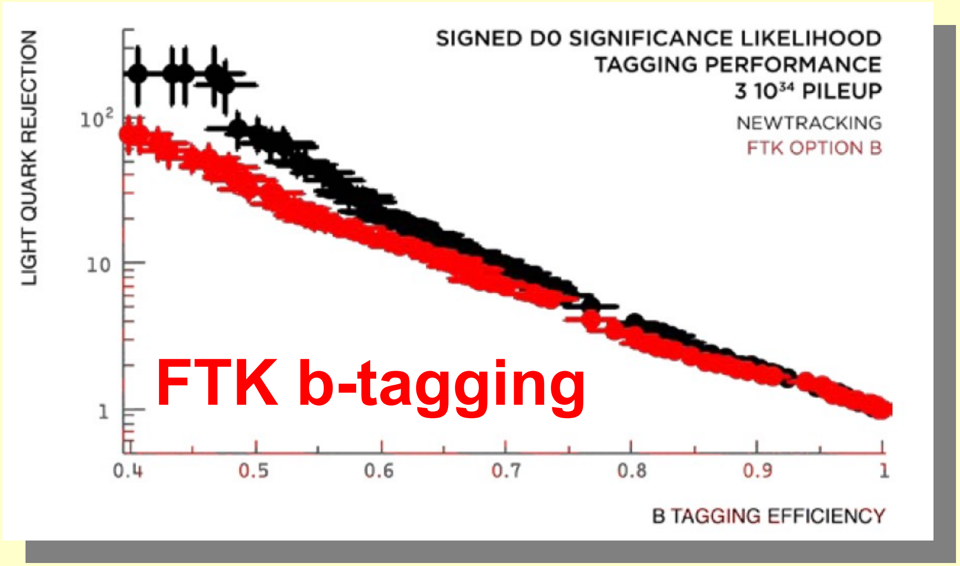
- Dedicated hardware to accelerate track reconstruction at second trigger level (L2)
- FTK exploits:
  - fast pattern **lookup > 800 M patterns** (AM chip)
  - fast track paramteter fits **within 50 μs** (DSPs)



ATLAS silicon tracker (phase I)



light quark rejection vs. efficiency

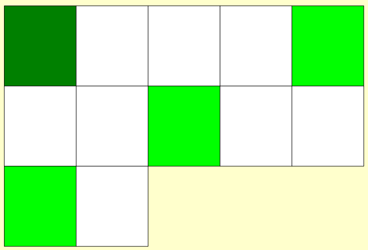


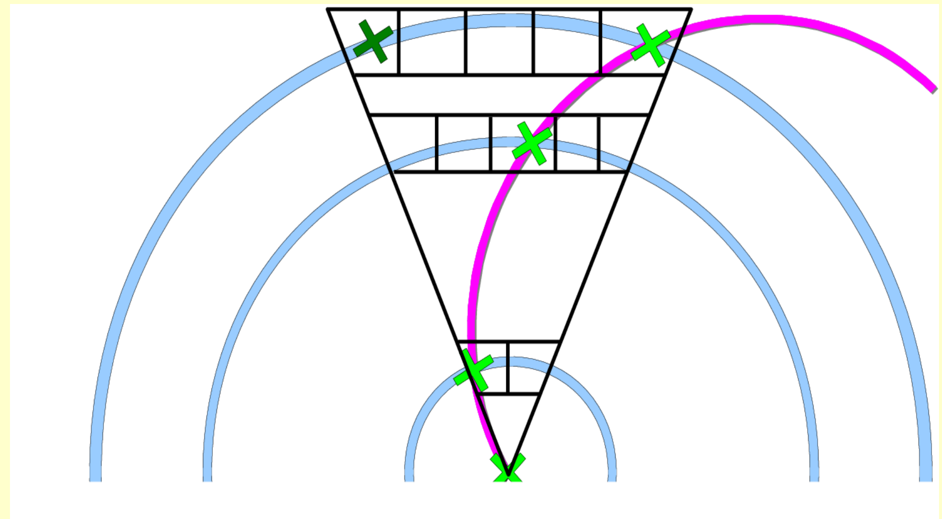
→ FTK talk by Björn Penning

Feature “Don't Care” Bits

Example:

hit pattern





unencoded hit representation

1	0	0	0	1
0	0	1	0	0
1	0			

↓

CAM

encoded hit representation

0x11 = b10001

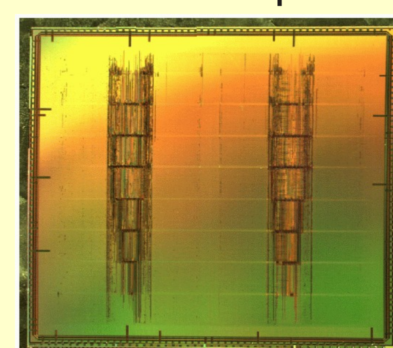
0x04 = b00100

0x10 = b10000

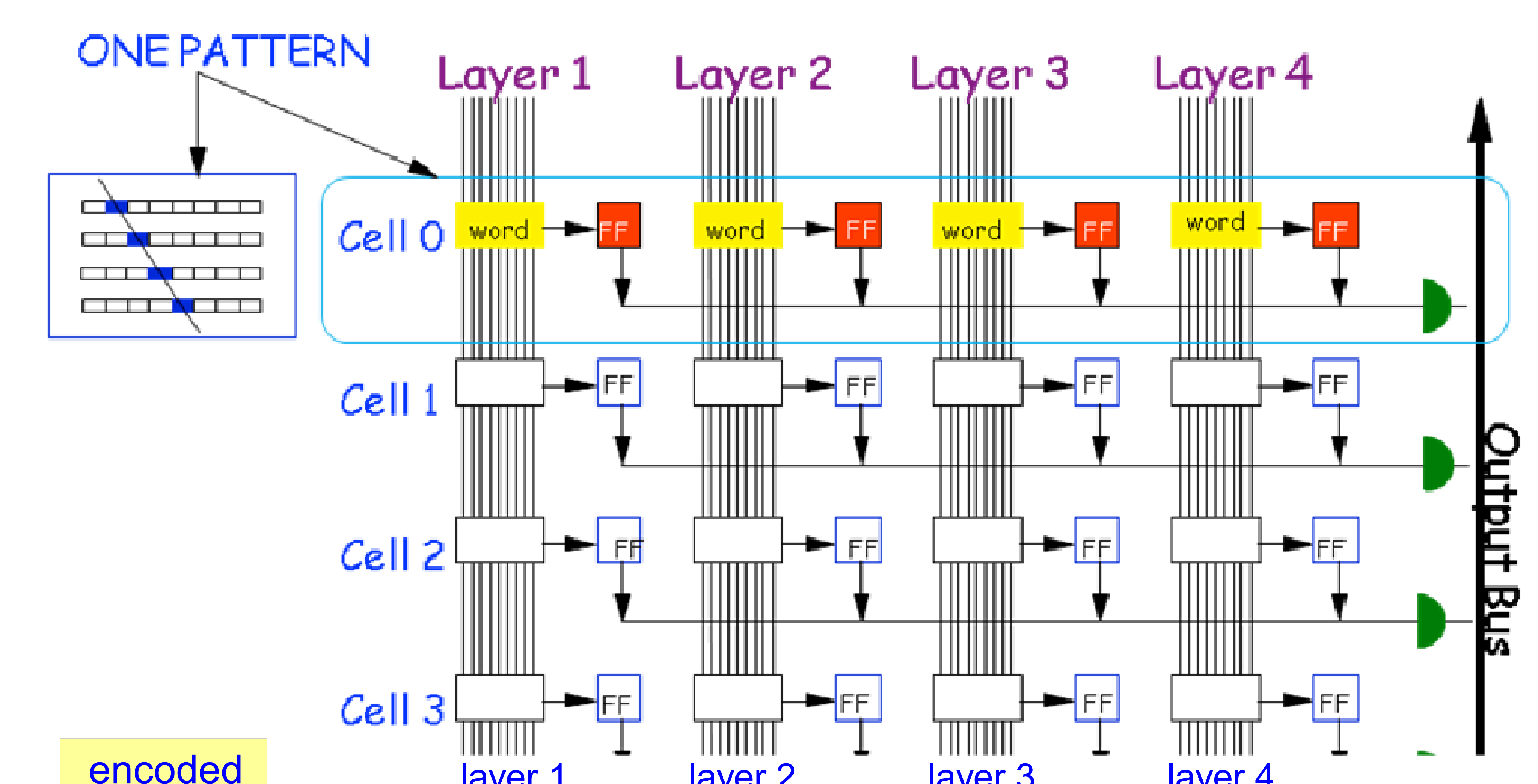
↓

CAM

AM chip



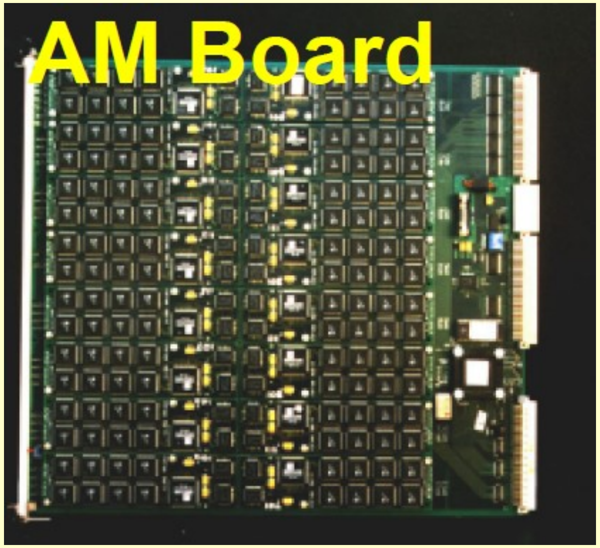
Associative Memory Chip

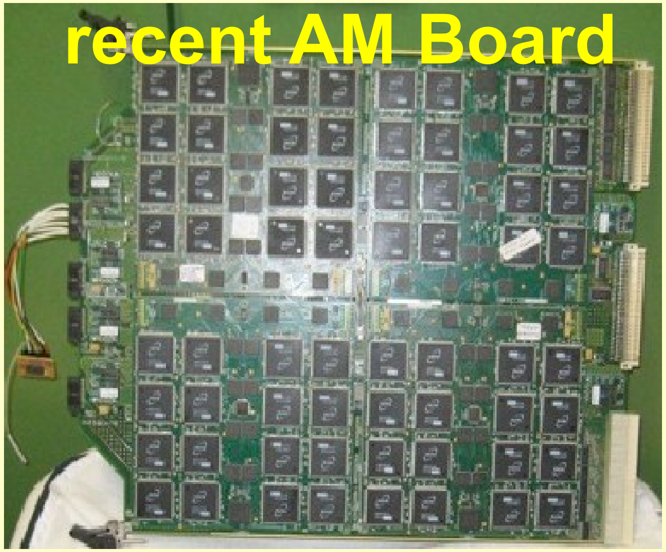


encoded address inputs

- sequential input of hits
- valid hit combinations are found "on the fly"

AM Chip Evolution





<u>Year 2000:</u>

- 256 chips
- **128** patterns/chip

~30k patterns/board

<u>Year 2006:</u>

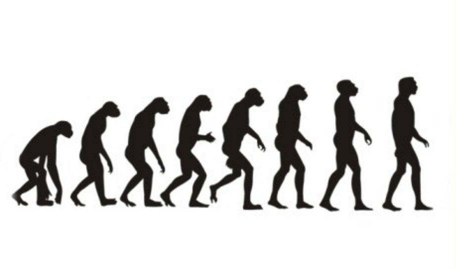
- 128 chips
- **5000** patterns/chip

~500k patterns/board

<u>Year ~2014:</u>

- 128 chips
- **120 000** patterns/chip

~15M patterns/board



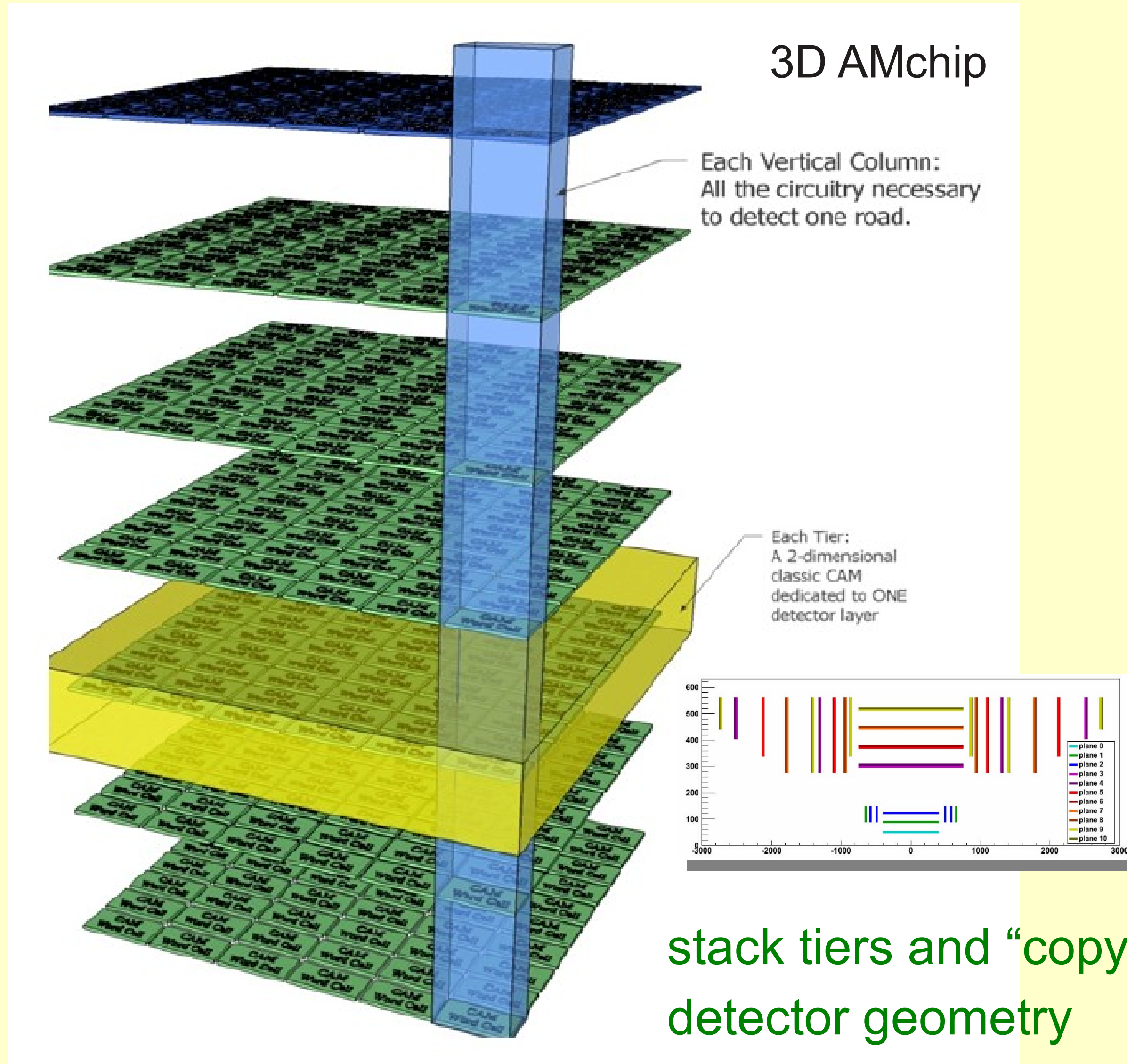
3D Opportunities

Key advantages over planar chip design

- more memory on chip
- traces factor 1000 shorter
  - → much faster
  - → reduced power

ideal design for planned L1 track triggers at ATLAS and CMS

NEURONS application (FP7)

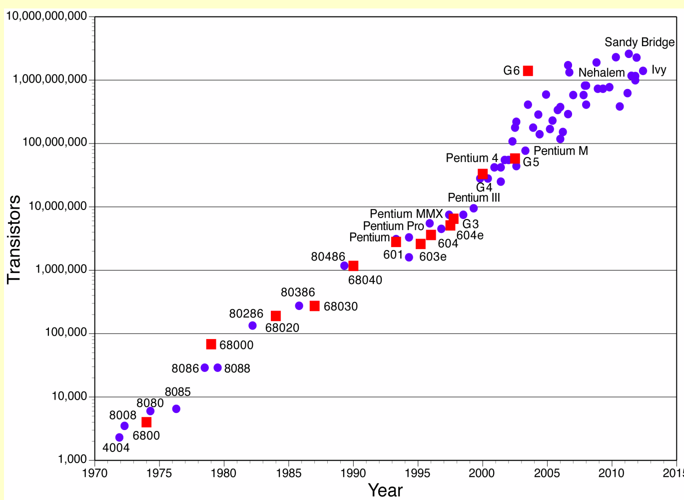


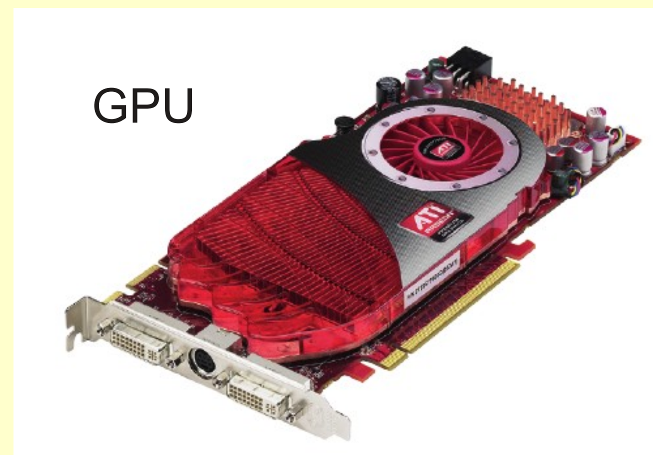
stack tiers and “copy” detector geometry

Future Directions of Track Triggers

thanks to progress in silicon industry...

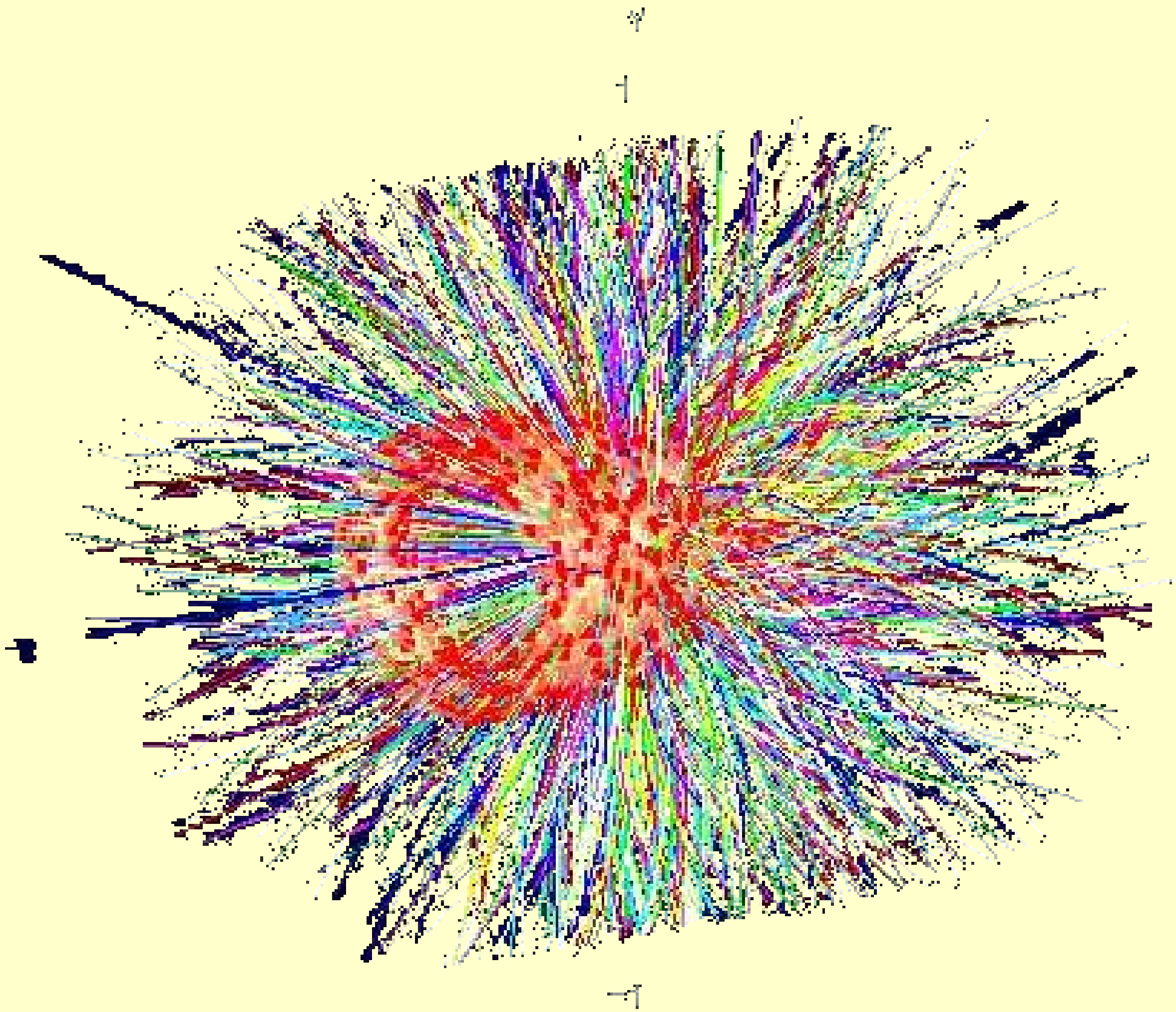
- **hit combinatorics problem addressed by modern CAMs**
  → opportunities for custom-made 3D ASICs
- **track fitting problem addressed by fast (parallel) processing units (cores) and since recently by graphical processing units** (→ next talk Nik Berger)





- **triggerless data acquisition systems will more and more replace standard multi-level trigger architectures: track trigger → track filtering**

Backup



The High Luminosity Regime

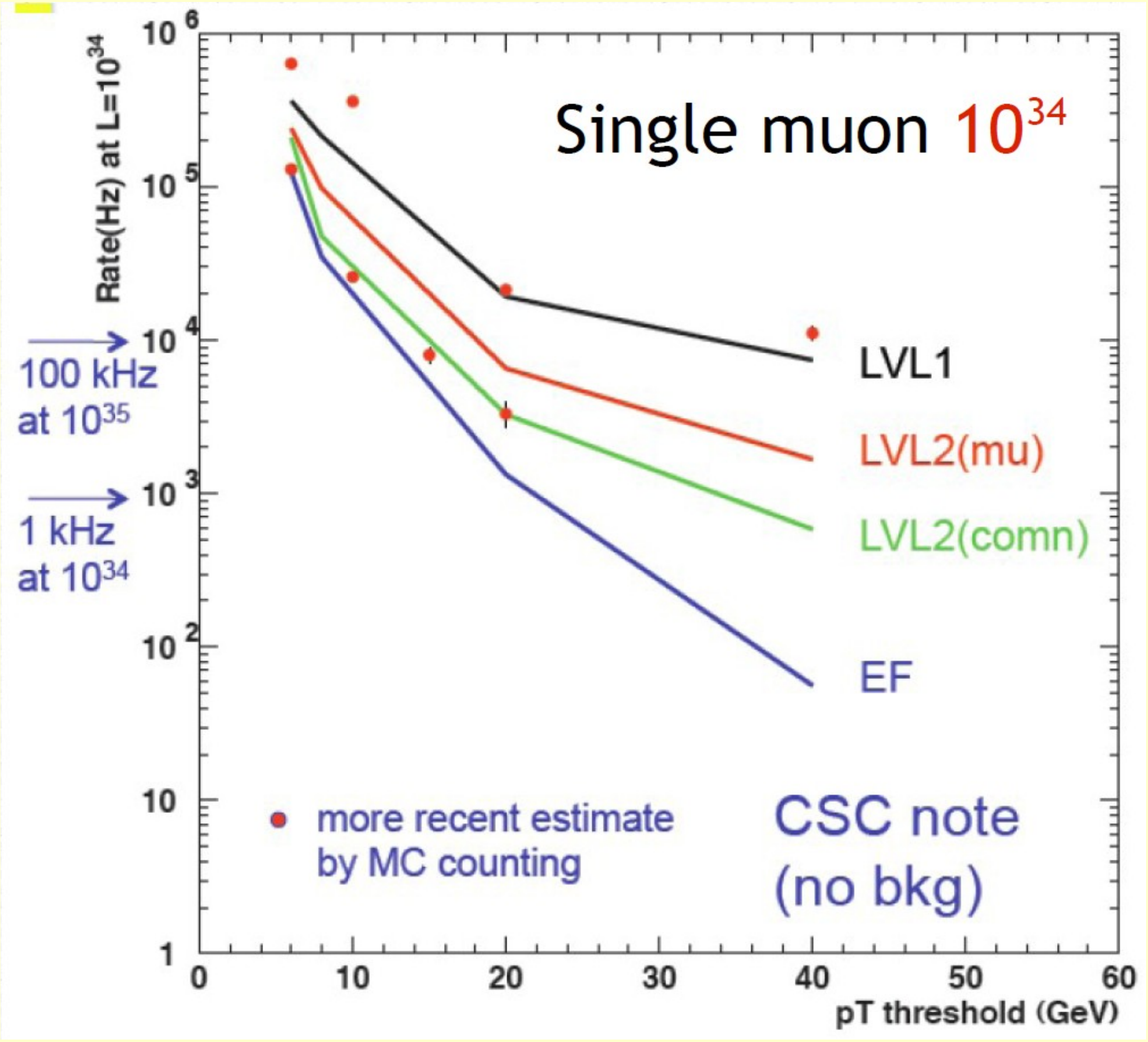
ATLAS muon identification

(similar plot for CMS)

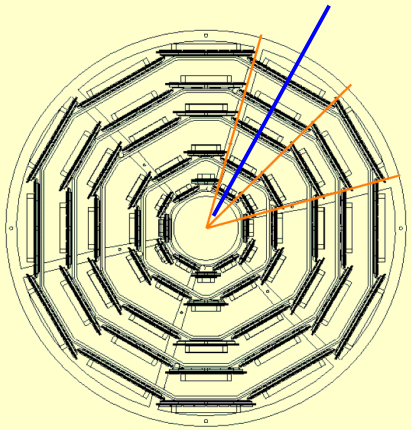
- muon trigger rates reasonable after linking with inner detector (L2)

- but reduced selectivity at higher pile up rates!

- **Idea:** **exploit track-muon link already at first level**

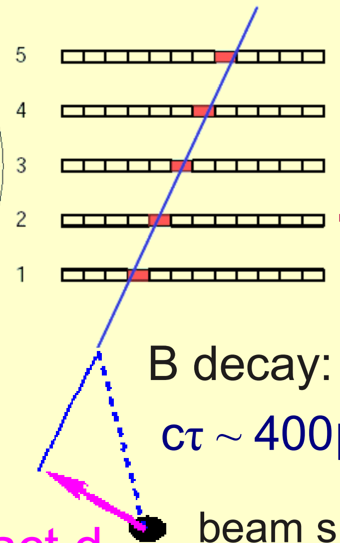


SVT Trigger: Lookup with AM Chip



Silicon Tracker (SVT)

Coarse patterns



logical equations:

hit_1 & hit_2 & hit_3 & hit_4 & hit_5

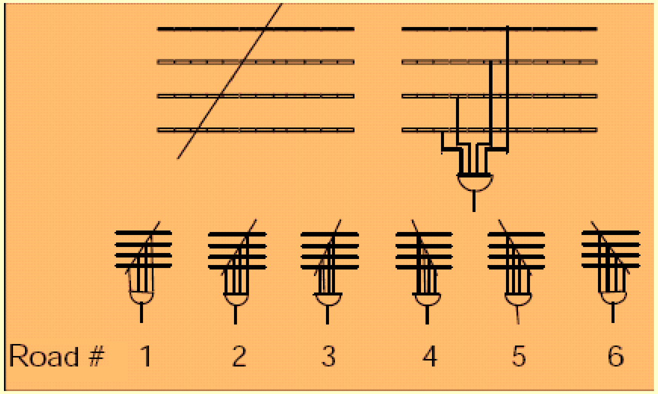
B decay:

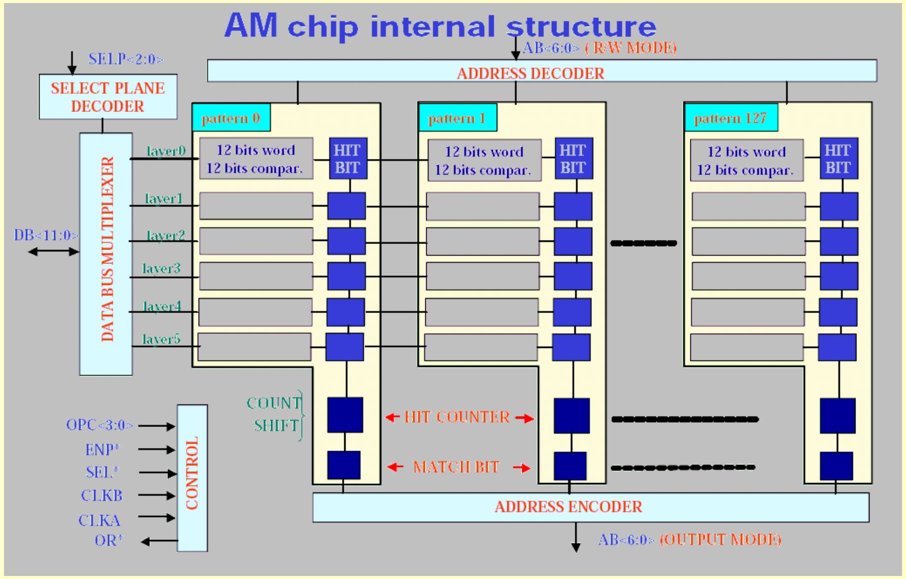
$c\tau \sim 400\mu m$

beam spot

impact d_{ca}

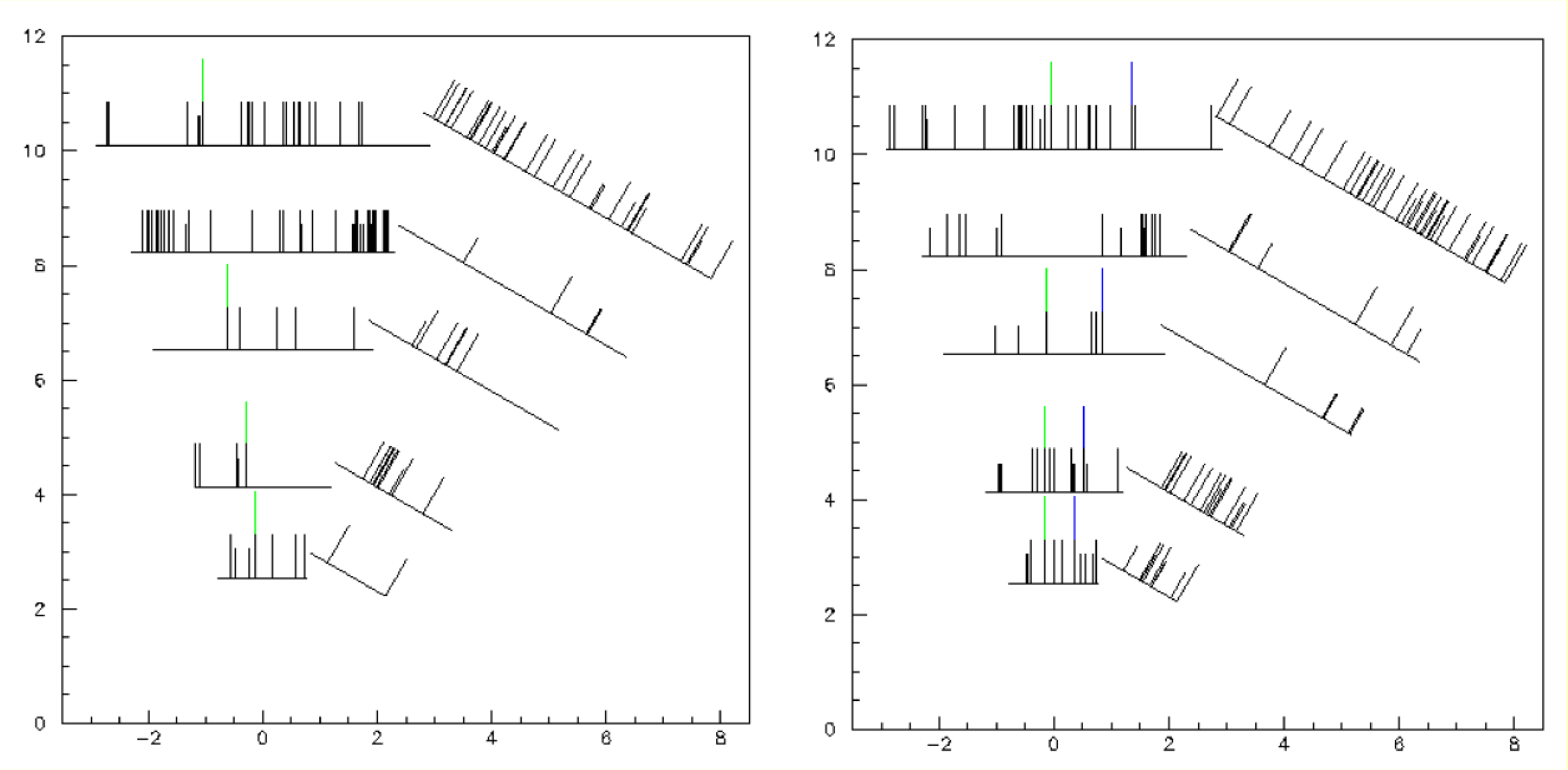
Associative Memory





AM Chip
(INFN-PISA)

CDF SVT: The Track Finding Task

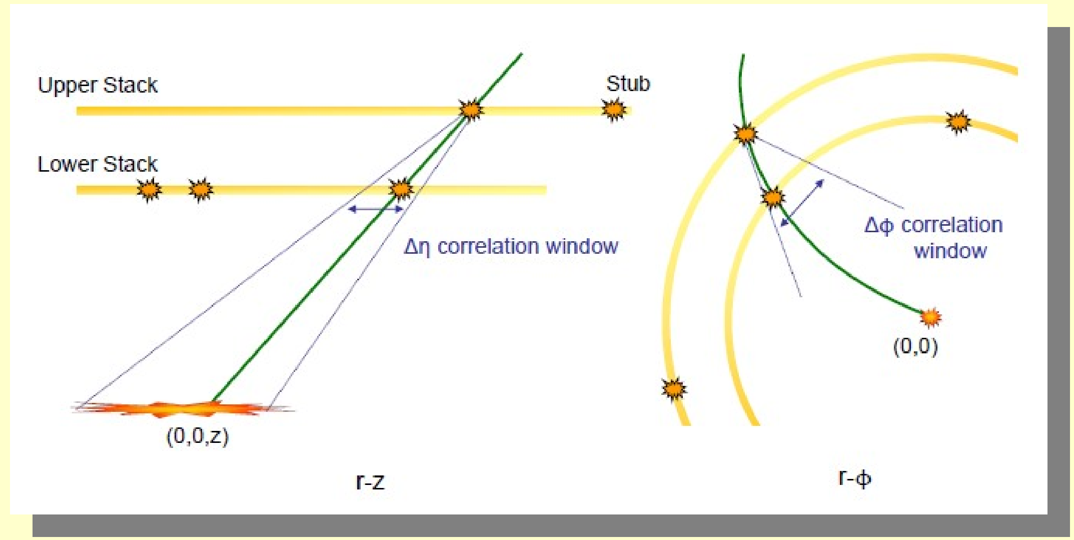


from Luciano Ristori

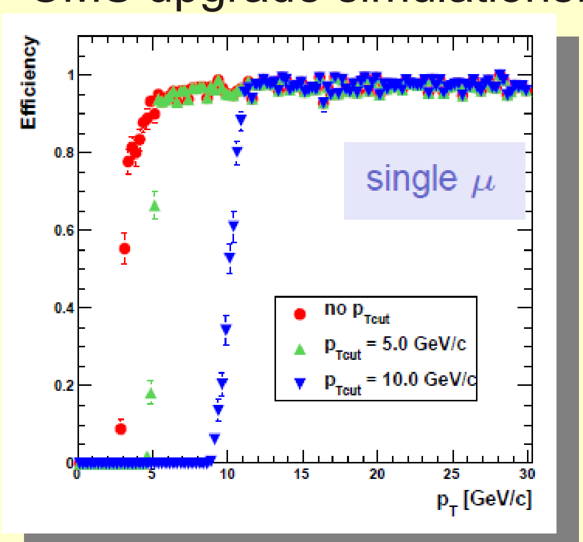
On Detector High P_T Track Filter

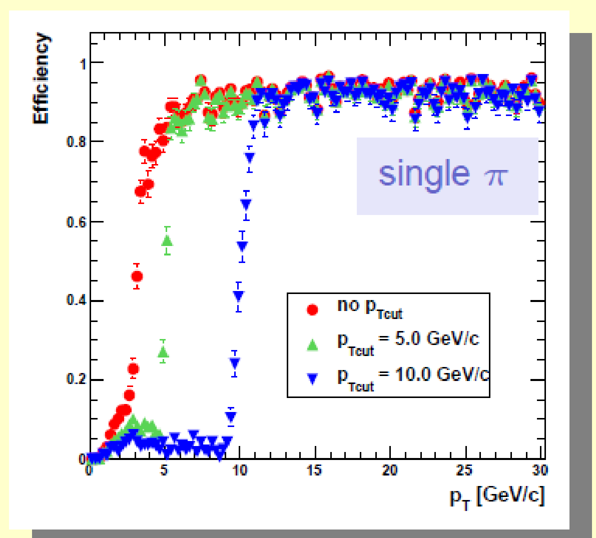
exploit two or more stacked layers

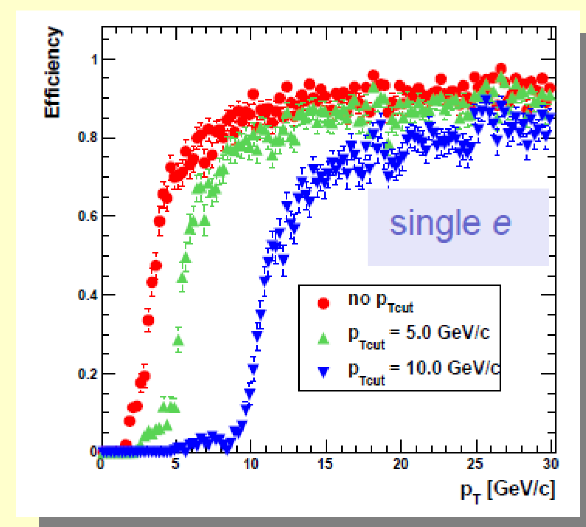
CMS: baseline design
ATLAS: design option



CMS upgrade simulations:

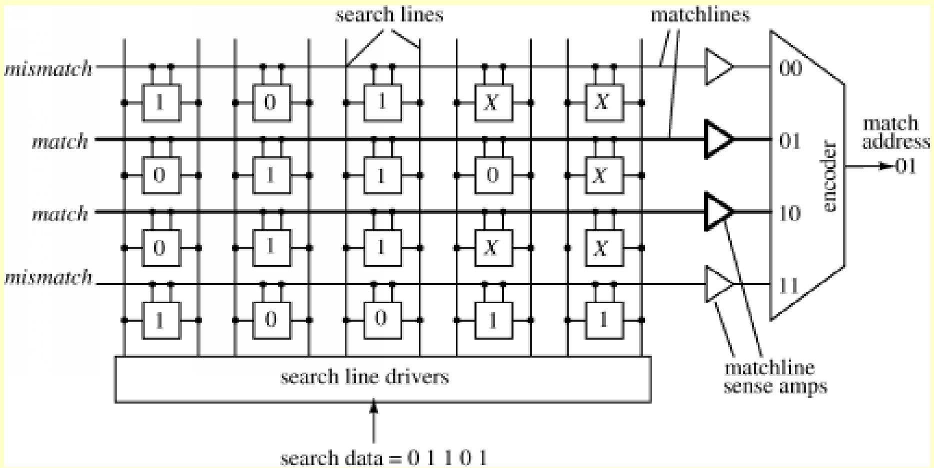






CAM vs. AM chip

Content Addressable Memory

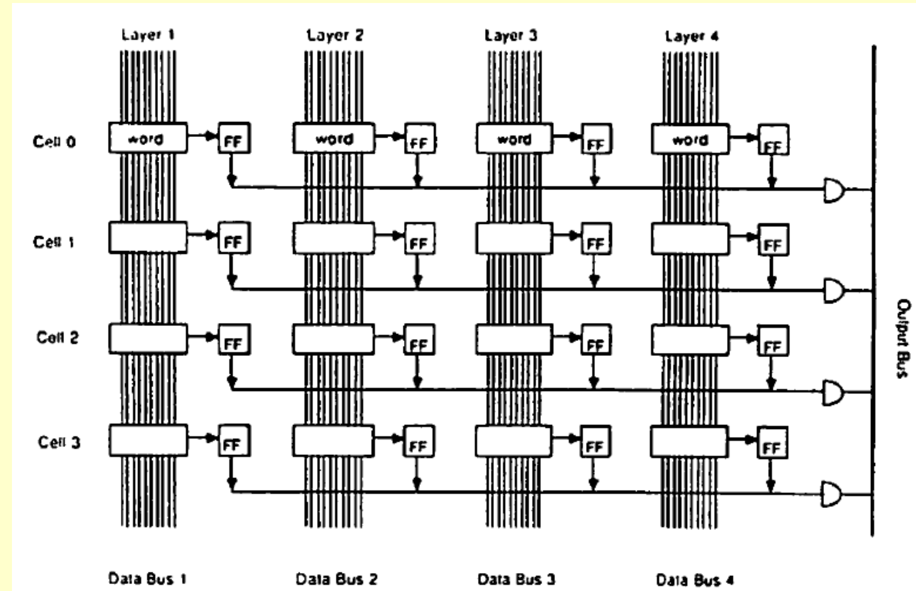


- high input bandwidth (unencoded)
- parallel input (fast)
- matches can be exclusive
- very high flexibility (e.g. 5/6)

X	X	X	X	1
X	1	0	X	X
1	X			

X	X	X	X	1
X	X	1	X	X
1	X			

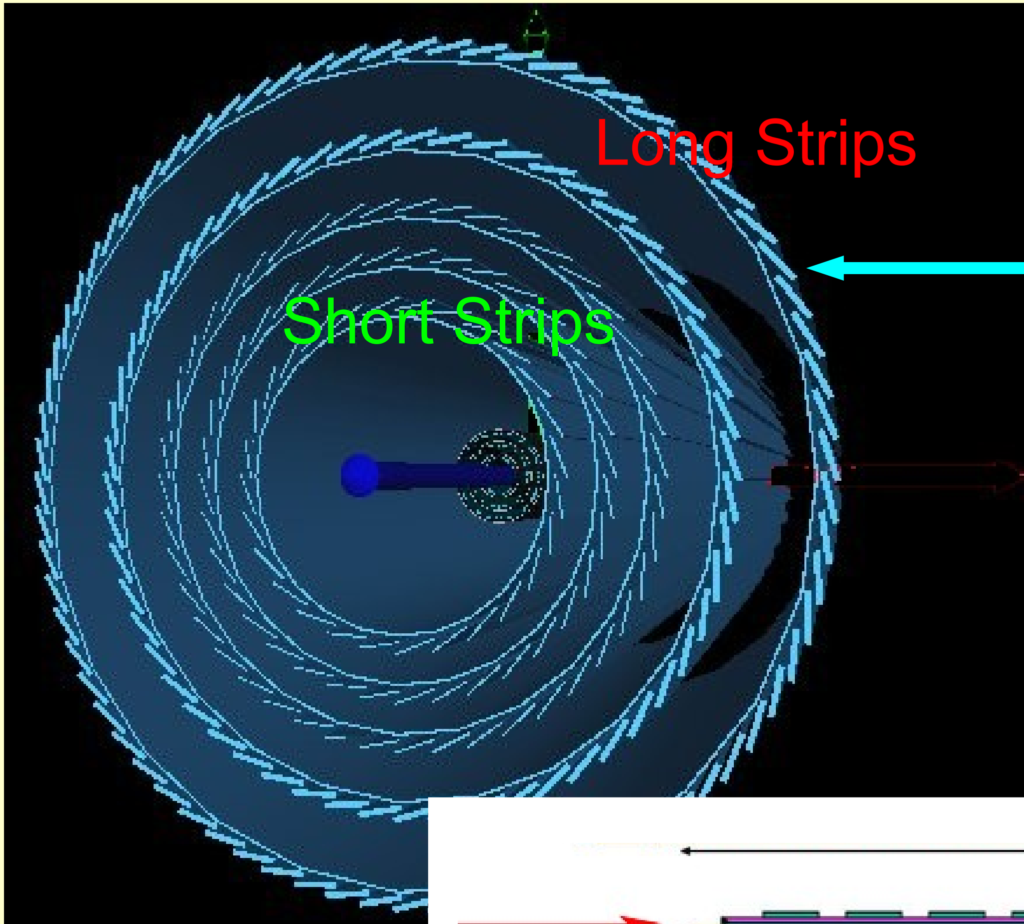
Associative Memory



- small input bandwidth (hit address)
- “economic design”
- input sequential (slow)
- several similar matches possible

(→ hit/road warrior) track isolation!

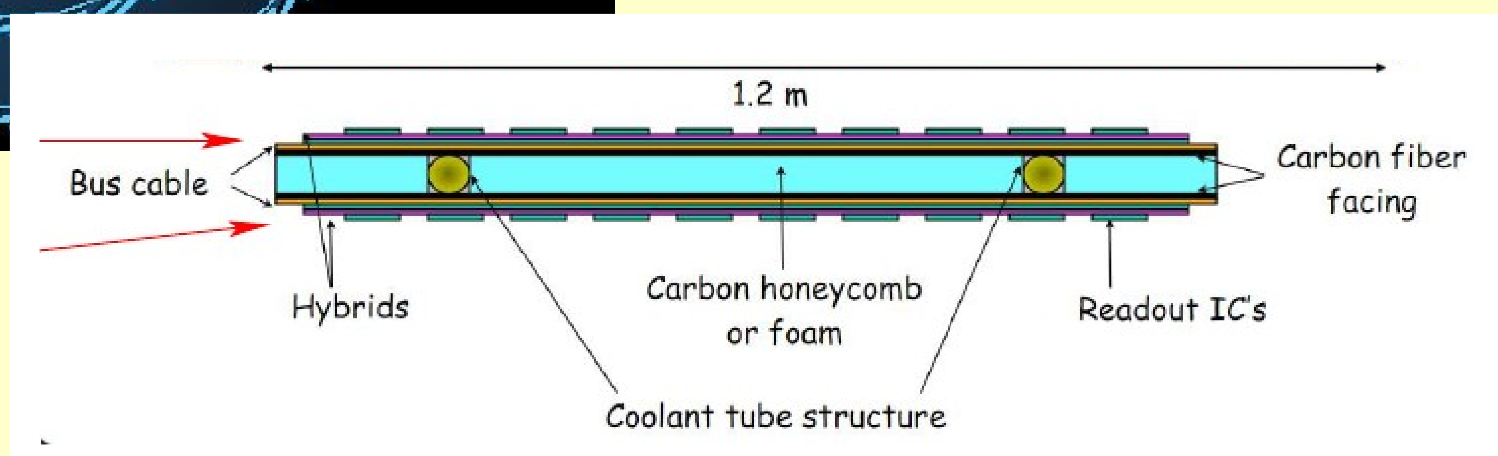
ATLAS Utopia Strip Layer Design for Phase II



Double strip layers

- gap 7.35 mm
- tilted by 10 (16) degrees
- 80 µm pitch
- stereo angle (standard)

→ no stereo angle for track trigger

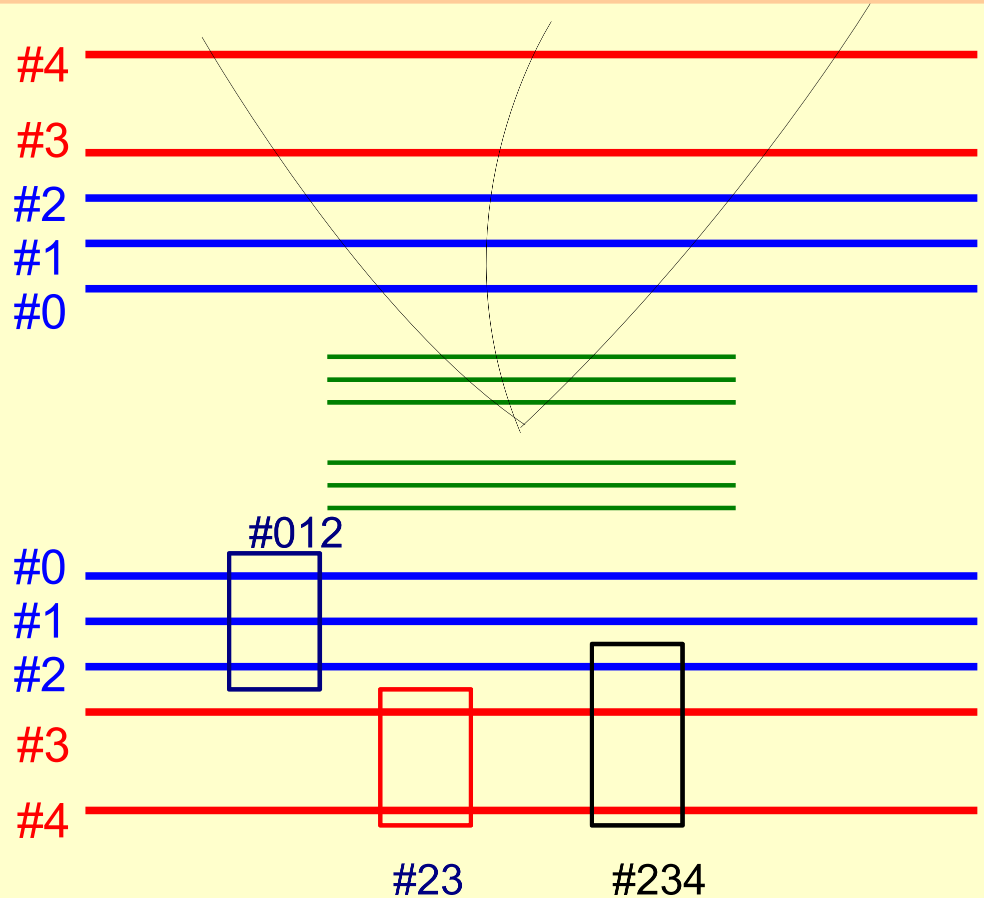


Pixel + Strip Sensor Layers

Long Strips (*Δz=10cm*)

Short Strips (*Δz=2.5cm*)

Pixel (not used)



Layer combinations studied for track trigger:

- #0, #1, #2 (only short strips)
- #3, #4 (only long strips)
- #2, #3, #4 (mixed, outer layers)