Pixel high rate test pulses

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- psi46dig ROC is designed for 120 Mpx/s
  - expected in layer 2 at $2 \cdot 10^{34}/\mathrm{cm}^2\mathrm{s}$
- multiple test pulse patterns
- present test board limitations

Data Rate Estimations

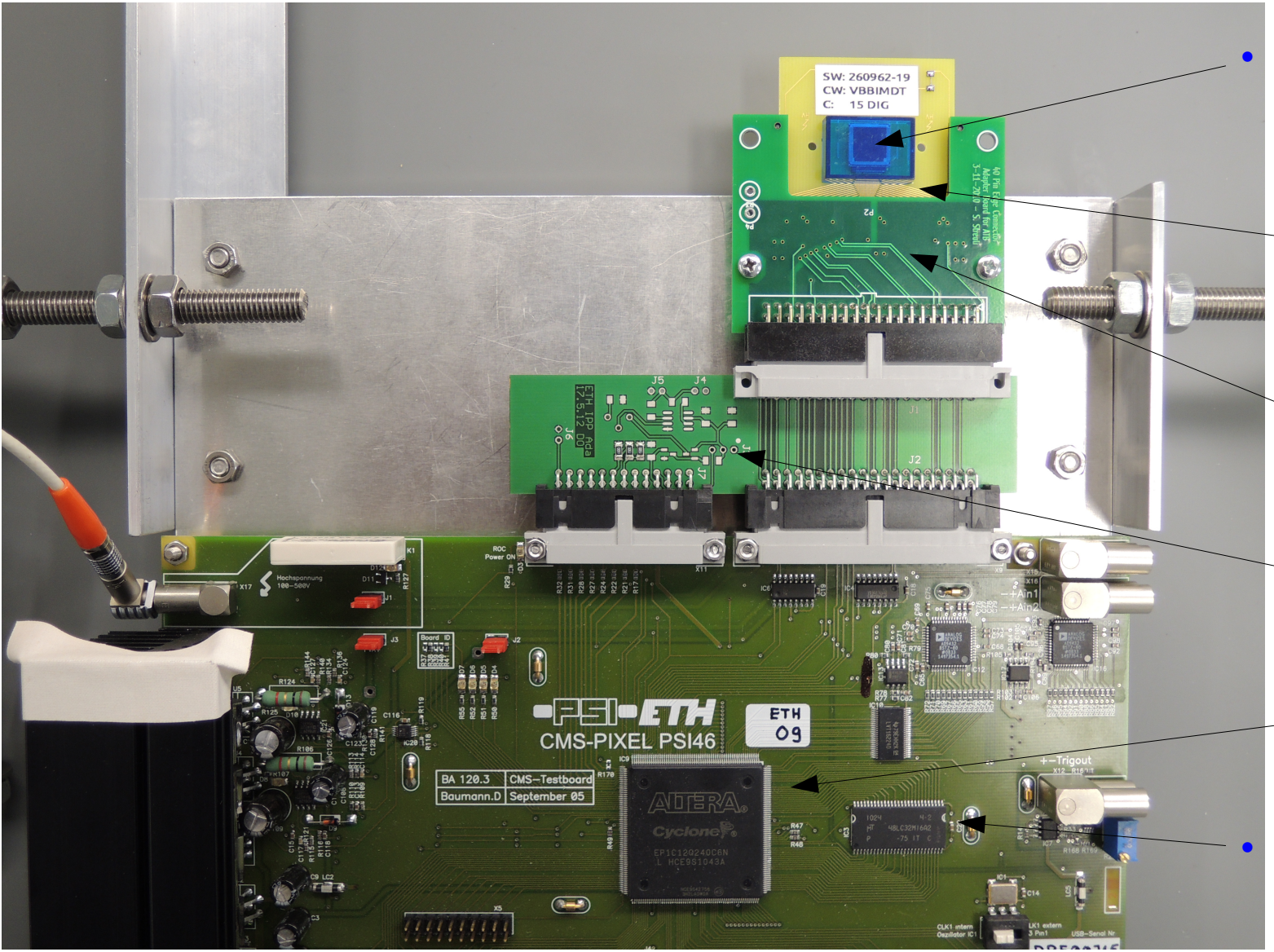
- Simulation with Pythia Z2 tune and GEANT4
- Assuming 24 bits per hit, 100 kHz level 1 trigger rate
- Peak luminosity = $2x10^{34}cm^{-2}s^{-1}$, σ_{tot}=80mb, σ_{signal}=1.5mb, 25 ns BC

Layer	1 @ 2.9cm		2	3	4
Pixel fluence [MHz/cm^2]	520		119	52	27
Hits / trigger / module	190		40	18	8.4
MBit/link/sec	435		118	66	45

1 ROC = 0.65 cm^2

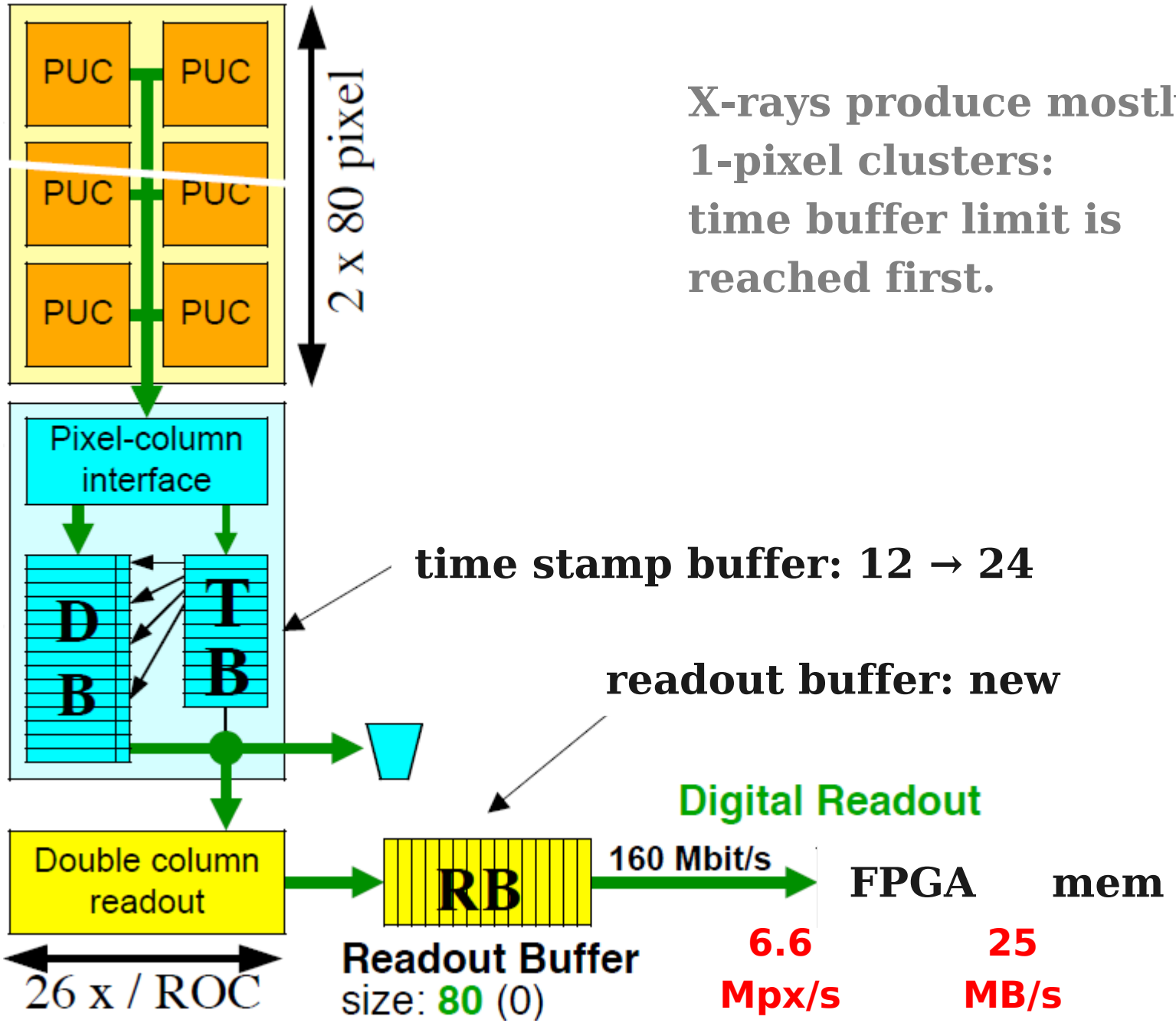
Hans-Christian Kästli,
CMS Upgrade plenary,
20.7.2011

psi46 test board



- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
  - ETH adapter card for digital 160 MHz differential signal directly into FPGA (LCDS into LVDS)
- 64 MB memory

double column readout



X-rays produce mostly 1-pixel clusters: time buffer limit is reached first.

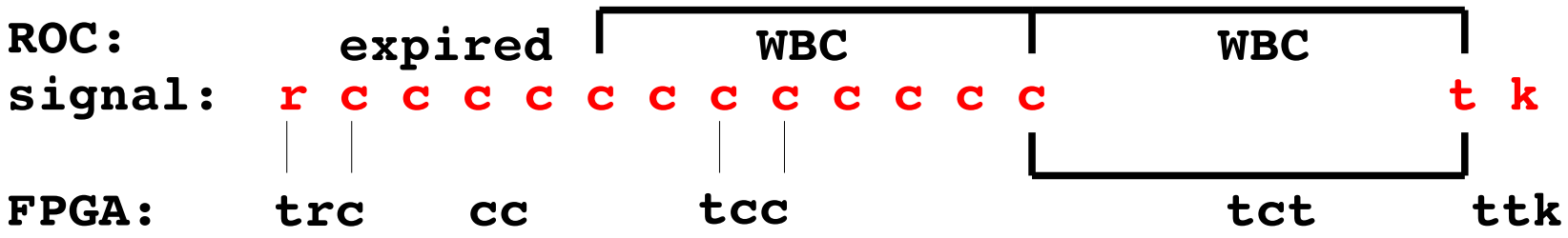
test board signals and steering

signal sequence from FPGA to ROC:

reset – *n*×calibrate – trigger – token = r c(ccc) t k

tbParameters.dat:

trc	10	time between reset and cal [BC]
cc	12	calibrate counter *n*
tcc	20	time between calibrates [BC]
tct	153	time between calibrates and trigger
		WBC = tct – 5 = 148
ttk	10	time between trigger and readout token [BC]
trep	50	trigger prescale [events]



High rate ROC test

pixels read out:

$$f_{read} = f_{trig}\ n_{pix/DC}\ n_{DC}$$

pixels active:

$$f_{act} = f_{trig}\ n_{cal}\ n_{pix/DC}\ n_{DC}$$

limits:

f_{read} : write < 25 MB/s into memory, < 6.6 Mpx/s ROC rate

n_{cal} <= 24 time buffers per double column

$n_{cal}\ n_{pix/DC}$ < 80 data buffers per double column

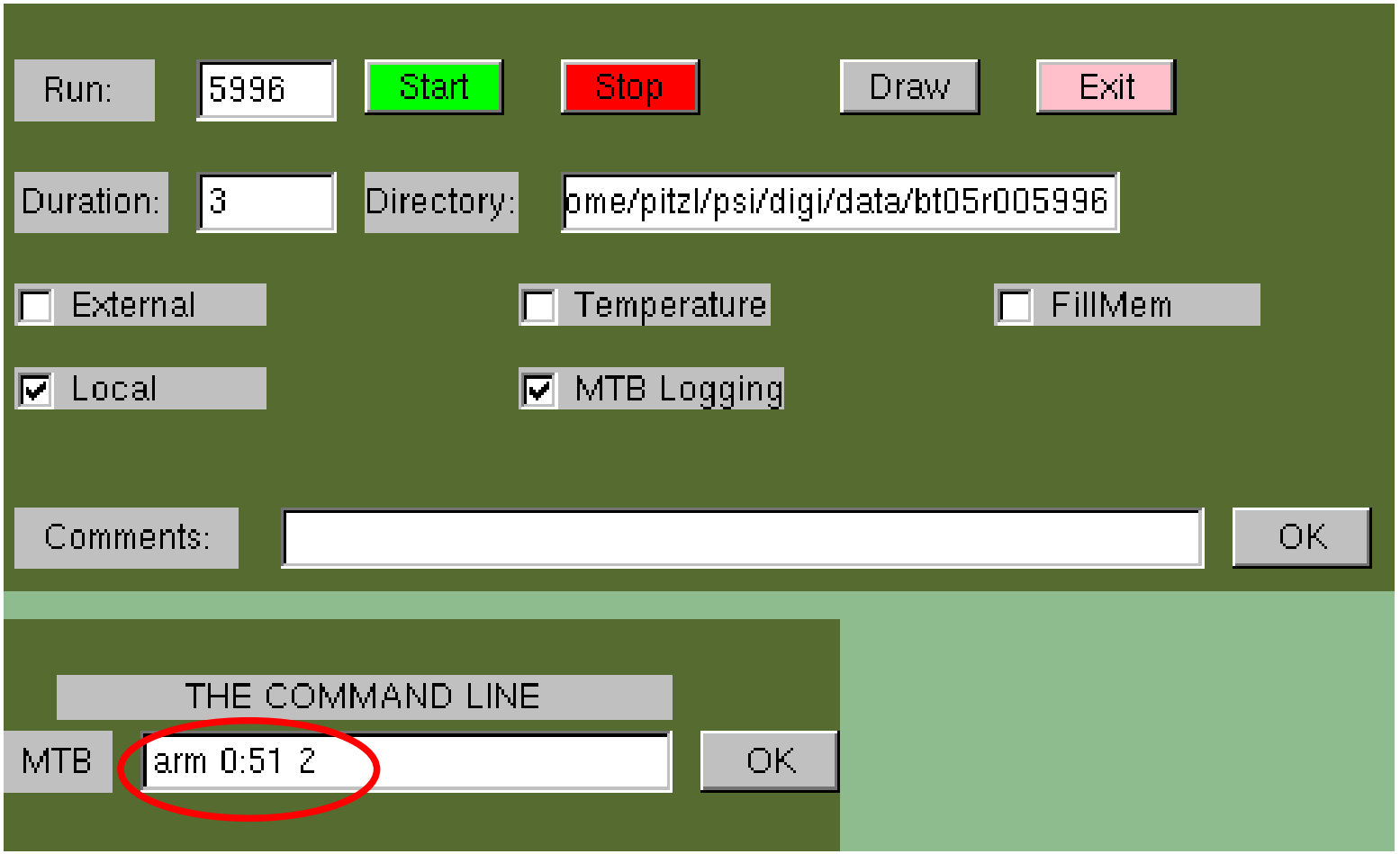
n_{DC} <= 26 double columns per ROC

possible:

$n_{pix/DC} = 4,\ n_{cal} = 19,\ f_{read} = 6.6$ Mpx/s => $f_{act} = 125$ Mpx/s/ROC

$n_{DC} = 26,\ f_{trig} = 64$ kHz

takeData with test pulses

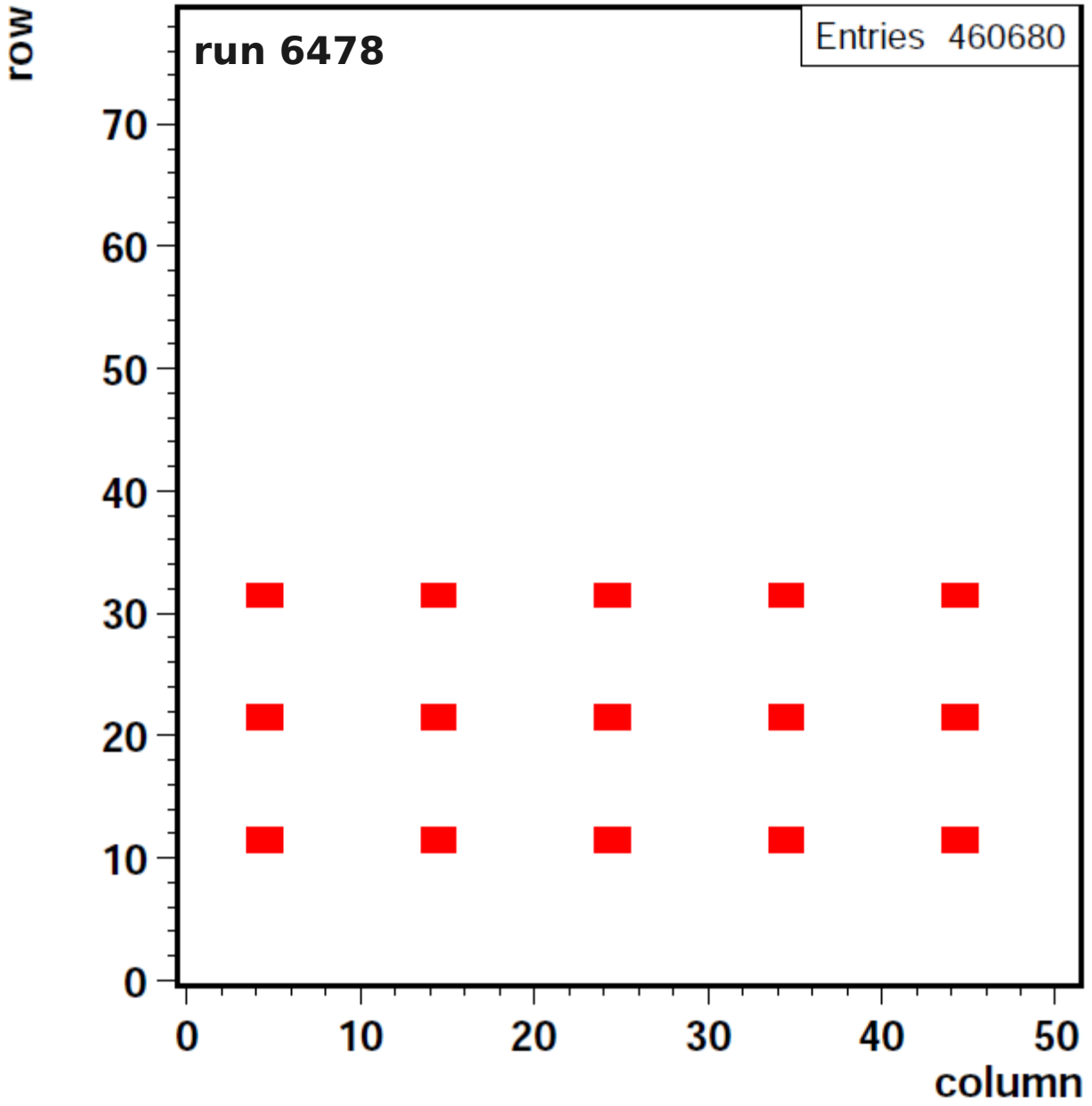


activate test pulse for columns 0..51 row 2

(any test board or ROC command can be given here)

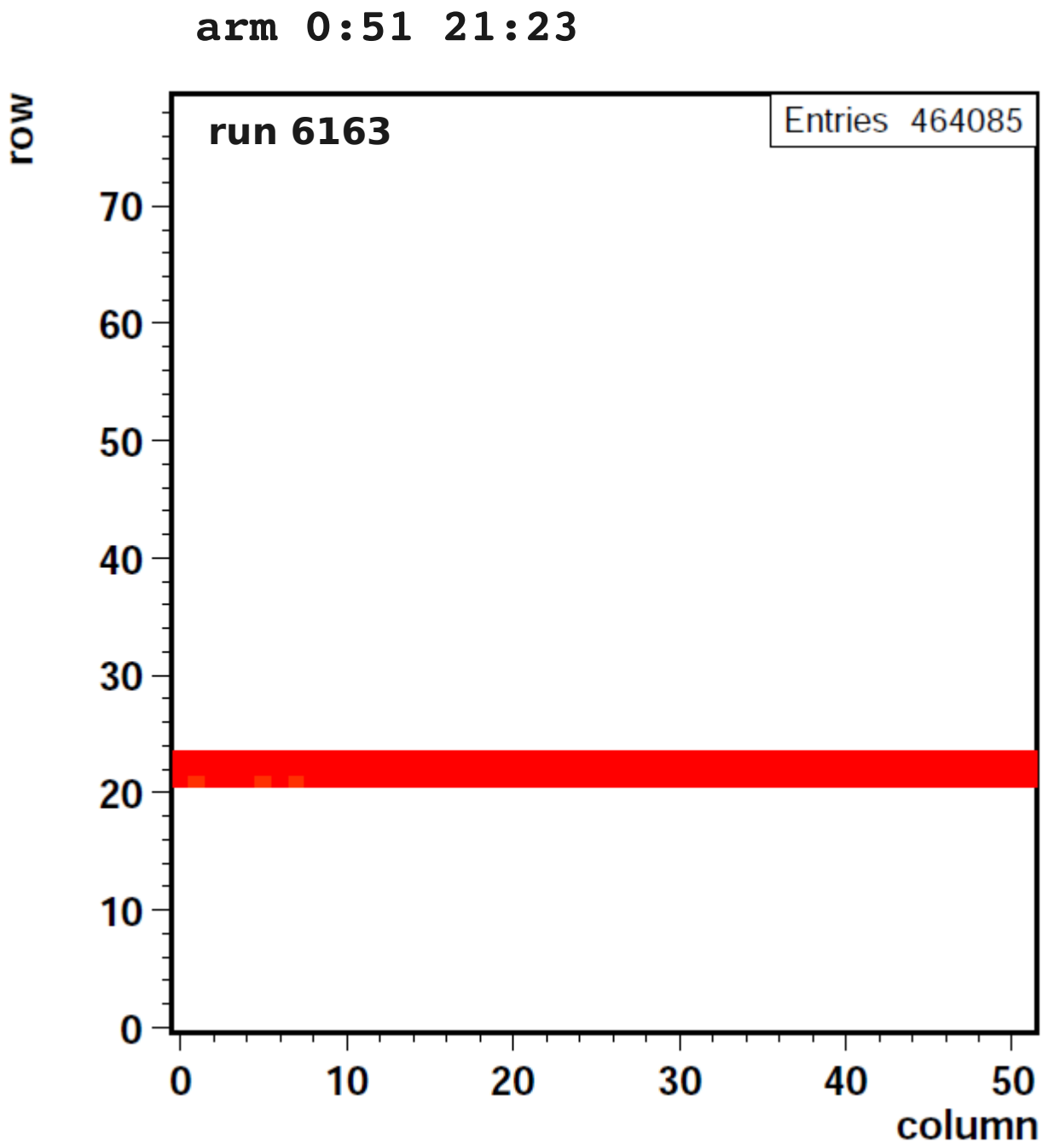
test pulse cluster pattern

`arm 4,5,14,15,24,25,34,35,44,45  11,12,21,22,31,32`



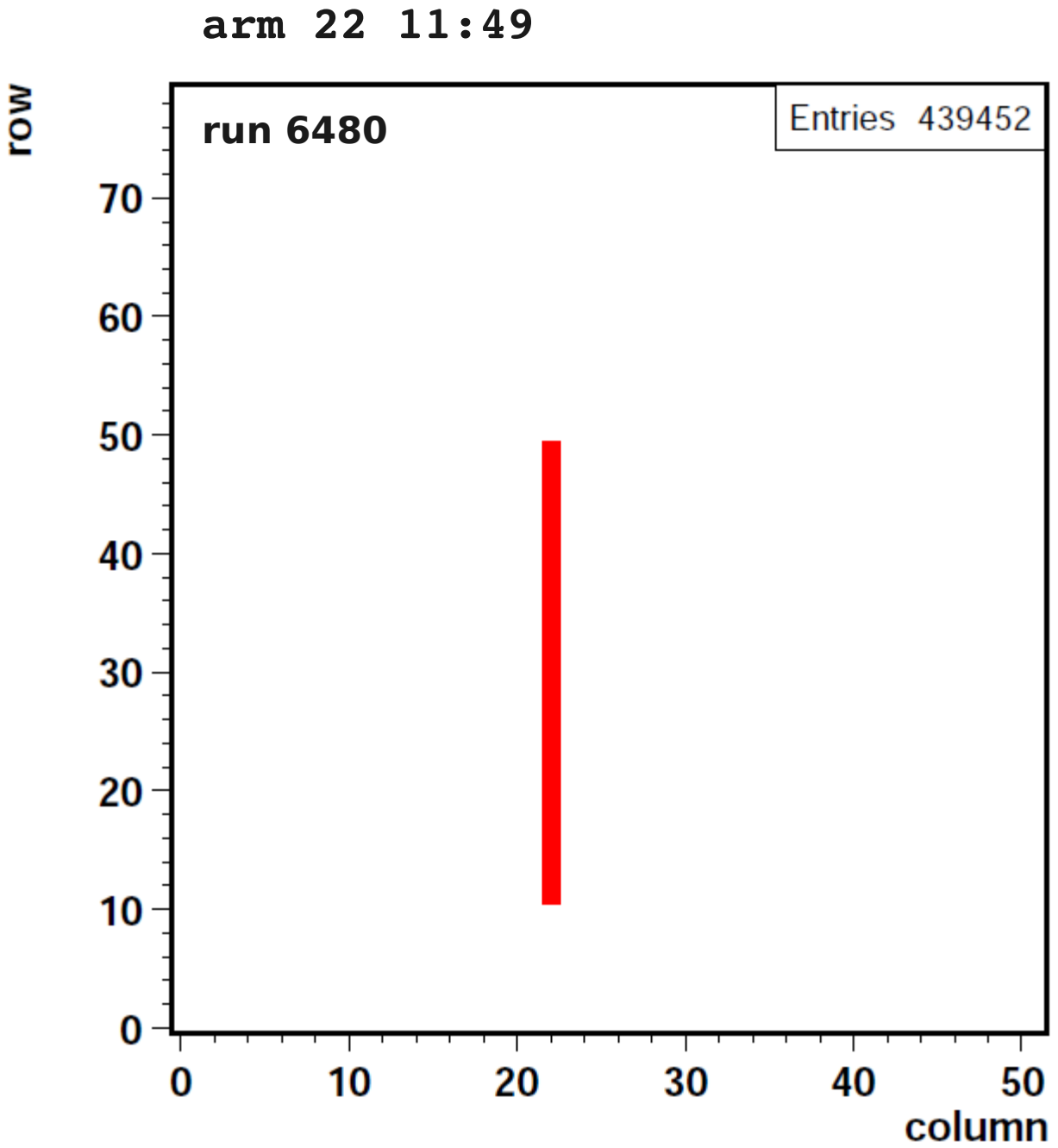
- 60 pixels pulsed:
  - 15 clusters
  - 2×2 pixels/cluster
- 31.3 kHz trigger rate (`trep 5`)
  - 1.9 Mpx/s readout
- 100% efficiency
- no data errors

high rate test



- 156 pixels pulsed:
  - 3 per column
- 11.2 kHz trigger rate (`trep 14`):
  - 1.8 Mpx/s read out.
- 12 calibrate pulses:
  - **21 Mpx/s active.**
- 13 calibrate pulses:
  - no data from FPGA
- 100% efficiency
- no data errors

single column test



- 39 pixels pulsed:
  - in one double column
- `cc = 2:`
  - data buffer almost full (78)
- 31.3 kHz trigger rate (`trep 5`)
  - 1.2 Mpx/s readout
  - **2.4 Mpx/s/DC active**
  - **corresponds to 64 Mpx/s/ROC active?**
- 100% efficiency, no data errors

Current FPGA limitations

Data from the digital ROC are not densely packed:

4 bits into one word (2 bytes): 25% filing

=> f_{read} < 2.1 Mpx/s

A factor 3 could be gained here.

The new PSI test board will fix that.

Multiple calibrates (`rcccctk`) are only possible at low trigger rate:

```
cc  6: max 19.6 kHz (trep >  8), 12 Mpx/s active
cc  9: max 15.4 kHz (trep > 12), 18 Mpx/s active
cc 12: max 11.2 kHz (trep > 14), 21 Mpx/s active
cc 17: max  8.7 kHz (trep > 18), 15 Mpx/s active
```

'Event FIFO' on the FPGA too small?

Goal: `cc 19 and 64 kHz`

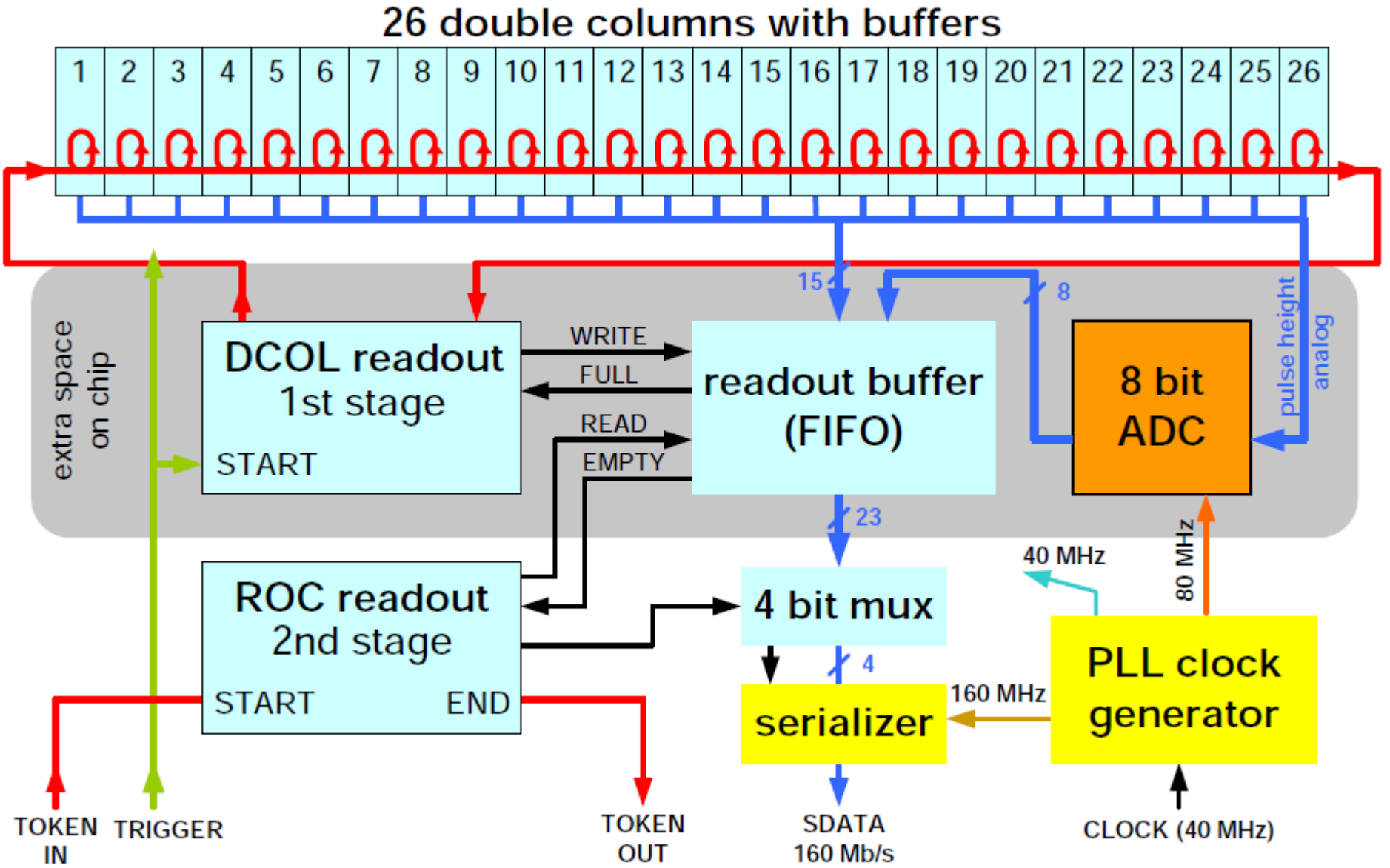
Under study at PSI (Beat Meier).

Summary

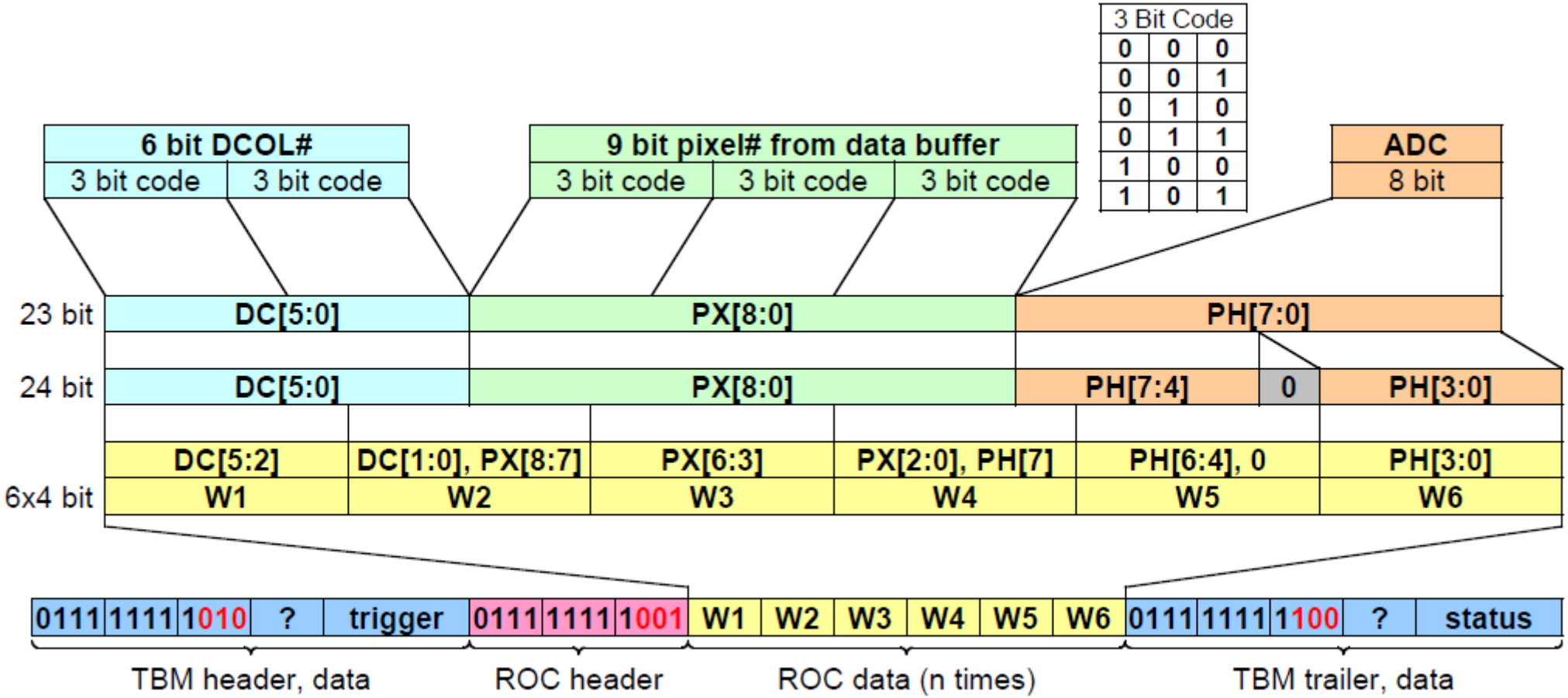
- Multiple calibrate pulses can be given from the test board to the ROC:
  - cluster patterns can be programmed,
  - the entire data buffer (80/double column) can be exercised.
  - efficiency and data integrity can be measured.
- The ROC can transfer up to 6.6 Mpx/event (24 bit/pixel at 160 MHz):
  - With 19 calibrate pulses we could simulate a pixel activity of 125 Mpx/s per ROC.
- Present FPGA firmware limits:
  - < 2.1 Mpx/s readout (data packing)
  - < 21 Mpx/s activity (FIFO size?)
- The new PSI test board should get us closer to the maximum...

Back up

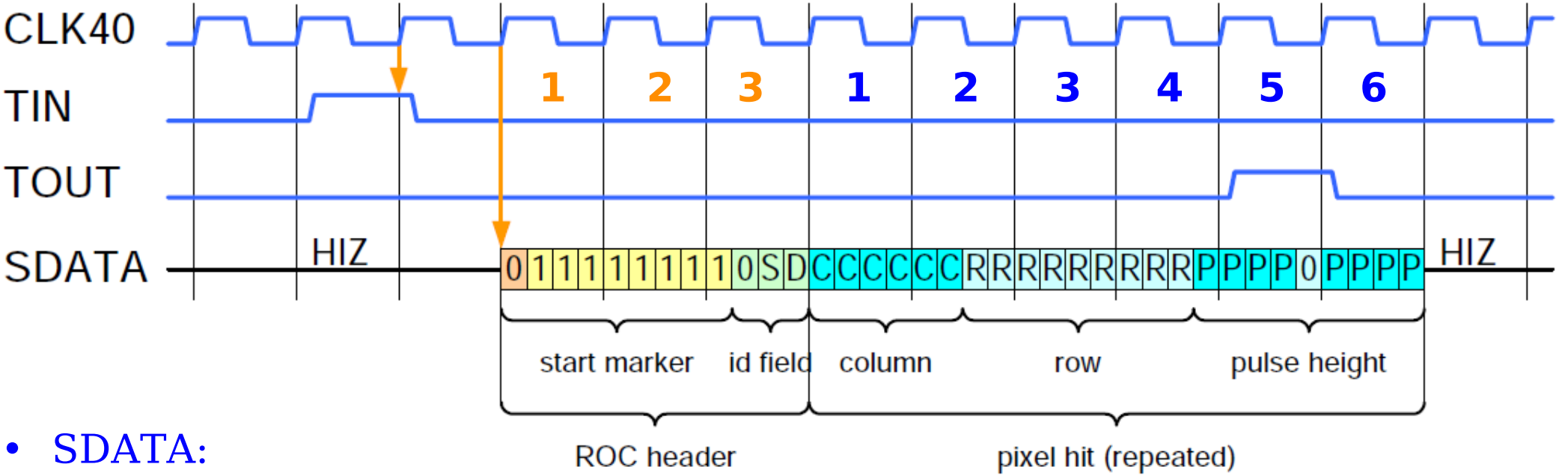
psi46dig periphery



digital ROC data format



digital ROC data format



- SDATA:
  - 160 MHz
  - 4 bits per 40 MHz clock cycle
- FPGA FIFO:
  - 4 bits stored per data word (2 bytes)
  - (will be packed better on new digital tb)
- empty ROC:
  - 3 header words
- per pixel hit:
  - 6 data words

thanks to Simon Spannagel (KIT) for the digital decoder