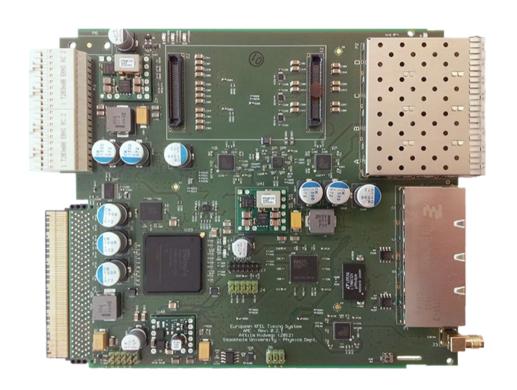
Update on x2Timer

Holger Kay

DESY - msk







Overview

- 1. The interfaces of the x2Timer
- 2. The RJ45 connectors
- 3. The RTM connector
- 4. Working modes of the x2Timer
- 5. What do we need to update on x2Timer

1. The x2Timer board

Developed by Attila Hidvegi

Stockholm University

3 channel transmitter piggyback

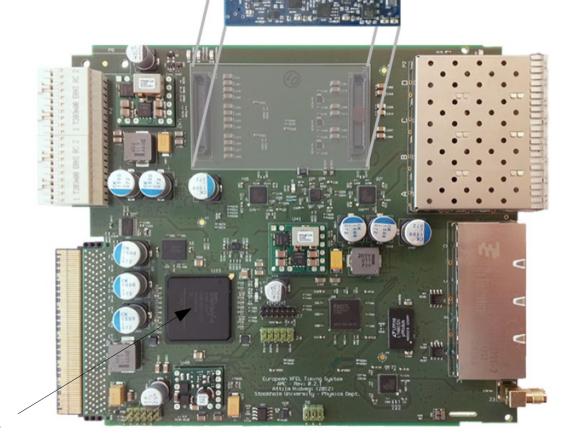
Drift compensation of the fiber cable

RTM connector

AMC connector

8 Triggers 2 Clocks
Identical to x1Timer

Spartan 6 FPGA



4 SFP connectors

Receive and Transmit

1.3Gbit timing stream

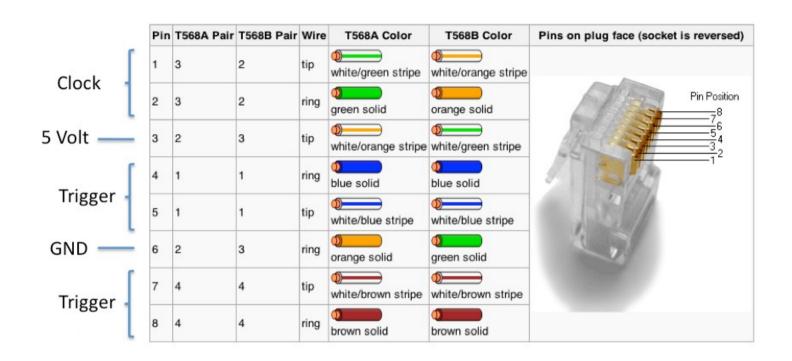
4 RJ45 connectors

- 6 lvds trigger outputs
- 3 lvds clock outputs
- 4 lvds trigger inputs

RF input

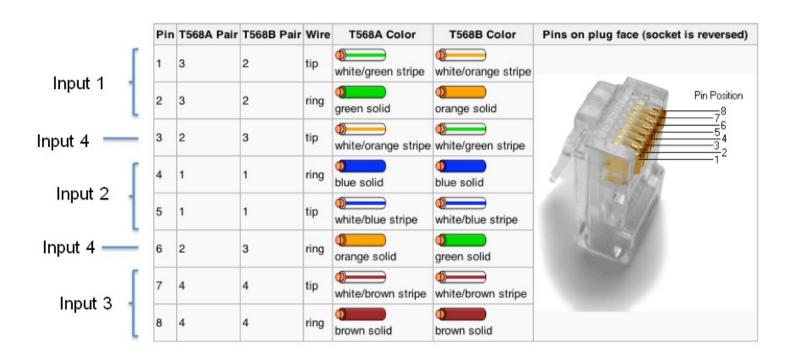
1.3GHz ref. clock

2. Rj45 Connector 1, 2 and 3



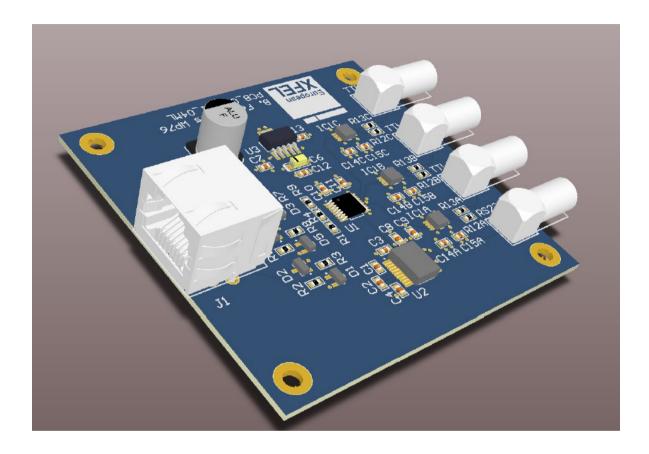
- Allows the use of Ethernet patch cable (cheep and easy to handle)
- ≥ 2x Trigger and 1 Clock output
- Switchable 5V 250mA (not compatible to Power Over Ethernet)
- > Allows active level converters (LVDS to TTL)

2. Rj45 Connector 4



- This connector has 4 LVDS inputs
- > No power supply. Pin 3 and 6 are used for an input

2. The activ level converter



- ➤ Made by Patrick Gessler and Bruno Fernandes from XFEL
- > 2x Trigger output and 1x Clock output with 5V TTL level
- >RS232 data output

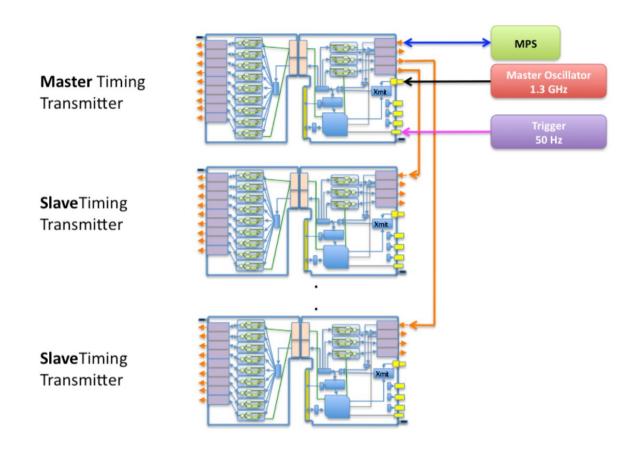
3. Signals on the RTM connector

<u>Signal</u>	<u>Number</u>	<u>Usage</u>
I2C bus for Piggiback	9	Control up to 3 Piggibacks
Interrupt	9	
REF-Clock	1	Cable drift compensation
Atmel PDI interface	1	Piggiback remote firmware update
Timing input	1	Input and Output for the 1.3Gbit
Timing output	1	Timing stream
I2C bus for SFP connectors	9	Configuration of the SFP connectors
Trigger signals	9	RTM Trigger Outputs
12V, 3.3V	1	Power supply
JTAG interface	1	General purpose Programing interface
I2C bus	1	General purpose
Trigger/Clock input/output	2	General purpose connected to FPGA
Clock output	1	General purpose from clock switch

3. Planned RTM boards

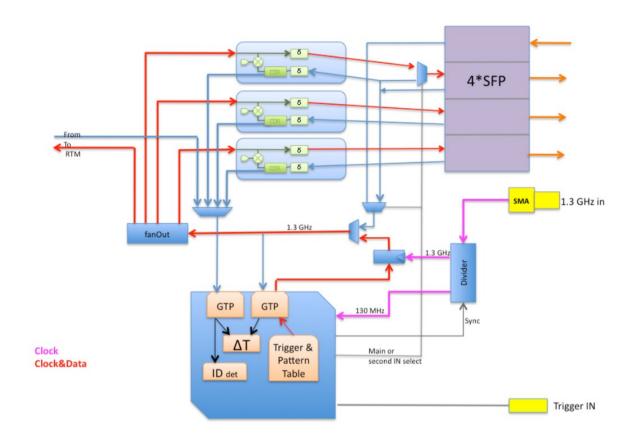
- >RTM with 9 SFP connectors only
 - Used for master timing transmitter
- >RTM with 9 trigger outputs only
- RTM with both, trigger outputs and SFP connectors
 - Not finaly defined

4. x2Timer as timing transmitter



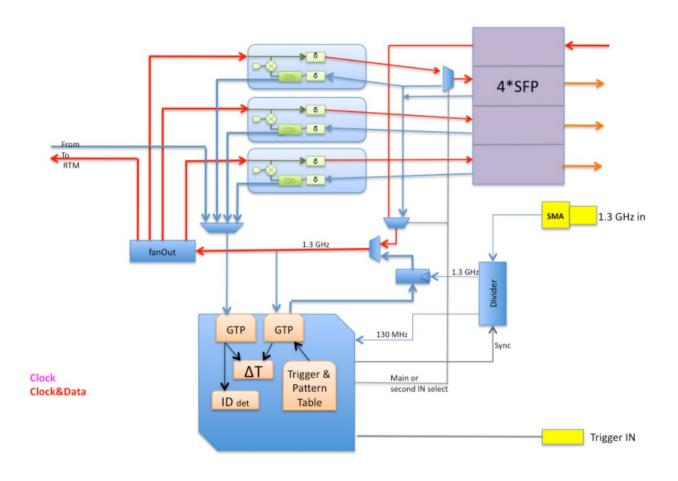
- > Master Transmitter becomes signal from MPS, MO and 50Hz sync
- > Transmitter distributes timing signal via fiber on RTM and front
- Slave Transmitter redistributes signal from master

4. x2Timer as master transmitter



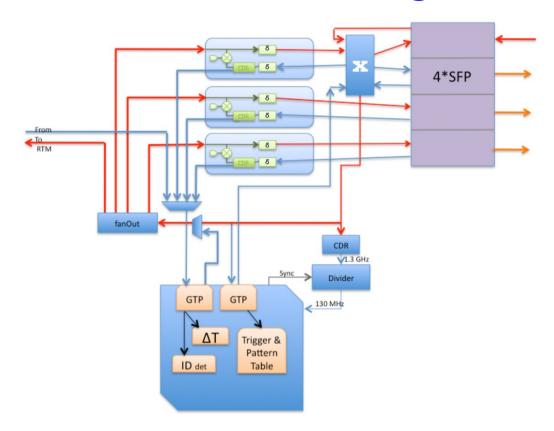
- ➤ Reference clock is dividet by 10 to 130MHz
- > Timing Data Stream is generated in FPGA
- > Timing Data Stream is distributed over cable drift compensation

4. x2Timer as slave transmitter



- Slave transmitter redistributes timing signal
- > It uses the cable drift compensation for each output

4. x2Timer as timing receiver



- > Timing receiver recovers the clock via a CDR chip
- > It also works as a slave transmitter

5. What do we need to update on x2Timer

- ➤ Hardware (x2Timer, RTM boards, cable etc.)
- ➤ New Firmware, Driver, Server
- ≥2 fiber cable between each receiver and transmitter

Thank you for your attention