LLRF controller status update

mTCA specific

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DESY

Outline

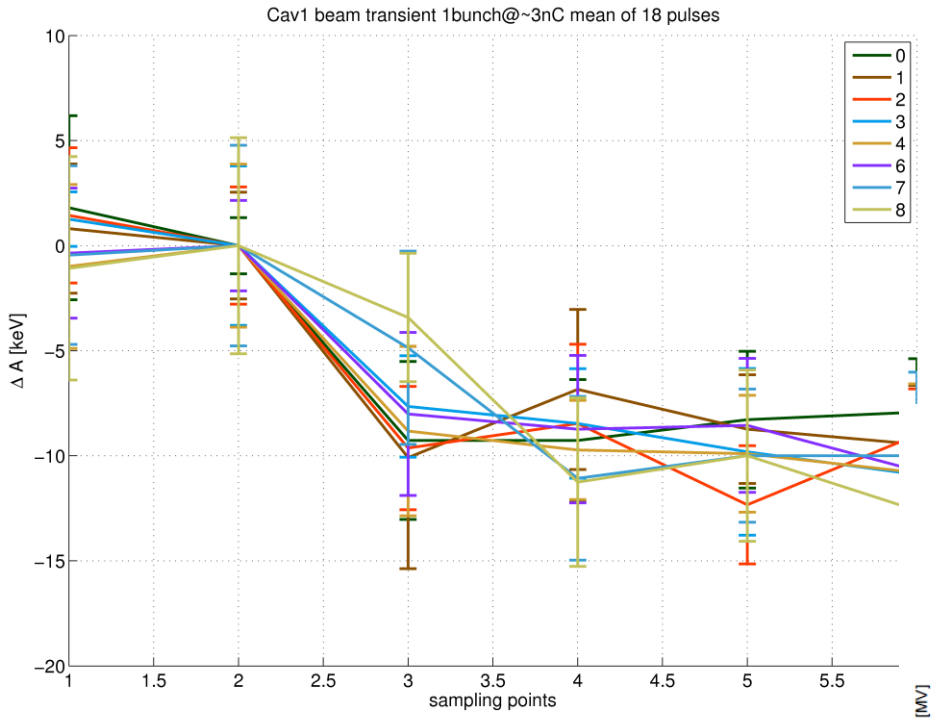
- ADC frontend implementation
  - Tested functionalities
  - Missing parts and next steps
- uTC controller functionality
  - Integrated and comissioned blocks
  - Next features to be integrated
  - BLC example
- Facility installations
- (High level software) ⟸ **Moved to 2nd talk**

Comissioned functionalities

- Adjustable attenuators (server based setting) ✓
  - Issue detected Sunday at ACC67 test with recent DWC
  - Automated signal conditioning
  - Increase sensitivity for calibration
- ADC functionality and data readout ✓
  - Raw ADC data available, permanent readout
  - Overflowing signature readout
  - Overflow reaction
  - Attenuator setup (phase shift indep.)
- IQ detection with variable sampling steps (mov. Average, down sampling) ✓
  - Calibration procedure combined with sampling
  - Down sampling with variable delay adjustment
  - SC, NC application (f.sampl)
  - Cavity response alignment
- IIR filter functionality (pass band mode notch) ✓
  - Different filter schemes, server based parameter upload
  - Automated setup with online FFT
  - Low-pass for noise reduction on F/R
- AP computation ✓
  - DAQ preparation and limit detection
  - Cross calibration DAQ channel
  - Signal bit conversion FPGA – Server
- PVS computation and data transfer ✓
  - Limited bit-size, communication bandwidth trough LLL
- DCM missing

Single bunch beam transient (sampling delay influence)

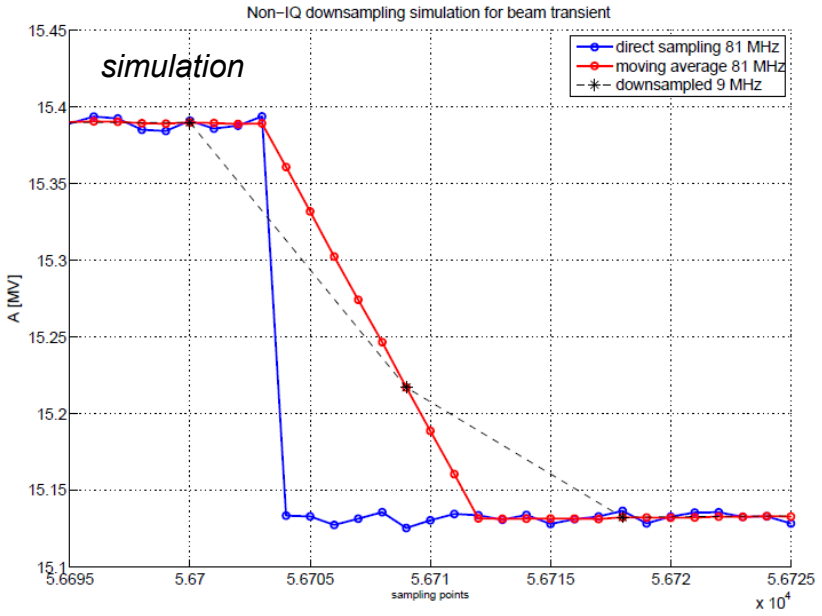
measurement



Induced voltage drop

$$V = -\left(\frac{r}{Q}\right) \cdot q_B \cdot \pi \cdot f_0$$

Charge [nC]	0.1	0.5	1	2	3
Voltage drop [kV]	0.4	2.1	4.25	8.5	12.7

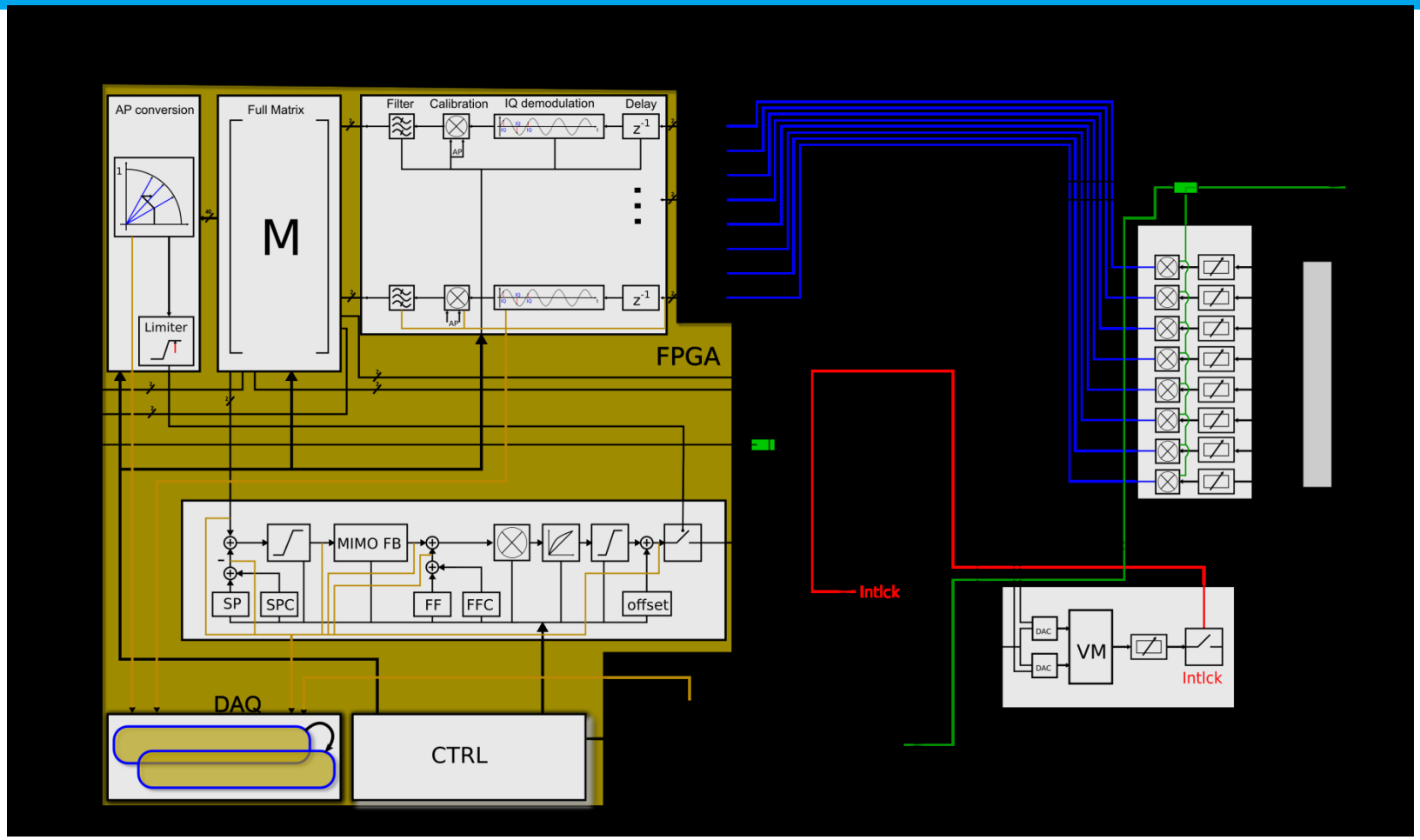


- Delay adjustment for cavity signal alignment (cable, beam travelling)
- Equal beam loading compensation
- Downsampling optmization

To be done next

- New ADC front end board SIS8300L
  - Firmware migration and adaptation
  - Decoupling FW functional and application part
  - Data transmission through LLL
  - DCM integration and performance test
- Single cavity regulation **DWC + SIS8300 + uTC+ uVM → SIS8300L + uDWC_VM**
  - Controller migration + additional functionalities
  - Different facilities to be equipped (see talk Holger, Matthias)
  - Use of hardware resources for latency optimization
- Firmware / server documentation and manual
  - Test procedures for FW loads
- Possible adaptation for future projects

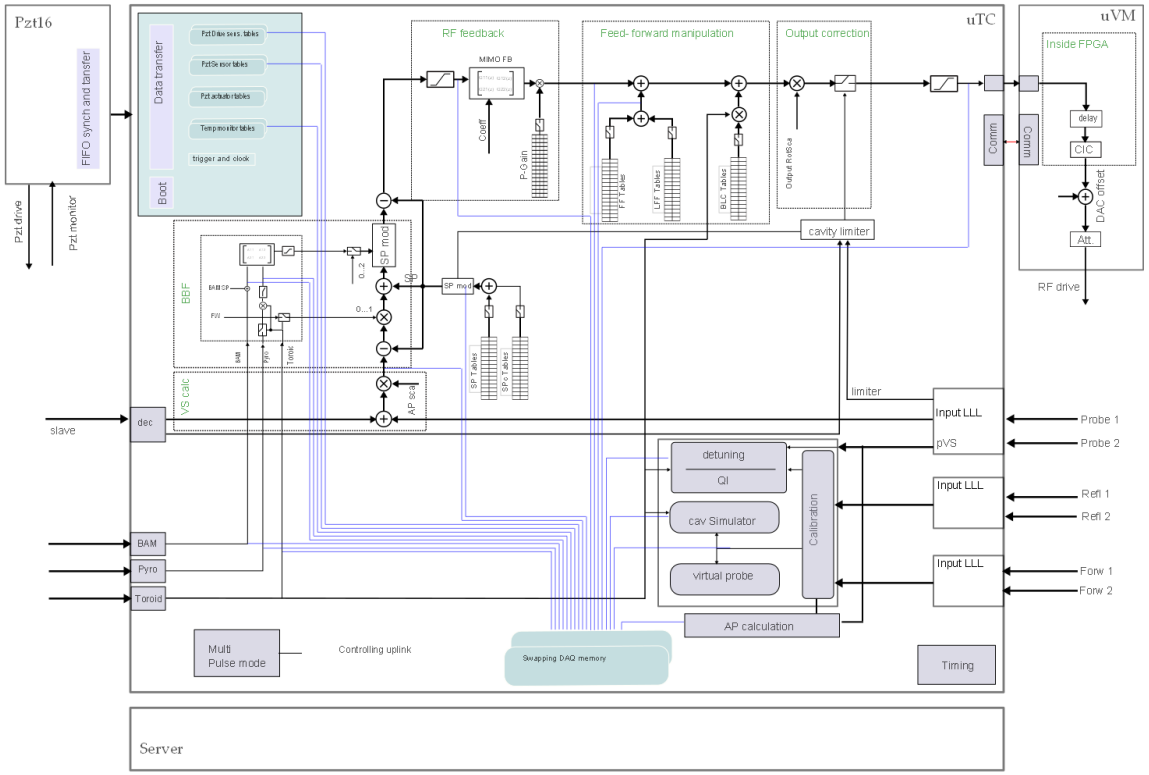
Single cavity regulation functional block diagram



- Merging uTC + SIS Firmware within new SIS8300L AMC module
- Additional LLL for signal transmission/ integration with additional subsystems (backplane, SFP front)
- Direct feedback loop with low latency, optimization of proccessing steps
- Multi purpose matrix for signal combination

uTC functionality update

- Basic controller applications are commissioned
  - SP, FF, P-Feedback and loop parameter adjustment
- Additional controller functionalities
  - MIMO FB (4th order upgrade missing), LFF integration
  - Cavity limiters, pre-limiters, smooth table generation



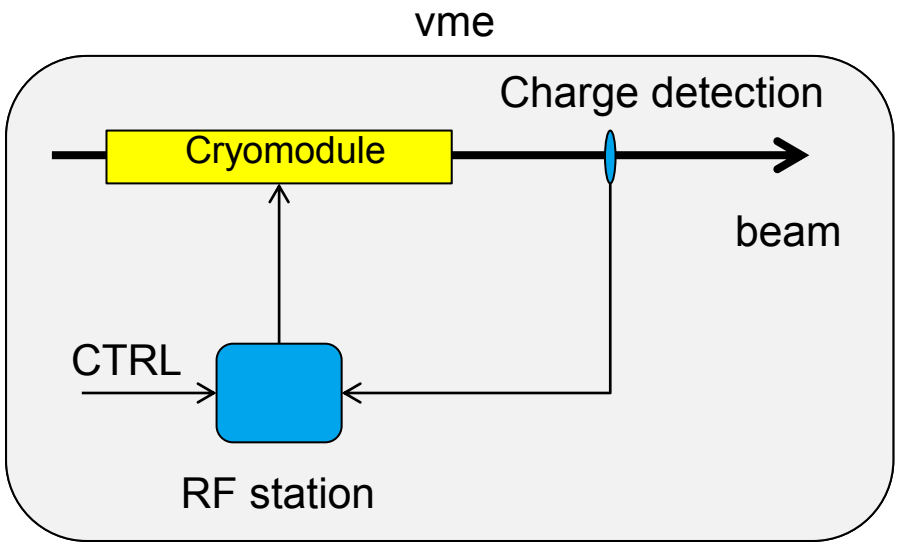
- Closed loop operation
- Limited FPGA Mem space
- Upgrade new uTC Version
- Communication BW increase (LLL)
- Loop delay measurement
- Controller optimization
- Gain scheduling
- Bit-level definition

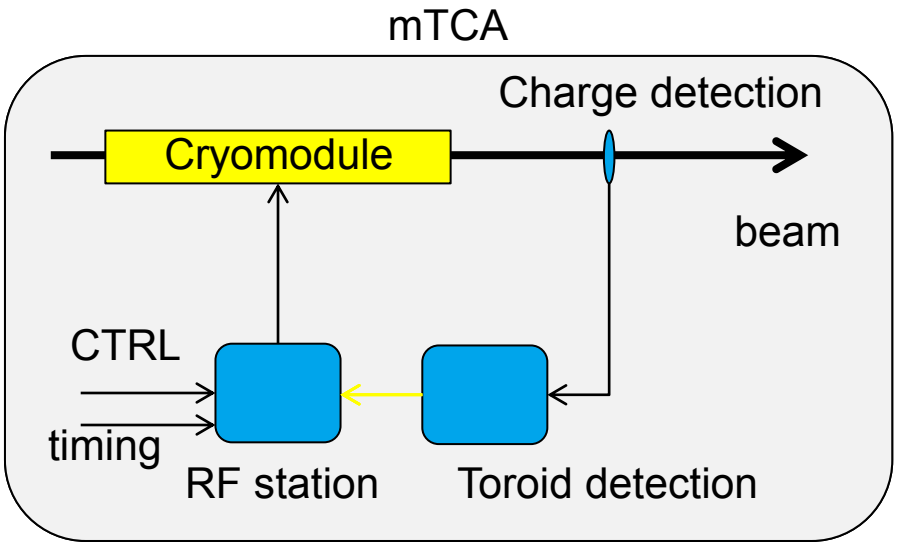
uTC functionality to be integrated

- Forward and reflected signal calibration
  - Detuning and QI measurement on the board
- Piezo communication and DAQ module
  - Reserved space on uTC, excitation computation/load
- Communication and control of VM
  - Adjustable delay and attenuation
  - DAC offset compensation
  - Interpolation CIC filter
- Integration of beam based signals
  - BAM and BCM signals
  - Protocol for beam based information
  - Signal, calibration information, error flag
- Master slave communication module
  - Two separate FW versions
  - Bit level for controller parameters and tables
- Intercommunication for RF stations
- Multi beam operation (integration of timing signals on FW level)

Implementation transition to mTCA platform

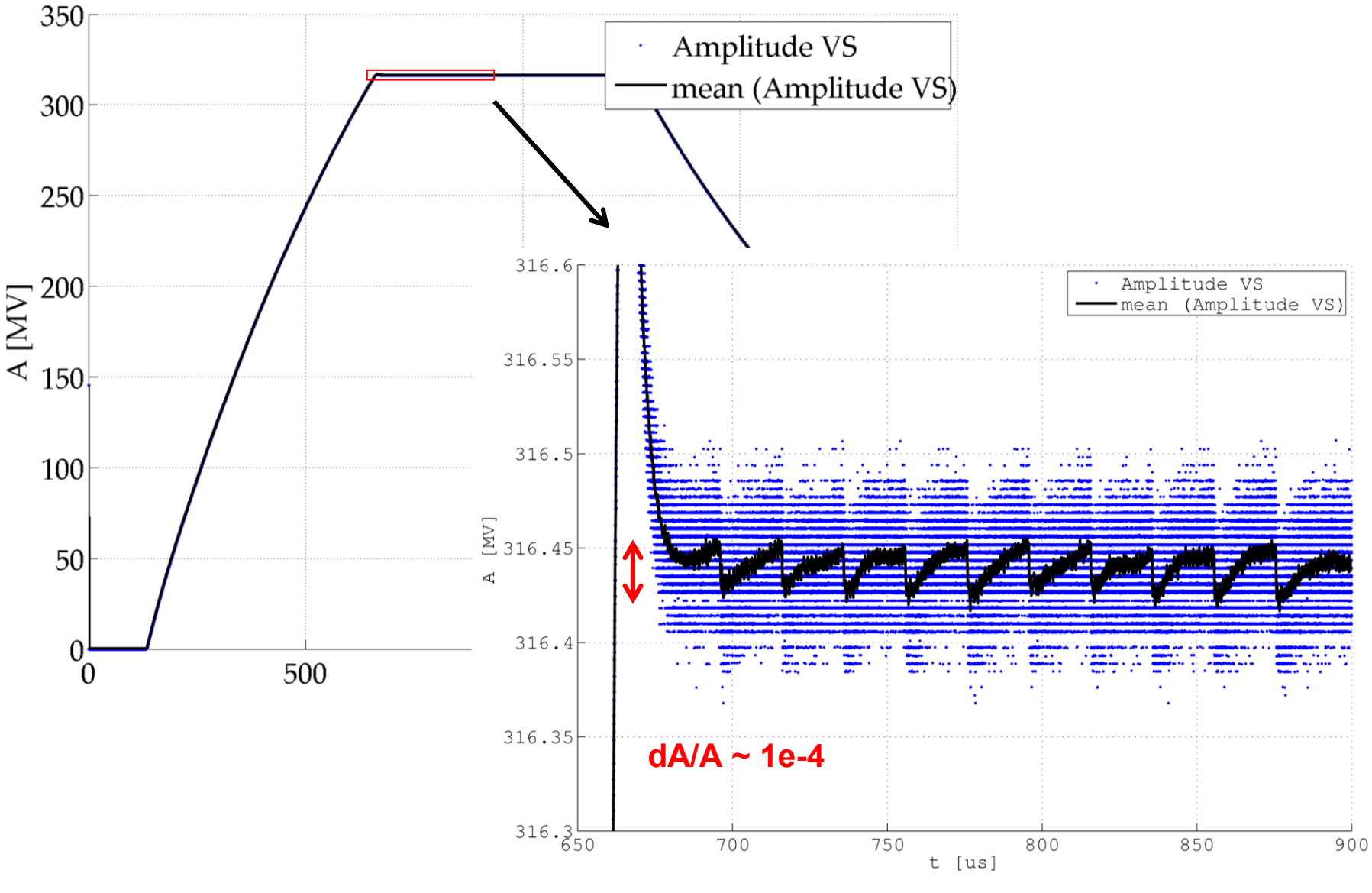
- Detection done outside controller board
  - Optical data transfer (common protocol for all beam based information)
  - Integration with timing system (fast MPS)





- A-priori information about expected beam pattern and charge (level)
  - Various beam pattern within one pulse (later pulse to pulse)
- 9 MHz sampling @ max. beam rep rate of 4.5MHz
  - Beam on/off sample and hold functionality

Beam loading at ACC23 without compensation



FLASH LLRF installations

- We want to run mTCA based LLRF system after FLASH shutdown
- Infrastructure, HW and software updates to new boards **4 month !!!**

System	Installation	Date	Issues/ remaining	Note
RF gun	Inside tunnel	07/2013	Different HW configuration, RF cabling inside tunnel	Single cavity regulation
ACC1	Injector hutch + tunnel	09/2011 07/2013	BAM,BCM, Toroid cabling inside tunnel	Main development system, corelation meas.
ACC39	Inside tunnel	07/2013	HW availibility ?	ACC1/39 comb. test
ACC23	Inside tunnel	12/2012	To be exchanged with current ACC67 setup	Radiation, remote test system, first 6 ADC ch.
ACC45	Cryo annex	07/2013	Copy of ACC67 installation	RF recabling needed, currently 67 splitted
ACC67	Cryo annex	10/2012 02/2013 ???	New DWC att not controllable, test failed	Master-slave configuration

Discussion proposals

- BBF, cabling needed, optical synchr. infrastructure prerequisite
  - Functionality not mandatory at beginning, communication link installation
- Beam loading compensation to be tested
  - Cabling to be done for all inner tunnel crates
  - Problem with old uTC, FPGA mem space (new uTC board)
- Master slave configuration to be tested
  - Initial test at ACC67 (before recabling?)
- Synchronization server (system transition)
- Backup solution VME part/full
- Priority list definition
- HW list for FLASH installation (type, configuration)

Thanks for your attention