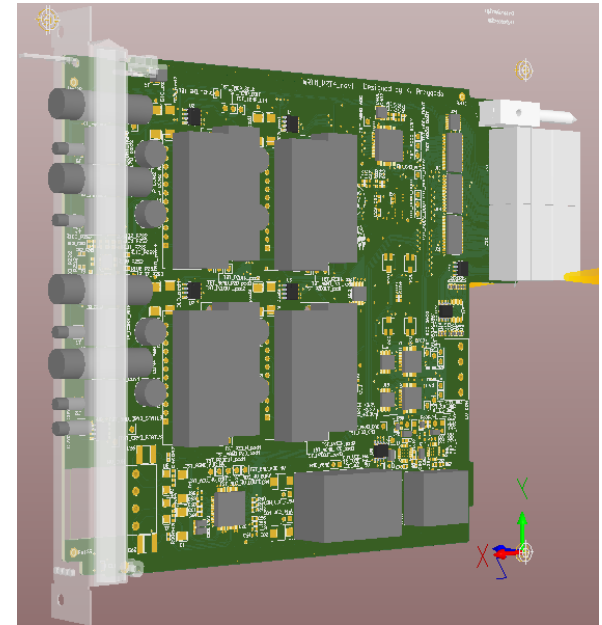


Konrad Przygoda

Workshop Seminar
2013.02.20

Motivation

- > **HVF_MTCA project (AP1.4.2.3)**
- > **Design low cost Piezo driver**
- > **Suitable for two main applications in RF technology:**
 - Piezo based frequency tuner control for SC cavity (support for single cavity RF controls)
 - Piezo based laser oscillator control for laser to RF synchronization
- > **Control electronics must be fitted to MTCA.4 hardware architecture**

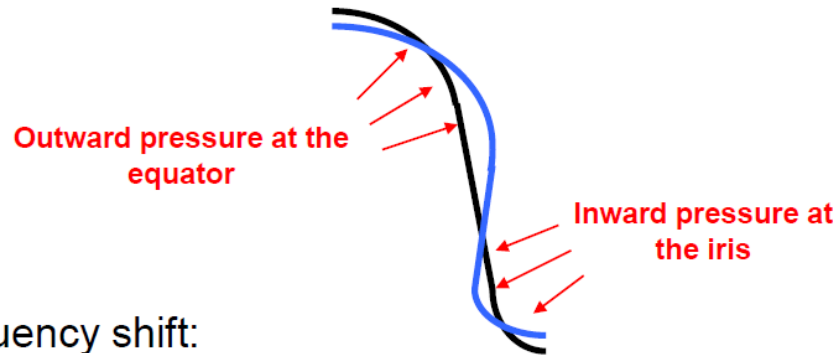


Problem#1

Pressure deforms the cavity wall:

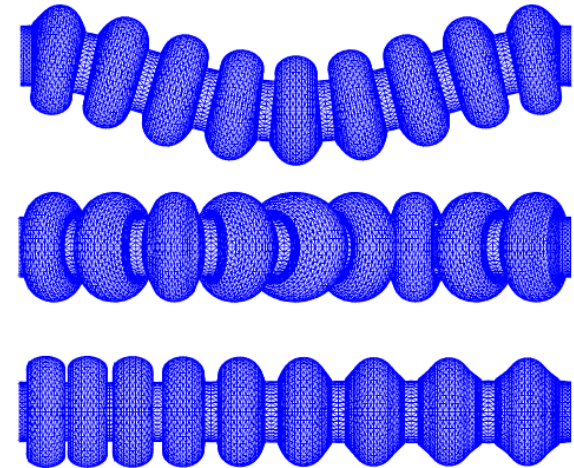
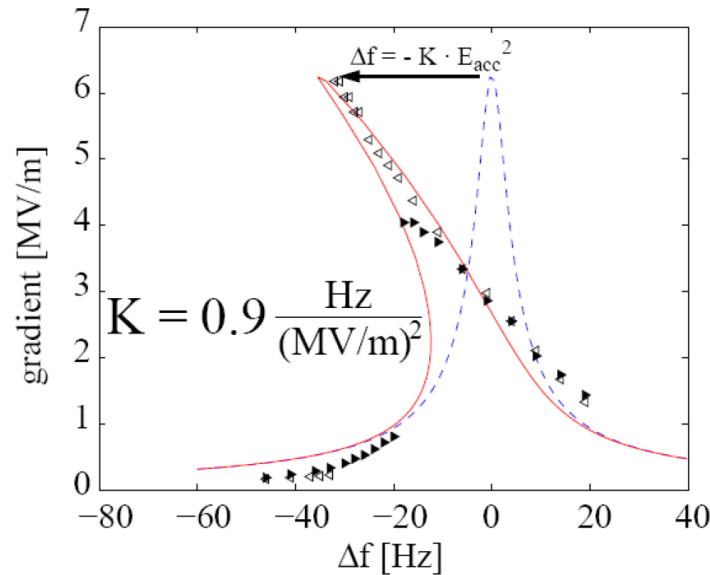
RF power produces radiation pressure:

$$P = \frac{\mu_0 H^2 - \epsilon_0 E^2}{4}$$

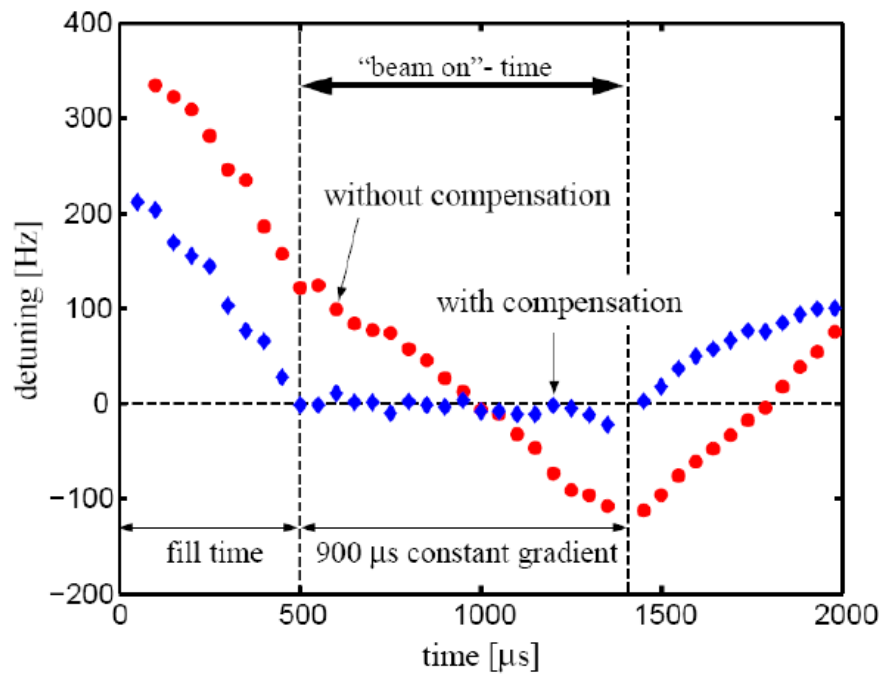
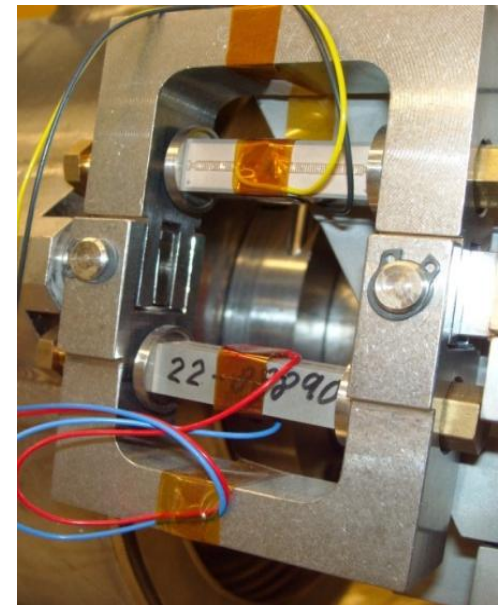


Deformation produces a frequency shift:

$$\Delta f = -k_L E_{acc}^2$$

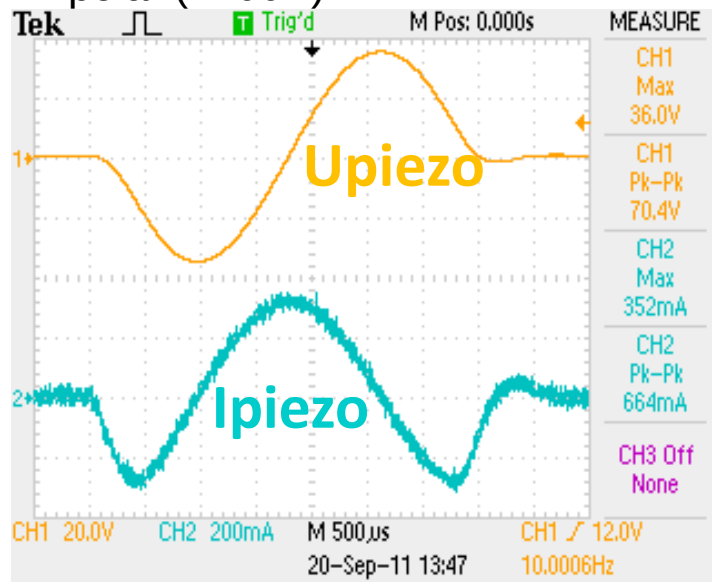


Solution#1

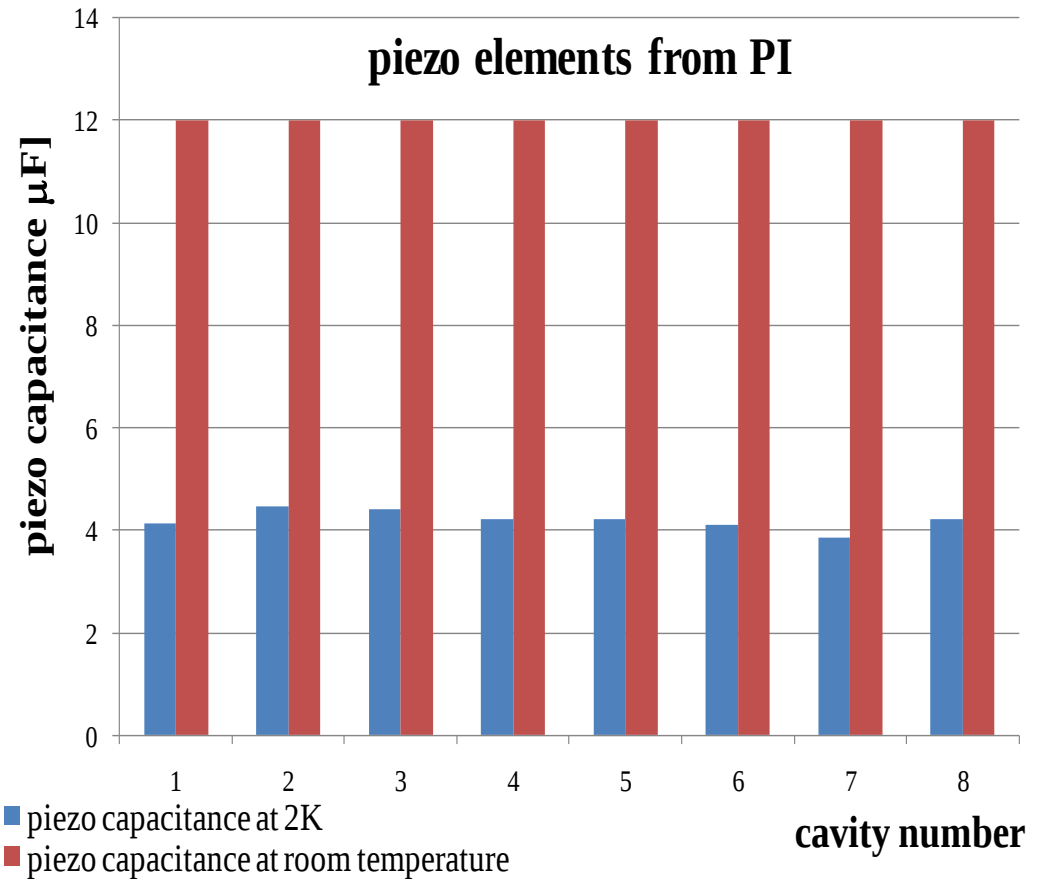
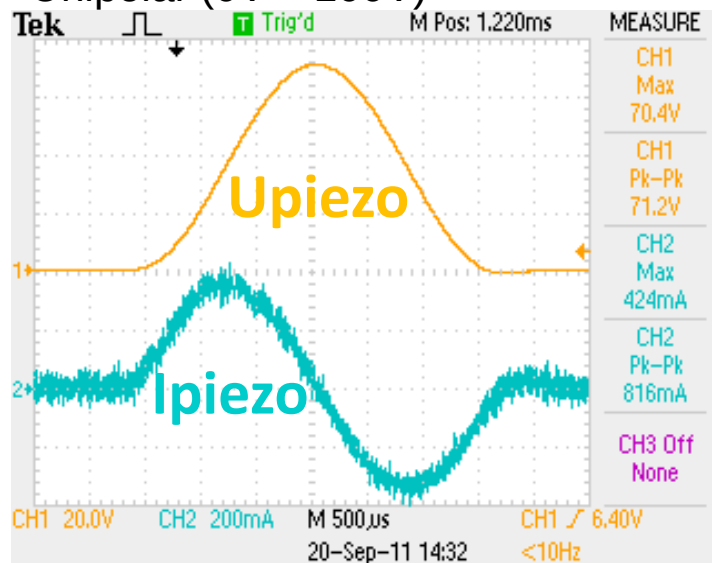


Piezo control drive for cavity tuner (LFD)

Bipolar ($\pm 100\text{V}$)



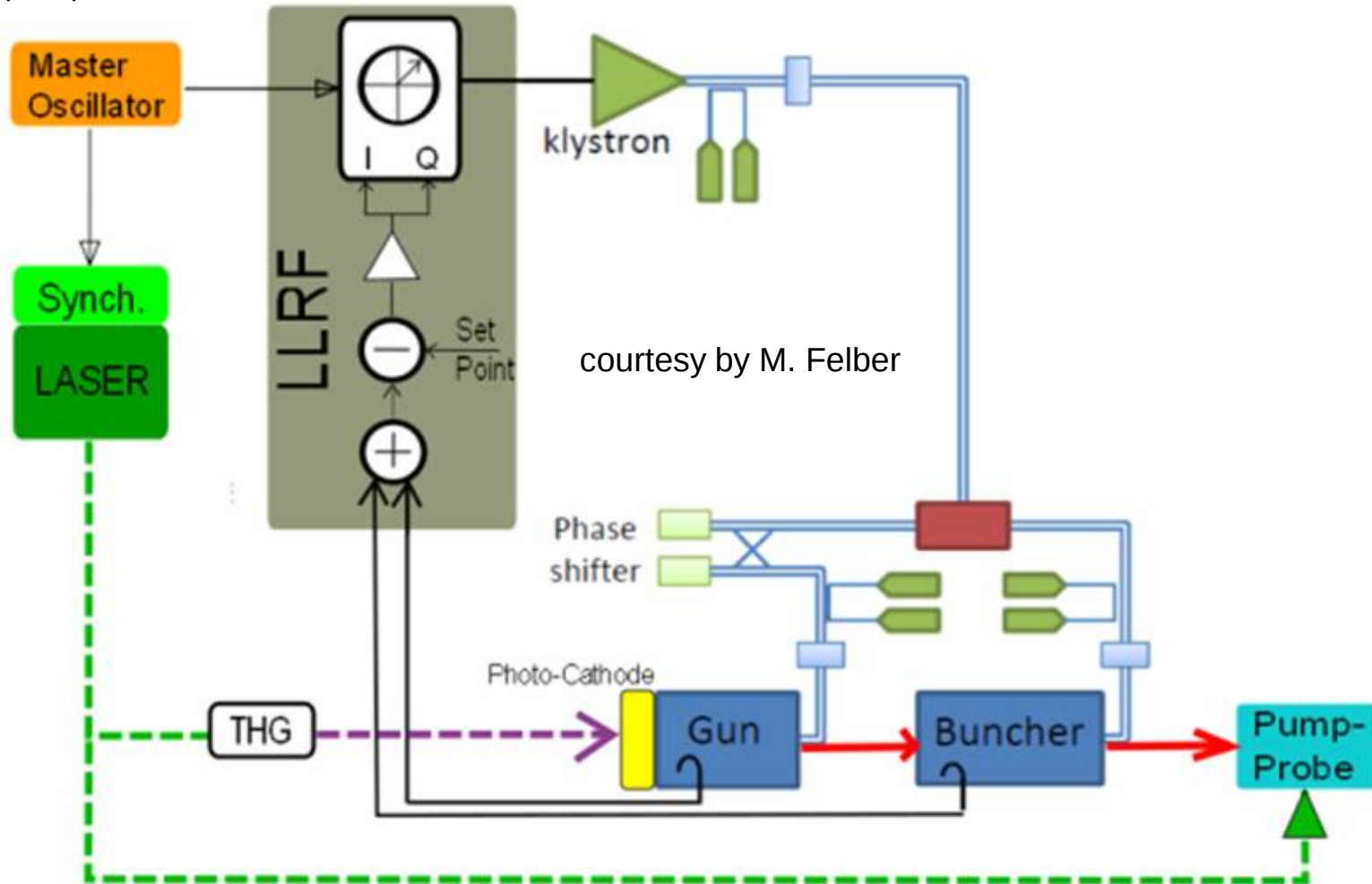
Unipolar ($0\text{V} \div 100\text{V}$)



Acceptable voltage range (in room temperature):
-20V $\div$ 130V

Problem#2

- Minimize residual jitter between the laser (Ti:SA) pulse train and the master oscillator reference (MO)



Expected piezo capacitance

series RA part no.		unit	RA 12/24 P-401-10
motion ($\pm 10\%$)*	open loop	μm	12
capacitance ($\pm 20\%$)**		μF	2.9
resolution***	open loop	nm	0.03
resonant frequency***		kHz	18
stiffness***		N/ μm	160
blocking force***		N	2000
pre-load		N	300
dimensions	length L	mm	36.5
	diameter D2	mm	24
	diameter D1	mm	9
weight		g	75

technical data

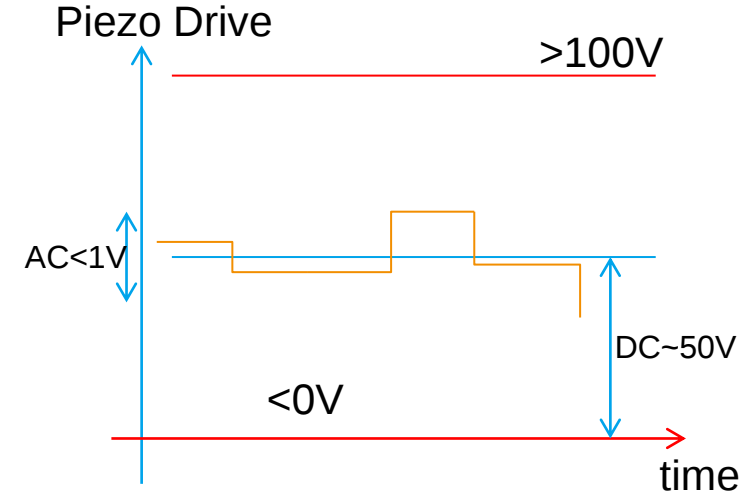
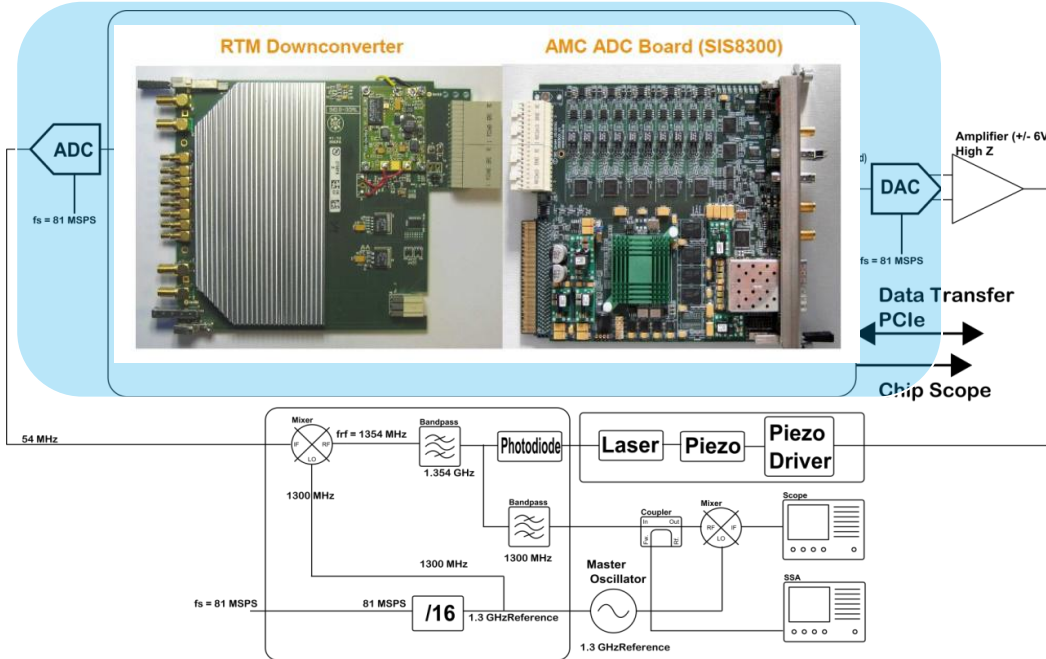
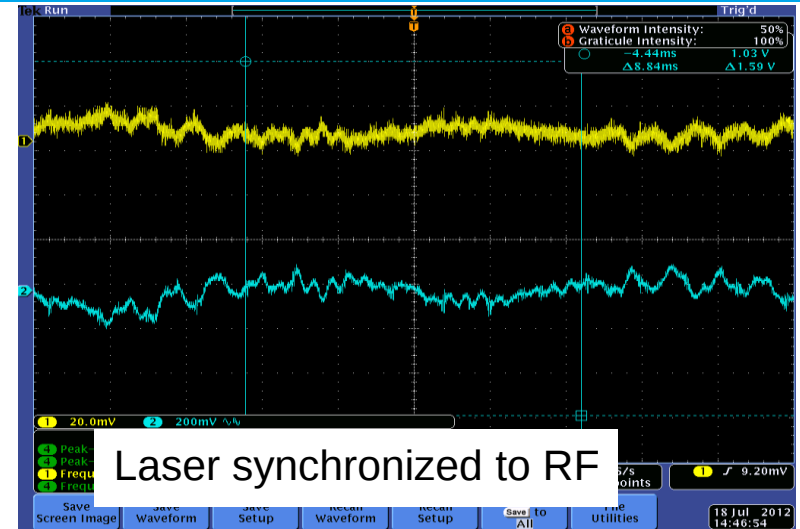
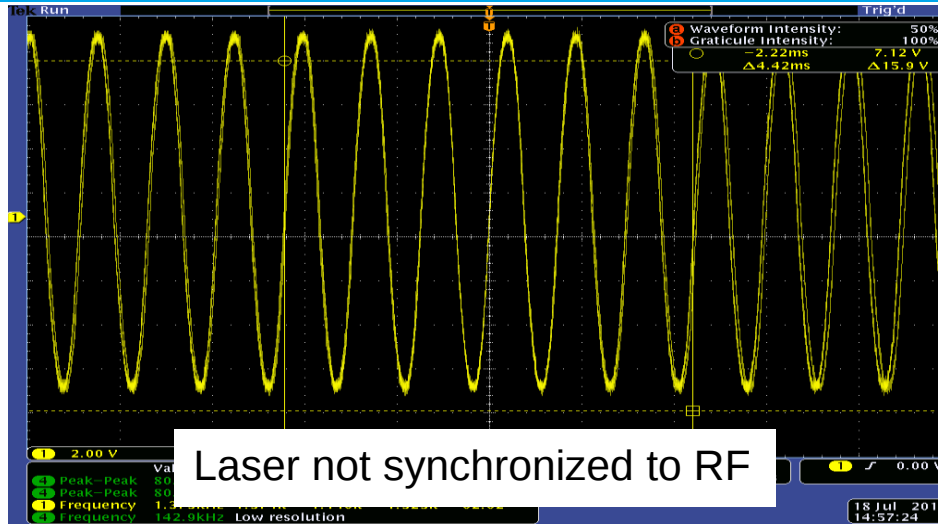
- operating voltage: -20 to +130V
- housing series RA: stainless steel
- bottom plate:
 - thread M12x0.5, spanner flats: 20mm for RA XX/24
 - thread M18x0.5, spanner flats: 27mm for RA XX/35
- optic adapters for RA series with inside thread
(part no. P-400-05 for RA XX/24 and P-400-10 for RA XX/35 series)

series PA part no.		unit	PA 4/12 P-150-00	PA 8/12 P-151-00
motion ($-10/+20\%$)*		μm	4.5	9.5
open loop				
capacitance ($\pm 20\%$)**		μF	0.34	0.7
resolution***		nm	0.009	0.019
open loop				
resonant frequency***		kHz	65	40
stiffness***		N/ μm	190	90
blocking force***		N	850	850
pre-load		N	150	150
dimensions	diameter D	mm	12	12
	length L	mm	22	26
series PA with spherical end R2.5 part no.			PA 4/12 R2.5 P-150-50	PA 8/12 R2.5 P-151-50
dimensions	length L	mm	23	27

technical data

- operating voltage: -20 to +130V
- housing: stainless steel
- top plate: thread M3
spanner flats: 3.5mm
- bottom plate: thread M3
spanner flats for PA XX/12 series: 10mm
spanner flats for PA XX/14 series: 12mm

Solution#2



courtesy by M. Felber & U. Mavric



System requirements (1)

> **Double width MTCA.4:**

- Rear-Transition Module (RTM), Zone3 Class D1.[0..2] compatible
- AMC Module support and standalone operation

> **High voltage power supply:**

- 0 V ; +100 V (unipolar)
- ± 100 V (bipolar)

> **Low voltage power supply:**

- +3.3 V; +5 V; ± 15 V

> **No. of input channels: 4 (4 x piezo sensors):**

- ADC sampling rate: min. 100 kSPS per channel

> **No. of output channels: 4 (4 x piezo actuators) :**

- DAC sampling rate: min. 100 kSPS per channel



System requirements (2)

- > **No. of monitoring channels: 16**

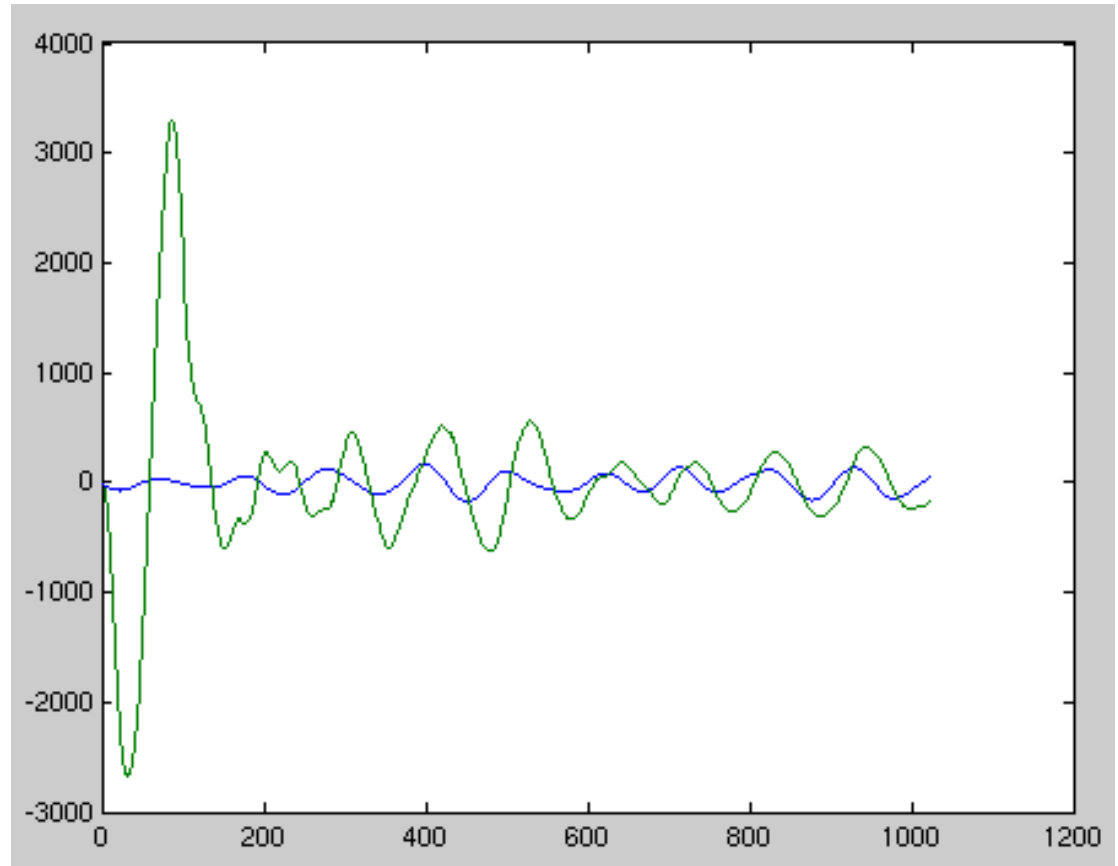
- 4 x IS – PZT input voltage
- 4 x VS – PZT output voltage
- 4 x CS – PZT output current
- 4 x HV – high voltage sense
(AC and DC components)

- > **Temperature sensors:** as close as possible to each power amplifier radiator
- > **Remote switching:** between piezo actuator and sensor functionality
- > **Interlock sensor:** to not operate piezo when cryomodule is warm



Piezo sensor input parameters

- Input impedance
 - $Z_{in} < 4 \text{ k}\Omega$
- Input voltage range
 - $\pm 2.5 \text{ V}$
- Input bandwidth (3 dB)
 - B: DC 100 kHz
- Noise level
 - $\text{SNR} < -70 \text{ dB}$
- Channel crosstalk
 - $\text{XT} < -60 \text{ dB}$

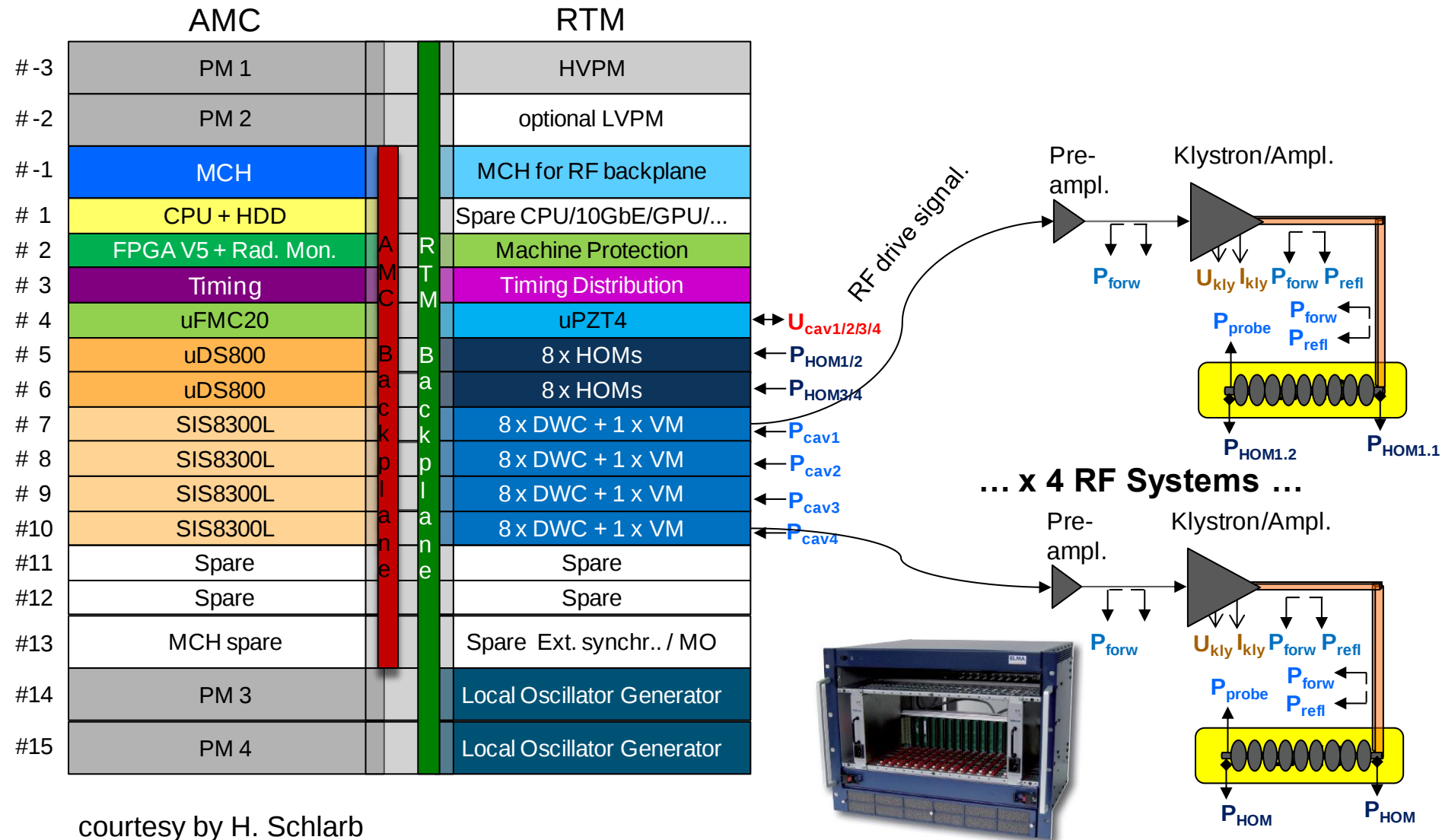


Driver output parameters

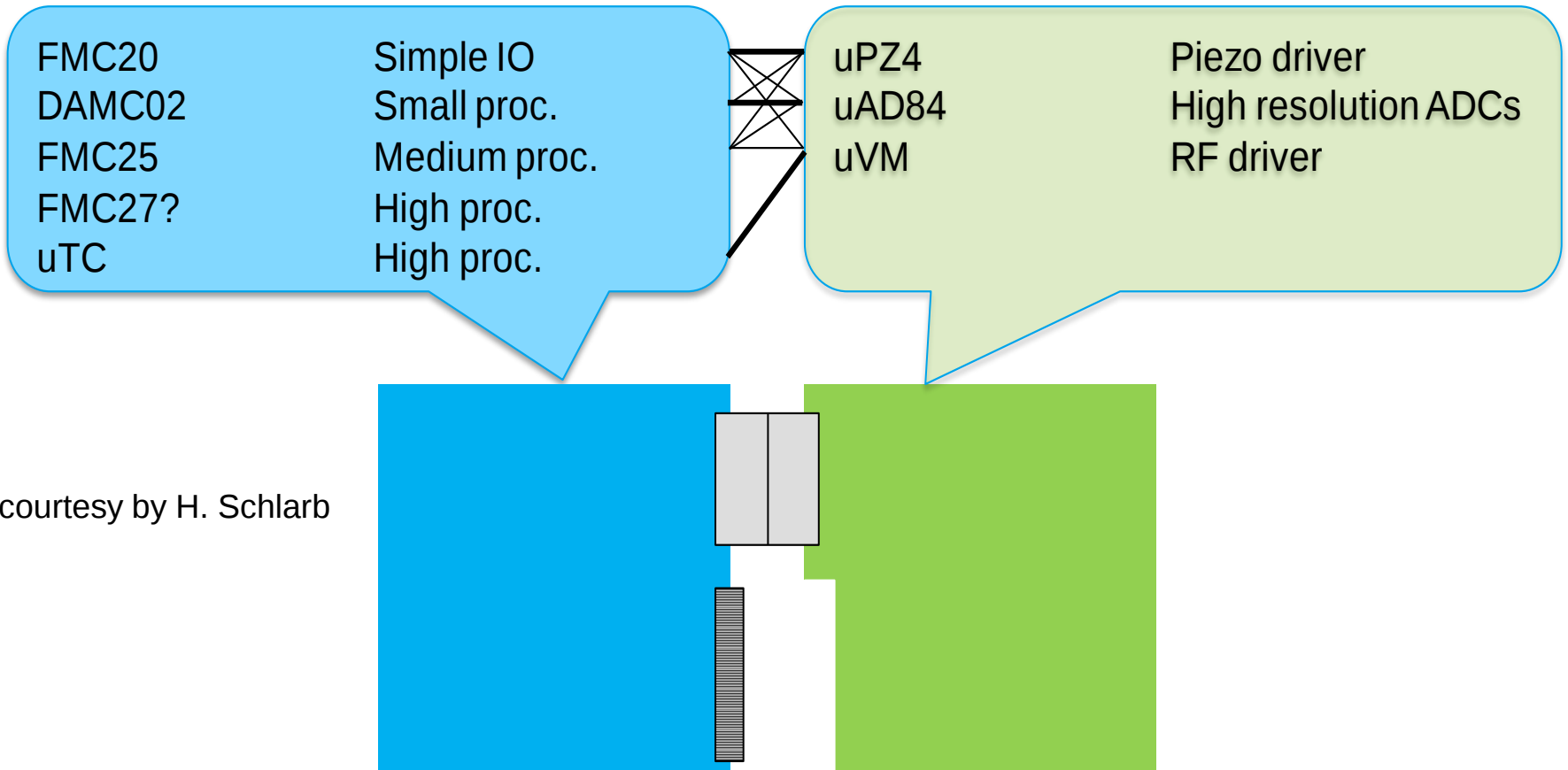
- > Output load
 - R_{load} : capacitive, $0.1 \div 6 \mu\text{F}$
- > Full power bandwidth (3 dB)
 - B: DC $\div$ 300 Hz (with maximum amplitude and load): Lorentz force detuning
- > Small signal bandwidth
 - B: DC 100 kHz (for nominal load of $1 \mu\text{F}$): Laser synchronization
- > Noise level
 - $\text{SNR} < -70 \text{ dB}$
- > Channel crosstalk
 - $\text{XT} < -60 \text{ dB}$ between any channels
- > Overvoltage protection
- > Overcurrent protection
- > Current slewrate limitation



Hardware architecture of MTCA.4 system



Single AMC-RTM combinations



courtesy by H. Schlarb

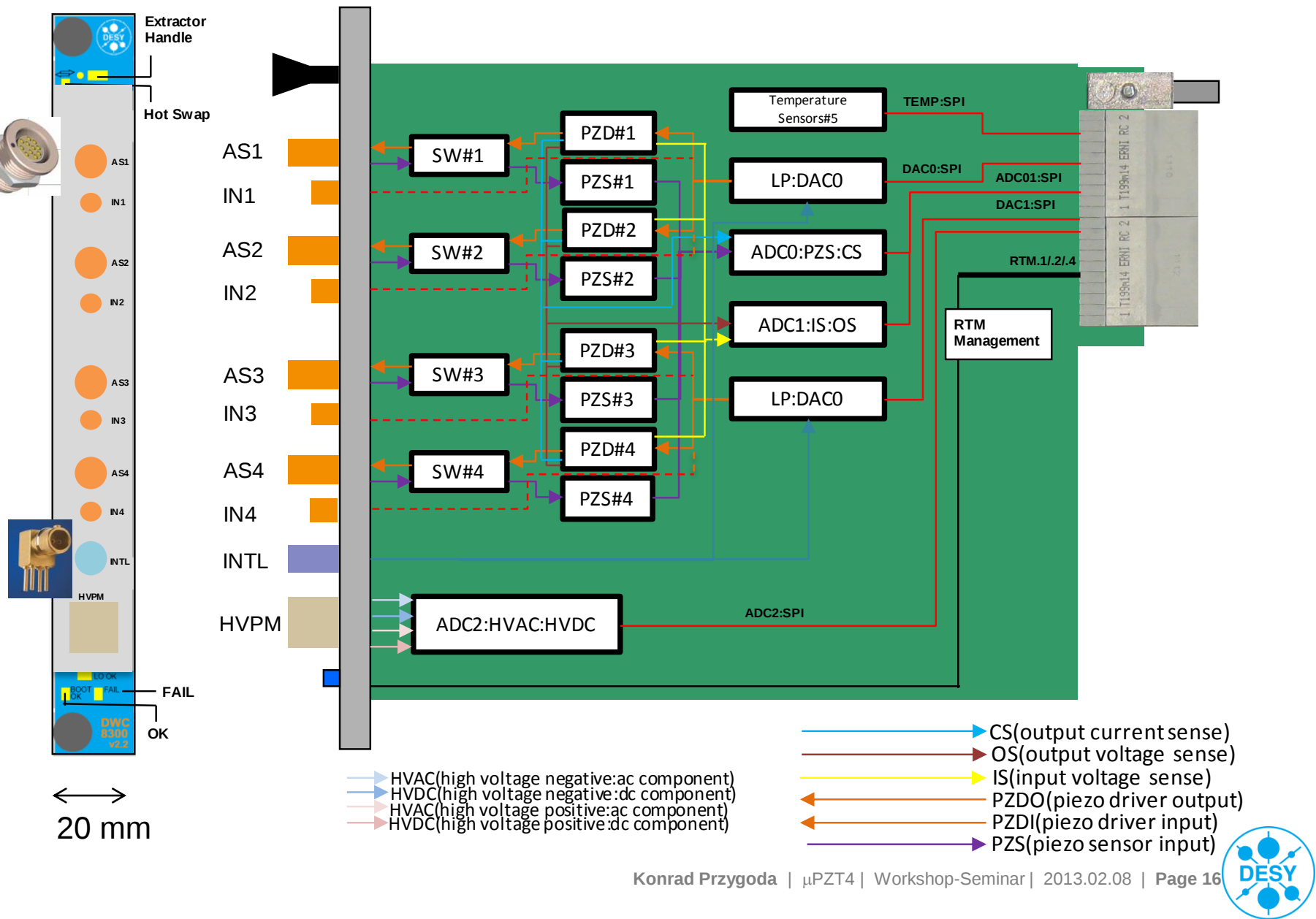
ZONE3 Class D1.[0..2] compatibility

Class D1.2 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK
		2	PWRA2	PWRB2	MP	SCL	TDI
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+
User -configuration		5	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+
		6	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO-
User Configuration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO-
		3	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO-
		4	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO-
		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO- / CC
Standard Gbit-Links		7	P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+
		8	P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+

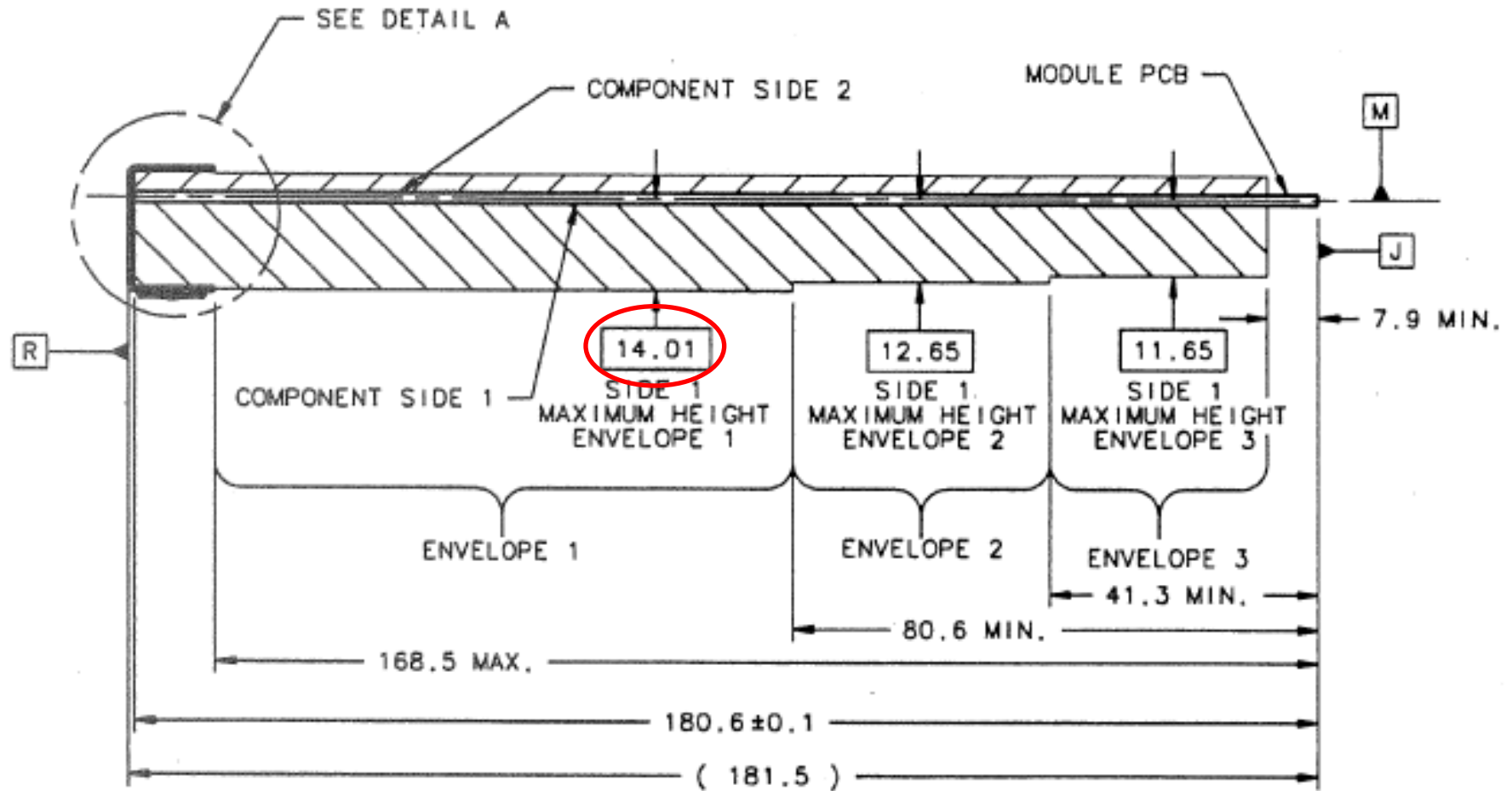
D1.2 – uTC



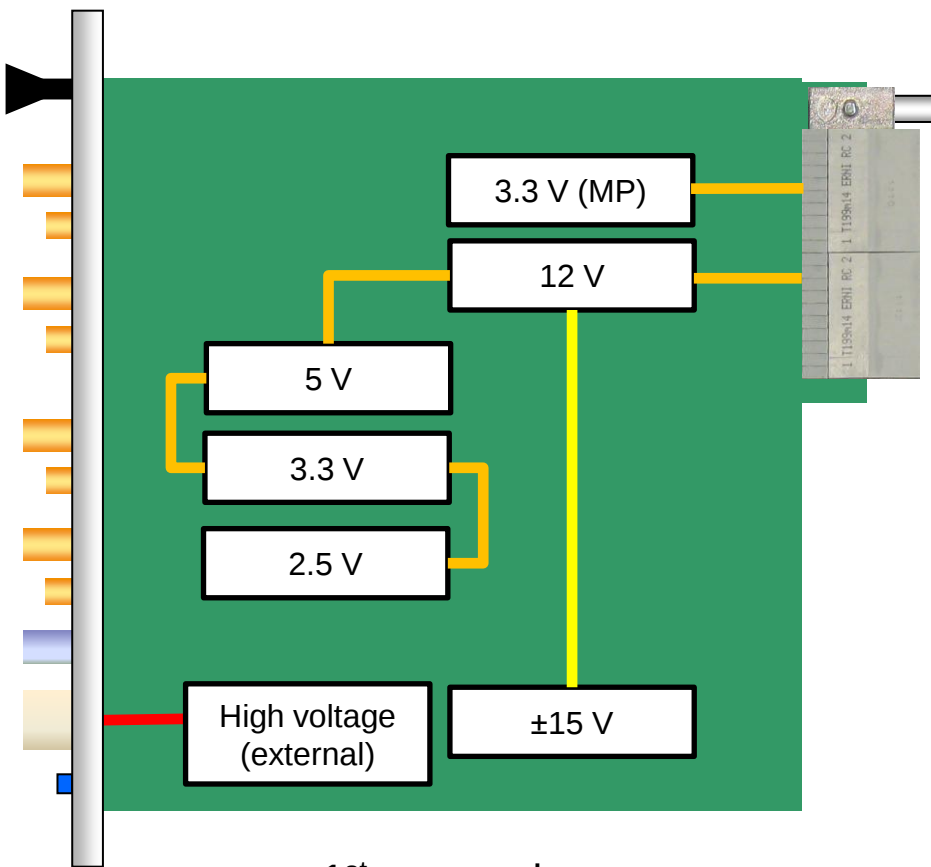
RTM- μ PZT4 block diagram



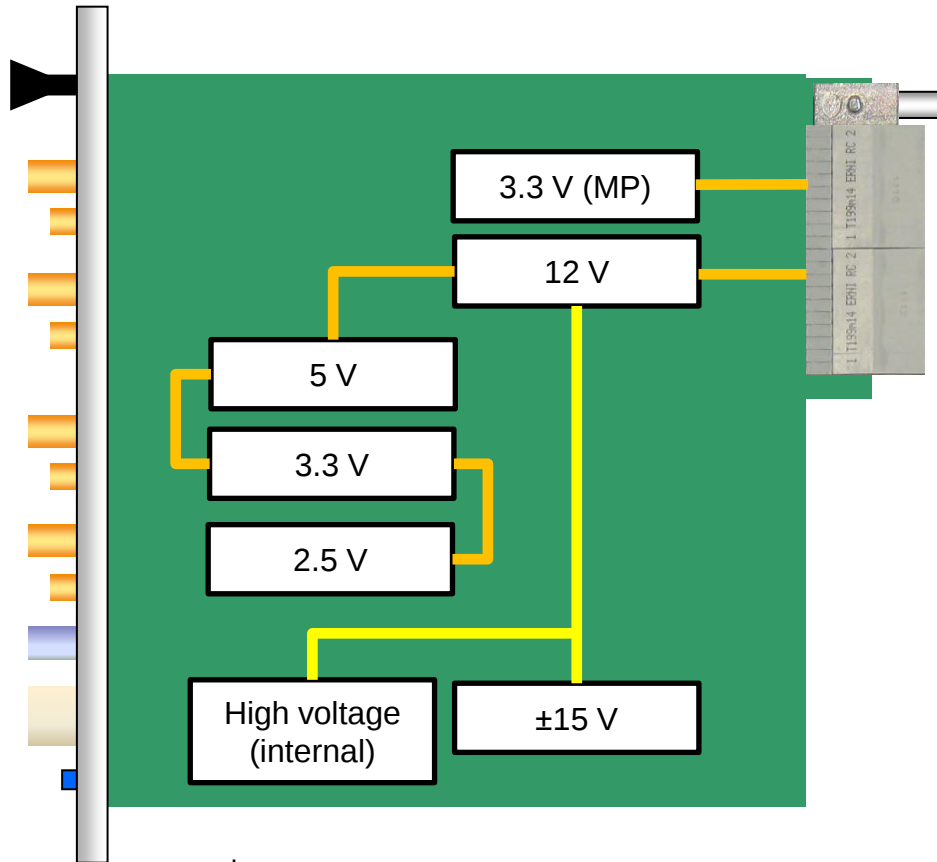
Available Maximum Height of Components for μ RTM



RTM- μ PZT4 – power supply layout proposal

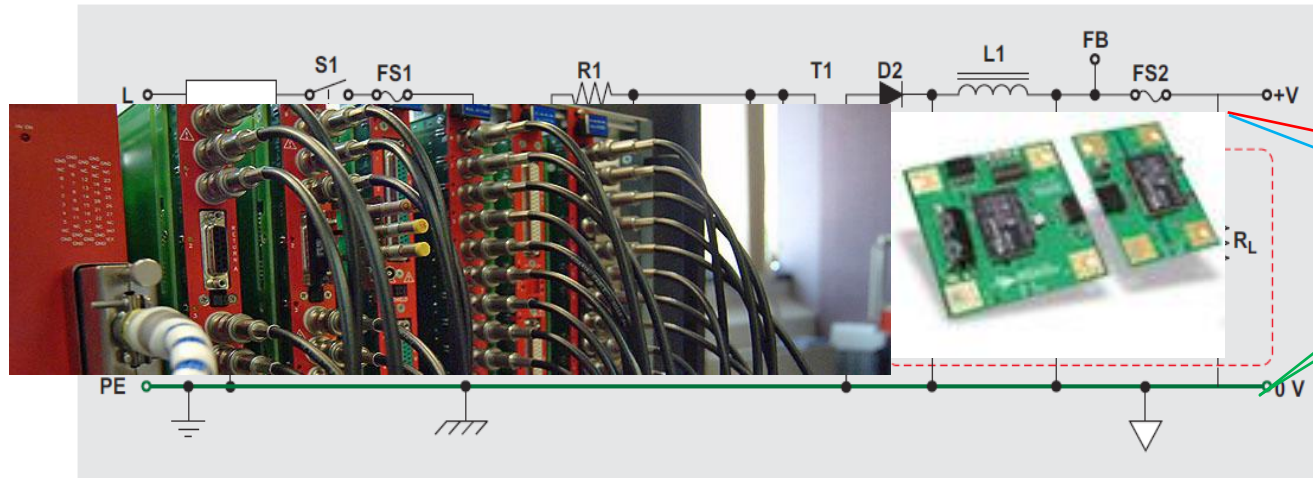


1st proposal

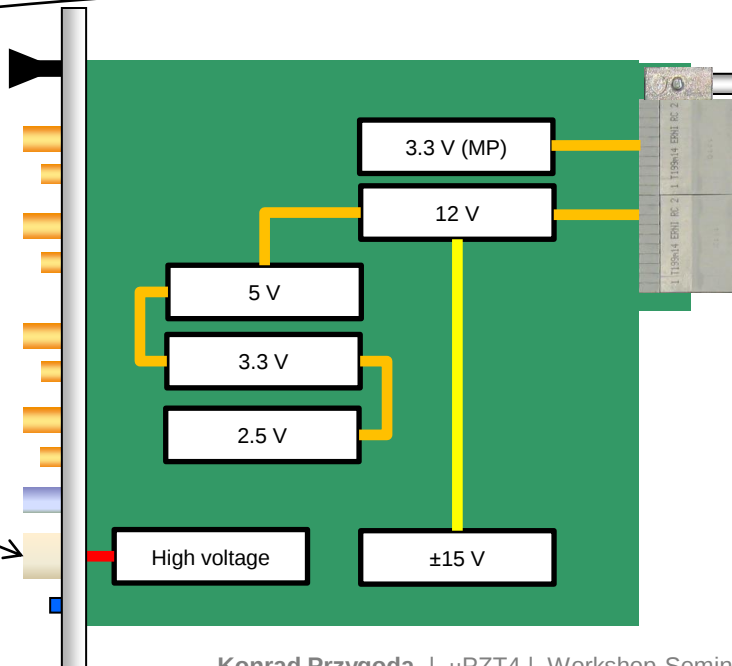
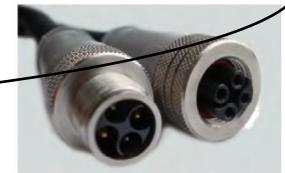
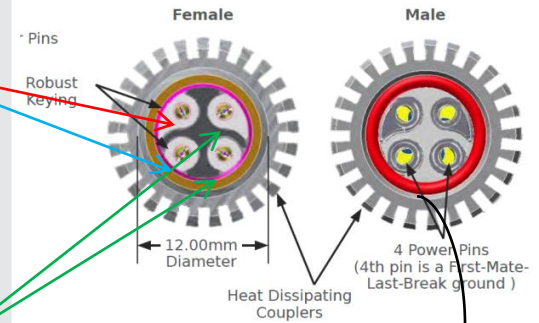


2nd proposal,
(directly or as mezzanine card)

Possible HVPM connection to RTM- μ PZT4 (1st proposal)



4-pin Version
(630V, 12.0A per pin,
up to 2.5mm² conductors)



M12 Brad
Power
Connectors
from Molex

High voltage connector with
screw based locking (4th
pin is PE and it is first
contact pin)

Power consumption – single channel

pulse mode

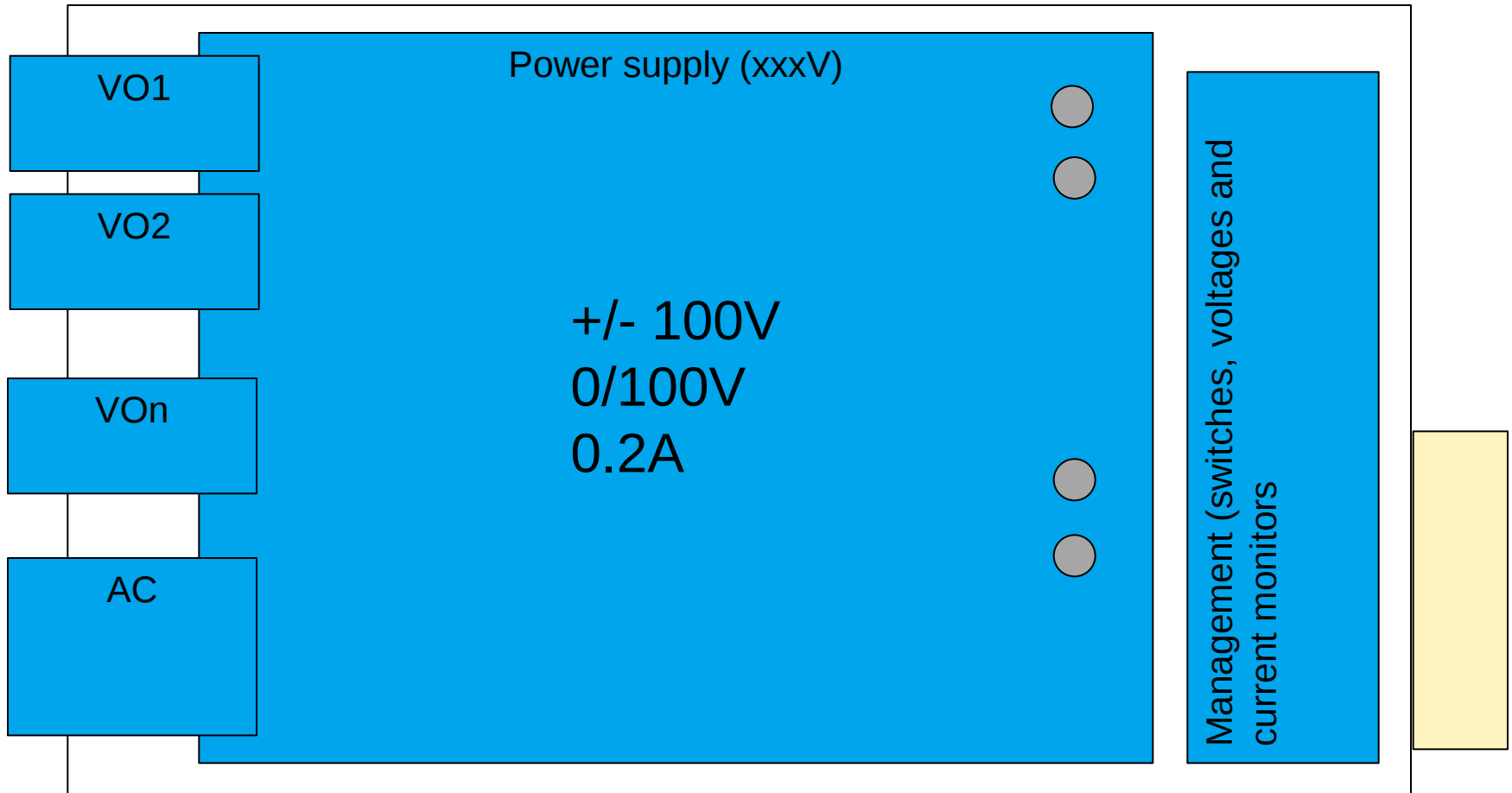
repetition [Hz]	frequency [Hz]	output voltage [V]	I _{vcc} [mA]	I _{out} [mA]
100	300	~100	21	~100
25	300	~100	15	~100

cw mode

frequency [kHz]	output voltage [V]	I _{vcc} [mA]	I _{out} [mA]
100	0.5	18	~10
100	1	24	~10
100	2	36	~10

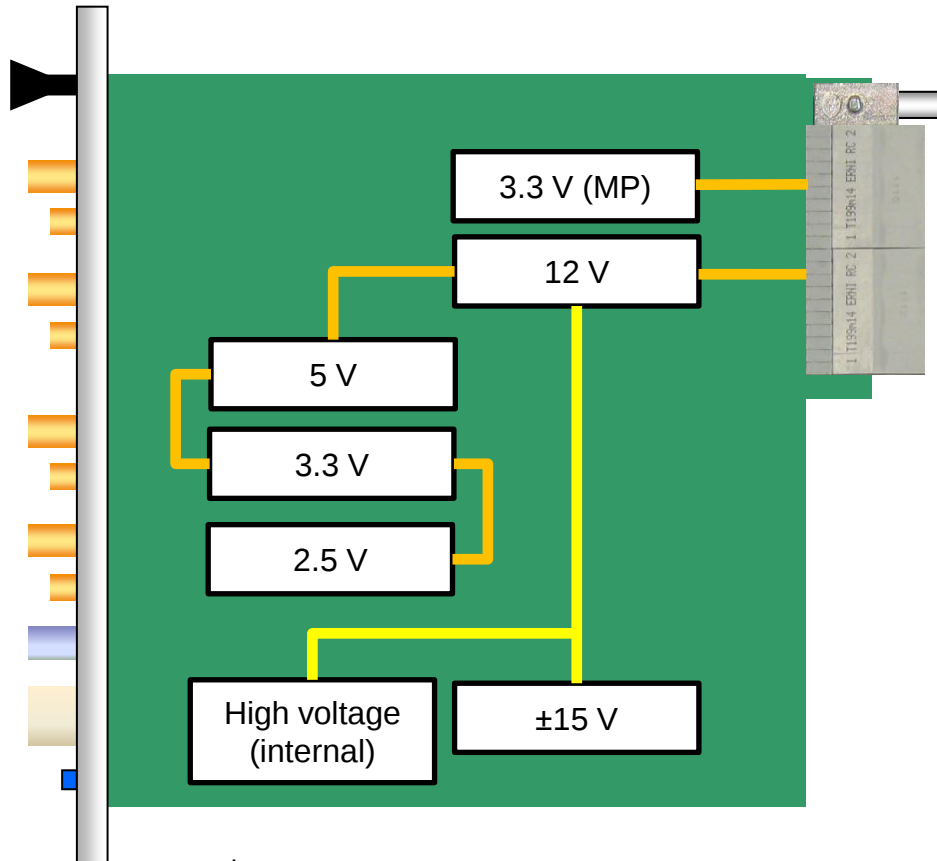


HVPM idea



courtesy by T. Jezynski

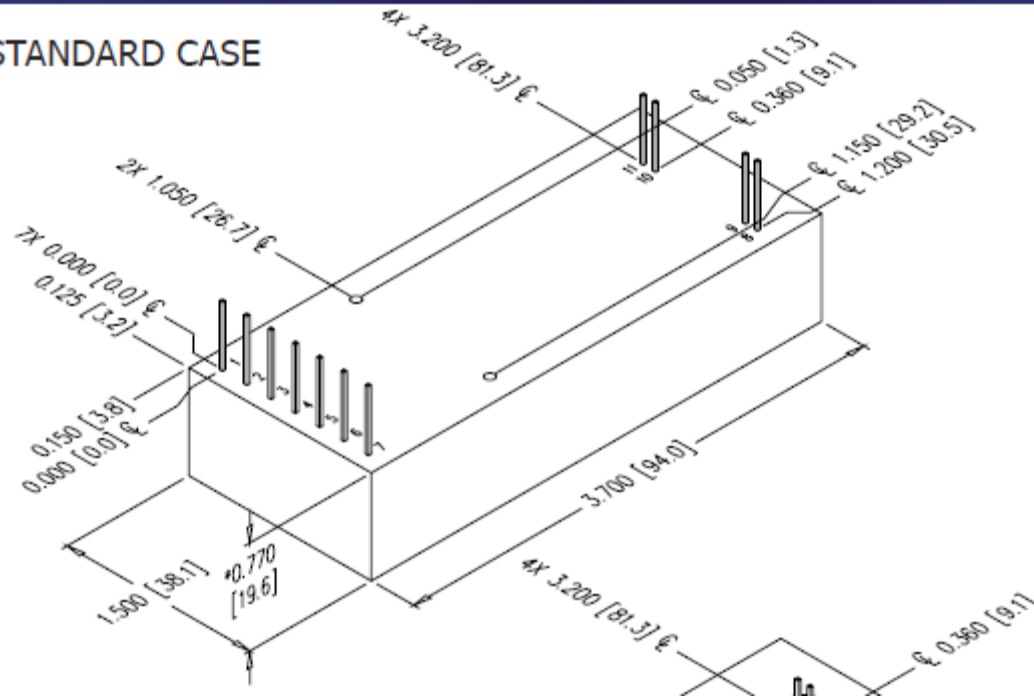
RTM- μ PZT4 – internal HVPM



2nd proposal,
(directly or as mezzanine card)

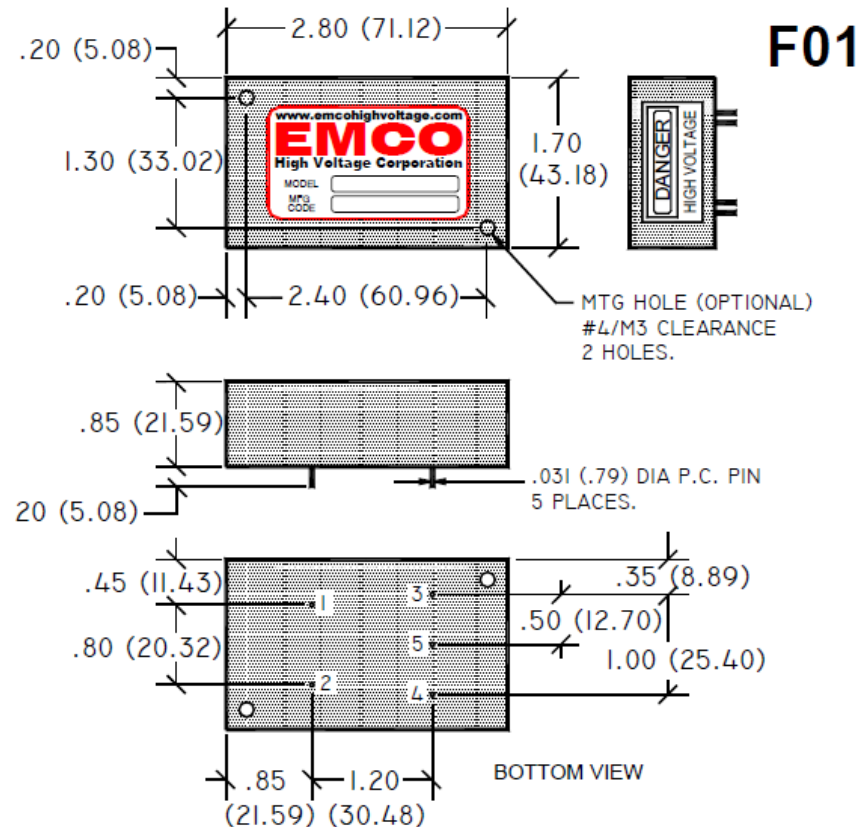
DC/DC converters (Ultravolt: up to 10W)

STANDARD CASE



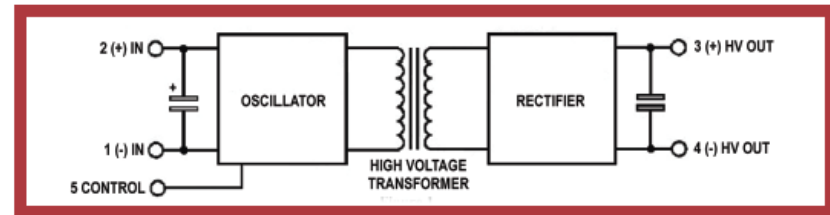
DC/DC converters (Emcohighvoltage: up to 10W)

MODEL	INPUT VOLTAGE	OUTPUT*2 VOLTAGE	OUTPUT*4 CURRENT	RIPPLE P-P
F01	0 to 12V	0 to +/-100V	100 mA	<1.0%



DC/DC converters (Emcohighvoltage: up to 1.5W)

**Extremely Low Profile: 0.128 inches
and volume of < 0.100 cubic inches²⁵**



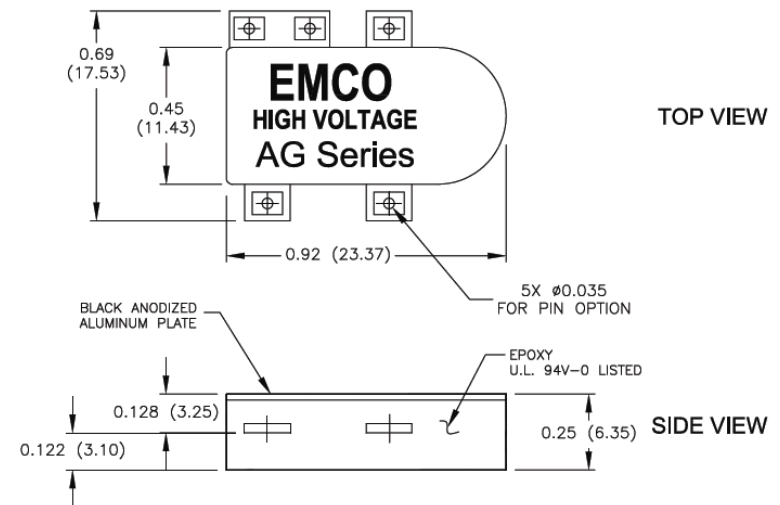
APPLICATIONS

Avalanche Photodiodes
Capacitor Charging
Electrophoresis
Photomultiplier Tubes
Piezo Devices
Mass Spectrometry
Sustaining Ion Pumps

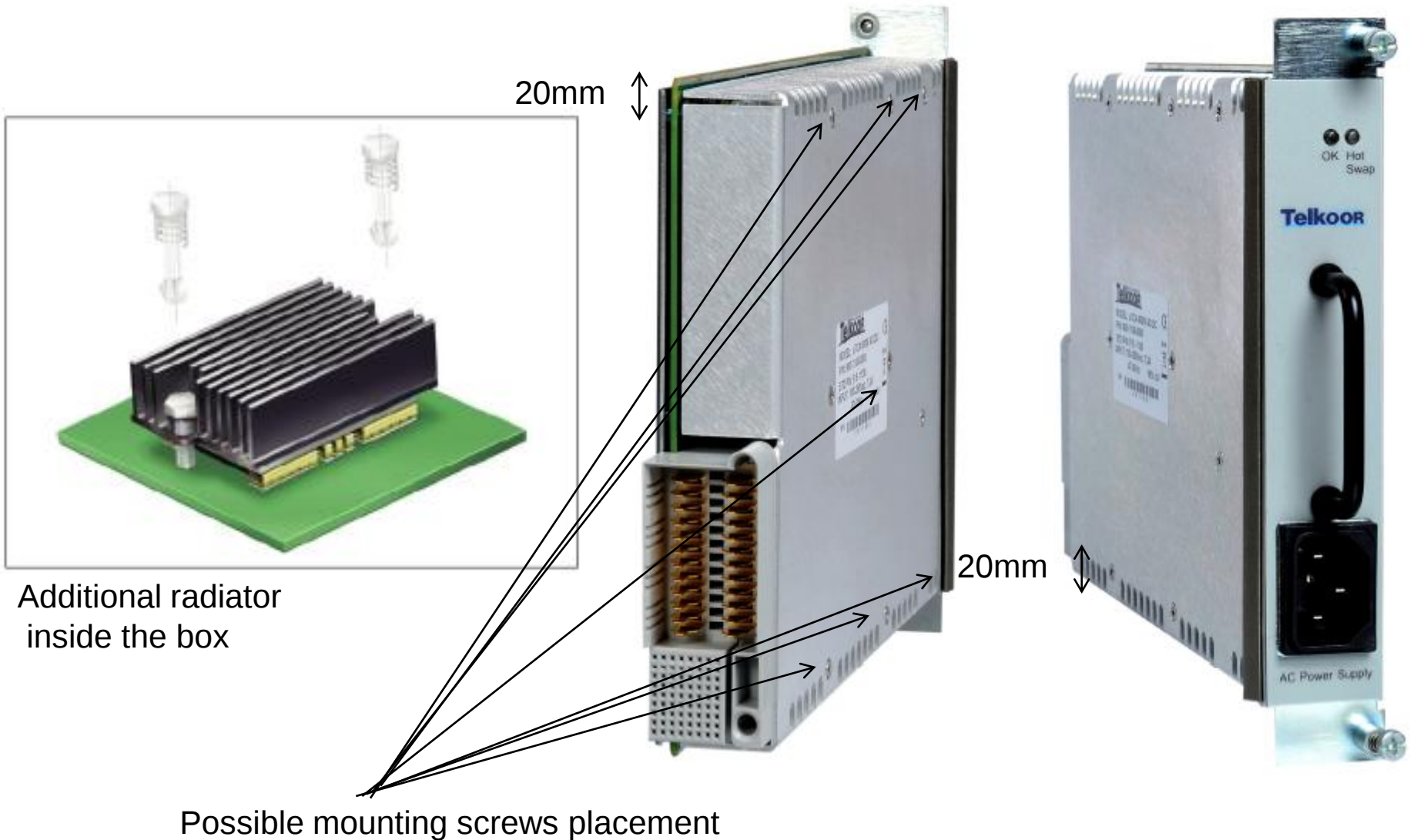


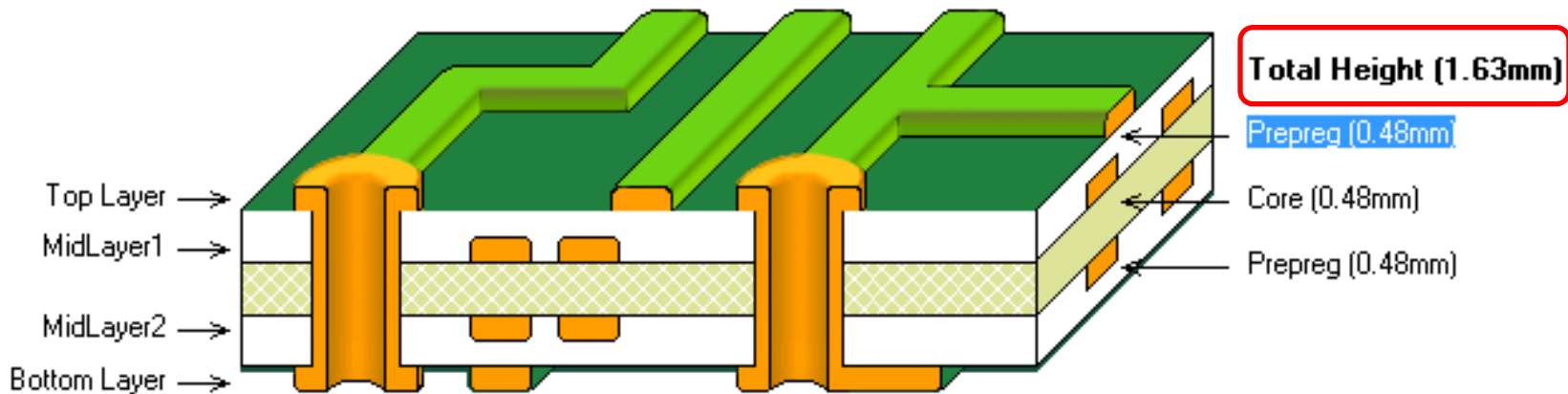
1: mezzanine card
with parallel 12V input
and 100V output

VDC	STANDARD 1 WATT - AG MODEL		1.5 WATT OPTION - AGH MODEL	
	MODEL	MAXIMUM OUTPUT CURRENT*1	MODEL	MAXIMUM OUTPUT CURRENT*1
100 VDC	AG01	10 mA	AGH01	15 mA



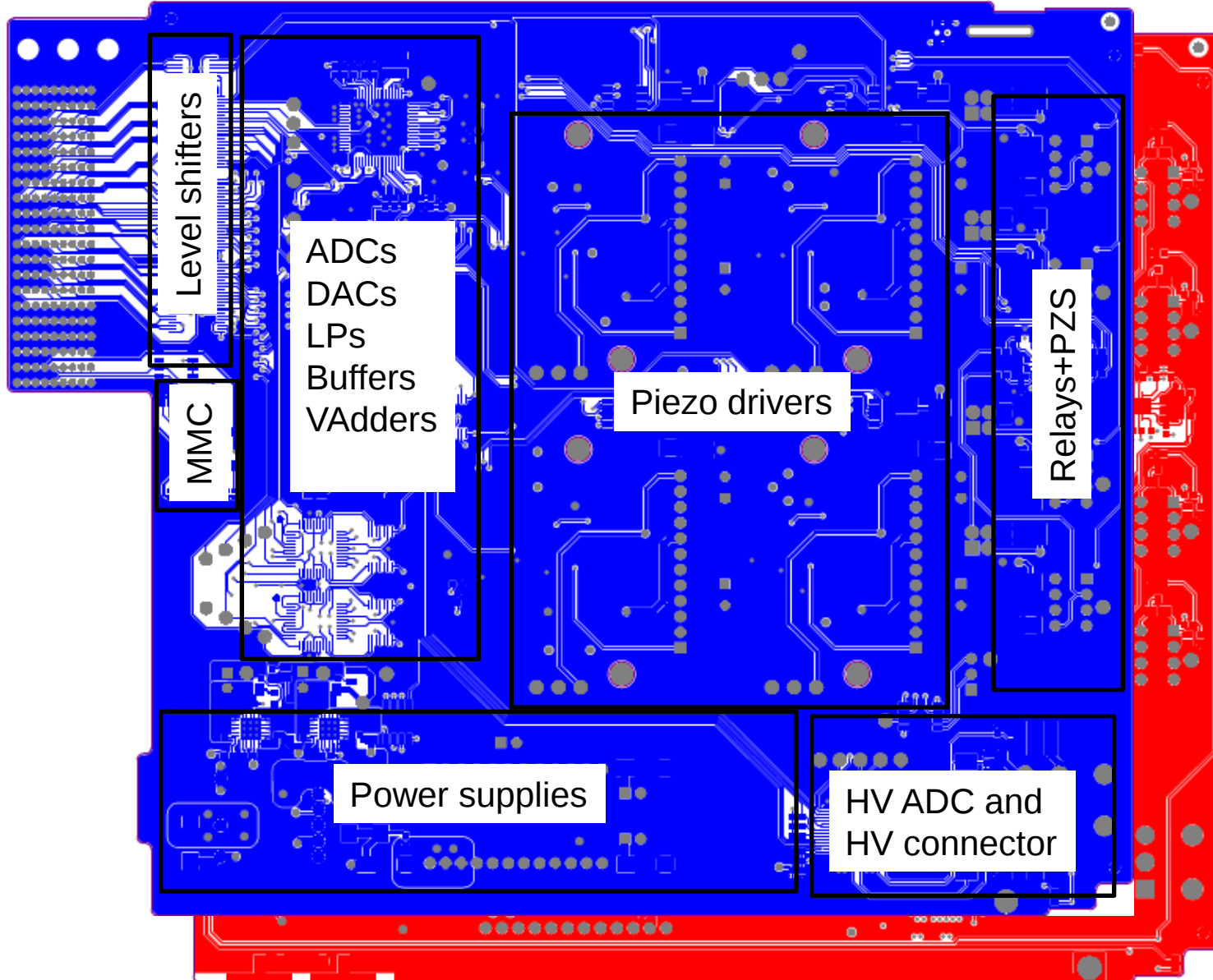
RTM- μ PZT4 packaging



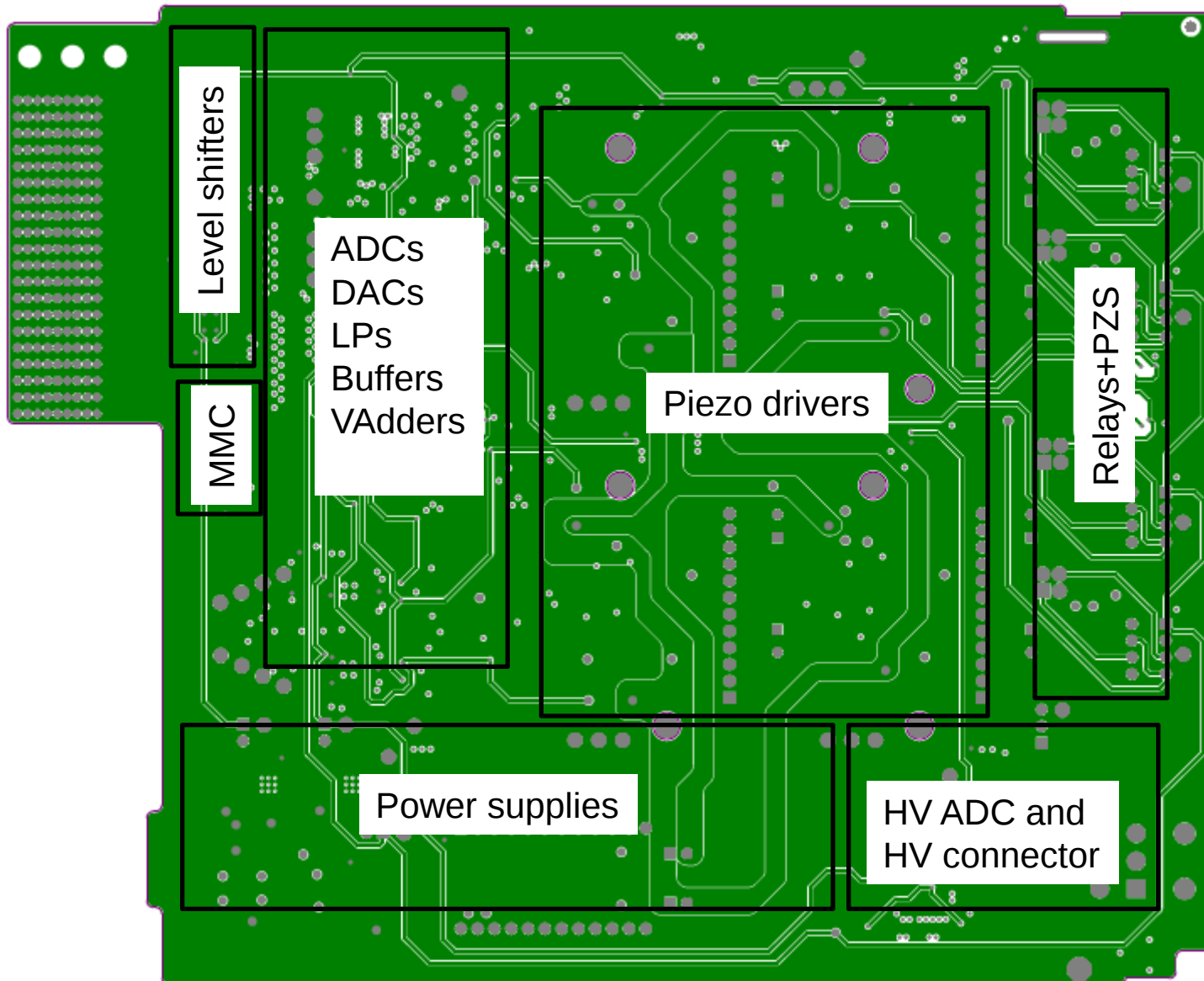


- The PCB board must be designed using 4 layerstack. The low voltage signals must be routed using outer layers. The high voltage signals as high voltage planes should be routed using inner layers and internal planes. The proposed material for PCB is FR-4 with standard cooper thickness of 35 mm and all pads covered with gold. Estimated minimum conductor width and spacing for piezo driver outputs are 0.3 and 0.2 mm respectively (100 V, 1.5 A). Maximum allowed PCB board thickness should not exceed 1.6 mm (4 layers with symmetric height of 0.48 mm should be sufficient) to fulfill maximum allowed height of the crucial components assembled on the PCB. Standard drilling of vias from top to bottom layer should be sufficient (no barred Vias needed).

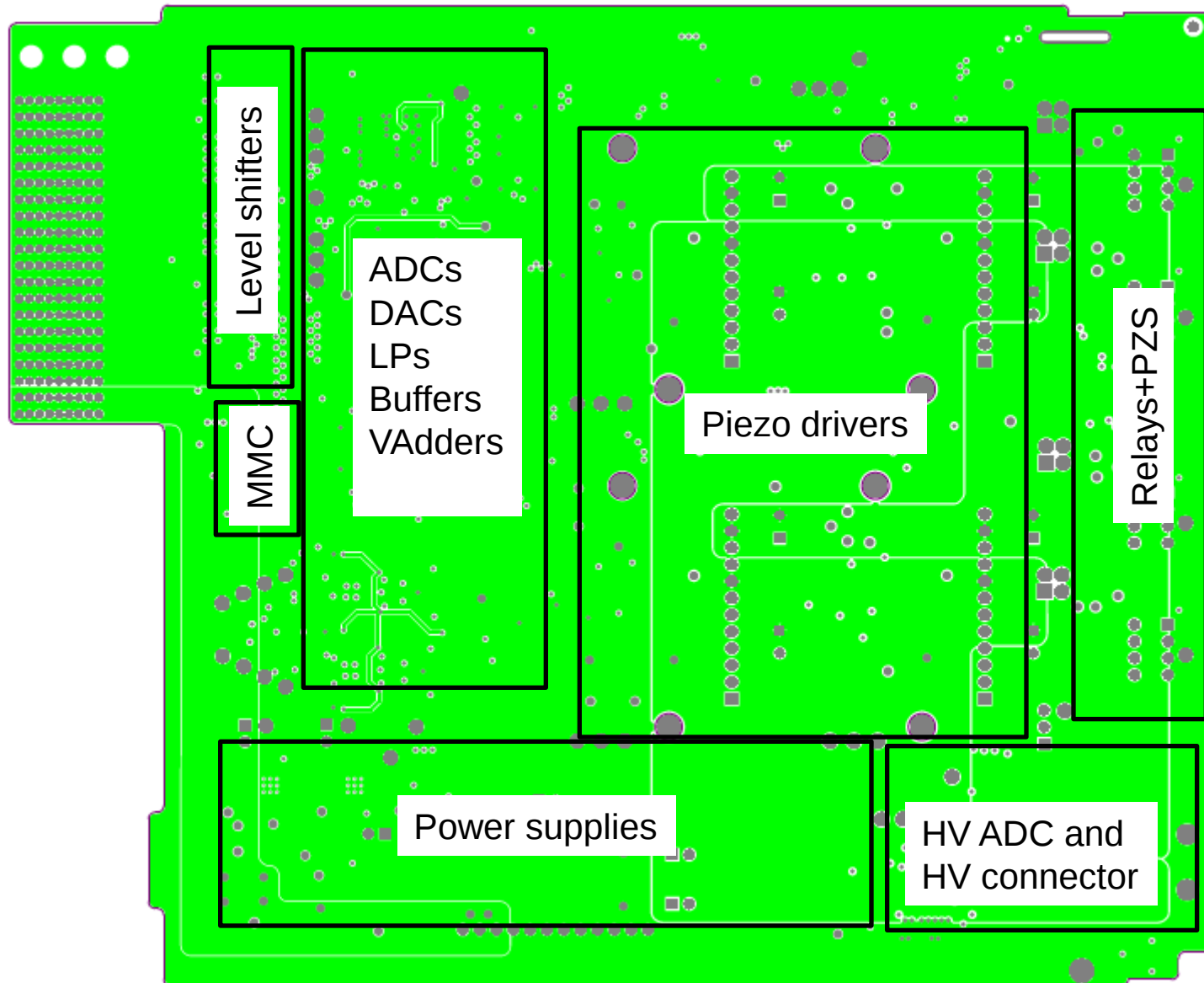
Bottom and Top Layers (digital and low voltage signals)



MidLayer1 Layer (+/-15V; high voltage PZD out)



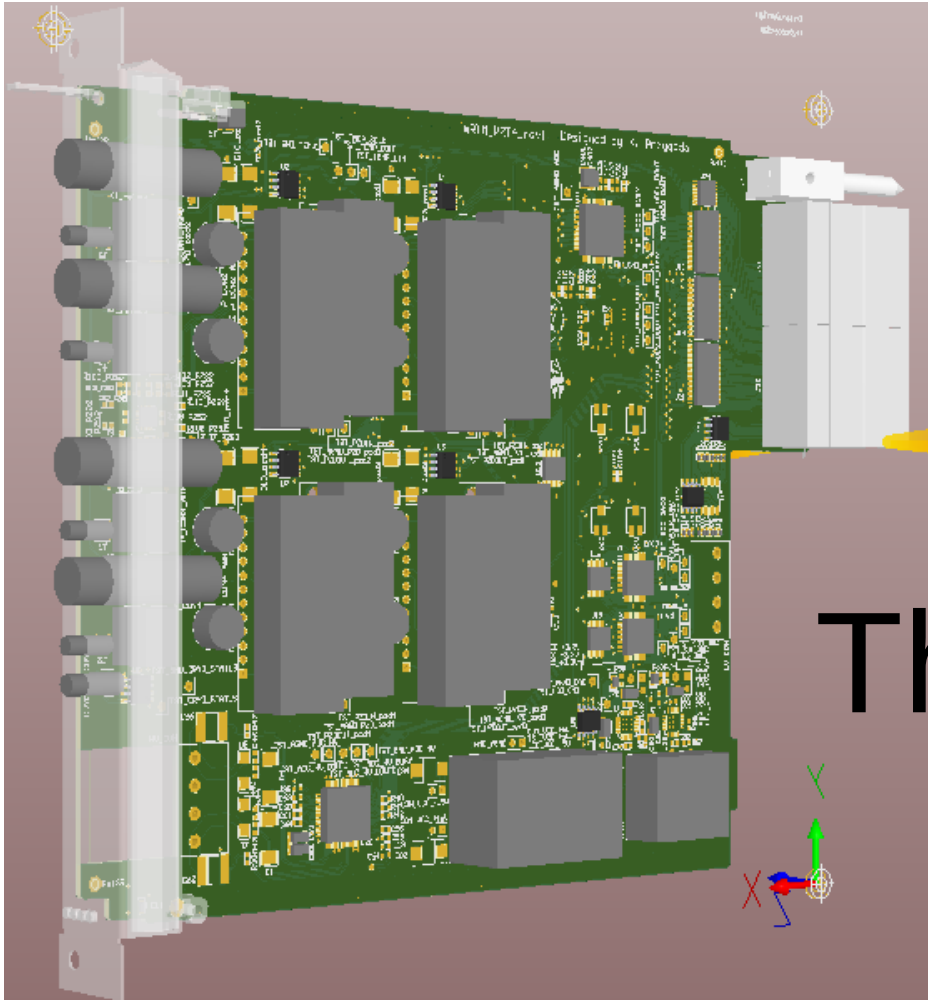
MidLayer2 Layer (HV power supply;12V)



Project status

- Initial electrical schematics finished
- Initial components placement finished
- Initial PCB routing finished
- Zone 3 pinout crosschecks according to last changes
- Crucial components life time estimation and ordering processes started
- Requirements collection for safety rules fulfilling i.e. using metallic cover, hv connection (lock connector??), internal power supply??
- Final PCB routing
- Gerber files generation and prototypes production





Thank You!

Possible latency

- > i.e. for 100 kHz closed loop bdw, we have delay = $\pi/4/2/\pi/100\text{kHz} \sim 1.25 \mu\text{s}$ delay (when assume of 45 degrees phase margin)
- > for 5 kHz closed loop bandwidth $\sim 25 \mu\text{s}$
- > DAC, ADC and FPGA data processing with $2 \mu\text{s}$ (500 kSPS), should give us more than 10 samples of allowed delay (1 sample IQ detection, 1 sample moving average, 1 sample PHASE calculation, 3 samples PI, 5 samples LP/NOTCH)
- > MGT serial link latency (125 MHz reference clock) up to 3 Gbs with SP6
- > ADCs clock at SIS (>81 MHz??)



Comments

- > Possibility for internal DC/DC converter 12=>+-100V (0.5A)
- > Piezo driver bdw <1V pp starting from 100 kHz
- > Spacing for metal housing
- > Output current estimation for <1V pp and capacitive load 1 μ F



Power consumption – single channel ($C_p \approx 1\mu\text{F}$)

Vcc [V]	Ivcc[mA]	frequency [Hz]	output voltage [V]
124	13	off	0
	38	300	~100
	57	500	~100
	104	1000	~100
	150	1500	~100
	193	2000	~100

frequency [kHz]	Output voltage [V]	temperature [°C]	Ivcc [mA]
10	1	21	20
10	2	21	33
10	5	21	68
10	10	23	127
10	15	28	185

