uTC
Board Status

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Agenda

- DAMC-TCK7 - next version of uTC
- Selected FPGA
- Costs Estimation
- Current Status
- Module Management Controller
- Next Step

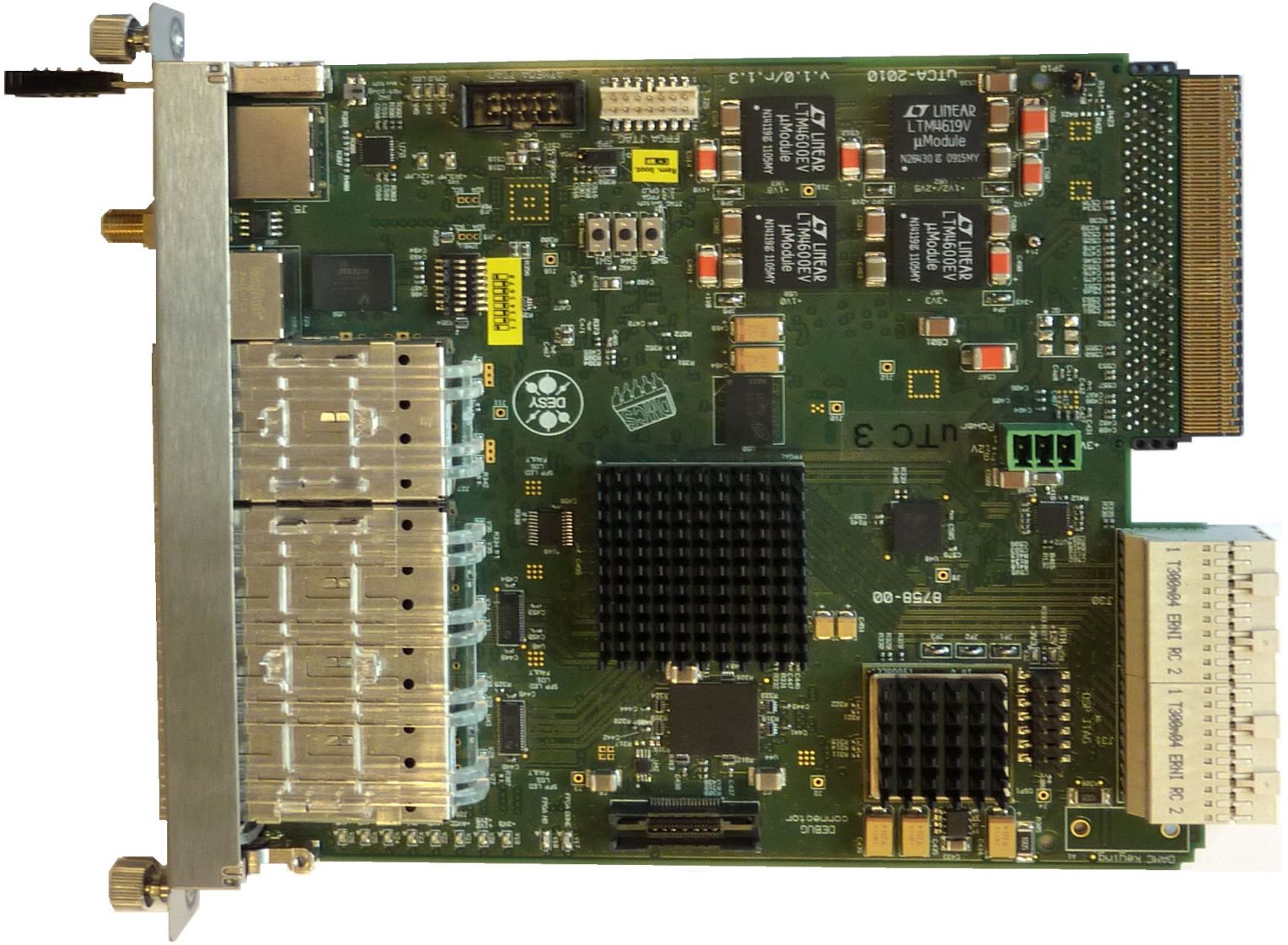
DAMC-TCK7 – Next Revision of uTC

DAMC-TCK7 (uTC rev.2.0) is a general purpose high-performance low-latency data processing unit designed according to the PICMG MTCA.4 spec.

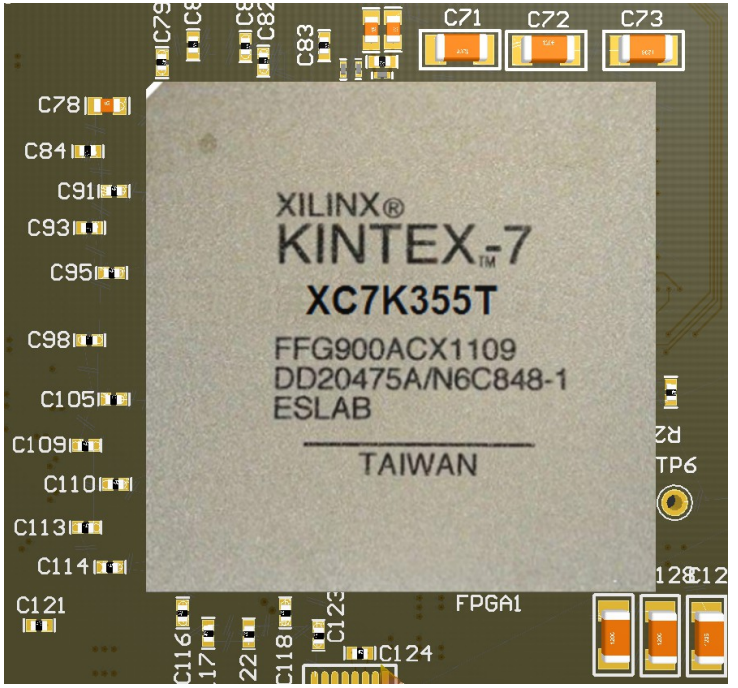
Application:

- **Low-latency Controller for LLRF Systems**
- **Digital Signal Concentrator Module for VETO 2D Camera System**
- Universal high-performance Data Processing Module:
  - High Energy Physics
  - Accelerators
  - Telecommunication
  - Image Processing
  - Medical Applications
  - Research & Development

uTC – Current Revision



FPGA Selection



- Kintex 7 **XC7K355T**-1FFG901C (LLRF)

  Slices: 55.650, DSP: 1.440, IOs/GTX: 300/24), HR pins (3V3), Price: ~1145 $ @ 50 pcs

- Kintex 7 **XC7K420T**-1FFG901C

  Slices: 65.000, DSP: 1.680, IOs/GTX: 380/28), HR pins (3V3), Price: ~1400 $

- Virtex 5 **XC5VSX95T**-1FFG1156C

  slices: 14.720, DSP: 640, IOs/GTX: 640/16), Price: ~2400 euro (Silica Germany)

- Virtex 6 **XC6VSX315T**-1FFG1156C

  slices: 50.000, DSP: 1.350, IOs/GTX: 600/20), Price: ~2000 euro (Silica Poland)

- Virtex 7 **XC7VX330T**-2FFG1157C

  slices: 51.000, DSP: 1.120, IOs/GTX: 600/20), Price: ~2900 euro (Silica Germany)

Cost Estimation

- FPGA: 1000 euro
- Other components: 700 euro
- PCB production: 1800 + n x 1000 euro
- PCB assembly: 250 + n x 450 euro

Total: 3355 euro (for n=10)

Total: 3191 euro (for n=50)

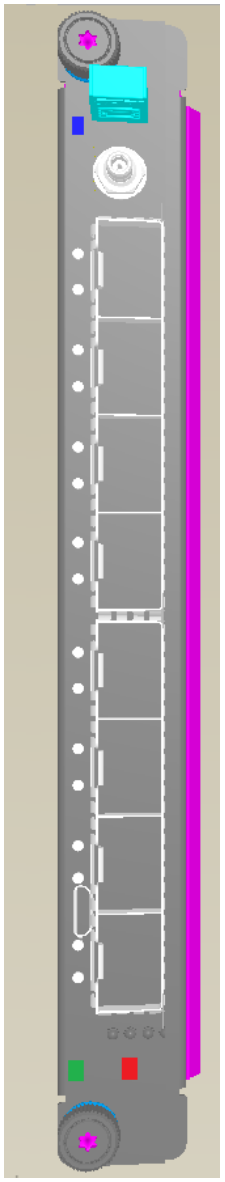
Current Status

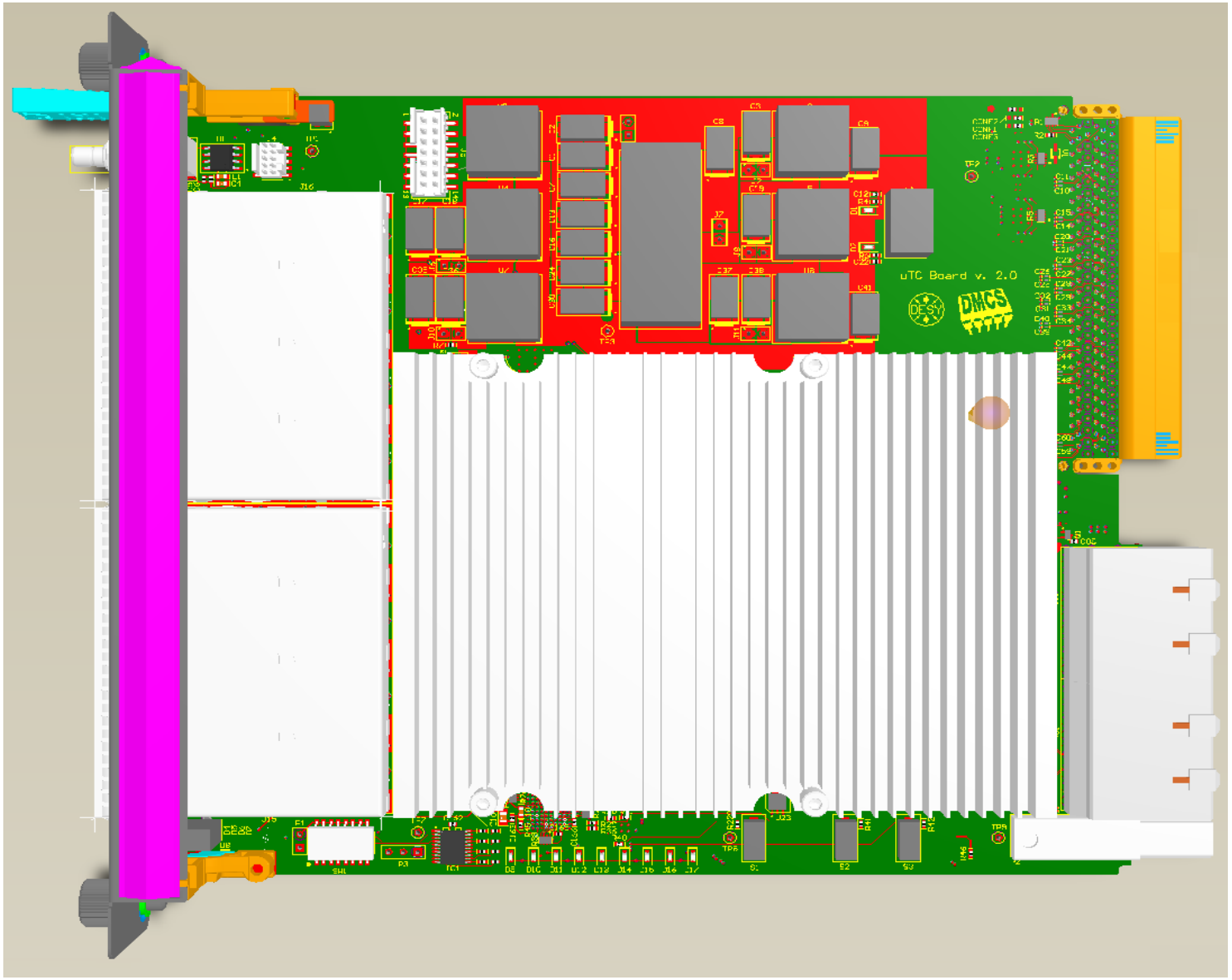
- Specification for DAMC-TCK7 available on 'N' drive
- Schematics were drawn and verified
- Placed and routed all components on PCB
- Some tests with Kintex 7 KC705 starterkit (high-speed links, PCIe, DRAM, etc.)
- Initial signal integrity simulations with Agilent ADS 2011.10
- Critical components are already collected (DDR3 memories, FPGAs, PLLs, etc.)
- Fabricated dummy PCB to verify components placement

Still not finished:

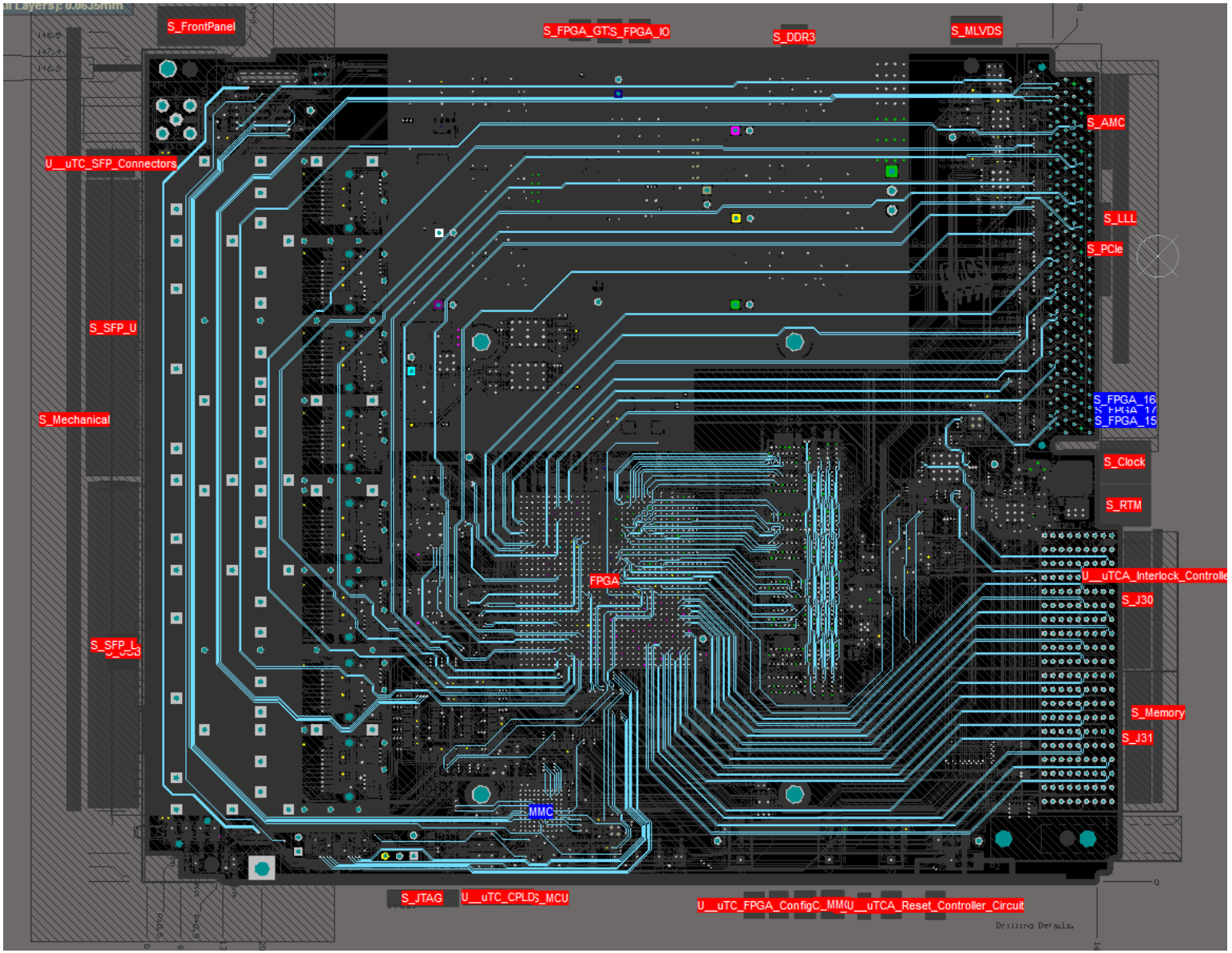
- Signal integrity - high-speed connections need to be tuned and finally simulated:
  - All GTX connections (PCIe, LLL, SFP+ and RTM)
    - Eye diagram
    - Crosstalk
  - DDR3 and Zone 3 – only tuning required
  - Careful analysis of clock lines (impedance, termination, clearance, etc.)
- Request missing components (resistors, capacitors, changed during design)

3D View of DAMC-TCK7 Board

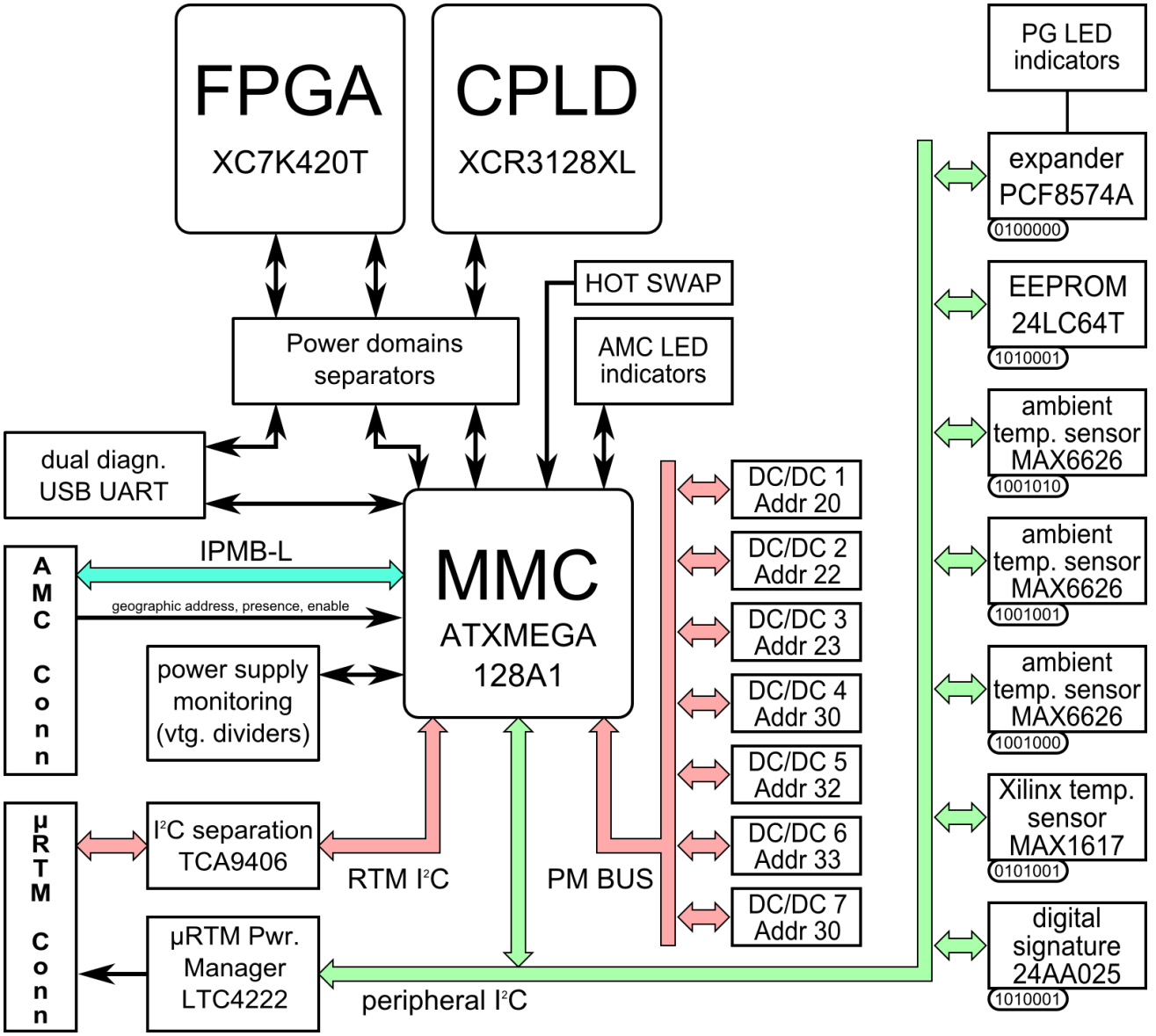




Layer 5 Routing – High Speed Connections



Module Management Controller



Next Steps...

- PCB production – the project should be ready for production within 2 weeks
  - Production with ILFA
- PCB assembly – we need to decide where the PCB will be assembled
  - Requirements for assembly?
  - Who will provide 'cheap' SMD components (resistors and capacitors)?
- Development of MMC
  - Code for ATXMega uC and CPLD
  - Drivers for all devices (DC/DC converters, sensors, RTM controller, etc.)
  - Zone 3 signals management (E-keying, Vref ?)
- Debugging of uTC submodules
- Testing submodules an GTX links
- ...

Summary

- Kintex 7 XC7K355T seems to be suitable FPGA for LLRF controller
- PCB design almost finished
- Started development of MMC firmware and learning Kintex 7
- Preparing PCB for assembly

SPARE SLIDES

Memory Topology

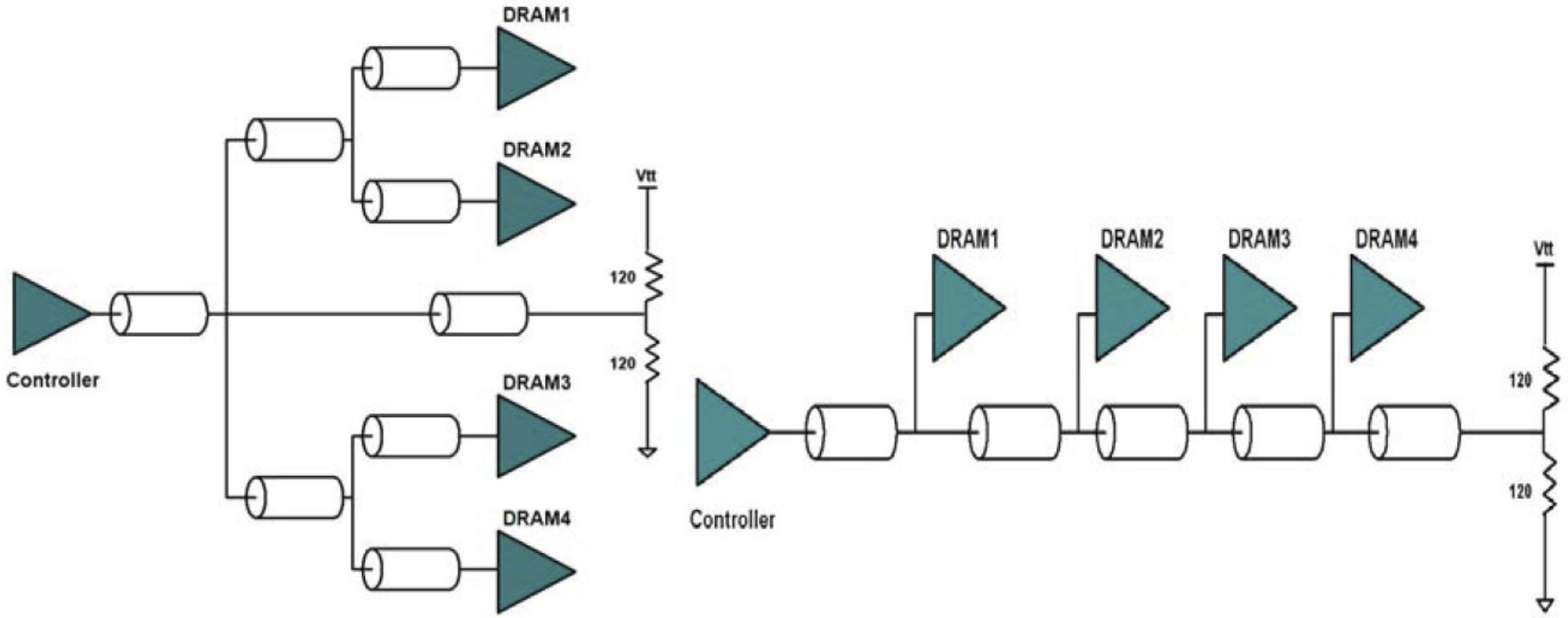
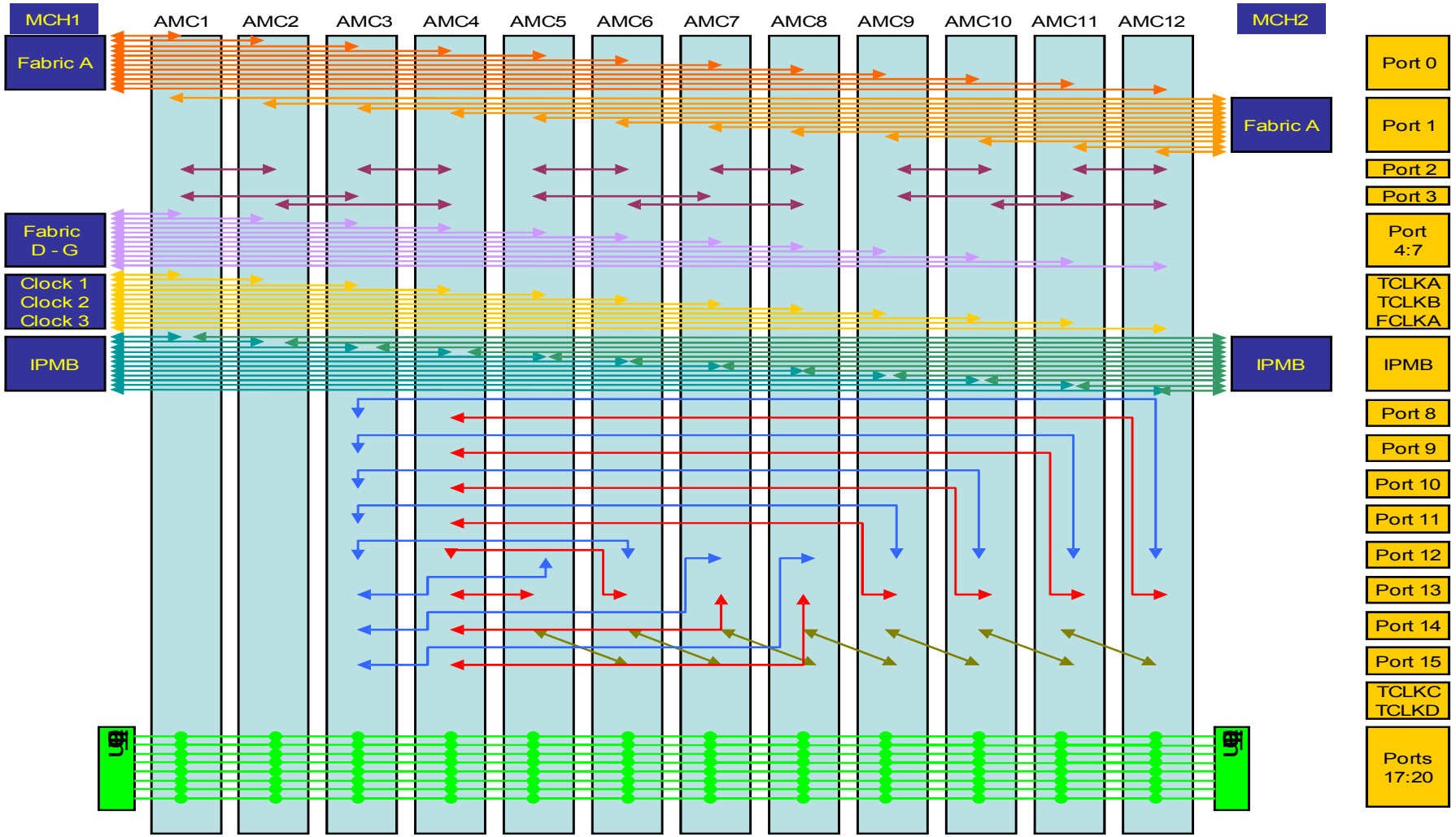


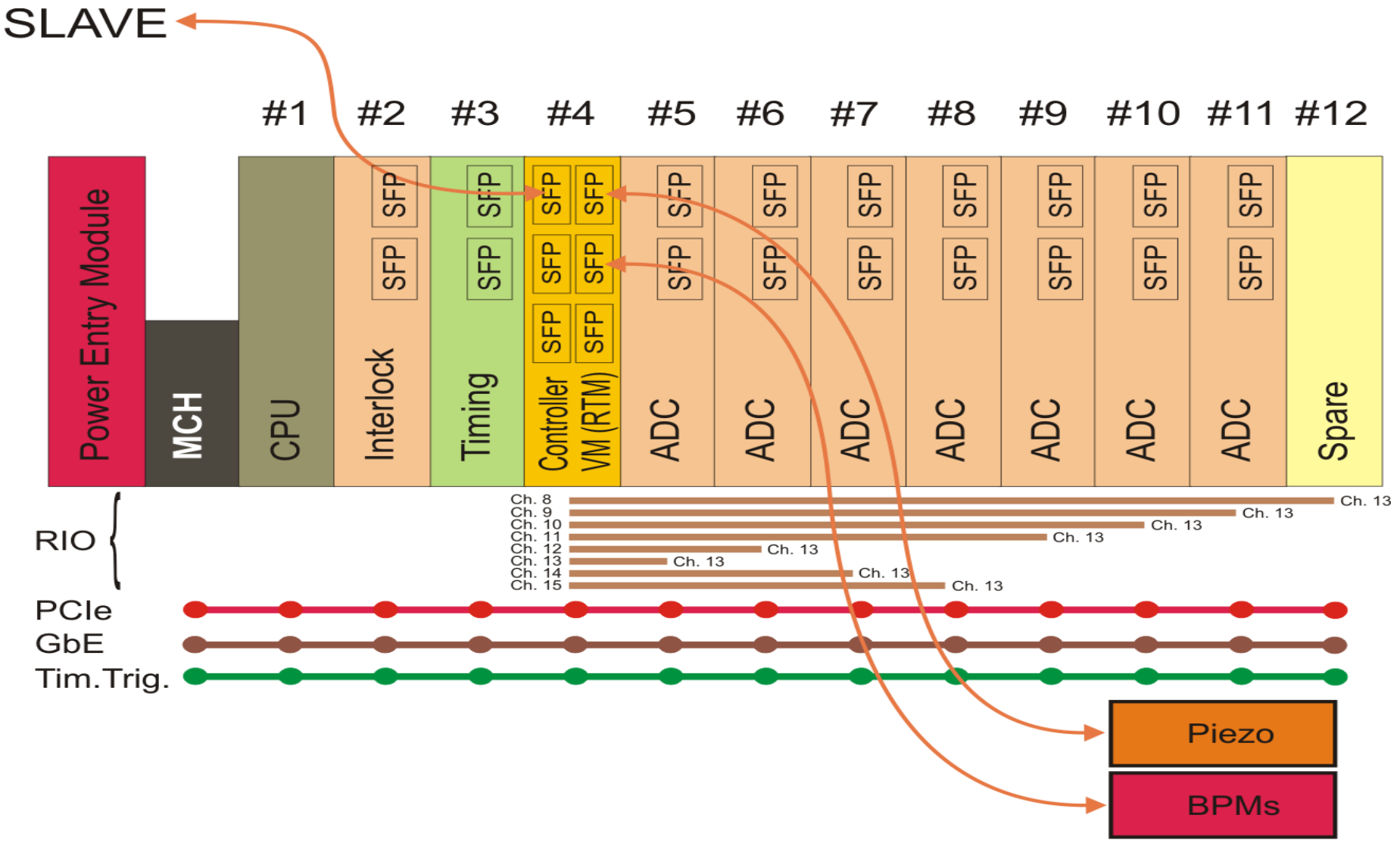
Figure 6: (a) DDR2 T-branch topology, (b) DDR3 fly-by topology

LLRF Backplane

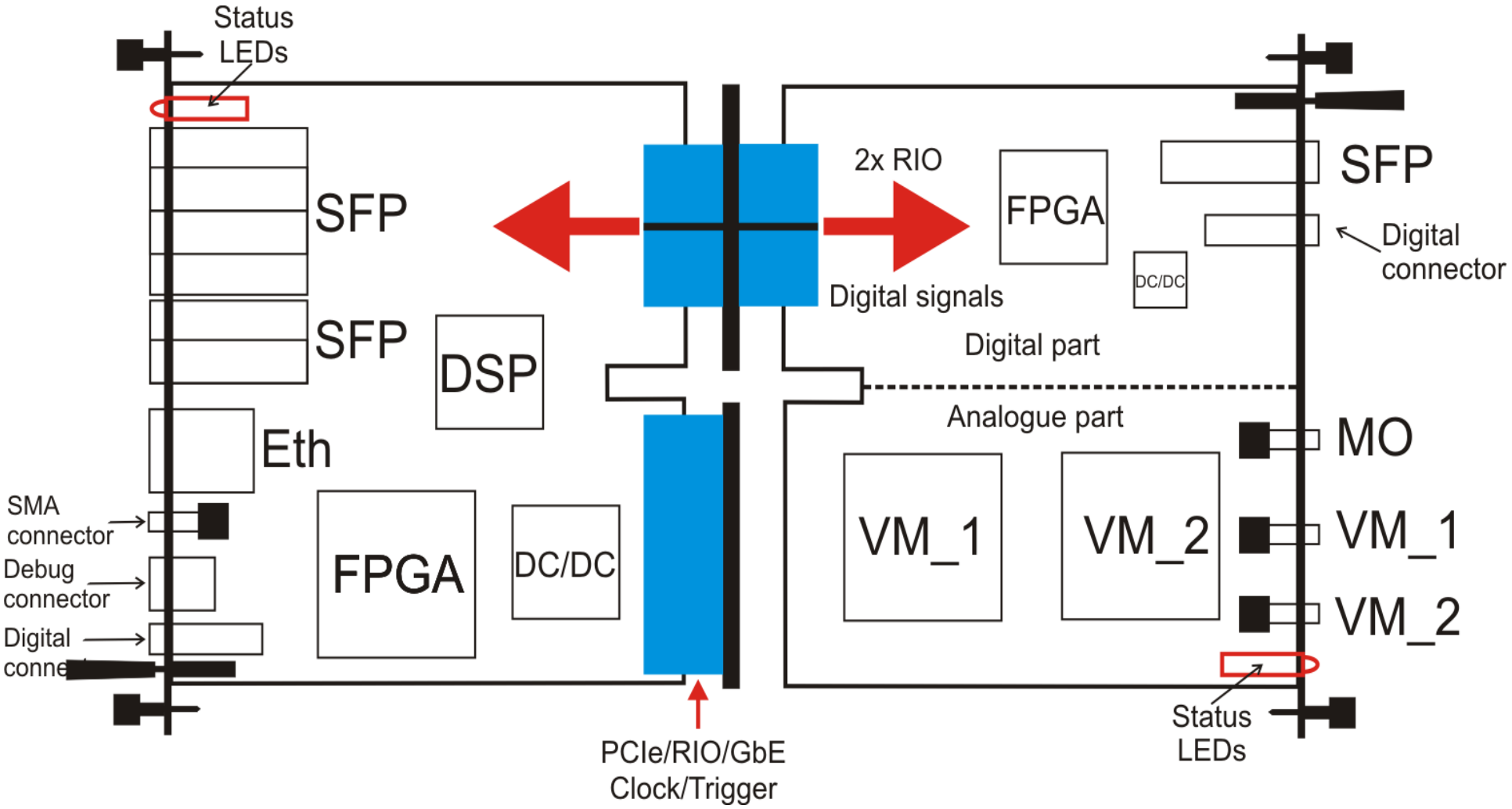
12-slots ELMA backplane



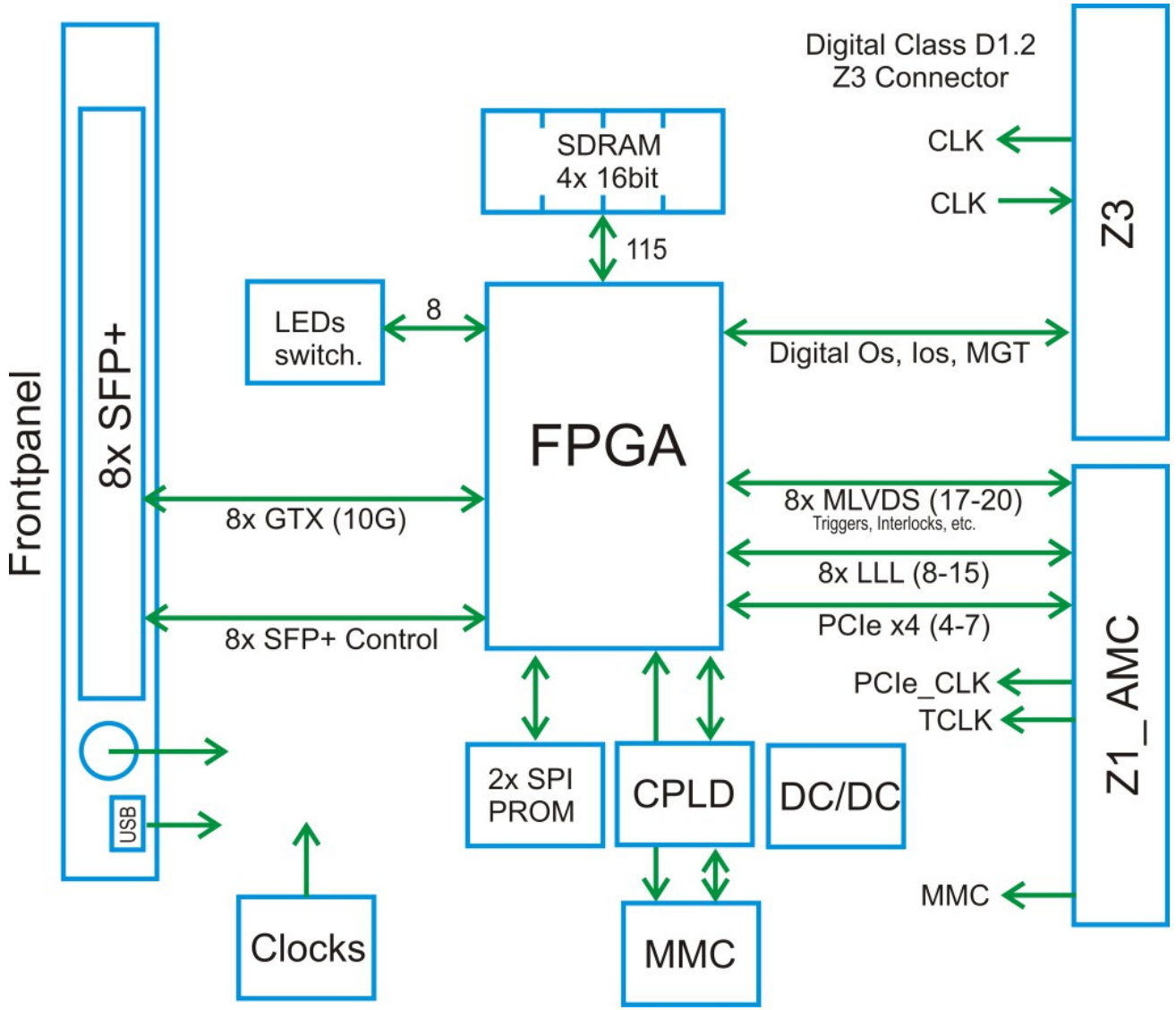
Interfaces in LLRF System



Idea of uTCA-based LLRF Controller



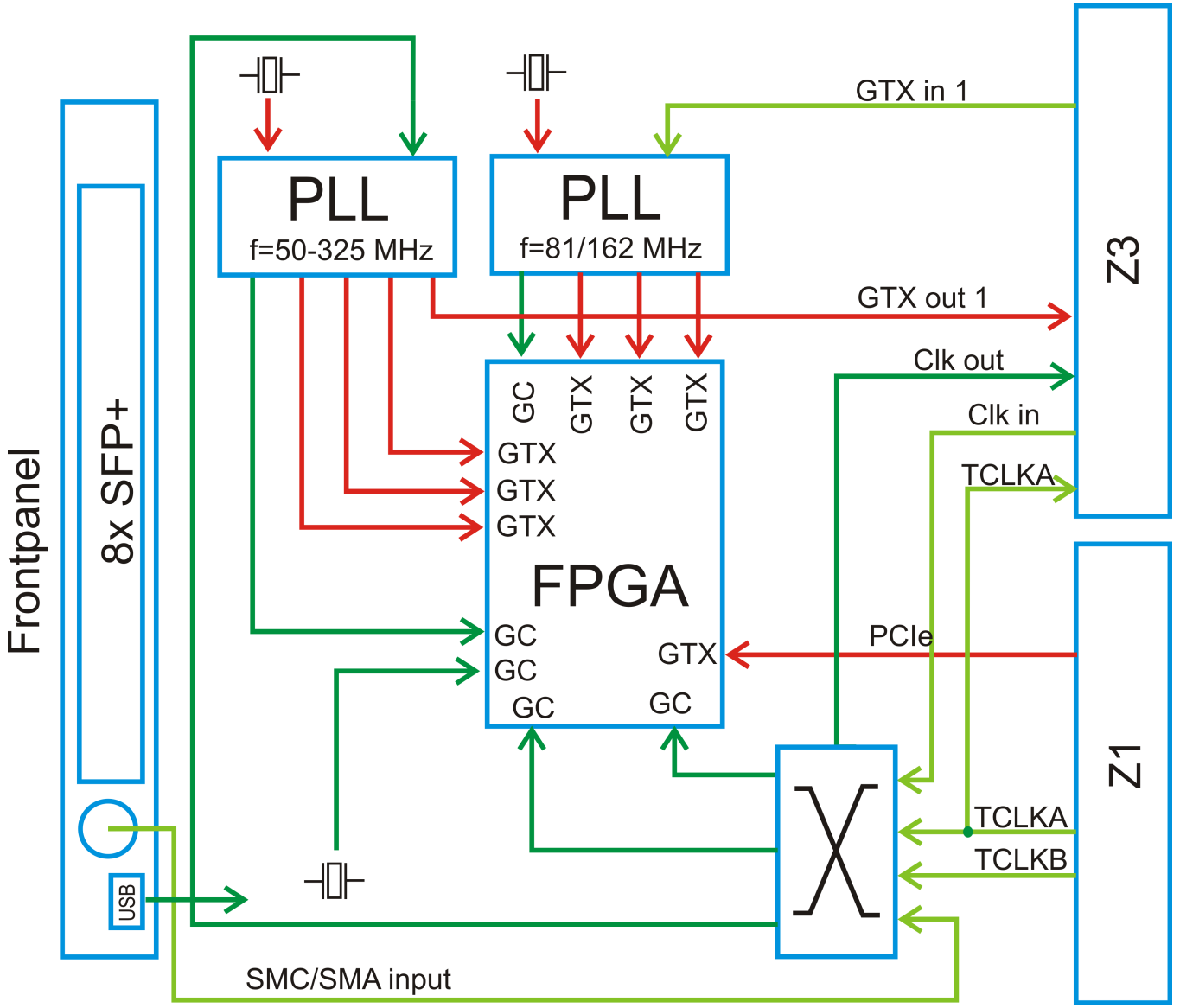
Block Diagram of DAMC-TCK7 Module



Clock Distribution on DAMC-TCK7

Provide clock for digital logic and GTX transceivers:

- PCIe (100 MHz)
- GbE (125 MHz)
- LLL (81.25/162.5 MHz)
- TCLK A/B
- Front panel - SMC connector
- RTM



Requirement for uTC – Memory

Estimated SDRAM DDR and SRAM QDR memory frequency for selected FPGAs

Device	Speed grade	DDR	QDR	Remarks
XC5VSX95T	-2	DDR2 = 300 MHz	QDR II = 300 MHz	Current uTC
XC6VSX315T	-2	DDR3 = 533.3 MHz	QDR II+ = 350 MHz	
XC7VX330T	-2	DDR3 = 800 MHz	QDR II+ = 500 MHz	
XC7K420T	-2/-3	DDR3 = 533.3 MHz	QDR II+ = 500 MHz	

Requirements for memory:

- Same memory configuration as on the SIS8300L
  - 4 chips in parallel (4x 16 bits data bus, common addresses, control signals)
- Question of chip availability is crucial