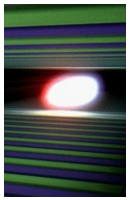
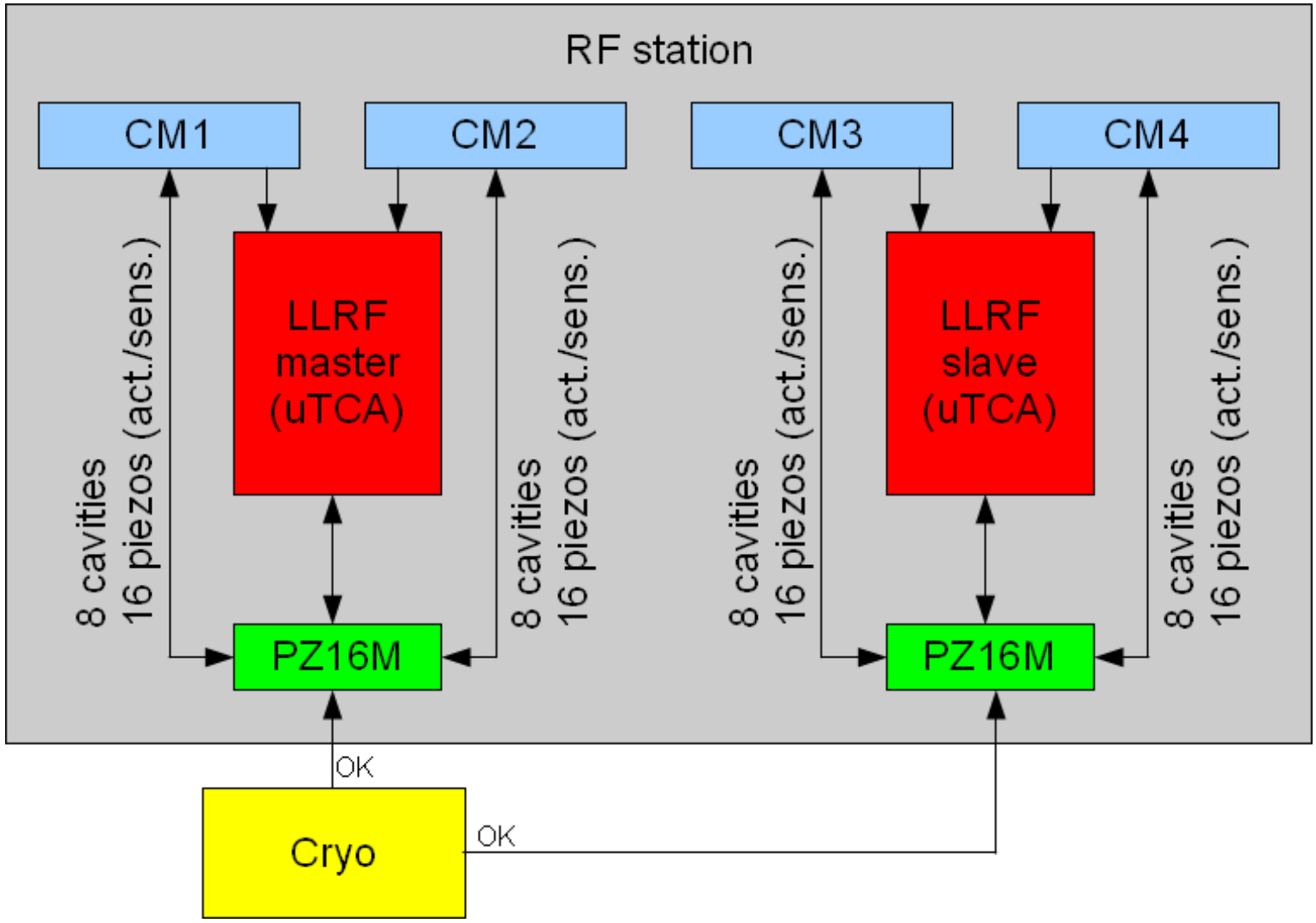


PZ16M – Status

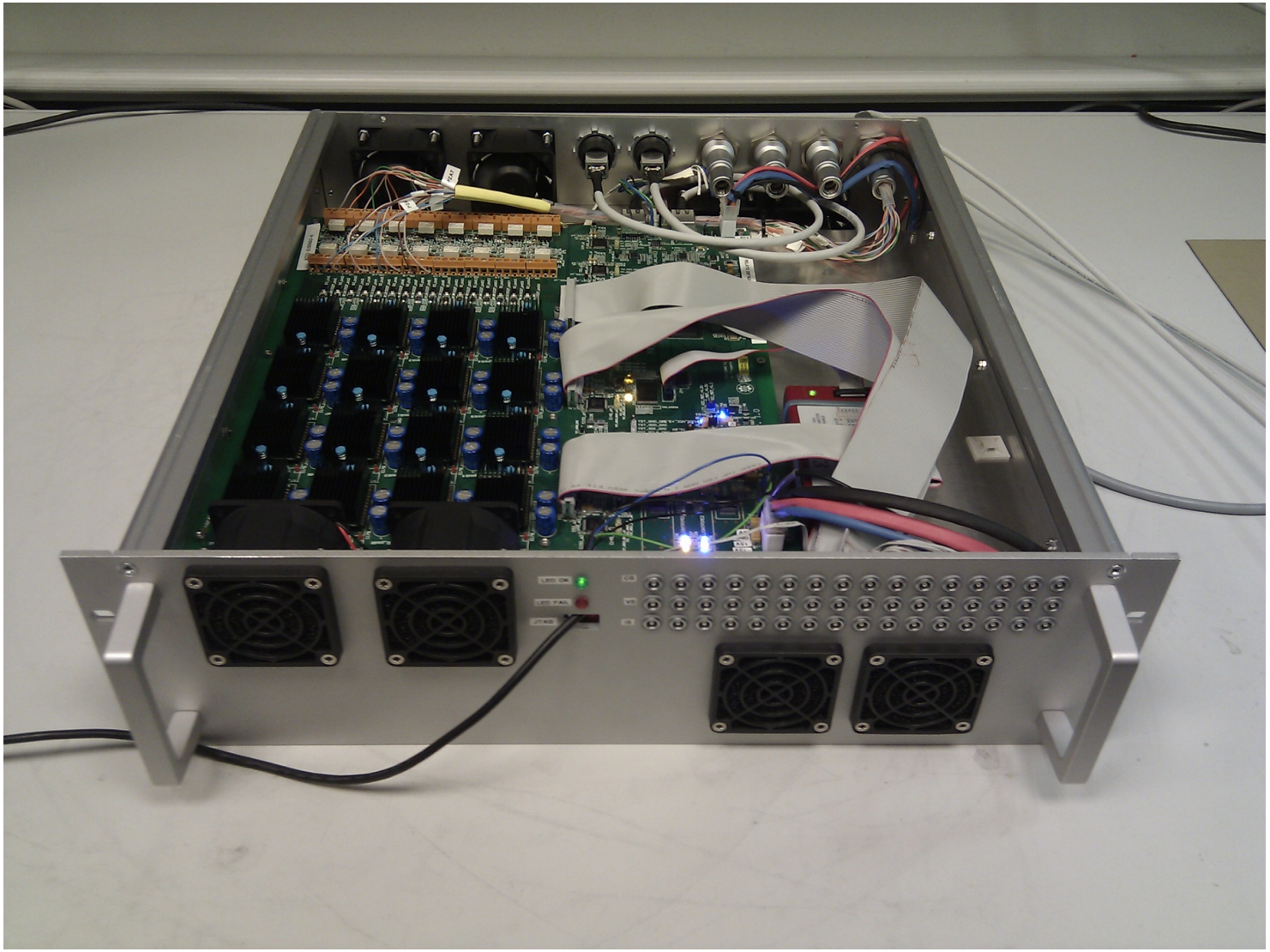
M.Grecki

17.12.2012 DESY

Architecture of the PCS for single RF station



Built prototype



Order status

- got offer from I-Tech for 10 pieces (3 - AMTF, 4 - FLASH, 3 – XFEL)
  - target price for series production close to estimation
  - DESY order prepared and sent for management acceptance
  - delivery time 6 months
- for mass production we have to prepare CFT (other companies needed)
  - ELKOMTECH and DMTEL contacted and NDA signed

Über - V 3 - an - V 4 -

Anlage 1 zur Bestell-Anforderung Nr.:

(erforderlich für Aufträge ab 3.000 EUR Anschaffungswert !)

1. Projektbezeichnung:	2. Bei Bauleistungen geschätzter Wert:
High frequency control system for FLASH and XFEL (PZ16M - Piezo Control System)	57 800€

3. Einzelaufgabe:
Production of PZ16M (Piezo Control System) for the LLRF uTCA System

4. Begründung für den Bedarf bzw. Verwendungszweck/Messproblem:
The PZ16M is a complete piezo control system consisting of piezo driving and piezo signal measurement unit together with monitoring and control circuitry. It is able to control and measure signals from 16 cavities simultaneously (32 piezos) with remotely configurable actuator/sensor piezo functions.
It provides 16b signal processing resolution both for driving and measurements. It is also equipped with piezo safety functions (overvoltage and overcurrent protection, current slew-rate limitation and cryo-interlock). The operating conditions are monitored by integrated temperature and voltage sensors.

5. Voraussichtliche Verwendungsdauer (nur für Elektronik): von 06/2013 bis Ende FLASH, XFEL

6. Leistungsbeschreibungen/eindeutige technische Spezifikation (als Grundlage zur Angebotseinholung):

6.1. General Electrical and Mechanical Specifications

Operation type	synchronous, triggered by trigger signal, disabled by interlock signal
Maximum repetition rate	25Hz
Trigger resolution	<1us
Channel number	16
Power supply	230V, 750W
Power dissipation	<150W with maximum excitation at all channels for 10Hz operation, <400W for 25Hz operation
Dimensions	19 inch, 3U
Control interface	bi-directional fibre link, at least 100Mb/s

6.2. Driver Output Parameters

Output load	Rload: capacitive, 2 ÷ 6uF
Output voltage range	-70V ÷ +70V
Output bandwidth (3dB) bandwidth is DC ÷ 3kHz	B: DC ÷ 300Hz (with maximum amplitude and load), for 10% of maximum amplitude the output
Noise level	<23mV rms (corresponds to 0.1Hz) SNR<-74dB
Channel crosstalk	XT<-60dB between any channels
Overvoltage protection	Umin=-85V and Umax =85V (clamping level)
Overcurrent protection	Imax<1.5A
Current slewrate protection	<50A/ms
Monitoring outputs	voltage type, signal range -2.5 ÷ +2.5V, for current monitoring output 1V must correspond to 1A

6.3. Sensor Input Parameters

Input impedance	Zin=4kOhm
Input voltage range	-2.5 ÷ +2.5V
Input bandwidth (3dB)	B: DC ÷ 1kHz
Noise level	SNR<-70dB
Sampling frequency	>3kHz (better 10kHz)
Channel crosstalk	XT<-60dB

6.4. Special features

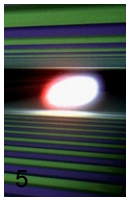
Piezo functionality switching between actuator and sensor	remotely switchable
Electromagnetic interference to the LLRF controller	<-90dBm (maximum 7mV of effective voltage induced)
Firmware downloading	locally (from EPROM) and remotely through serial link, maximum booting time 10s, at least 2 revisions of firmware must be available in ROM memory
Serial number of the board	the board must be identified by unique serial number readable remotely
Safety	the housing must be grounded to the safety ground.
Cooling	by airflow. Flow direction from front to back side.

6.5. Parameters Monitoring

Temperature monitoring	5 channels, resolution 0.5 deg.
High voltage monitoring	negative and positive supply voltage, DC and transients

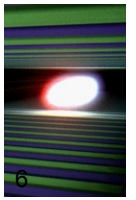
6.6. Delivery

Set of basic tests to be performed by the manufacturer

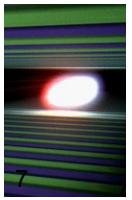


Power supplies (including high voltage)	level control, fluctuations, ripple (only checkout whether acceptable or not)
Control circuitry functionality	JTAG chain visibility, ROM and FPGA programming
Status diodes	checkout of the correctness of state monitoring
Communication link	checkout of the transmission in both directions
Internal logic tests	control circuitry and monitoring signals (voltages, temperatures, etc.) availability
DAC tests	signal generation (signal presence at monitoring outputs, relevance, for various conditions to check the whole signal range, presence of all codes etc.)
Piezo drivers tests	signal generation (signal presence at main and monitoring outputs, for various conditions to check the whole signal range, focus on stable driver operation over the full range of output voltage and load)
Protection tests	overvoltage and overcurrent, current slope limitation
ADC tests	acquisition of the test signal (signal presence, relevance, for various conditions to check the whole signal range, presence of all codes etc.)
Communication link error transmission	(pulling out fibre from socket – BE CAREFUL!! DO NOT LOOK AT THE FIBRE, sending wrong data) – to check the transmission error handling
Interlock test	activating/deactivating the interlock signal and checking results
Isolation tests	checkout of the isolation between the high voltage circuits and module case and other parts available to users

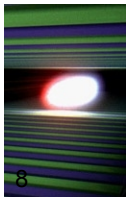
Set of performance tests to be performed by end user (DESY)



Communication link	BER measurements (<1E-9)
Characterization of high voltage power supply	voltage levels, ripple, stability under various operating conditions
DAC tests	signal generation (measurements of the noise level, linearity)
Characterization of driver characteristics	output voltage and current range, linearity, bandwidth
Power dissipation tests	temperature measurements with maximum load (test should least at least one hour after the temperature stabilizes)
Piezo driver crosstalk tests (channel to channel)	for various condition (with maximum output signal level and load)
ADC tests	signal acquisition (measurements of the noise level, linearity)
ADC crosstalk tests (channel to channel)	for various condition (with maximum input signal level)
Piezo Driver/ADC crosstalk tests	(from driver channel to ADC channel) for various condition (with maximum output signal level and load)

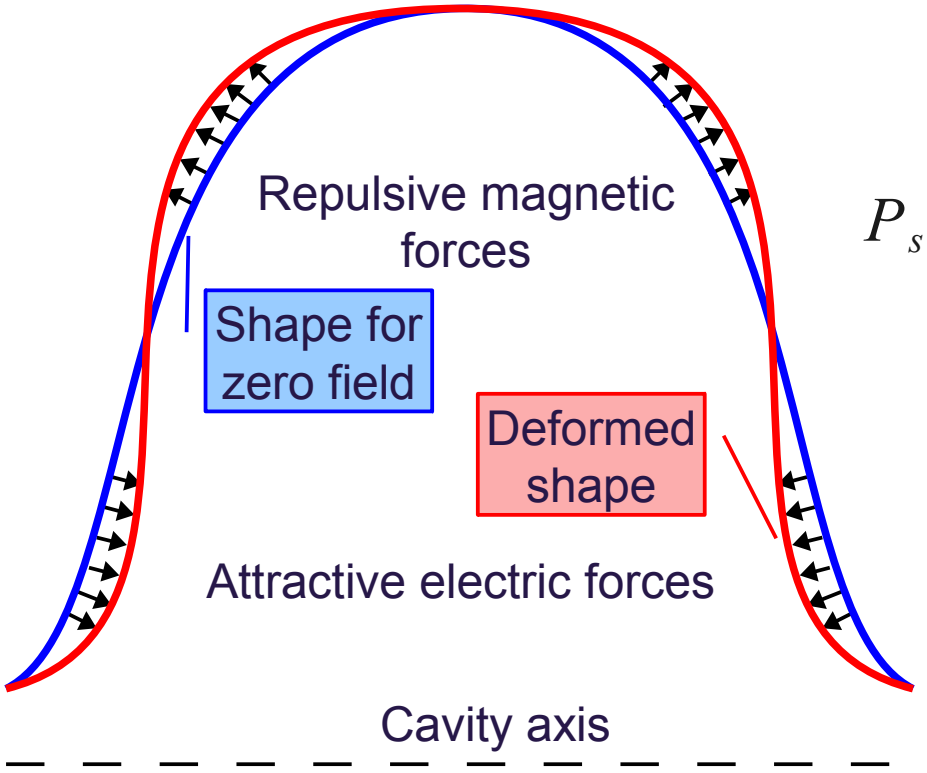


Thank you for your attention



Backup slides

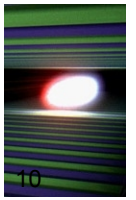
Lorentz Force Detuning (1)

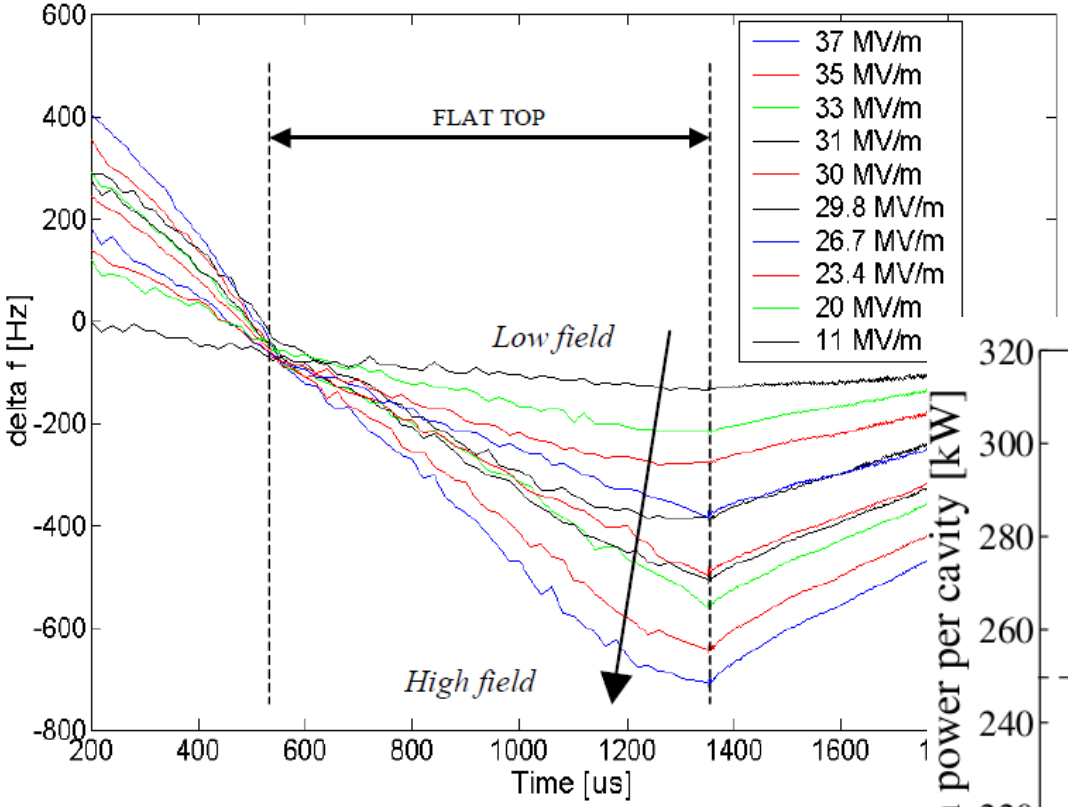


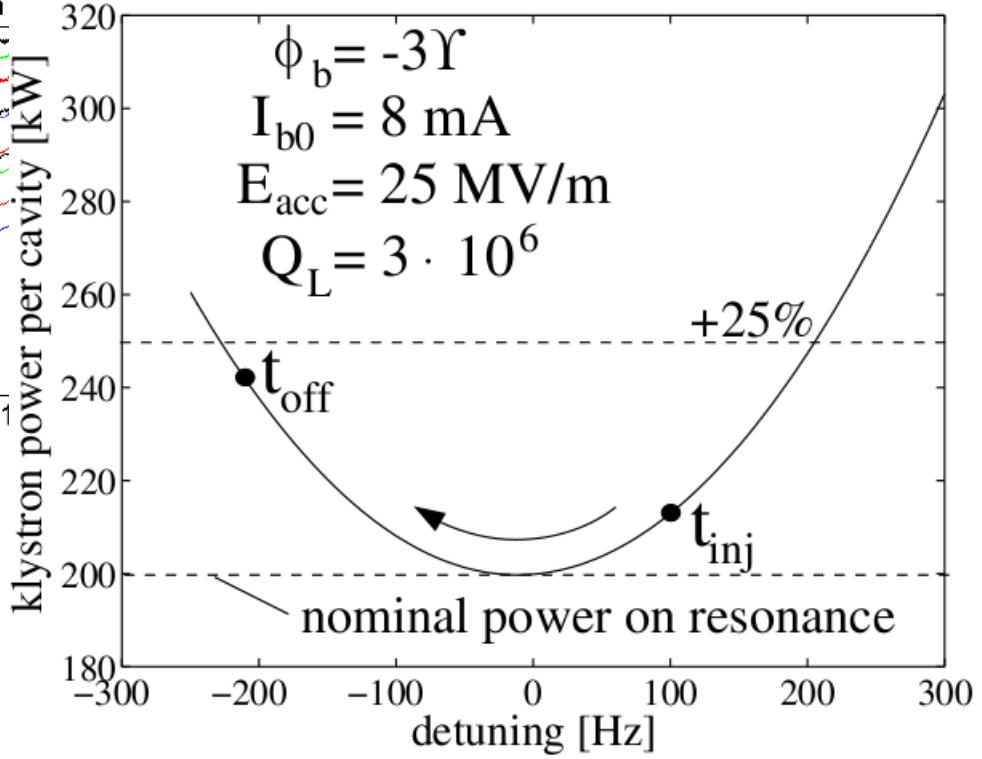
$$P_s = \frac{1}{4}\left(\mu |\vec{H}|^2 - \varepsilon_0 |\vec{E}|^2\right)$$

$$\Delta f_0 = (f_0)_2 - (f_0)_1 = -K E_{acc}^2$$

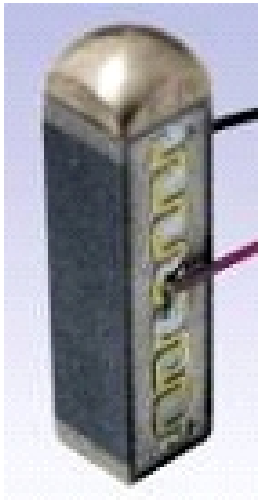
Lorentz Force Detuning (2)





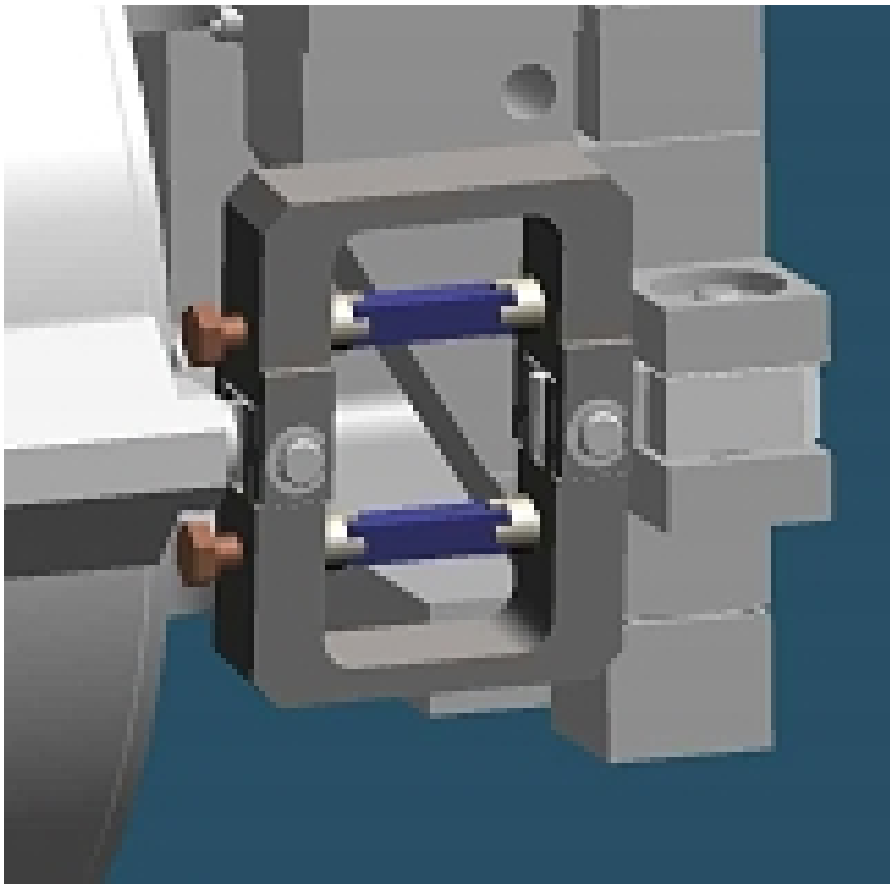


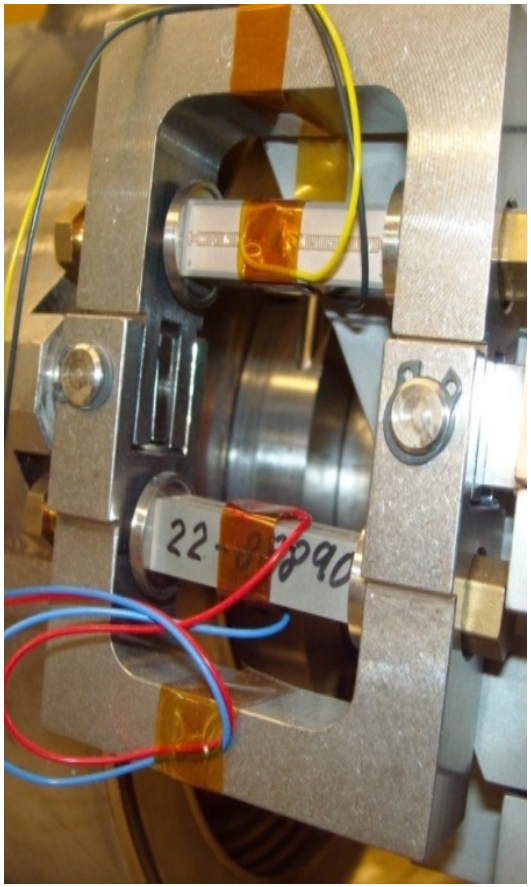
Piezo Tunerc



Manufacturer: **PI**
Dimensions: **10x10x36mm**

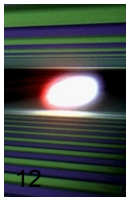
Manufacturer: **NOLIAC**
Dimensions: **10x10x30mm**





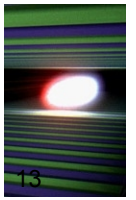
Piezos mounted in the cavity fixture

General parameters



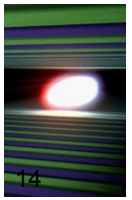
Operation type	synchronous, triggered by trigger signal, disabled by interlock signal
Maximum repetition rate	25Hz
Trigger resolution	<1μs
Channel number	16
Power supply	230V, 750W
Power dissipation	<150W with maximum excitation at all channels for 10Hz operation, <400W for 25Hz operation
Dimensions	19 inch, 3U
Control interface	bi-directional fibre link, at least 100Mb/s

Driver output parameters



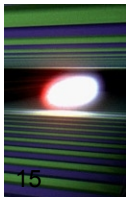
Output load	R_{load}: capacitive, 2 ÷ 6μF
Output voltage range	-70V ÷ +70V
Output bandwidth (3dB)	B: DC ÷ 300Hz (with maximum amplitude and load), for 10% of maximum amplitude the output bandwidth is DC ÷ 3kHz
Noise level	<23mV rms (corresponds to 0.1Hz) SNR<-74dB
Channel crosstalk	XT<-60dB between any channels
Overvoltage protection	U_{min}=-85V and U_{max} =85V (clamping level)
Overcurrent protection	I_{max}<1.5A
Current slewrate protection	<50A/ms
Monitoring outputs	voltage type, signal range -2.5 ÷ +2.5V, for current monitoring output 1V must correspond to 1A

Sensor input parameters



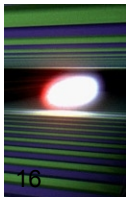
Input impedance	$Z_{in} \geq 4k\Omega$
Input voltage range	-2.5 ÷ +2.5V
Input bandwidth (3dB)	B: DC ÷ 1kHz
Noise level	SNR<-70dB
Sampling frequency	>3kHz (better 10kHz)
Channel crosstalk	XT<-60dB

Special features



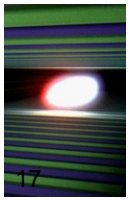
Piezo functionality switching between actuator and sensor	remotely switchable
Electromagnetic interference to the LLRF controller	<-90dBm (maximum 7μV of effective voltage induced)
Firmware downloading	locally (from EPROM) and remotely through serial link, maximum booting time 10s, at least 2 revisions of firmware must be available in ROM memory
Serial number of the board	the board must be identified by unique serial number readable remotely
Safety	the housing must be grounded to the safety ground. The board must be certified by D5 fulfilling requirements for the devices installed in accelerator control
Cooling	by airflow. Flow direction from front to back side. Depending on the power dissipation, may require forced airflow driven by fans. The cooling efficiency must be sufficient to keep the components temperature in the working region.

Overvoltage and overcurrent protection



- The overvoltage protection
  - output voltage level of the piezo driver is clamped to the supply voltage levels by clamping diodes (±85V)
  - piezo voltage is limited by a discharge/overvoltage protection plug-in installed as close to the piezo as possible (at the patch-panel at the cryomodule). The plug is clamping the piezo voltage at the level of 120V by a Zener diode
  - cable between piezo control system and piezos should be a twisted-pair type in order to minimize the possibility of voltage induction from external electromagnetic fields.
- The overcurrent protection is realized by internal current limitation of the piezo driver integrated circuit (PB-51 from Cirrus Logic). The maximum current limit is set to 1.5A.

Connectors



Cavity C1...C16 - Piezo A	16 channels, Lemo Multipin connectors, location on the rear panel must agree with cable ducts
Cavity C1...C16 - Piezo B	16 channels, Lemo Multipin connectors, location on the rear panel must agree with cable ducts
Power supply connector	AC 230V, 10A, equipped with fuse 5A, EMI filter, line switch (for stand-by mode operation – fans only)

Communication link to the LLRF controller	SFP fibre, bidirectional transmission, single channel
Power switch	AC 230V, 10A
Status diodes	the following LEDs must be present on the front panel: •all functions OK (green) •not OK (red) •transmission (blue) •HV present (yellow)

JTAG connector for FPGA chain	The FPGA chain should consist of FPGA and its configuration EPPROM
Test pins for monitoring signals	To connect scope probe