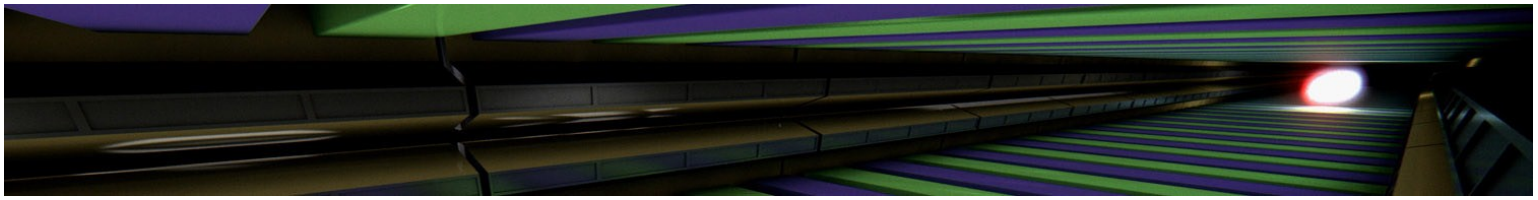


Recent software development for Optical Synchronization

(including Server for Laser synchronization based on down-conversion)

Tomasz Kozak

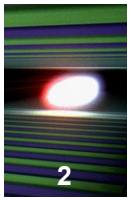
DMCS, TUL

Advanced Techniques in LLRF control for XFEL - Collaboration Workshop

Otwock-Świerk, 19-21 February 2013

European XFEL

Agenda



- Small introduction
- Software for Link Stabilization Units
- Software for VME DAC board
- Software for SIS8300+DwC Locking Scheme
- Future projects

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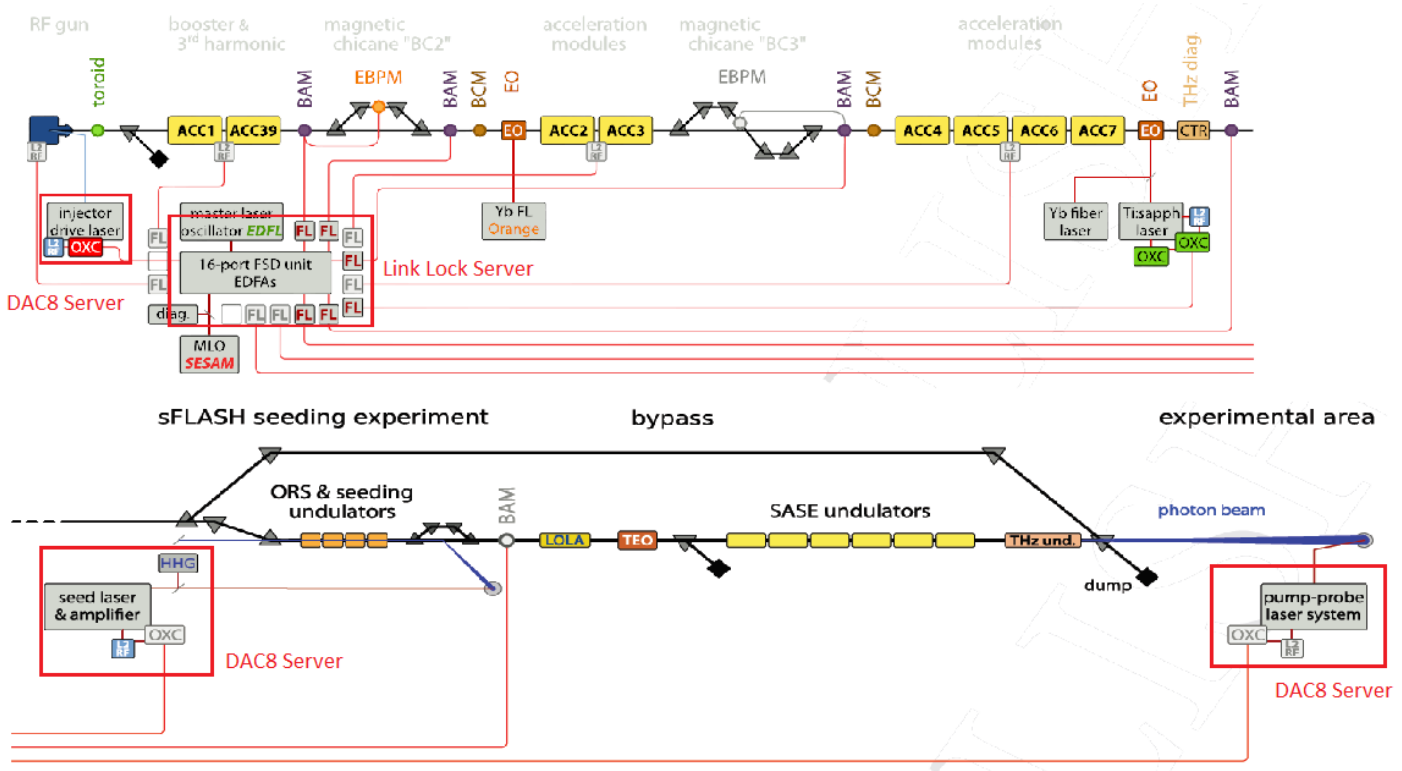
Short introduction – Where software is needed?

FLASH facility



Courtesy: S.Schulz

Additionally 26A Laboratory:

- used as Test Station for new development
- Two test links available
- Setup with VME DAC board

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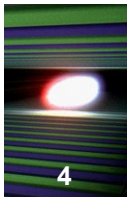
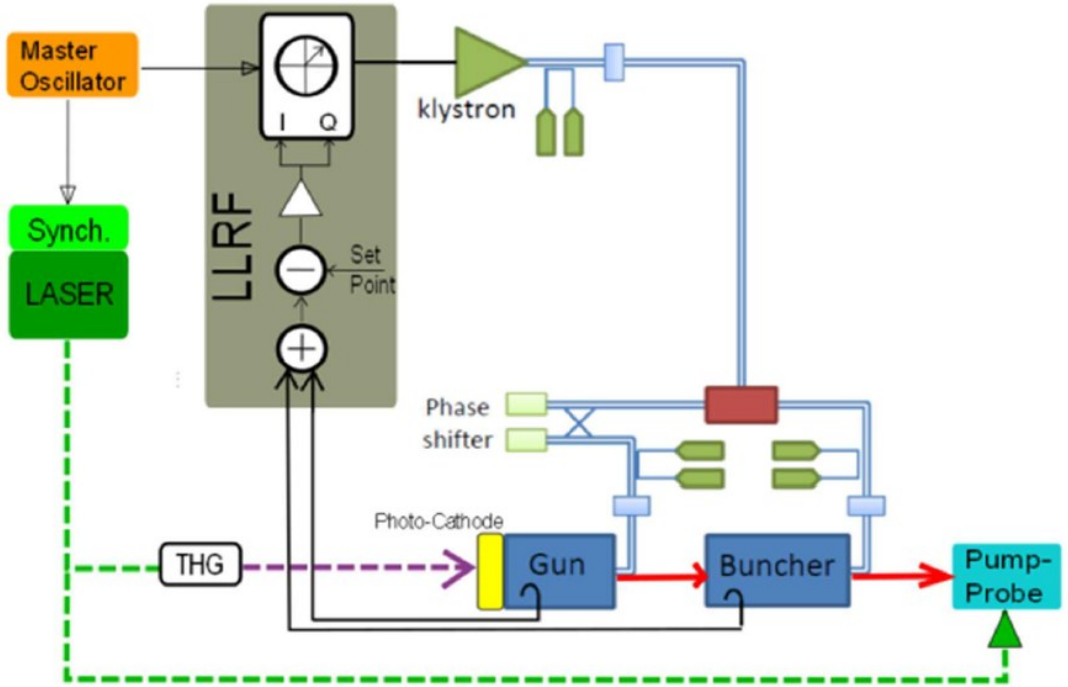
Short introduction – Where software is needed?



REGAE facility



Courtesy: M. Felber

REGAE synchronization highlights:

- 83MHz Ti:Sapphire Laser user as a PIL and Pump-Prope Laser (later)
- New Phase Detection at Intermediate Frequency Synchronization Scheme for RF-to-Laser Synchronization

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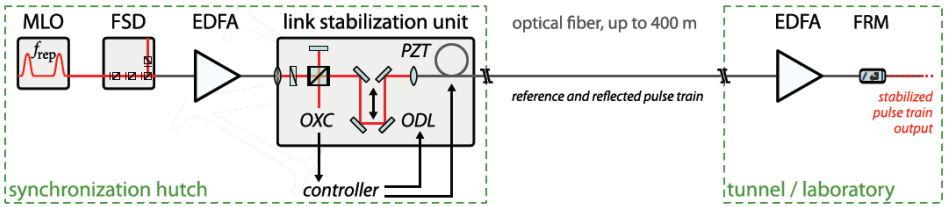
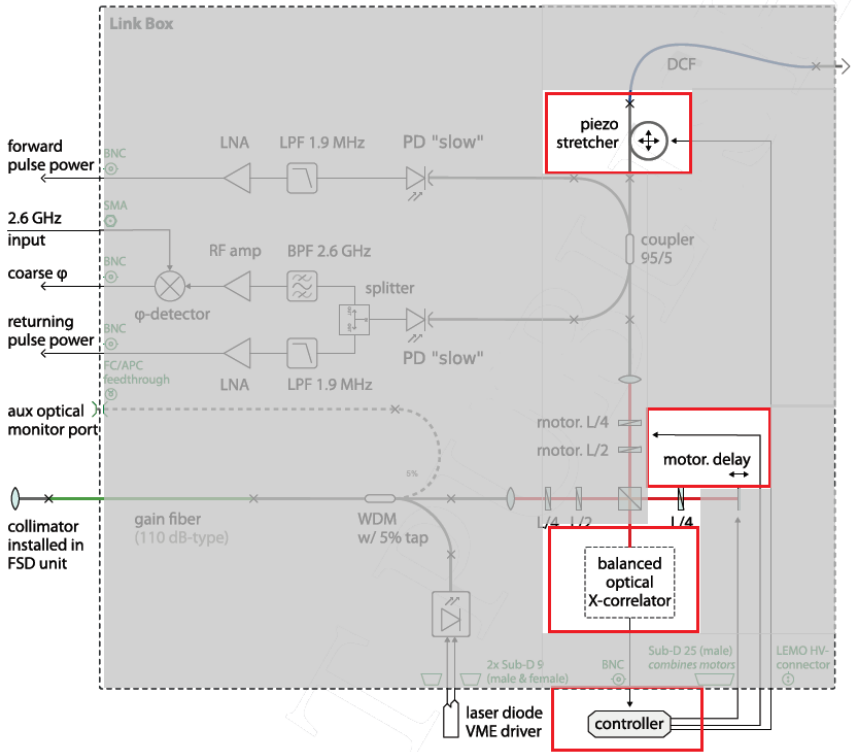
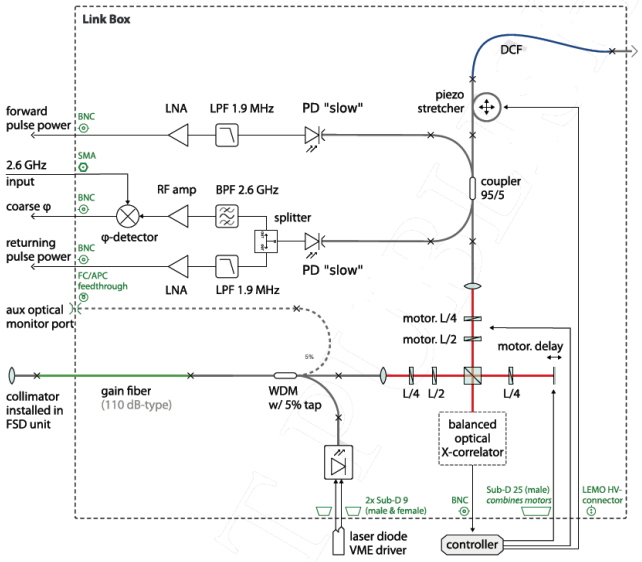
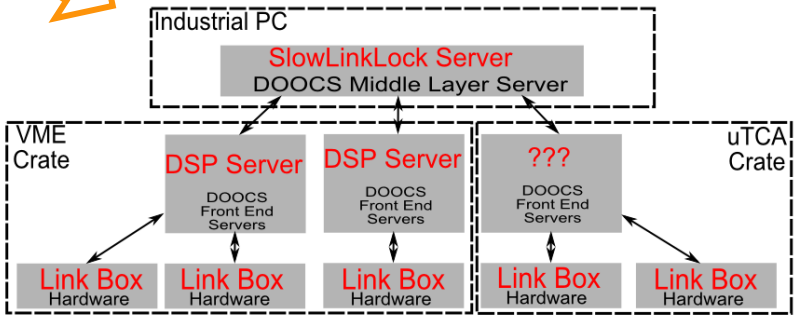
Link Lock Middle Layer Server



Courtesy: S.Schulz







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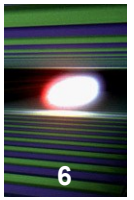
Link Lock Middle Layer Server



Aims for Server development

- Make links simple in use (one panel - one button features)
- Make link robust and decrese downtime (full automatization and exception handling)

Server features

- Jitter and long time drift calculations
- Locking the link using optical cross-correlator signal
- ‘Intelligent’ coarse tuning using stepper motors
- Fast and slow calibration of the cross-correlator coefficient
- Automatic search for the cross-correlator signal
- Control and monitoring of the laser diode driver front-end server
- Calculation of piezo-driver coefficient
- Advanced expecption handling and recovery

Server architecture

- Middle layer server – can be reused with MTCA
- Multithread software – separated threads for all long time routines
- Dedicated C++ classes for LLD supervision and motorized delay line (step motor)
- Advanced logging scheme – 5 logs priorities

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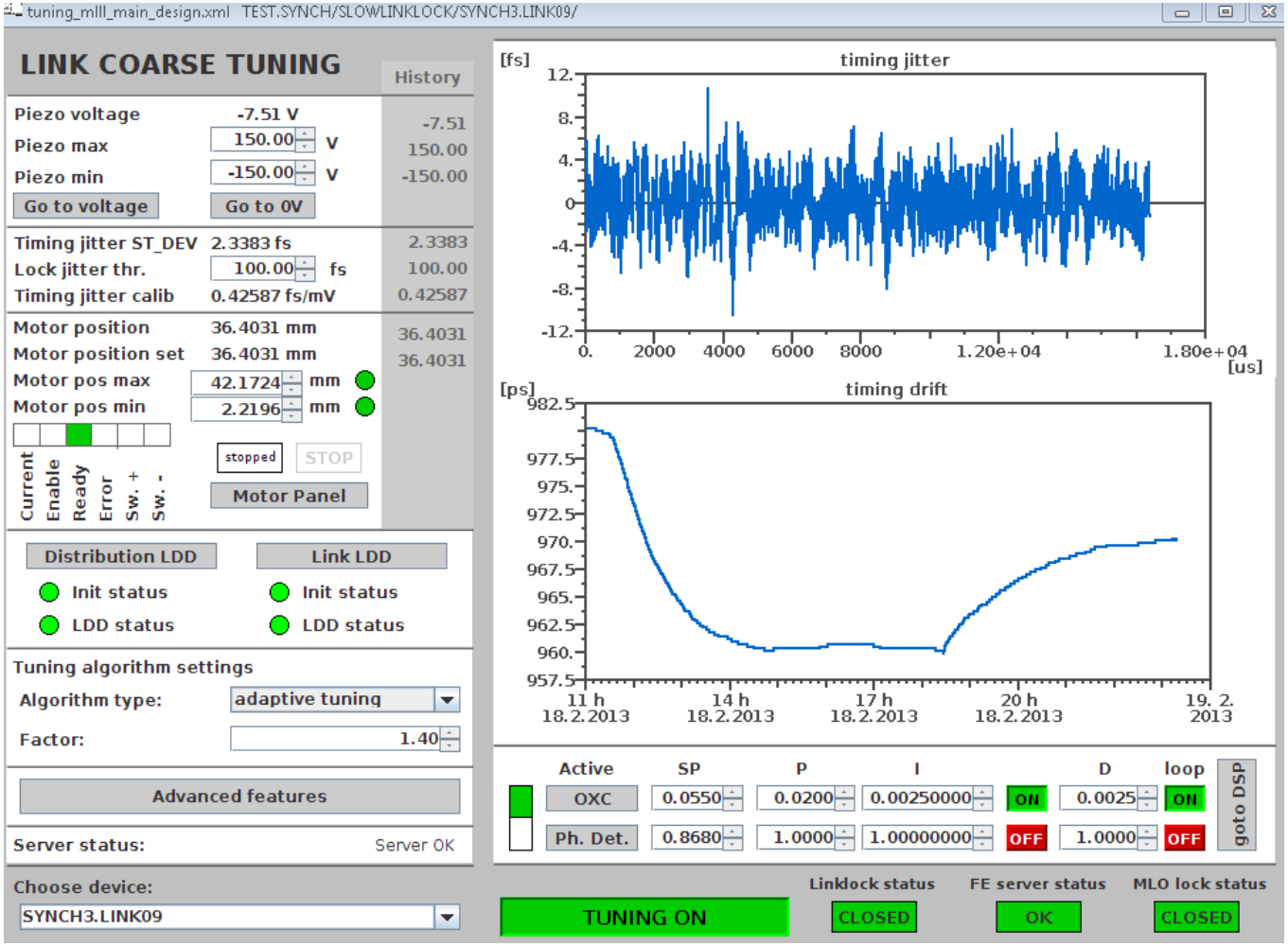
Link Lock Middle Layer Server



Link Lock Middle Layer Server main panel

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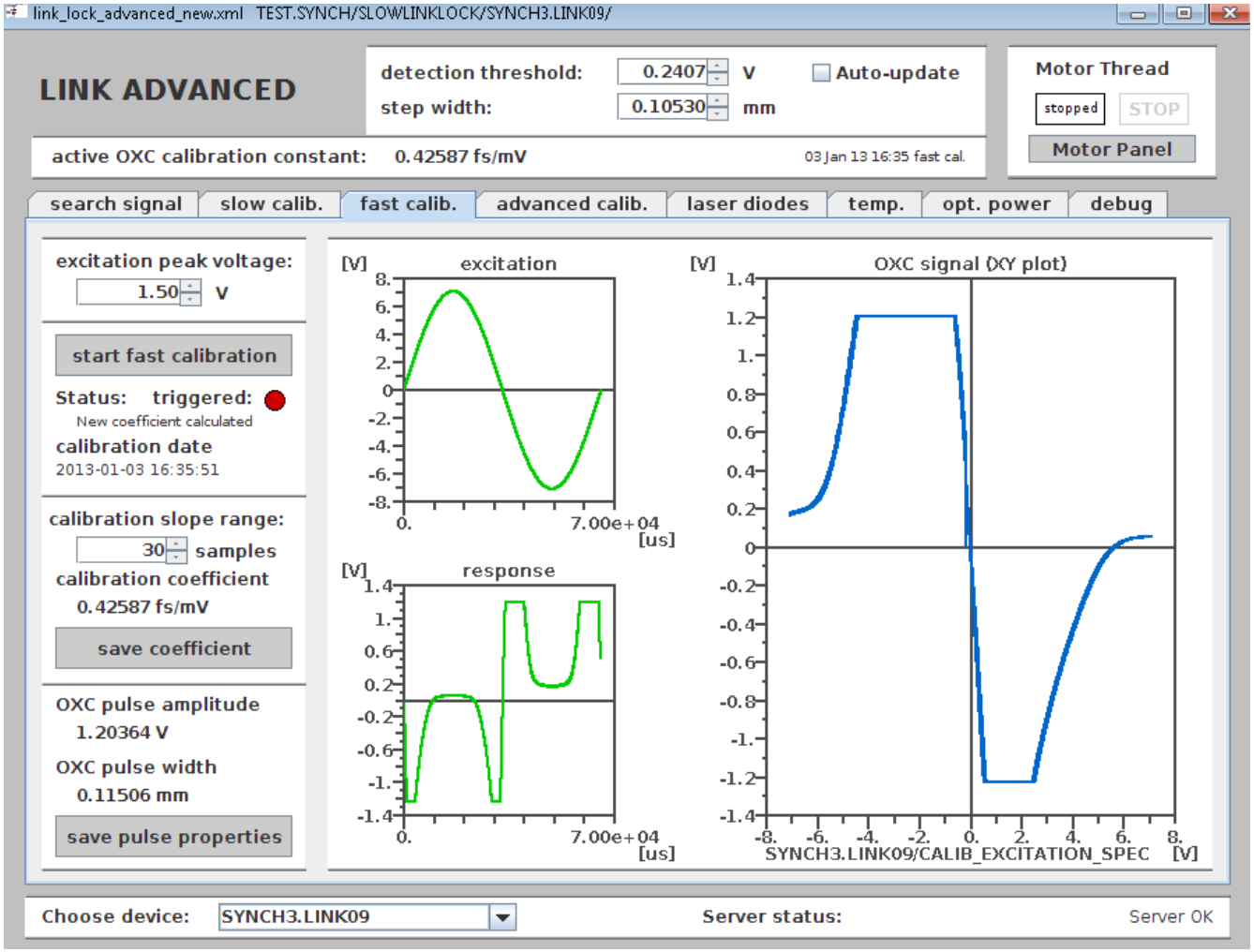
Link Lock Middle Layer Server



Link Lock Middle Layer Server advanced panel

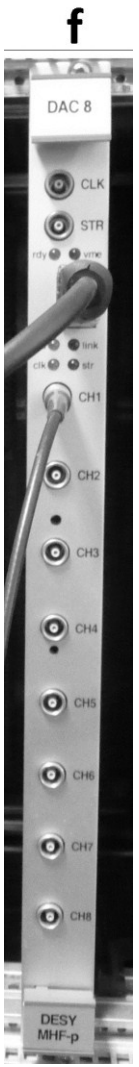
Server for VME DAC card – DAC8 Server

Aim for development:

- Have a person who is able to maintaine the board
- Fix firmware problems with software pathes
- Add additional features (e.g. phase scanner)

Server features:

- event-driven architecture of the server
- two independent sets of channels which can operate in different modes and with different settings
- phase scanner feature
- additional mode of operation dedicated for faster phase scanning
- improved memory writes mechanism
- DAC signal disturbance free recovery from server restart or crate crash/restart mechanism added



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Server for SIS8300+DwC Locking Scheme

New phase locking scheme based on downcoversion is applied in:

- REGAE
- Photo Injector Laser 3 at FLASH (ultra short pulse laser)

RTM Downconverter

AMC ADC Board (SIS8300)

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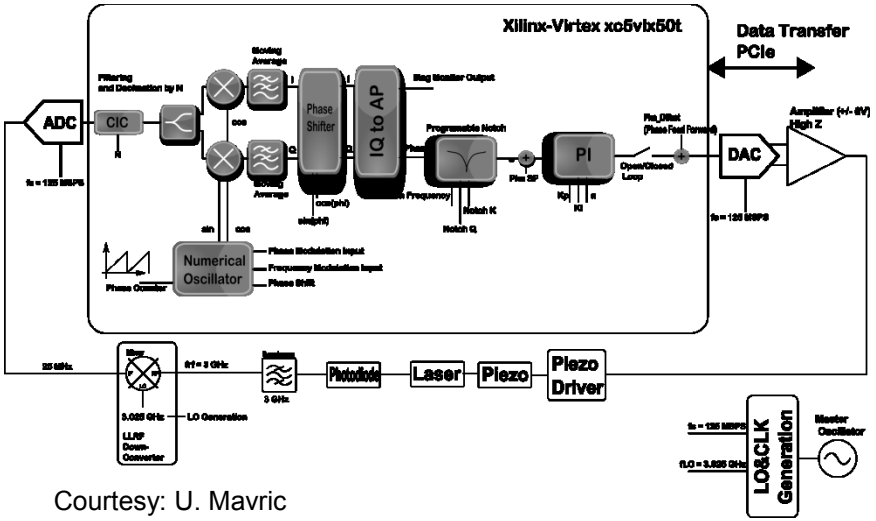
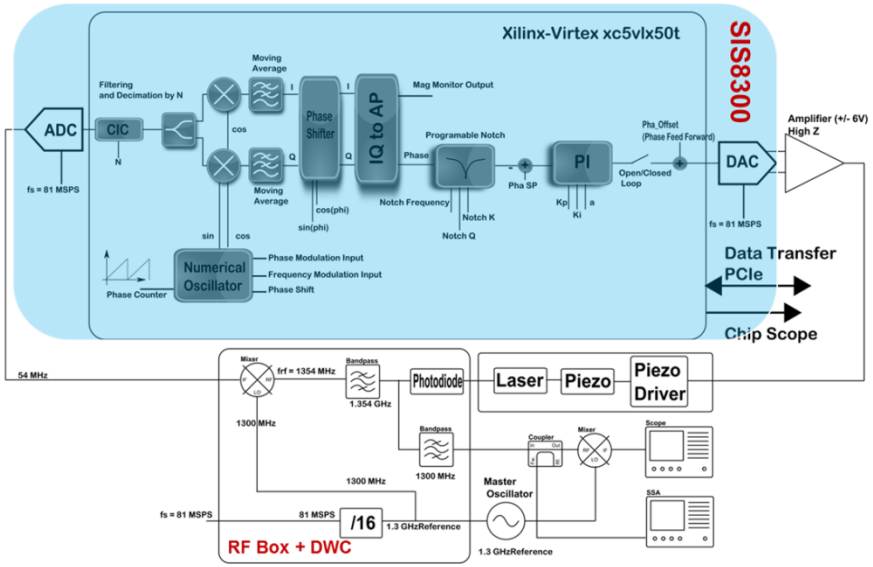
Server for SIS8300+DwC Locking Scheme

REGAE set-up



Courtesy: U. Mavric

PIL3 set-up



Controller in the FPGA:

- Developed by Uros with SysGen tool
- The same structure for both applications
- Differences in the ADC sampling rates

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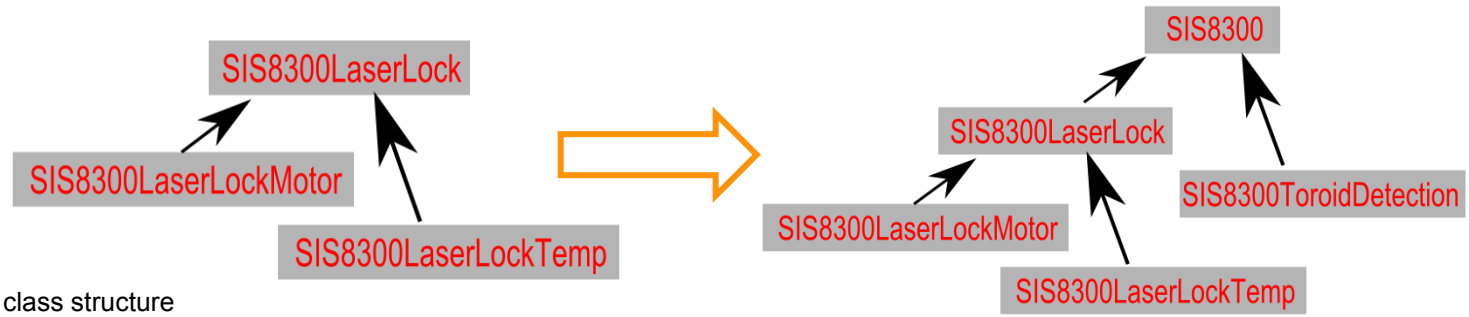
Server for SIS8300+DwC Locking Scheme

Server features

- Access to all registers with dedicated panels for application and board registers sets
- Auto-loading of defaults registers values after server restart (eg. after crate crash)
- 'Inteligence' coarse tuning with step motor/temperature
- Monitoring of DAC signal and lock lost detection in order to protect piezo driver
- Automatic 'one-button click' laser locking routine

Server architecture

- Integrated Middle layer and Front-End server functionalities (should it stay this way ??)
- Multithread software – separated threads for all long time routines (e.g. Coarse tuning, laser locking)
- Event driven architecture



Simpflied class structure

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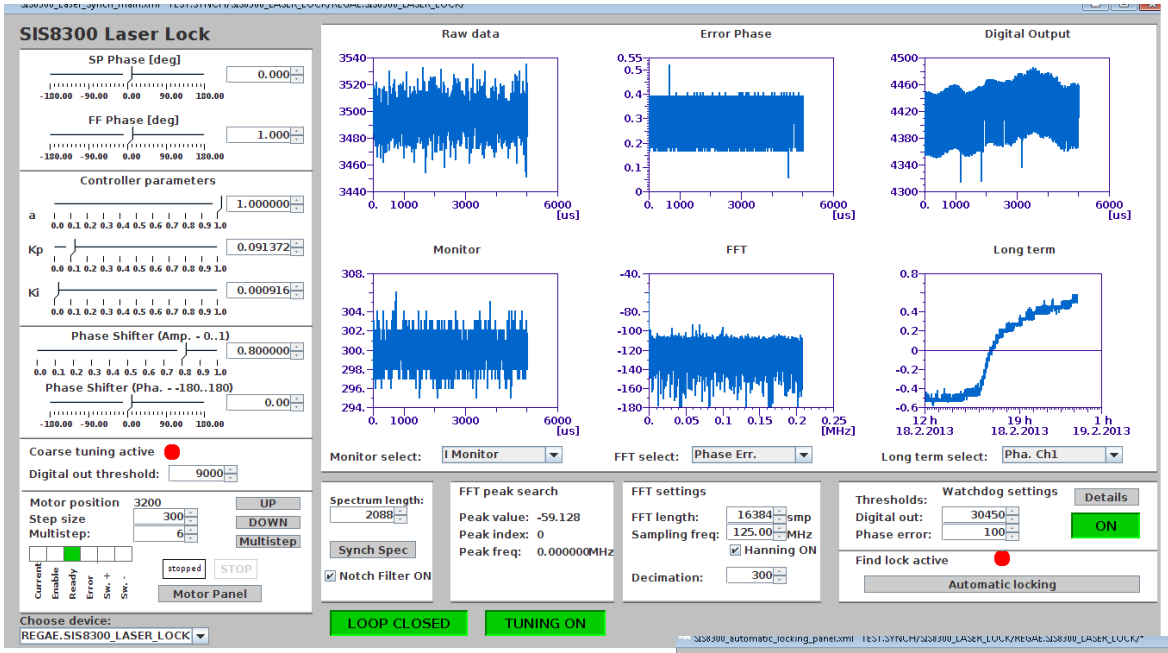
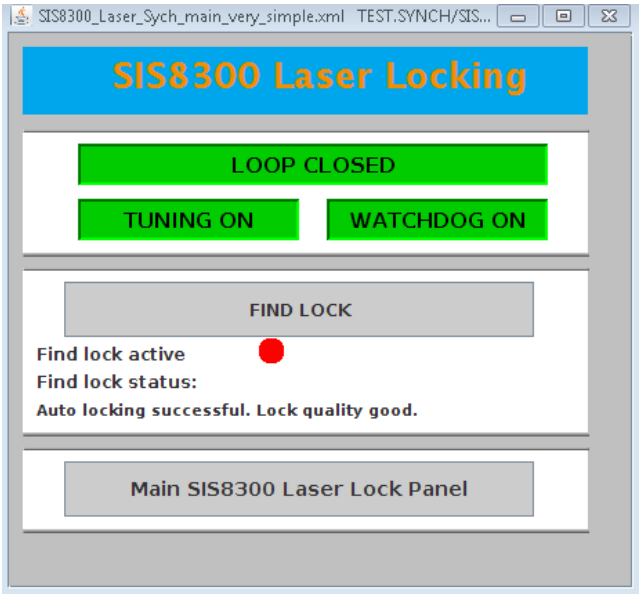
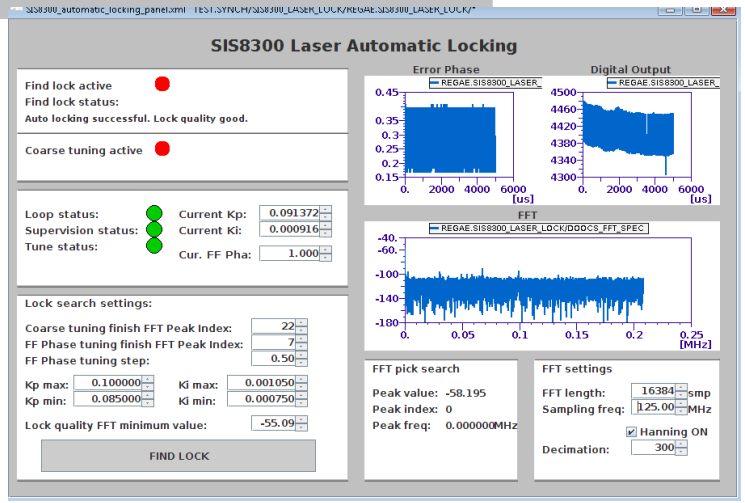
Server for SIS8300+DwC Locking Scheme



Advanced SIS8300 Lock Panel



Simplified SIS8300 Laser Lock panel



Auto locking advanced panel

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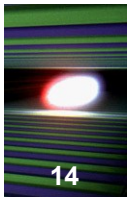
Future development



Slow link lock server

- Small bug fixing pending
- Adding phase detector support
- Addjusting server for new front-end server (DAMC2 based one)
- More inteligent scanning for finding OXC signal

SIS8300+DwC Locking Scheme Server

- Debugging DMA read error (only PIL3 location)
- Adding notch filter parameters calculation
- Adding ‘more intelligent’ coarse tuning routines
- A lot of minor adjustments – units, panel etc.

- System identification for finding optimal PI settings

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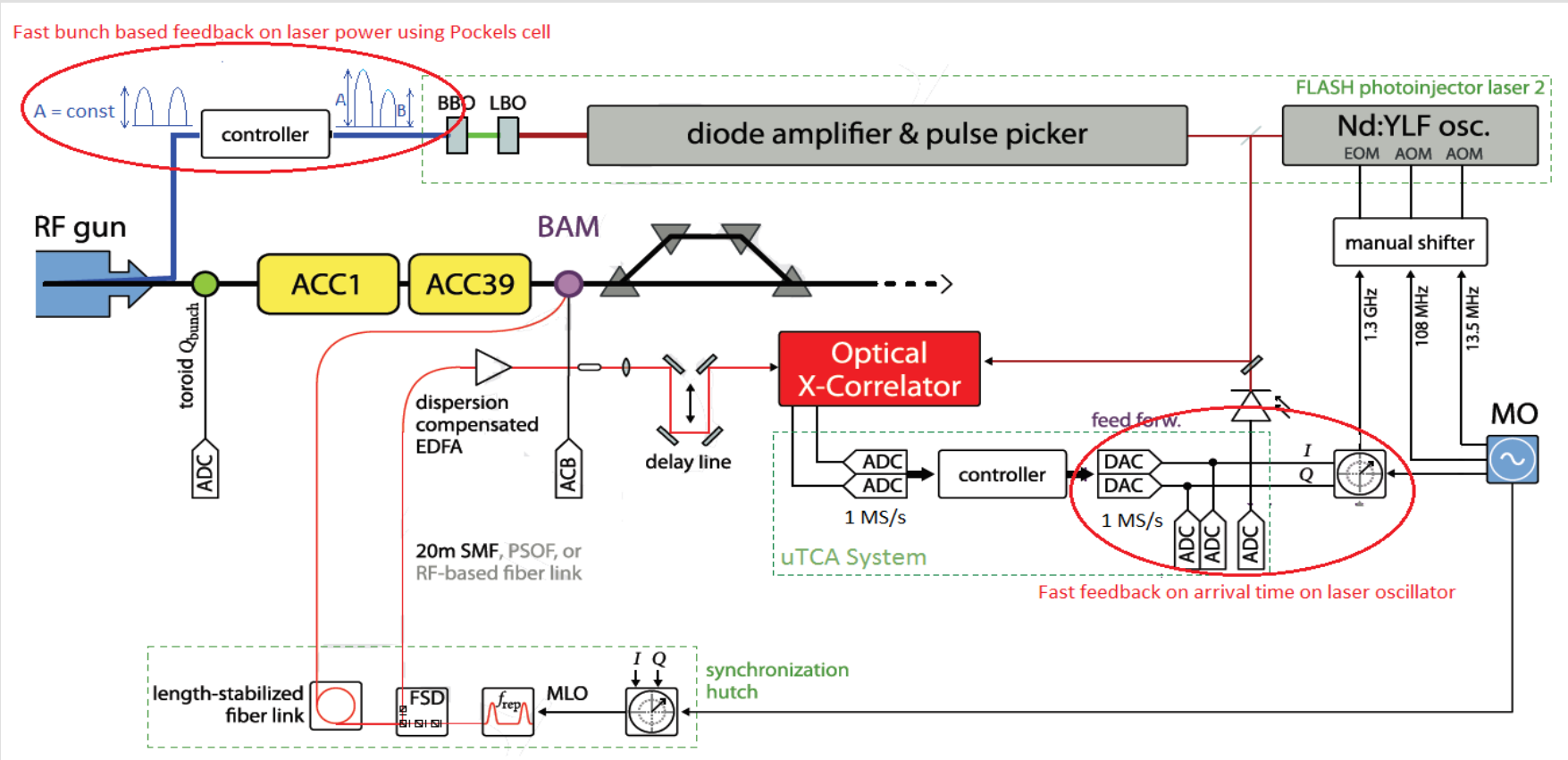
Future development

Future project:

- Laser Pulse Amplitude Stabilization with Pockel cell
- Fast feedback on arrival time



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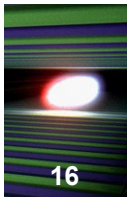
Thanks



Thank you for your attention

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Clip board – copy and paste

Headline

- first level
  - second level
    - ➔ third level

Headline

Texttext texttext
texttext texttext
texttext texttext

Keyword

1. Keyword
2. Keyword

- keyword
- keyword

Result Headline

- result text
- result text

Result headline

Result text, result text, result text

Result headline

- result text
- result text
- result text