

uFMC25 Status

Stefan Korolczuk

National Centre for Nuclear Research, Otwock-Świerk, Poland

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Agenda

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- 5 Next steps

uFMC25 main features

Main devices:

- Data processing FPGA: Virtex-5
- Board management FPGA: Spartan-6
- MMC device : ATxmega128

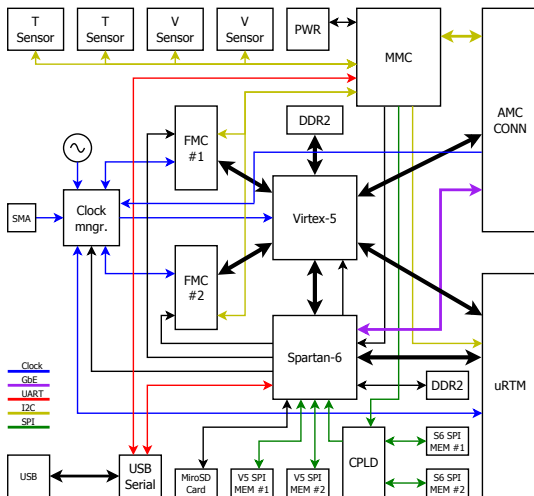
Connectivity:

- 2x FMC (both HPC)
- RTM D1.1 D1.2 D1.3 compatible
- Clocks, triggers and interlocks according to MTCA.4 specification

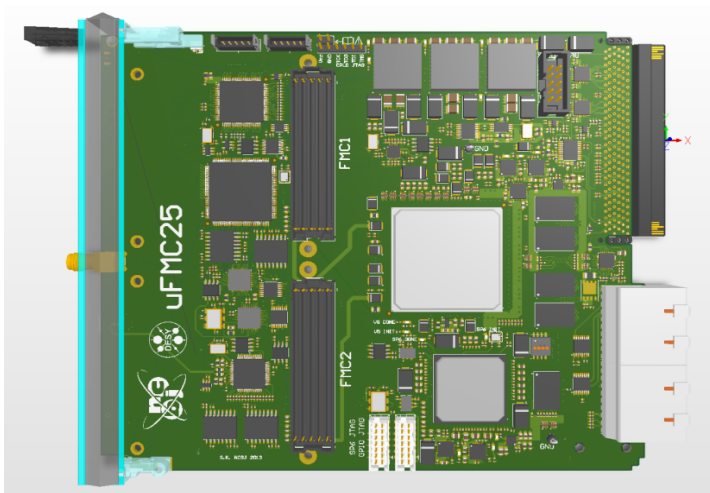
Debugging:

- USB-Serial interface to MMC and to Spartan-6
- Easy external powering for out-of-crate operation

uFMC25 main block diagram



uFMC25 top



Status

Status:

- Schematics: 99% finished (MMC will be ready during the workshop)
- PCB: 99% finished (MMC will be ready during the workshop)

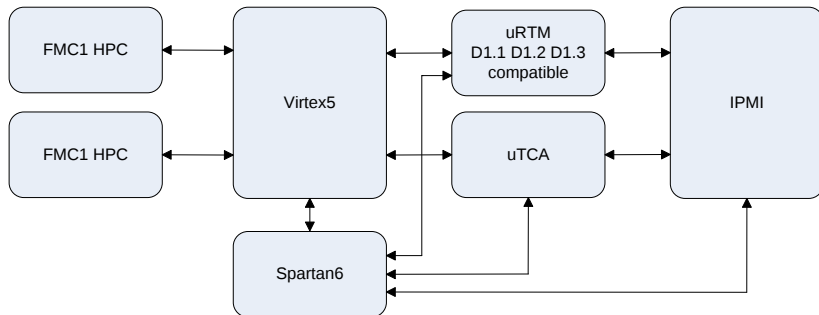
Next steps

- MMC will be ready during the workshop - up to 1 week from now to update schematics and PCB
- Reviewing - T.Jeżyński, J.Szewiński - 2 weeks from now
- BOM and ordering components - custom components, usually available at Farnell, Digi-Key, Avnet
- Production and assembly (8 pcs.) at ILFA - standard 14 layers technology; no blind vias, no buried vias
- VHDL initial projects imported from current testing board during production process - new member will be involved
- Board testing (2 persons)
- Implement core functionality: IPMI, Ethernet, remote configuration (3 persons)
- BAM FMC card test - collaboration with Samer Bou Habib
- working board delivery time - June 2013

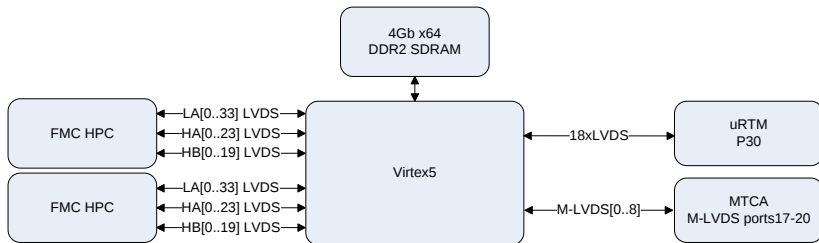
The end

Thank You

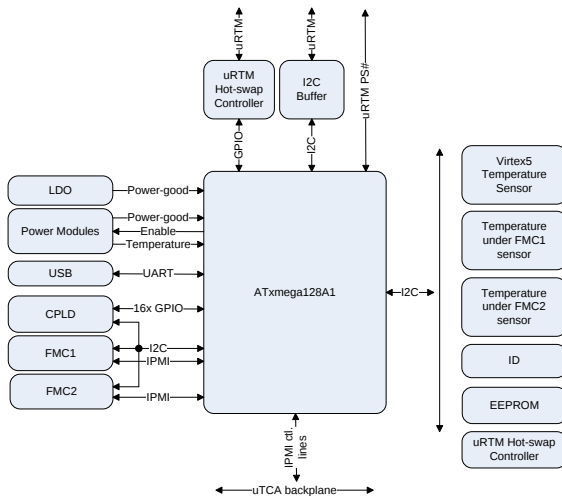
uFMC25 main block diagram



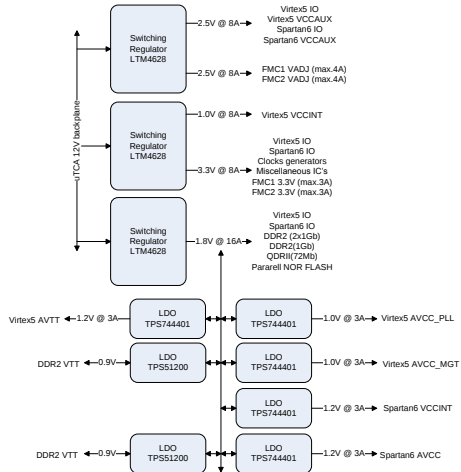
Virtex5 Connectivity



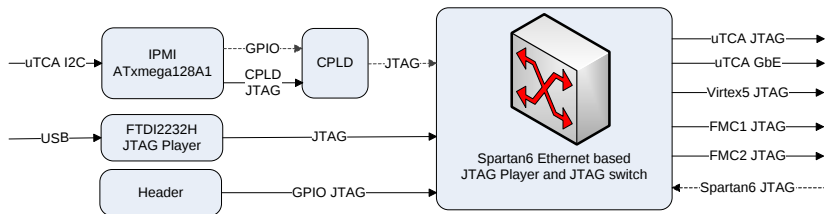
IPMI



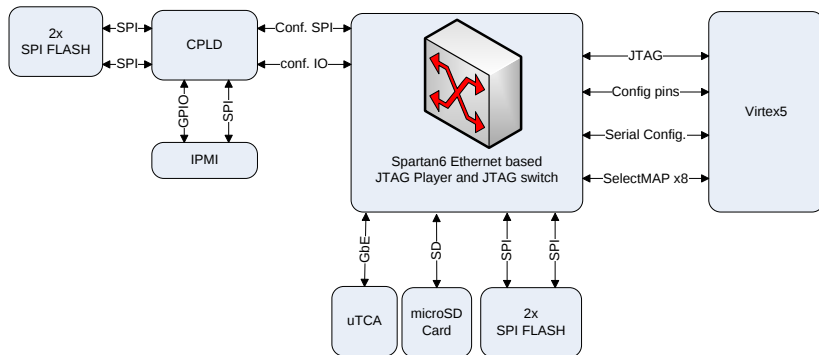
Power distribution



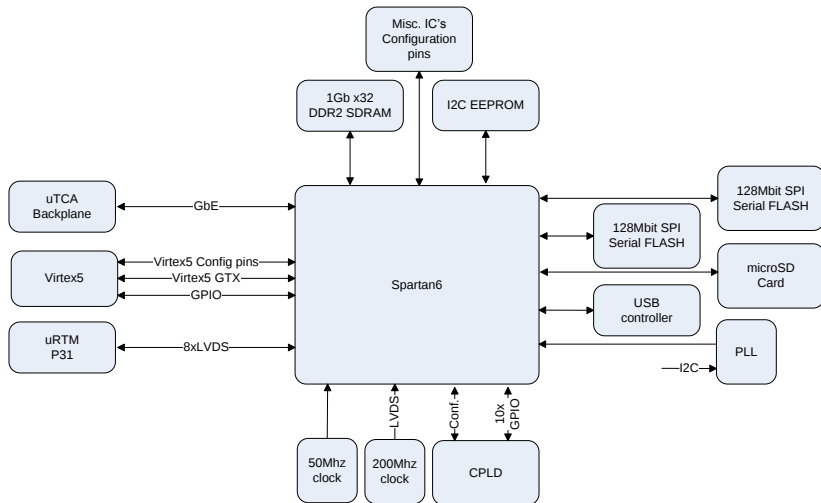
JTAG



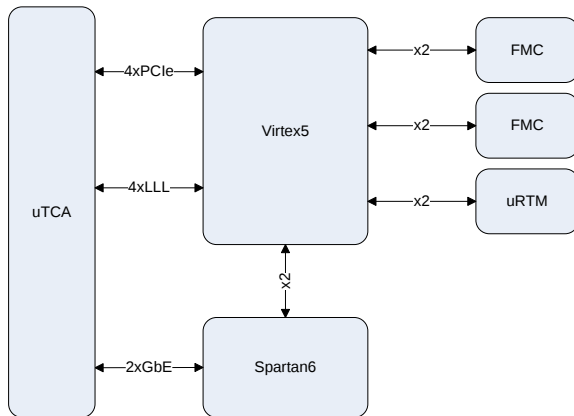
FPGA Configuration



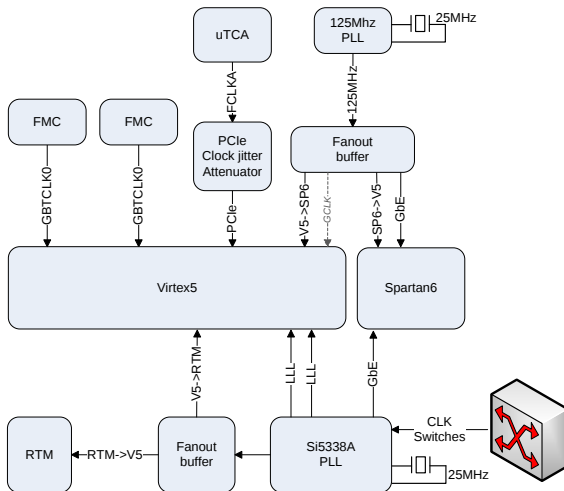
Spartan6



RocketIO



RocketIO clocks



Clocks Distribution Network

