Testing procedures and setup

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ISE

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Need of tests

- Errors in mass production
- System debugging expensive
- More than 1000 boards
- Quality Check needed - test stands
- Fast error reporting
- Comparable and reliable results
- Tracking operation history of a device

Test types

Single board tests

- Functional tests (factory), ie.:
  - Visual inspection
  - Power consumption
  - Management
  - etc.
- Performance tests (DESY), ie.:
  - Spectrum
  - Reflectivity
  - etc.
- Tested boards:
  uRFB, SIS8300, uRFB, uVM, uTC, uLOG, uPZT, uDS800, RTM HOM, RTM KLM

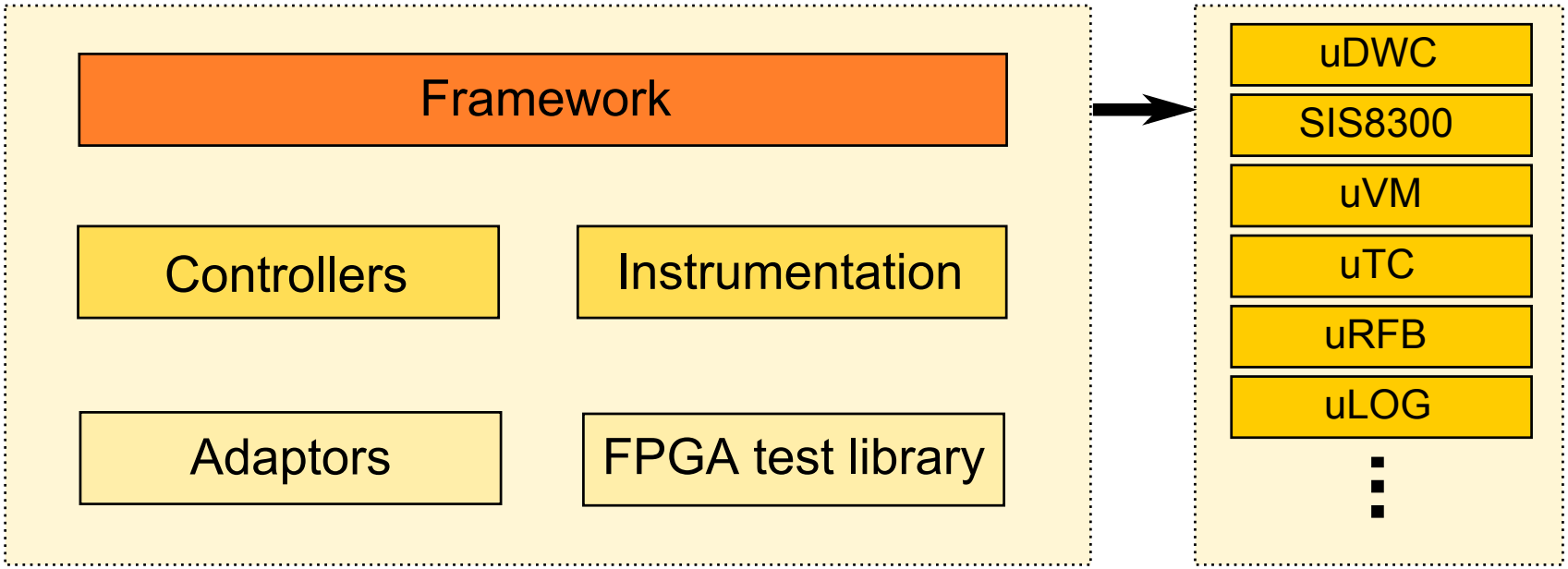
System tests

- Mounted crate tests
- Testing waveforms
- Montage, firmware/software version validation

Reliability tests

- Availability time
- uRFB - unable to hotswap
- Ageing, temperature shocks etc.

Project structure

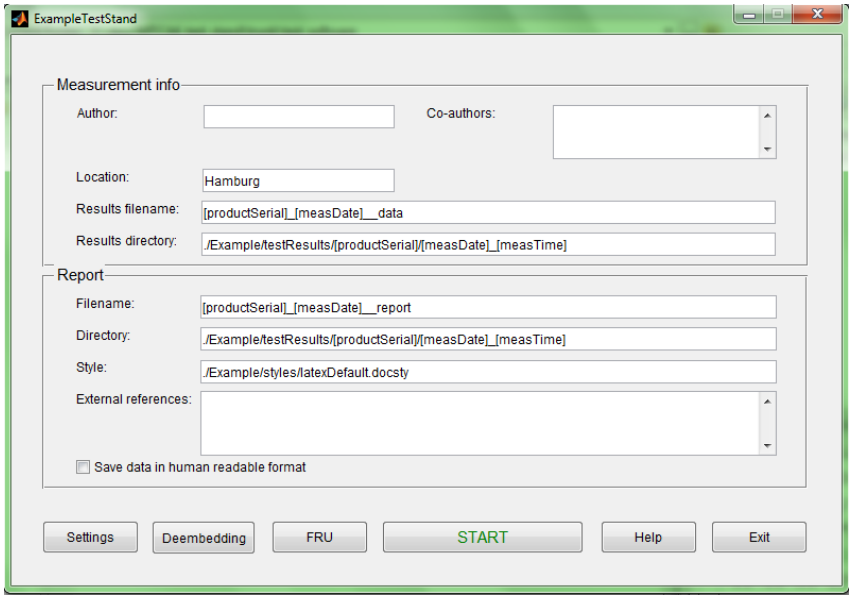


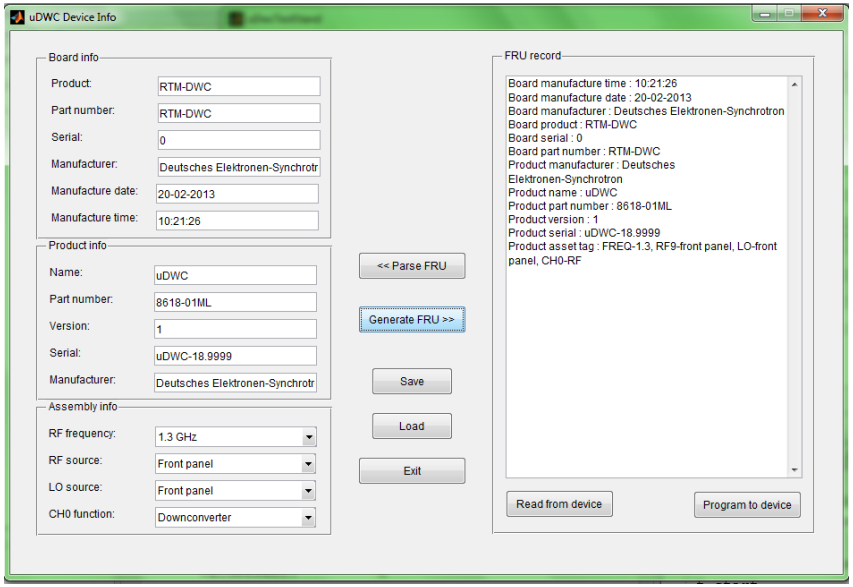
- Test stand core
- Board specific test stands

Core status

Framework

- Control of instrumentation, controllers, FPGA library blocks
- Complete test chain: measurement routines, data processing, report generating
- FRU editor, parser, read/write operations - specification?!
- Technical documentation, quick-start programming guide, programming guideline, example project, artificial data generation

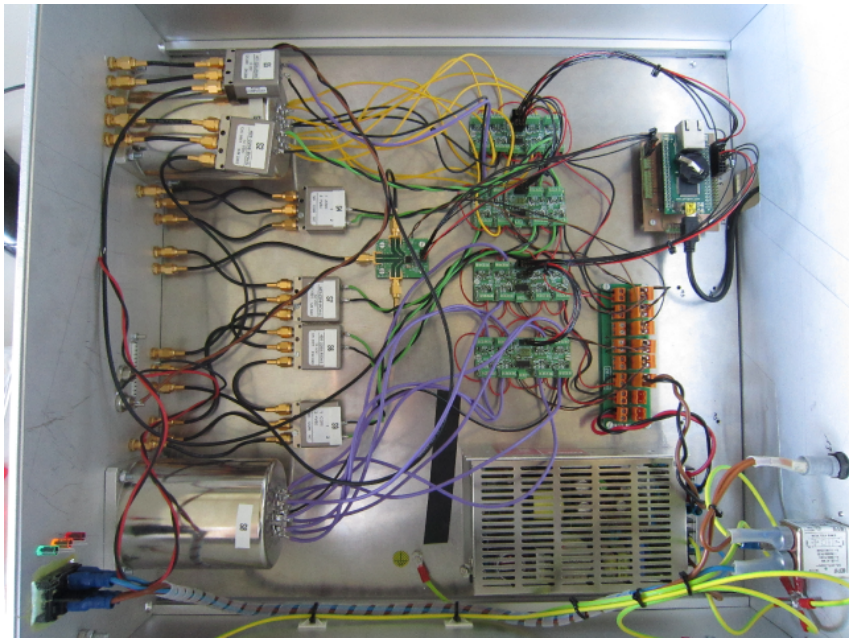




Core status

Hardware

- Zone3 adaptor A1 class RTM in production, AMC under design (production in 2 weeks), AMC connector adaptor design begins

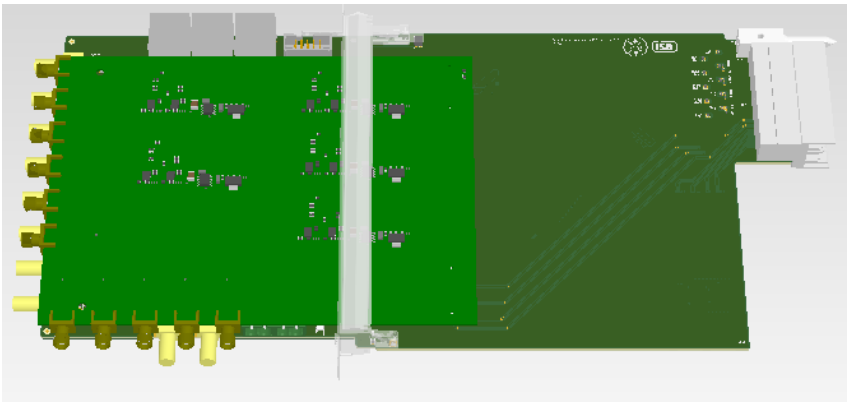


FPGA test library

- Replaces application layer, slow digital interfaces, clocks

Instrumentation

- Power supplies, RF generators, vector network analyzer, spectrum analyzer
- Signal distribution box, v.2 under design



Controllers

- ARM-based controller - slow digital interfaces: DIO, SPI, I2C
- FPGA-based controller - uTC based, project begins

Test stands status

In progress

- uDWC - final tests needed
- uRFB - software ready, needed: tests with instrumentation, final tests, user-documentation
- uVM - internal FPGA tests, software almost ready (except reporting), needed: tests with instrumentation, final tests, user-documentation
- uLOG - test procedure in progress
- SIS8300 - test procedure in progress

Core plans

1. Framework
   - Development frozen (deembedding, IPMI, data storage) - March
   - Stable version - April
2. Instrumentation
   - Signal distribution box v.2 -March
3. Hardware
   - Zone3 analogue adaptors -March, April
   - AMC connector adaptors -April
   - Zone3 digital adaptors - June
4. Controllers
   - FPGA based controller -March
5. FPGA test library
   - Adding RIO, BER, documentation -March

Test stands plans

Test stands

- uDWC - April
- SIS8300 - April
- uVM - April
- uRFB - April
- uLOG - May
- uTC - May
- uPZT - June
- uDS800 - June
- RTM KLM - July
- RTM HOM - July

uRFB reliability tests

- Ageing, temperature shocks, weak-points identification - October

Crate system tests

- Specification, waveform generation, servers link - October

Commercialization plans

- Licensing/selling/lending setups for functional and performance tests
- Different types of setups: software, software+instrumentation
- Adaptor boards licensing
- Installation, training, support, upgrades
- Participation of other groups (Kay Rehlich?), extensions

Problems and Questions

Problems

- Specification - we cannot measure without specification
  impressive total delay of 21 weeks!
- FRU and IPMI, MMC, Zone3 digital classes
- Limited manpower - part time works, too many projects

Questions

- Realistic schedule for mass production?
- New boards?
- Module tests?
- Board pairs? Do we have to cover also development and debugging?
- KDS integration - additional access?
- Extension proposals?
- Resources?

People

- Marcin Gosk - Zone3 adaptor boards
- Jacek Góralczyk - AMC adaptor board
- Maciej Grzegrzółka - uVM test stand
- Przemysław Kownacki - software framework
- Tomasz Leśniak - uLOG, uRFB test stands
- Anna Łysiuk - calibration, signal distribution hardware
- Igor Rutkowski - SIS8300 test stand
- Agnieszka Zagoździńska - uTC based controller