

Testing procedures and setup

Paweł Barmuta

ISE

February 20, 2013

Need of tests

- Errors in mass production
- System debugging expensive
- More than 1000 boards
- Quality Check needed - test stands
- Fast error reporting
- Comparable and reliable results
- Tracking operation history of a device

Single board tests

- Functional tests (factory), ie.:
 - Visual inspection
 - Power consumption
 - Management
 - etc.
- Performance tests (DESY), ie.:
 - Spectrum
 - Reflectivity
 - etc.
- Tested boards:
uRFB, SIS8300, uRFB, uVM,
uTC, uLOG, uPZT, uDS800,
RTM HOM, RTM KLM

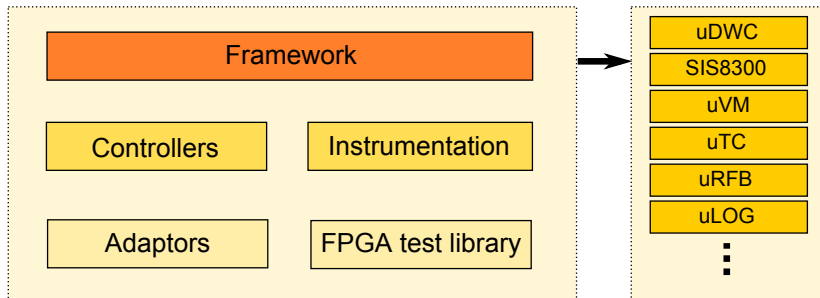
System tests

- Mounted crate tests
- Testing waveforms
- Montage, firmware/software version validation

Reliability tests

- Availability time
- uRFB - unable to hotswap
- Ageing, temperature shocks etc.

Project structure



- Test stand core
- Board specific test stands

Framework

- Control of instrumentation, controllers, FPGA library blocks
- Complete test chain: measurement routines, data processing, report generating
- FRU editor, parser, read/write operations - specification?!
- Technical documentation, quick-start programming guide, programming guideline, example project, artificial data generation

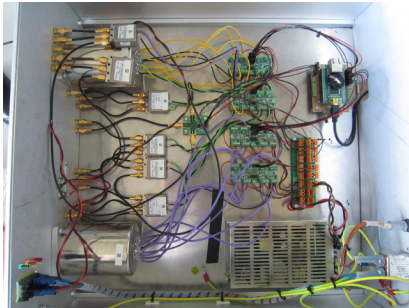
The top screenshot shows the 'ExampleTestStand' window. It has two main sections: 'Measurement info' and 'Report'. The 'Measurement info' section includes fields for 'Author', 'Co-authors', 'Location' (set to 'Hamburg'), 'Results filename' (set to 'productSerial_measDate_data'), and 'Results directory' (set to 'ExampleResults\productSerial\measDate_measTime'). The 'Report' section includes fields for 'Filename' (set to 'productSerial_measDate_report'), 'Directory' (set to 'ExampleResults\productSerial\measDate_measTime'), 'Style' (set to 'Example\styles\Default.docx'), and 'External references'. There is a checkbox for 'Save data in human readable format'. At the bottom are buttons for 'Settings', 'Deembedding', 'FRU', 'START', 'Help', and 'Exit'.

The bottom screenshot shows the 'uGWC Device Info' window. It has two main sections: 'Board info' and 'FRU record'. The 'Board info' section includes fields for 'Product' (set to 'RTM-OWC'), 'Part number' (set to 'RTM-OWC'), 'Serial' (set to '9'), 'Manufacturer' (set to 'Deutsches Elektronen-Synchrotron'), 'Manufacture date' (set to '29-02-2013'), and 'Manufacture time' (set to '10:21:26'). The 'Product info' section includes fields for 'Name' (set to 'uGWC'), 'Part number' (set to '8616-0 1ML'), 'Version' (set to '1'), 'Serial' (set to 'uGWC-16.9999'), and 'Manufacturer' (set to 'Deutsches Elektronen-Synchrotron'). The 'Assembly info' section includes fields for 'RF frequency' (set to '1.3 GHz'), 'RF source' (set to 'Front panel'), 'LO source' (set to 'Front panel'), and 'CH3 function' (set to 'Downconverter'). The 'FRU record' section shows a list of FRU records. There are buttons for 'Parse FRU', 'Generate FRU', 'Save', 'Load', 'Exit', 'Read from device', and 'Program to device'.

Core status

Hardware

- Zone3 adaptor A1 class RTM in production, AMC under design (production in 2 weeks), AMC connector adaptor design begins

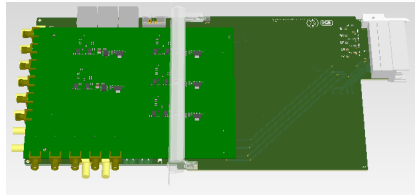


FPGA test library

- Replaces application layer, slow digital interfaces, clocks

Instrumentation

- Power supplies, RF generators, vector network analyzer, spectrum analyzer
- Signal distribution box, v.2 under design



Controllers

- ARM-based controller - slow digital interfaces: DIO, SPI, I2C
- FPGA-based controller - uTC based, project begins

In progress

- uDWC - final tests needed
- uRFB - software ready, needed: tests with instrumentation, final tests, user-documentation
- uVM - internal FPGA tests, software almost ready (except reporting), needed: tests with instrumentation, final tests, user-documentation
- uLOG - test procedure in progress
- SIS8300 - test procedure in progress

- ① Framework
 - Development frozen (deembedding, IPMI, data storage) - March
 - Stable version - April
- ② Instrumentation
 - Signal distribution box v.2 - March
- ③ Hardware
 - Zone3 analogue adaptors - March, April
 - AMC connector adaptors - April
 - Zone3 digital adaptors - June
- ④ Controllers
 - FPGA based controller - March
- ⑤ FPGA test library
 - Adding RIO, BER, documentation - March

Test stands

- uDWC - April
- SIS8300 - April
- uVM - April
- uRFB - April
- uLOG - May
- uTC - May
- uPZT - June
- uDS800 - June
- RTM KLM - July
- RTM HOM - July

uRFB reliability tests

- Ageing, temperature shocks, weak-points identification - October

Crate system tests

- Specification, waveform generation, servers link - October

Commercialization plans

- Licensing/selling/lending setups for functional and performance tests
- Different types of setups: software, software+instrumentation
- Adaptor boards licensing
- Installation, training, support, upgrades
- Participation of other groups (Kay Rehlich?), extensions



Problems and Questions

Problems

- Specification - we cannot measure without specification
impressive total delay of 21 weeks!
- FRU and IPMI, MMC, Zone3 digital classes
- Limited manpower - part time works, too many projects

Questions

- Realistic schedule for mass production?
- New boards?
- Module tests?
- Board pairs? Do we have to cover also development and debugging?
- KDS integration - additional access?
- Extension proposals?
- **Resources?**

- Marcin Gosk - Zone3 adaptor boards
- Jacek Góralczyk - AMC adaptor board
- Maciej Grzegorzówka - uVM test stand
- Przemysław Kownacki - software framework
- Tomasz Leśniak - uLOG, uRFB test stands
- Anna Łysiuk - calibration, signal distribution hardware
- Igor Rutkowski - SIS8300 test stand
- Agnieszka Zagoździńska - uTC based controller

