DESY studies

Ganna Dolinska, Ievgen Korol, Hanno Perrey, Daniel Pitzl

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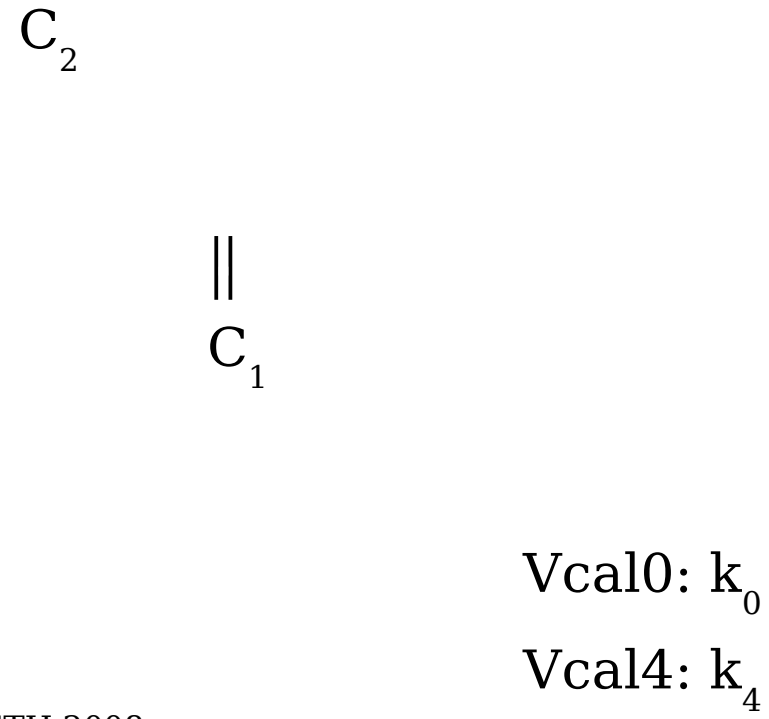
updated 18.12.2012

- test pulses: gain and capacitance ratios
- Ru source: clock stretch works for digital ROC
- beam test: psi46dig chip39 at I_A = 25 mA

calibration pulses



P. Trueb, PhD, ETH 2008

- Two amplitude ranges for Vcal:
  - large (high gain), selected with CtrlReg 4
  - small (low gain), selected with CtrlReg 0
- Two injection paths:
  - standard calibration (switch 1)
  - air capacitance from pad on ROC to sensor (switch 2), used for bump bond test.
  - air capacitance depends on bump height.

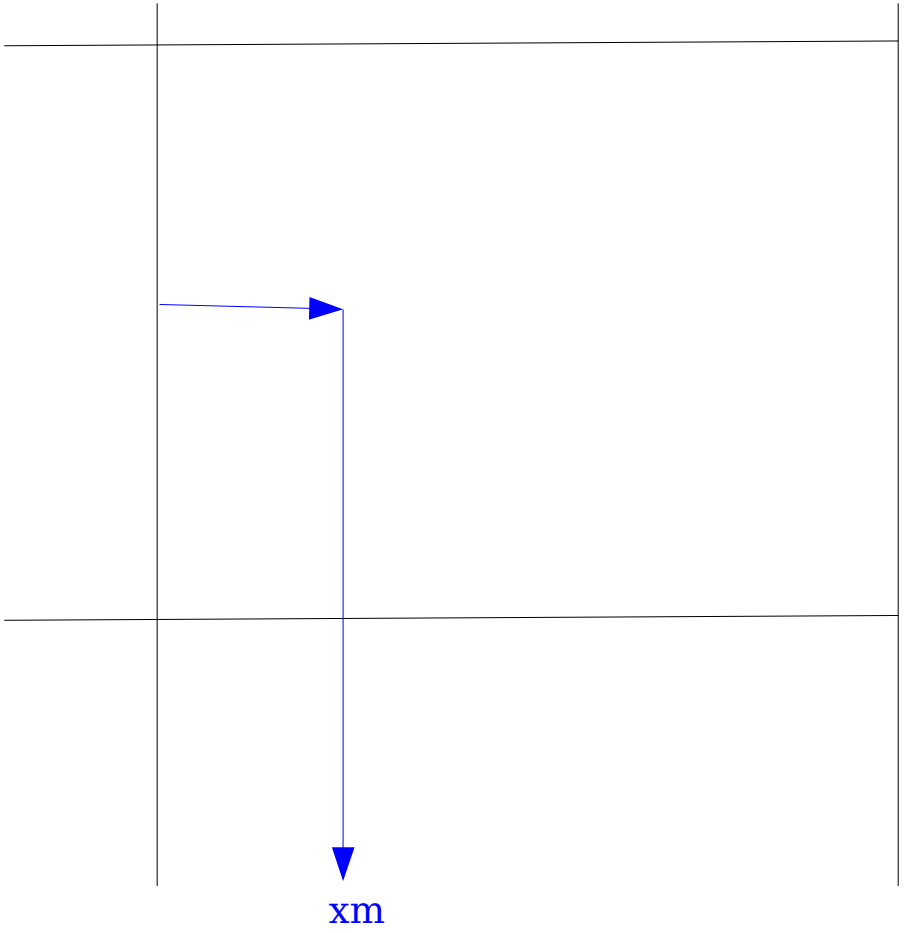
Pulse height vs small Vcal

- CtrlReg 0: small Vcal
- Switch 1: direct path
- Digital Chip 39
  - with sensor, -90 V
  - Ia 25 mA
  - trim 29
  - Pixel (0,6)
- Straight line fit
  - slope = $g_{01} = k_0 C_1$

Slope g_{01} distribution

- CtrlReg 0: small Vcal
- Switch 1: direct path
- Digital Chip 39
  - Ia 25 mA
- $\langle g_{01} \rangle = k_0 C_1 =$ 0.222 ADC/DAC

Pulse height vs large Vcal



- CtrlReg 4: large Vcal
- Switch 1: direct path
- Digital Chip 39
  - with sensor, -90 V
  - Ia 25 mA
  - trim 29
  - Pixel (0,6)
- Weibull fit:
  - slope = derivative at mid point
  - $g_{41} = k_4 C_1$

slope g_{41} distribution

psi46dig

- CtrlReg 4: large Vcal
- Switch 1: direct path
- Digital Chip 39
  - Ia 25 mA
- $\langle g_{41} \rangle = k_4 C_1 =$ 1.622 ADC/DAC

Pulse height with sensor air capacitance

- CtrlReg 4: large Vcal
- Switch 2: sensor path
- Digital Chip 39
  - with sensor, -90 V
  - Ia 25 mA
  - trim 29
  - Pixel (0,6)
- line fit below test pulse saturation:
  - $g_{42} = k_4 C_2$

g_{42} distribution

psi46dig

- CtrlReg 4: large Vcal
- Switch 2: sensor path
- Digital Chip 39
  - Ia 25 mA
- $\langle g_{42} \rangle = k_4 C_2 =$ 0.092 ADC/DAC

calibration ratios

C_2

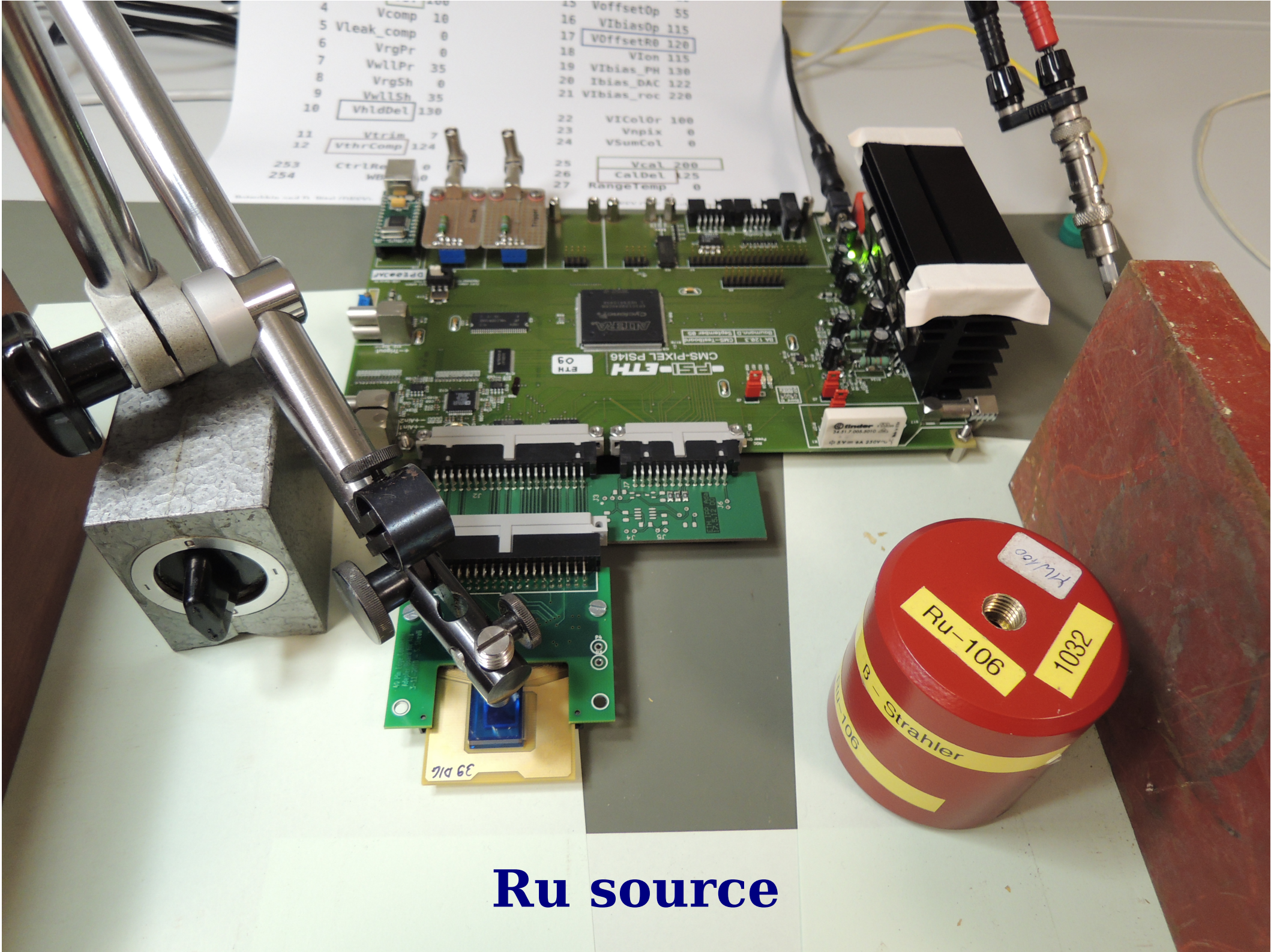
$\|$

C_1

Vcal0: k_0

Vcal4: k_4

- Digital Chip 39
  - Ia 25 mA
- Large / small Vcal:
  - $k_4 / k_0 = 7.3$
- capacitances:
  - $C_2 / C_1 = 0.057$
- To be repeated with DESY bump bonded sensors.

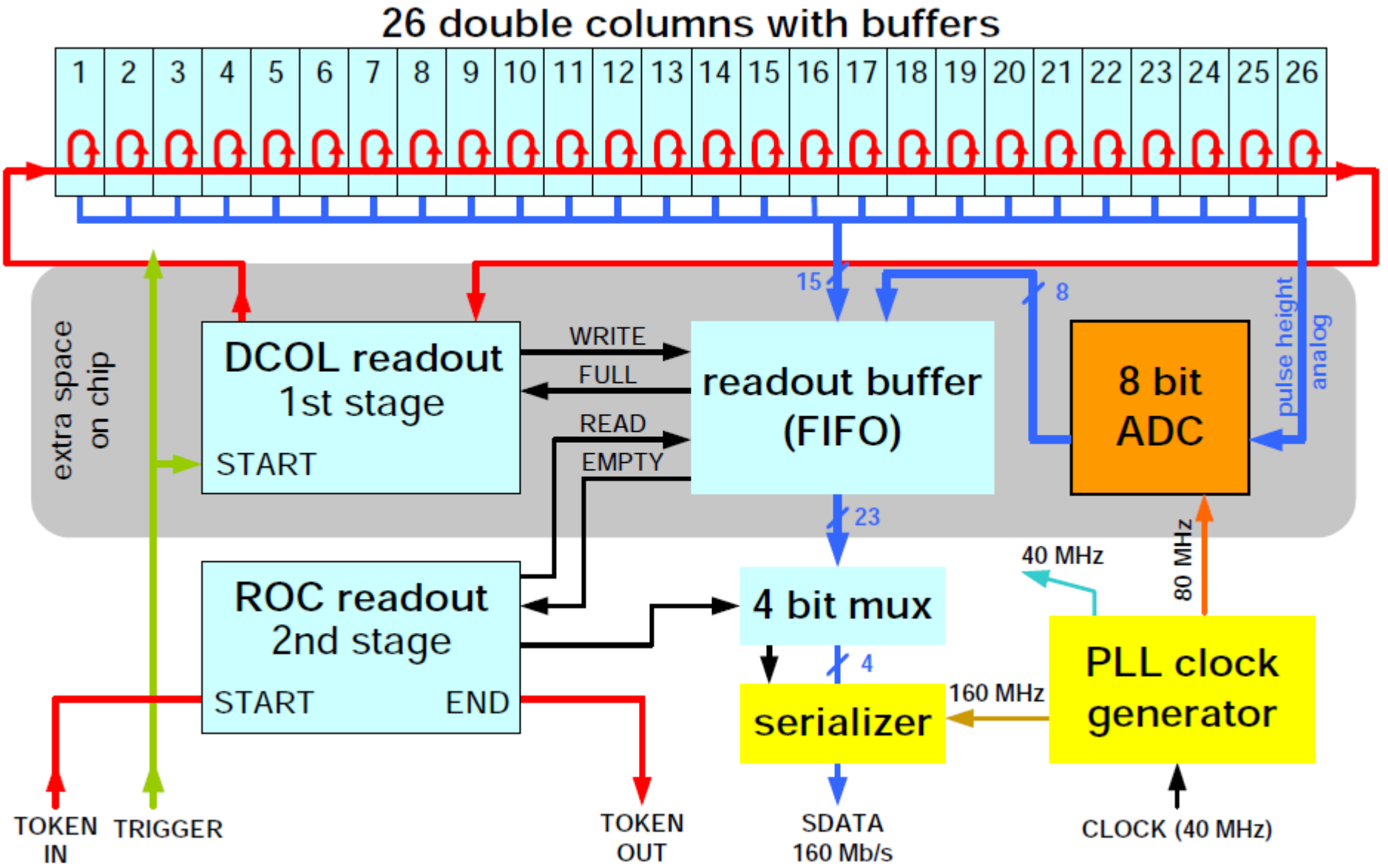

Vcomp 10
Vleak_comp 0
VrgPr 0
VwllPr 35
VrgSh 0
VwllSh 35
VhldDel 130
Vtrim 7
VthrComp 124
VoffsetOp 55
VIbiasOp 115
VOffsetRO 120
VIon 115
VIbias_PH 130
Ibias_DAC 122
VIbias_roc 220
VIColOr 100
Vnpix 0
VSumCol 0
Vcal 200
CalDel 125
RangeTemp 0
CMS-PIXEL PSI46
Ru-106
1032
B - Strahler

Ru source

Clock stretch for source tests?

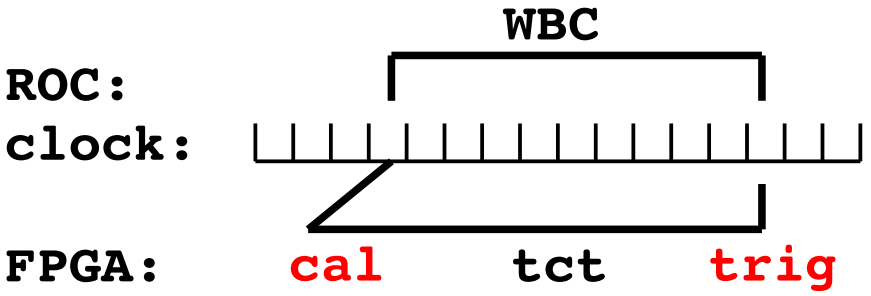
- Beta or X-ray sources cannot be triggered
  - have to use test board internal trigger: random
  - 40 MHz clock: (very) low hit probability for weak sources
- Clock stretch: 
  - FPGA can extend one clock cycle by up to 65'535 to 1.6 ms.
- Digital ROC has PLL:
  - 40 MHz → 80 MHz for ADC
  - 40 MHz → 160 MHz for readout
  - PLL stops when 40 MHz is missing
  - Does is restart fast enough for the readout?
  - Yes!

psi46dig periphery



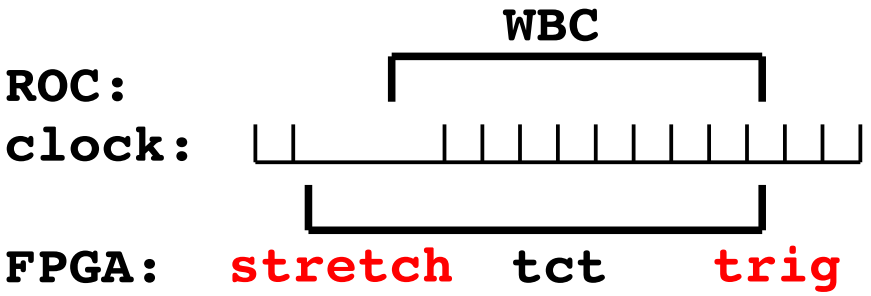
test board and ROC timing

psi46expert test pulses:



WBC = tct – 5 **5 = Cal and comparator delay**

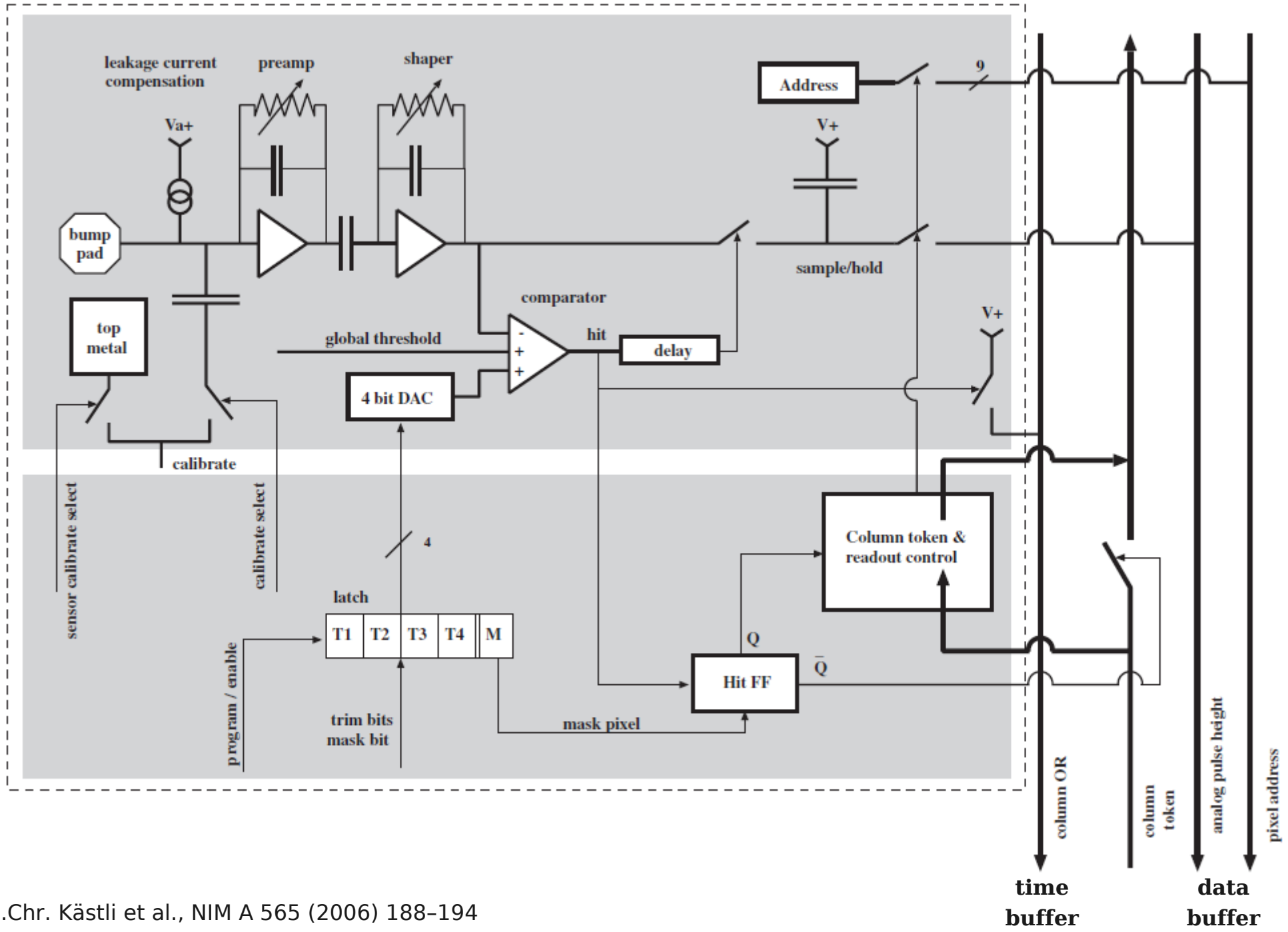
takeData clock stretch



WBC = tct – 3 **3 = comparator delay**

Recommended: WBC = 160 to allow transfer of up to 79 pixels per double column.

psi46 pixel unit cell



H.Chr. Kästli et al., NIM A 565 (2006) 188–194

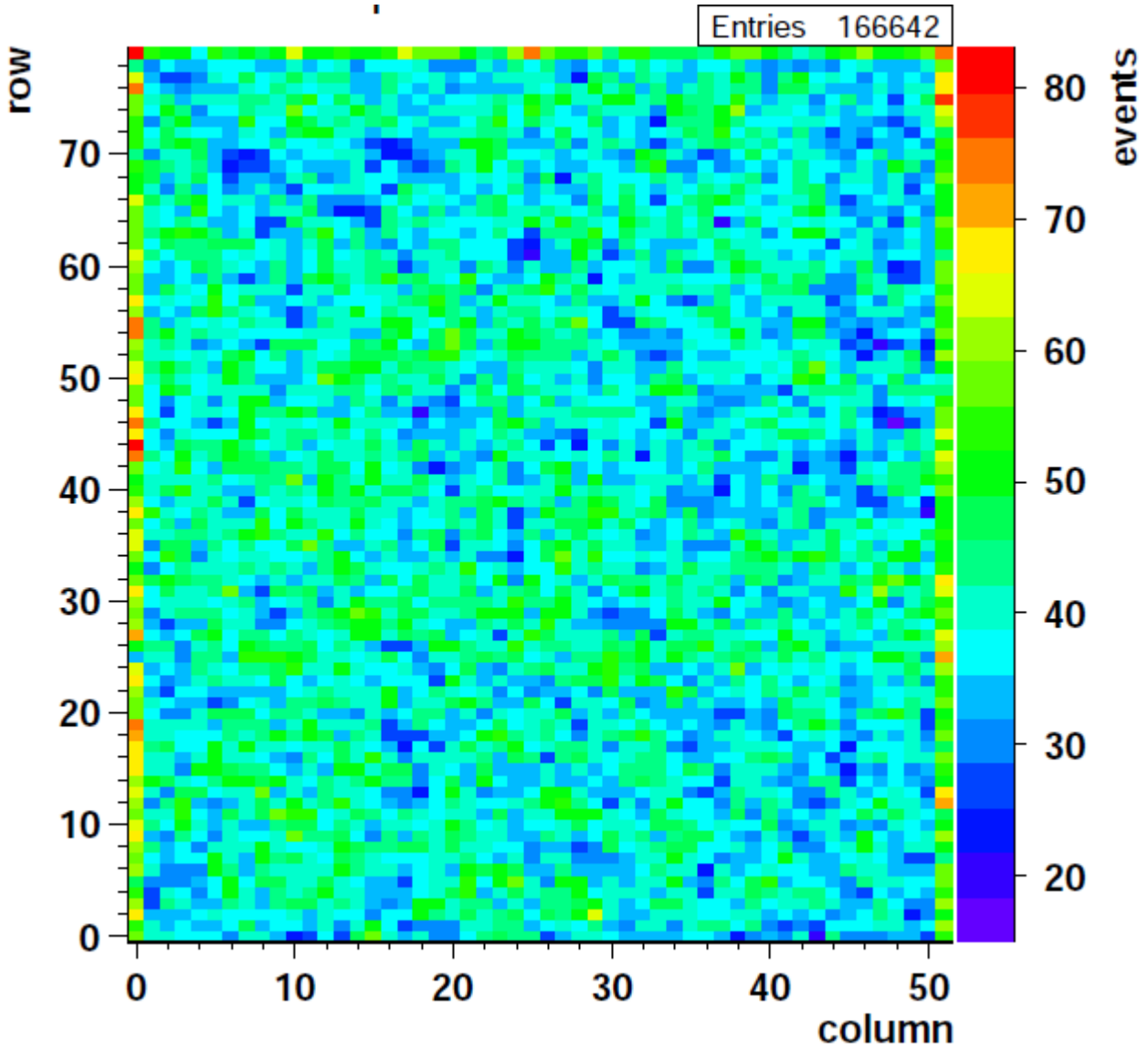
tbParameters for psi46dig source test

```
 8   clk    0  # [ns]
 9   sda   22  # [ns]
10   ctr    0  # [ns]
11   tin   68  # [ns]
12   rda   60  # [ns]

17   trc   20  # time-reset-calibrate [bc]
18   tcc   80  # time-cal-cal [bc]
19   tct  251  # time-cal-trig [bc] WBC 248 in daqFrame.cc
20   ttk   16  # time-trigger-token [bc]
21  trep  160  # trigger repetition delay
22    cc    1  # calibrate counter

77   spd    0  # board speed, 0 = 40 MHz
```

Ru source

- $Ru^{106} \rightarrow Rh^{106} \rightarrow Pd^{106}$:
  - pure beta emitter,
  - E_{max} 3.54 MeV,
  - half life 1.02 y,
  - DESY Ru source #1032 has ~5 kHz activity today (scintillator).

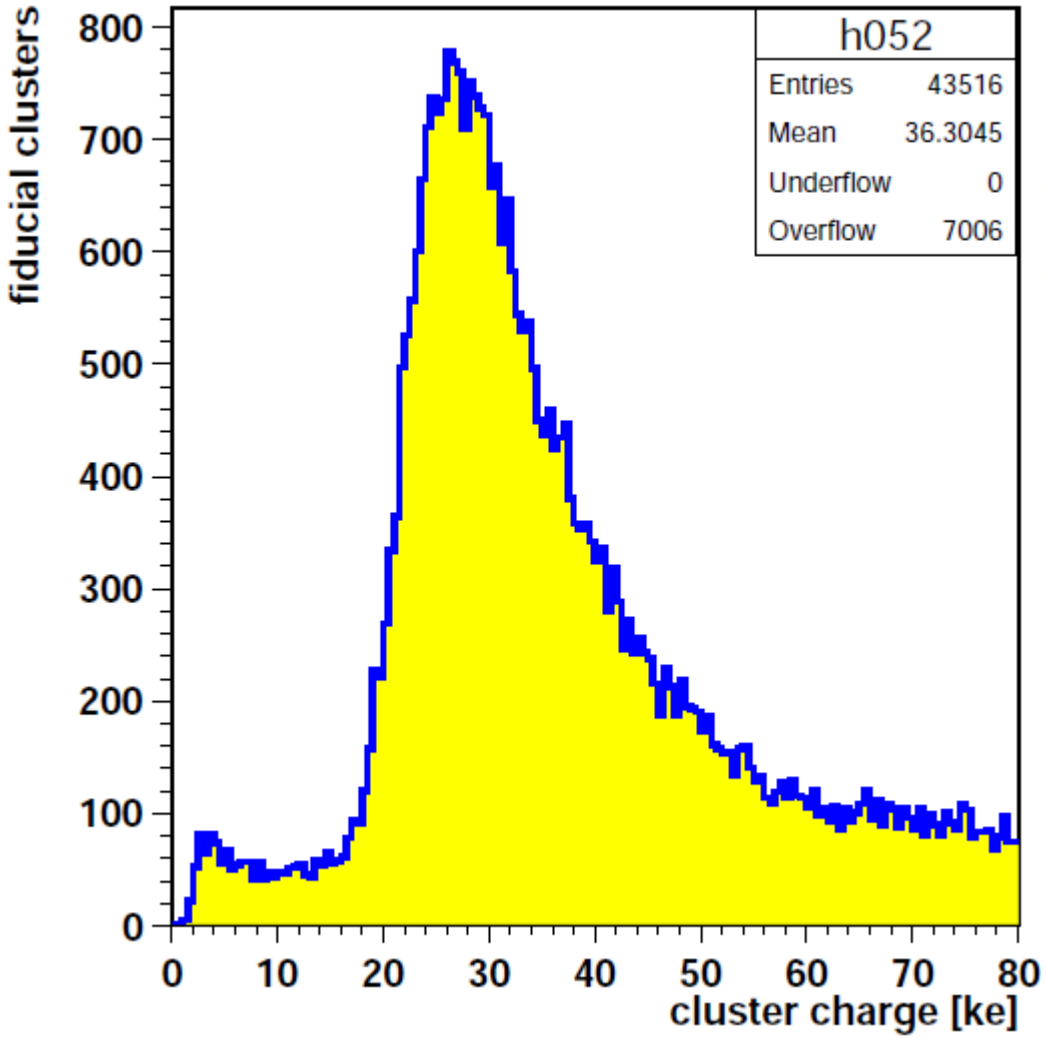
Ru source hit map



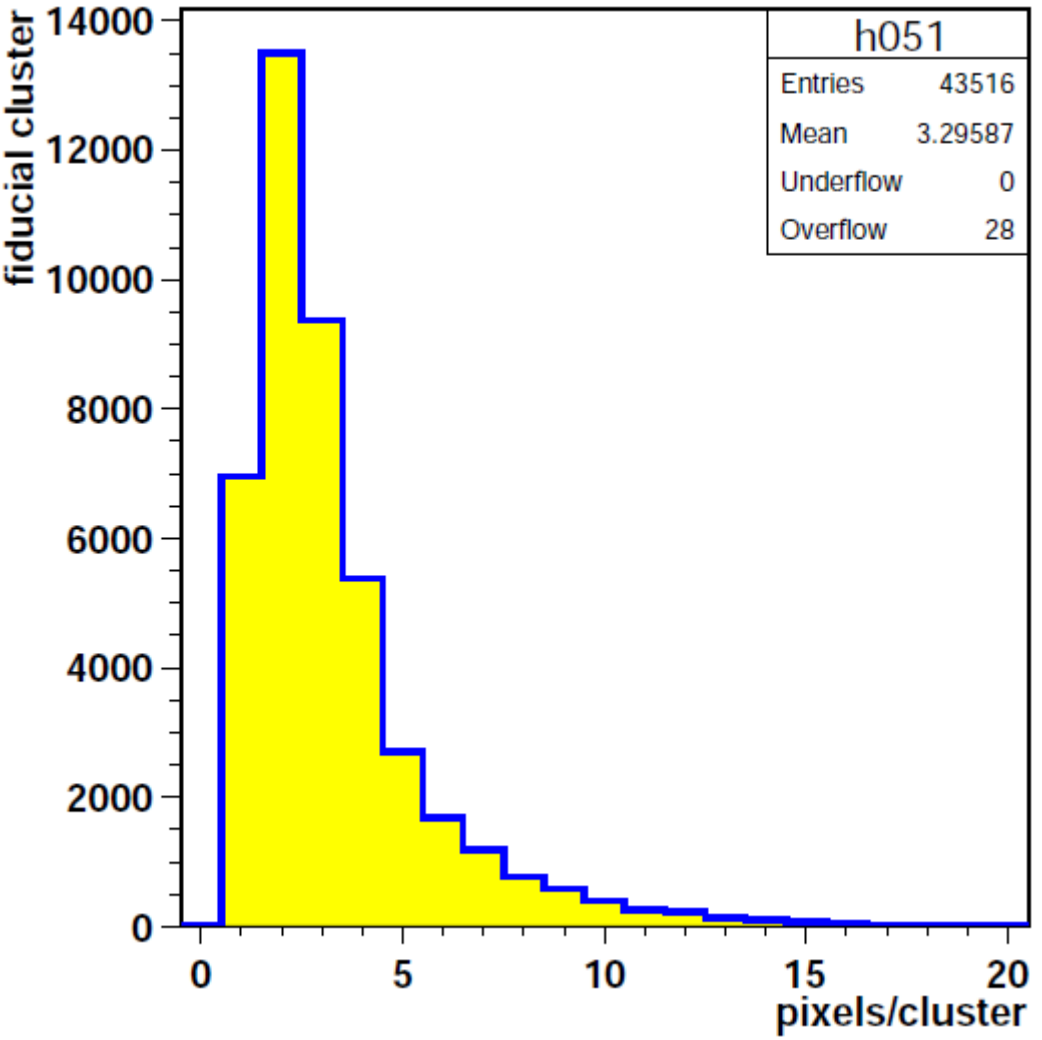
- Ru source, 300 s.
- digital chip 39
  - Ia 25 mA, trim 35
- sensor -90 V bias
- WBC 248 with tct 251
- trep 160
  - trigger rate 975 Hz
- **Clock stretch 40'000 = 1 ms**
  - 0.34 clusters/trigger

Ru source

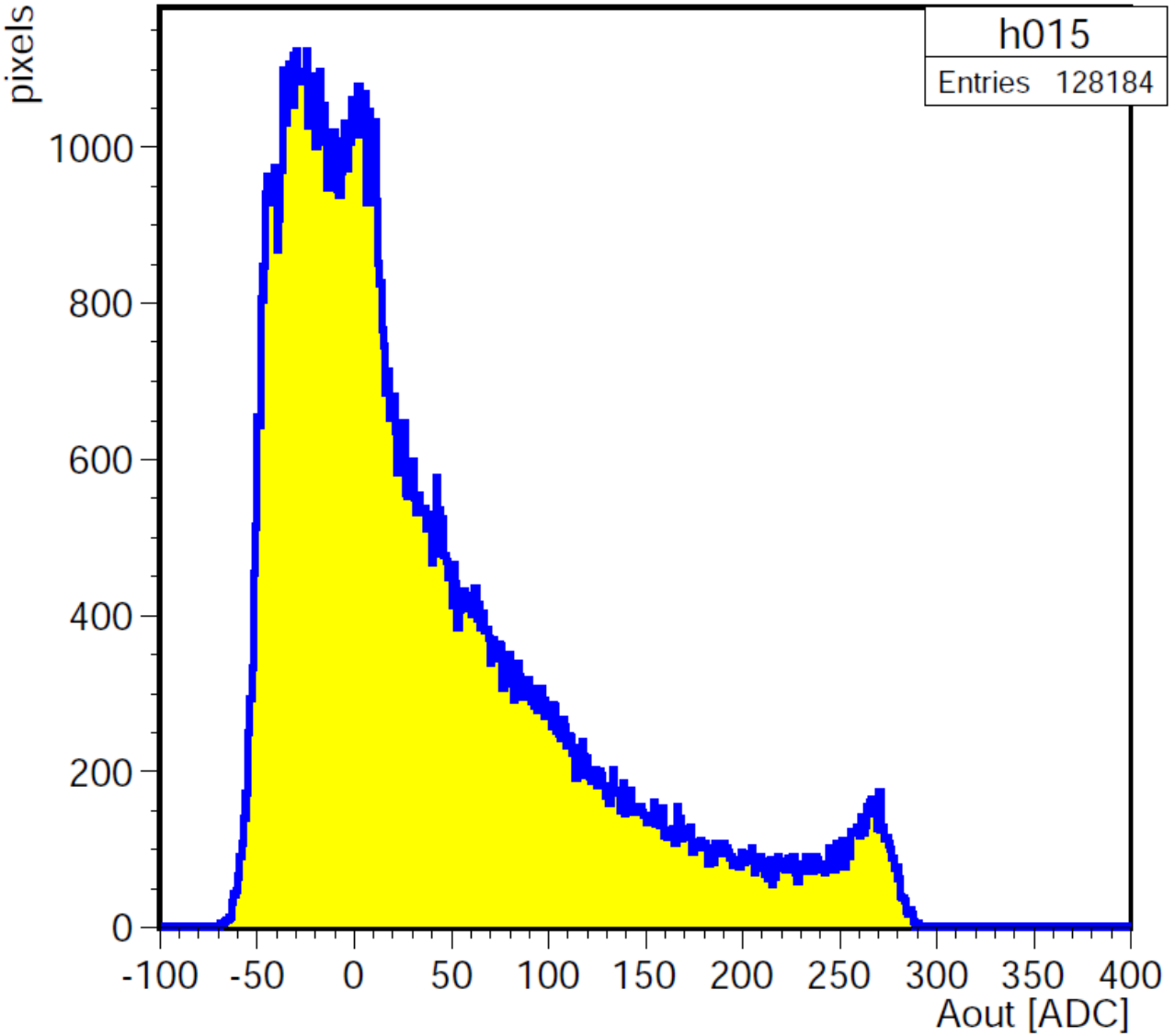
Cluster charge



Cluster size

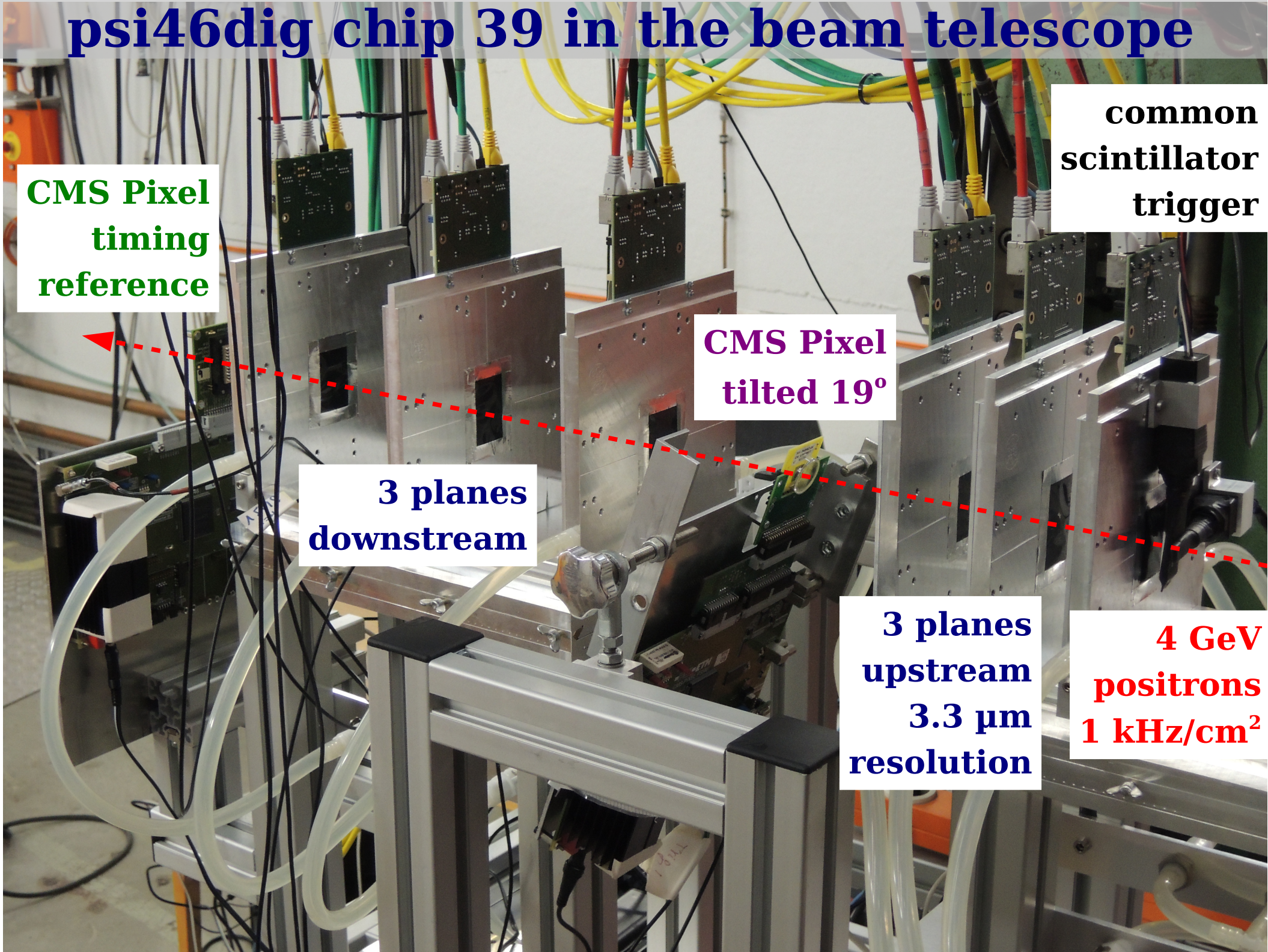


Pixel pulse height

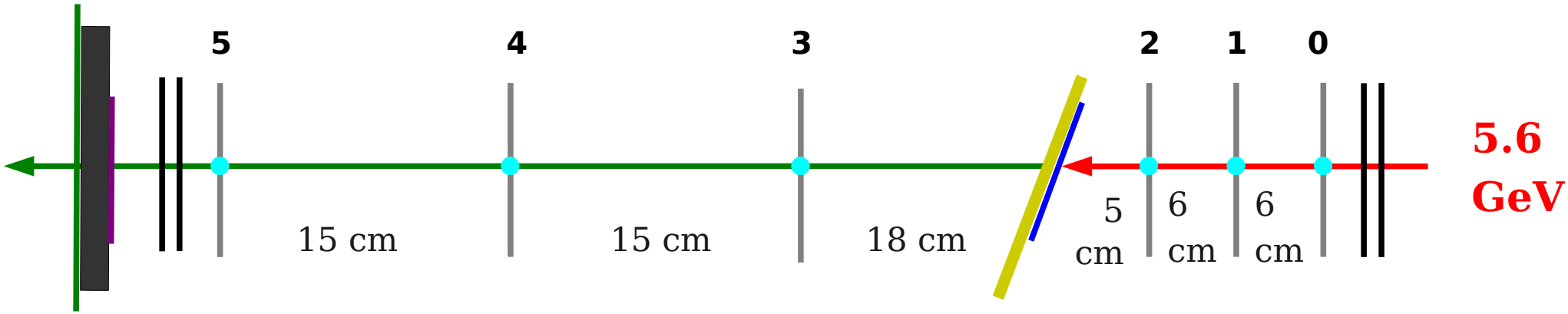


- Ru source, 10s.
- Pulse height per pixel:
  - no clustering,
  - no gain calibration.
  - ROC preamp saturation for large pulses.

psi46dig chip 39 in the beam telescope



test beam set up

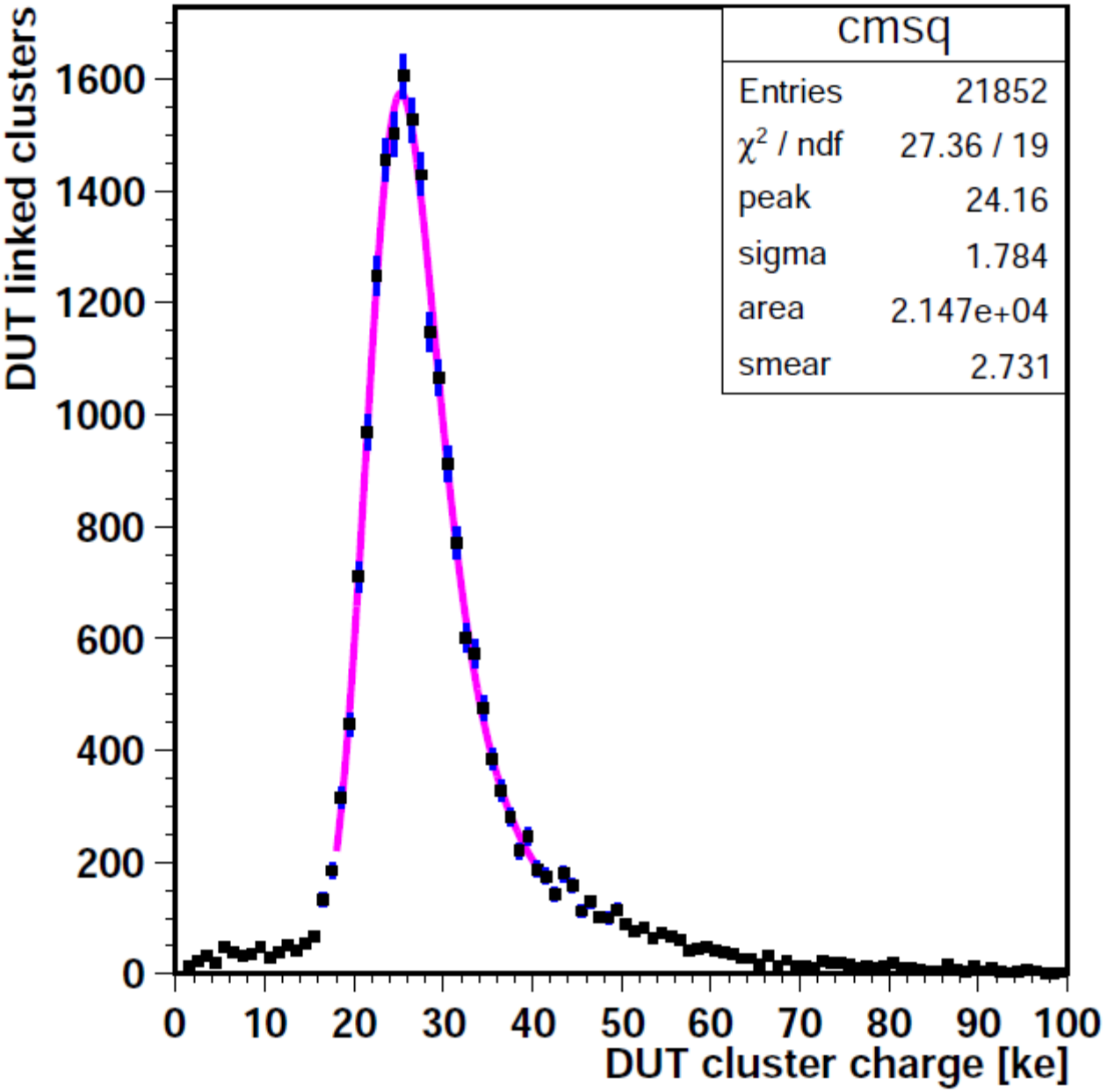


- Upstream arm 0-1-2:
  - as close as possible to DUT, but allow for tilting
- DUT = single chip module, tilted by 19°,
- Downstream arm 3-4-5:
  - equally spaced between DUT and REF
- REF = single chip module for timing, as close as possible behind scint
- trigger: 4-fold scintillator coincidence, 1×1 cm^2 area

Dec 2012 beam test

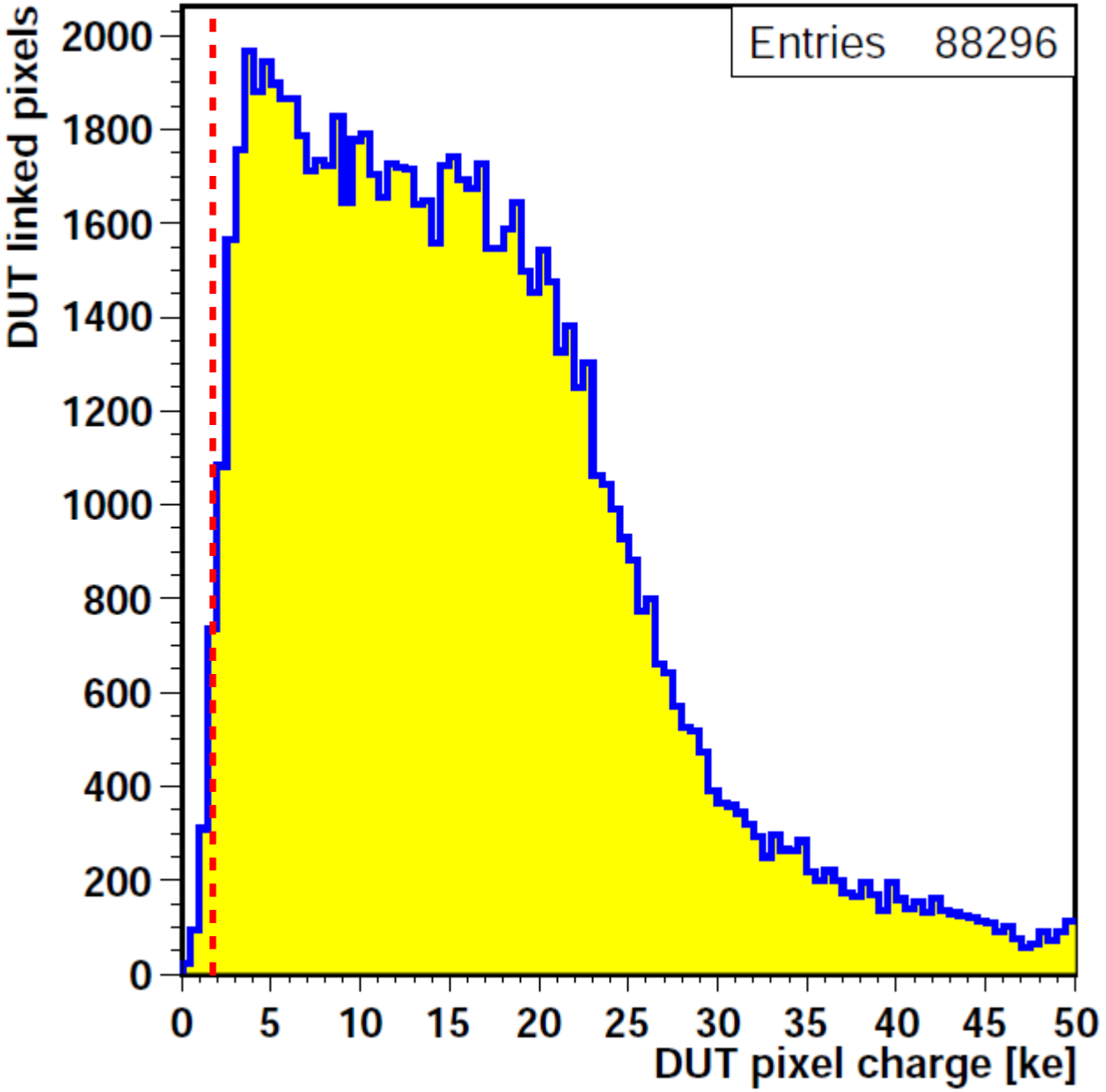
- Operate digital ROC at lower analog current:
  - Aug and Sep beam test was done at 35 mA (relict of xdb problem)
  - in CMS: 35 mA/ROC is the power supply limit
  - now: tune, trim, and operate at 25 mA (PSI default)
- Try to operate at lowest threshold:
  - trim 35 = 1.75 ke
  - trim 29 = 1.45 ke
- Use psi46dig chip 39:
  - on loan from Uni HH
- Beam conditions: difficult
  - DORIS runs for Olympus at 2 GeV topping up every 2 min
  - Olympus runs electrons every 2nd day
  - PETRA run positrons, topping up every minute
  - Low duty cycle for test beam, frequent timing jumps

Landau distribution from digital ROC



- digital chip 39
- Telescope run 5178:
  - bias -150V
  - threshold 1.75 ke
  - tilt 19°
- PH-vs-Vcal: Weibull fit, nominal gain 50e/DAC used.
- Cluster charge distribution fit by Landau ⊗ Gauss
  - peak at 24 ke as expected: gain 50 confirmed.

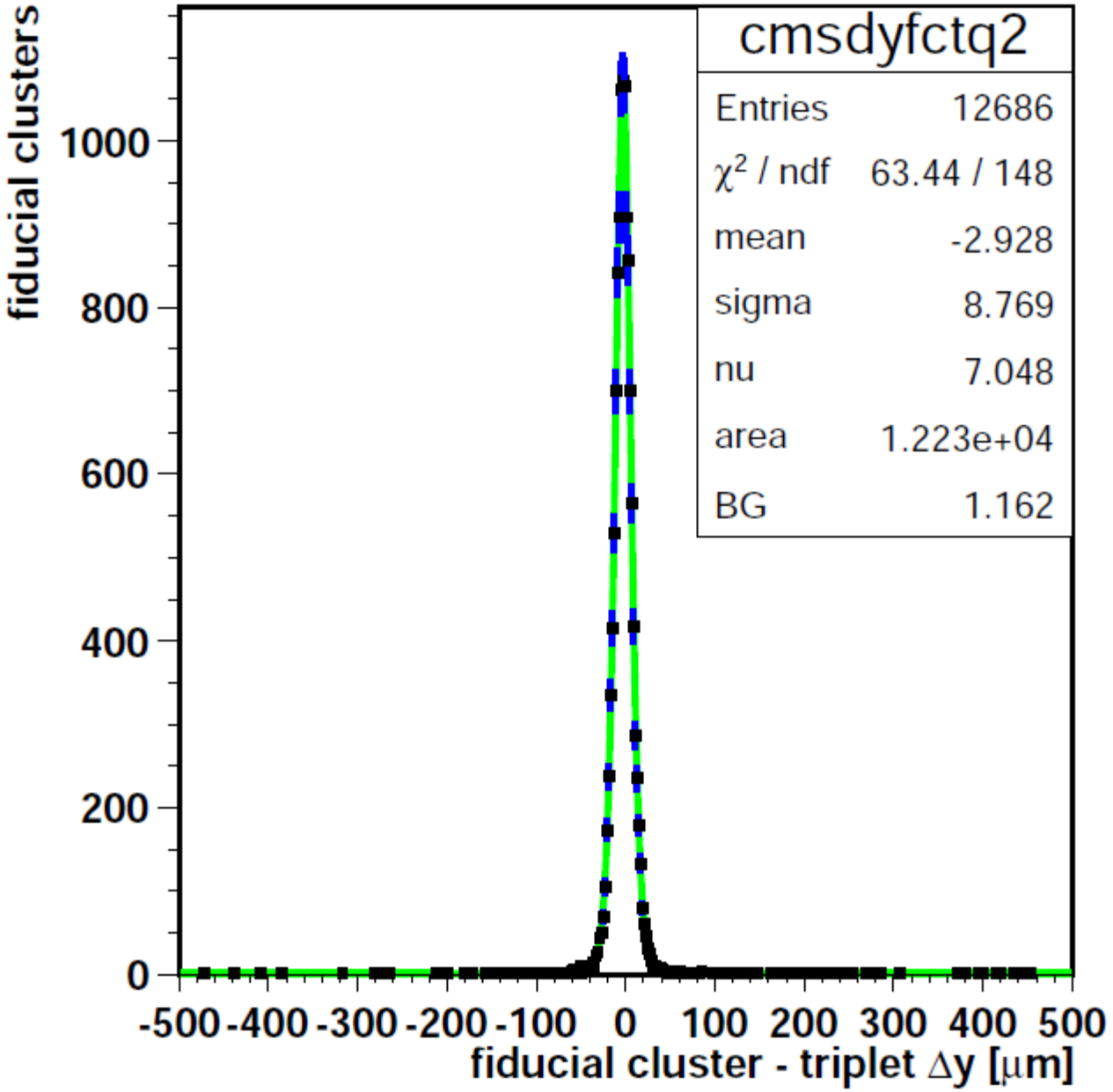
Pixel charge distribution

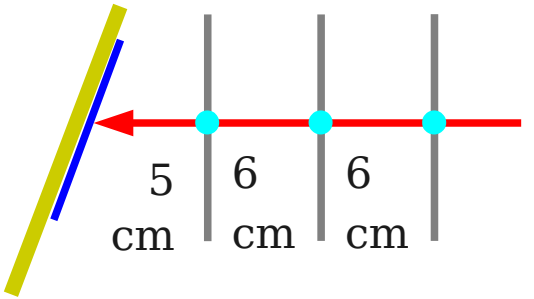


- digital chip 39
- Telescope run 5178:
  - tilt 19°
- Mostly 2-pixel clusters due to tilting
- Smallest pixel charge confirms 1.75 ke threshold trimming.

row resolution with digital ROC

dig chip39, trim 35, run 5178, 4 GeV, 19° tilt

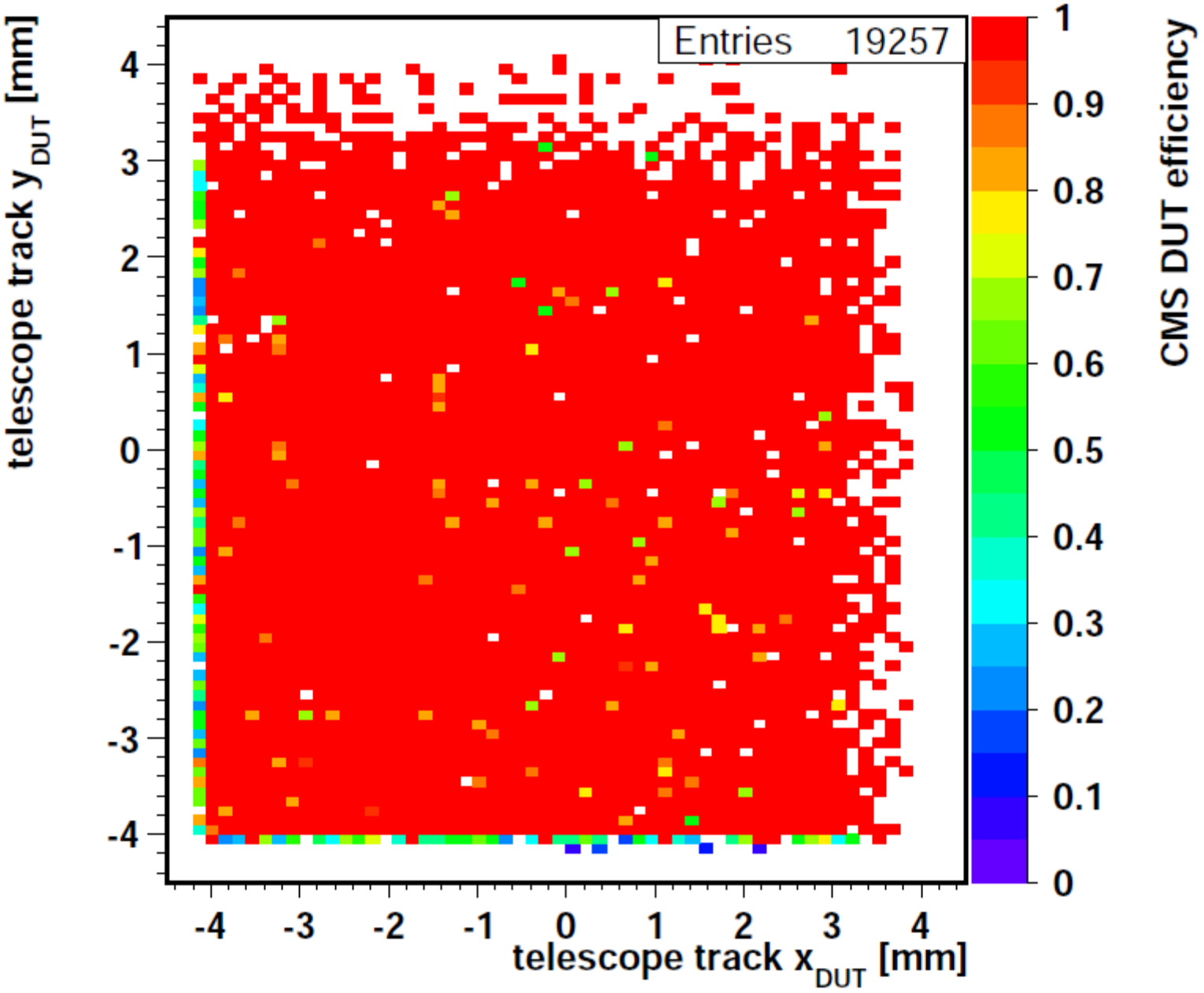




- Vertical = rows
  - CMS pixel = 100 µm.
- Residual:
  - σ = 8.8 µm,
  - telescope extrapolation: 6.3 µm,
  - **CMS pixel intrinsic resolution: 6 µm**
  - **Our best so far!**

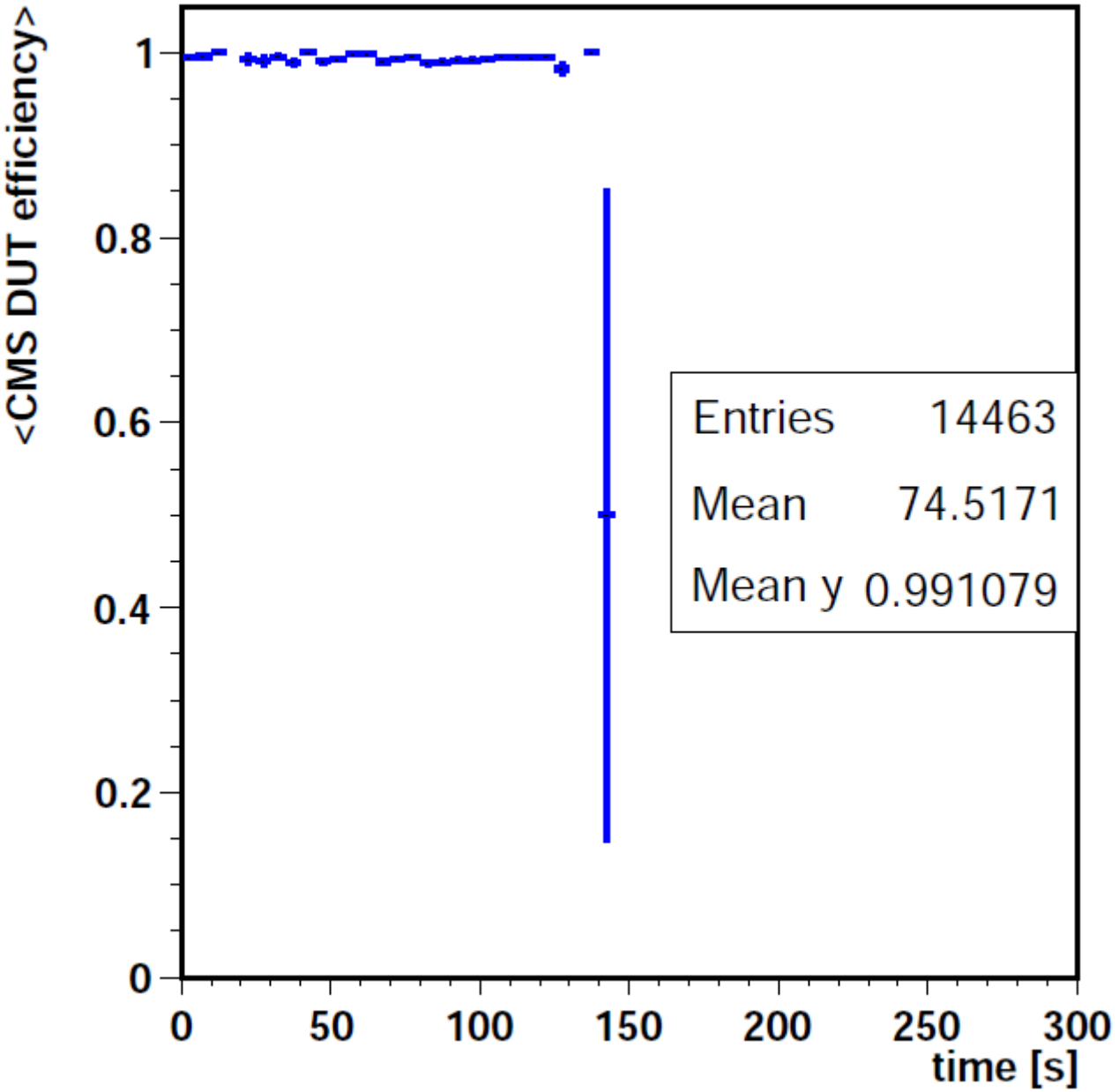
digital ROC efficiency map

eff = (dig linked clusters) / (telescope tracks with REF cluster)



- chip 39
  - I_A 25 mA
  - trim 35
- run 5178
- tilt 19°
- **99.1% in fiducial volume**
- **REF and D?UT aligmnemt not perfect**

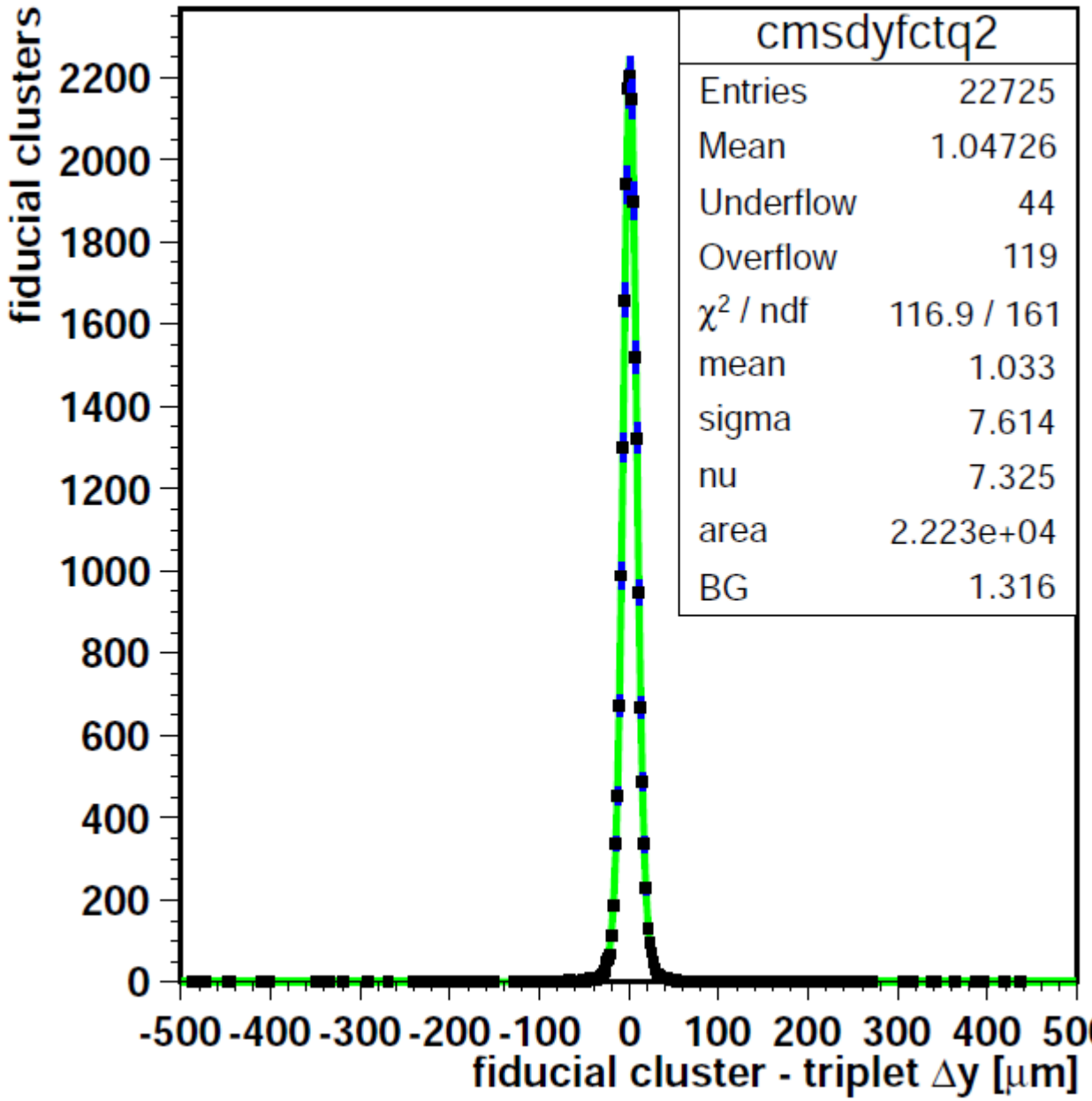
efficiency history

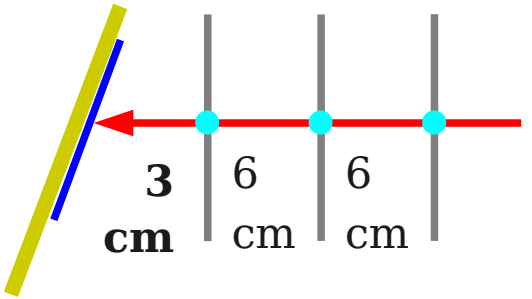


- digital chip 39
  - 19° tilt
  - trim 35 (1.75 ke)
  - run 5178
- fiducial region:
  - track 0.1 mm from edge
- 99.1% over 2 minutes
- then synchronization with telescope lost...

row resolution with digital ROC

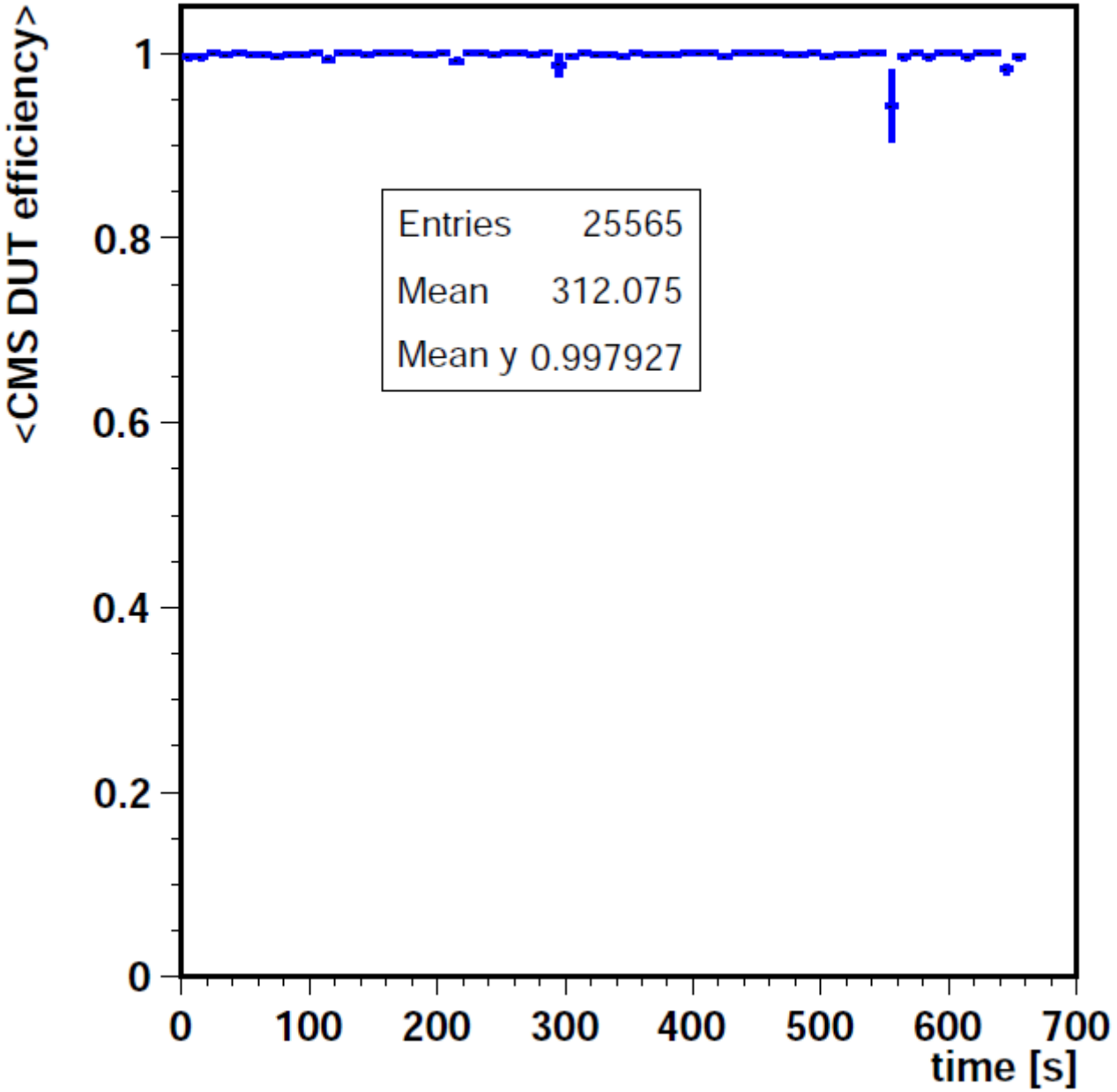
dig chip39, trim 29, run 5238, 4.4 GeV, 19° tilt





- Vertical = rows
  - CMS pixel = 100 µm.
- Residual:
  - σ = 7.6 µm,
  - telescope extrapolation: 4.8 µm,
  - **CMS pixel intrinsic resolution: 6 µm**
  - **Our best so far!**

efficiency with 1.45 ke threshold



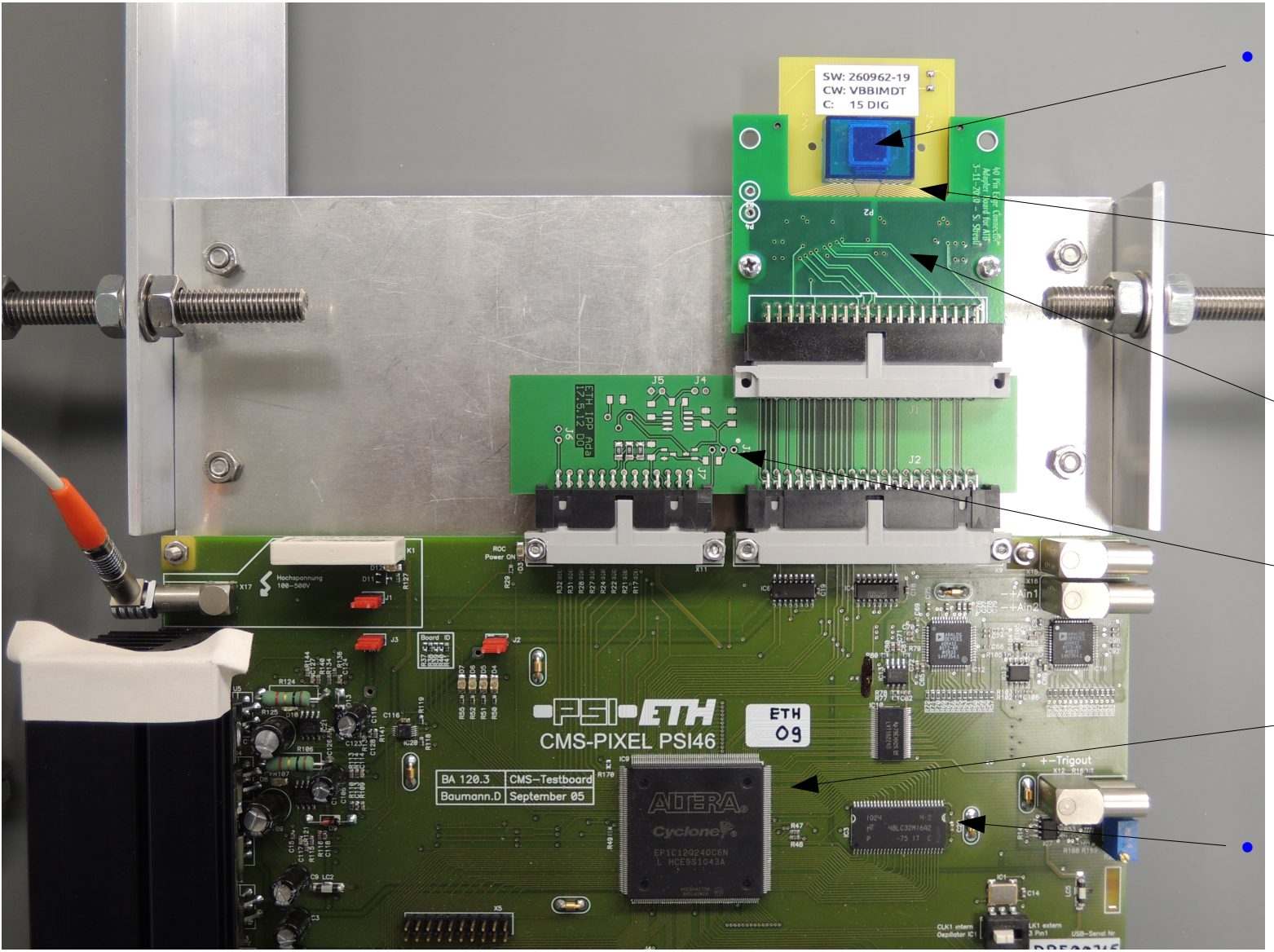
- digital chip 39
  - 19° tilt
  - **trim 29 (1.45 ke)**
  - run 5238
- fiducial region:
  - track 0.1 mm from edge
- <eff> = 99.8% over 10 minutes.

Summary

- Test pulse gain and capacitance ratios measured
  - can be used to monitoring bump bonding (height)
- Clock streetch works for the digital ROC
  - good for source tests
- Digital ROC 39 with sensor measured in the test beam:
  - tuned and trimmed for 25 mA analog current
  - threshold 1.45 ke works nicely
  - resolution is 6 µm at 19^{o} tilt: our best so far
  - efficiency 99.8%

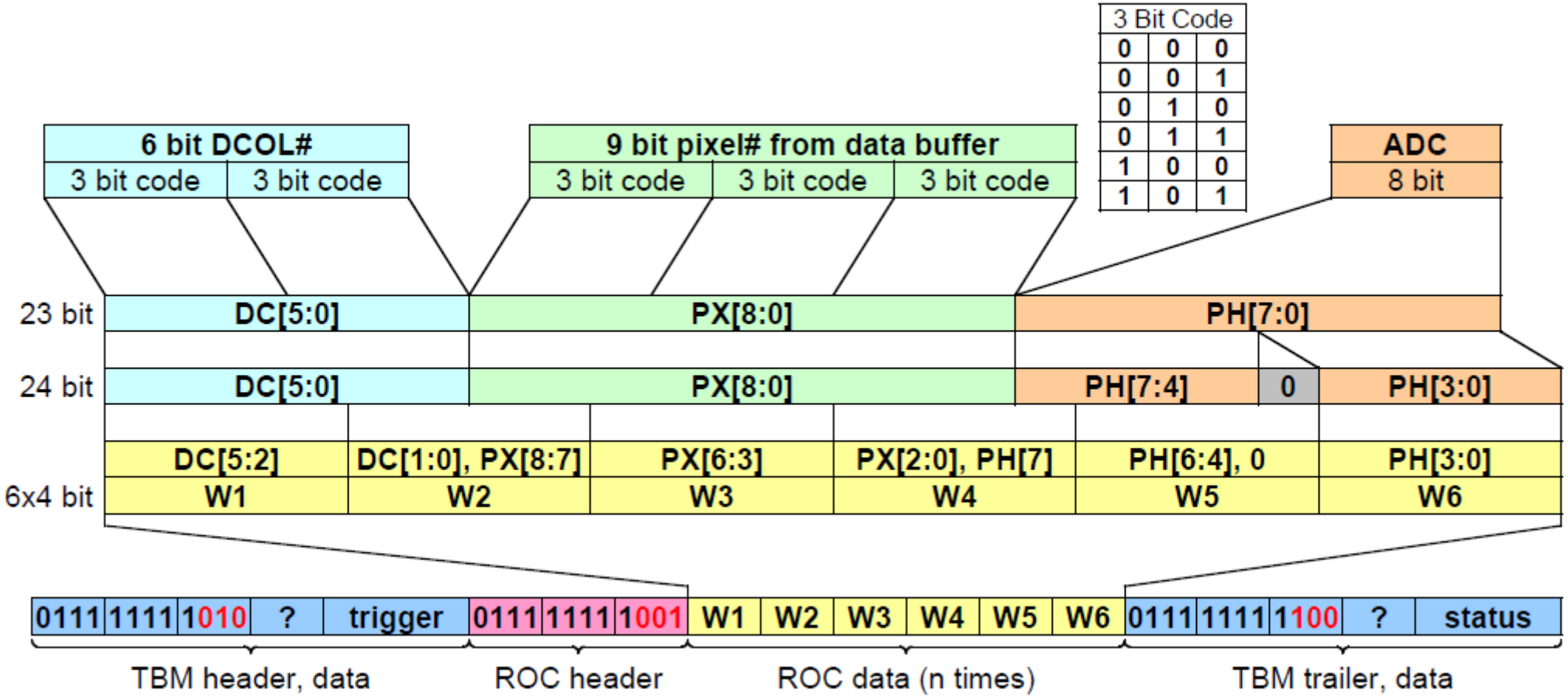
Back up

psi46 test board with digital ROC

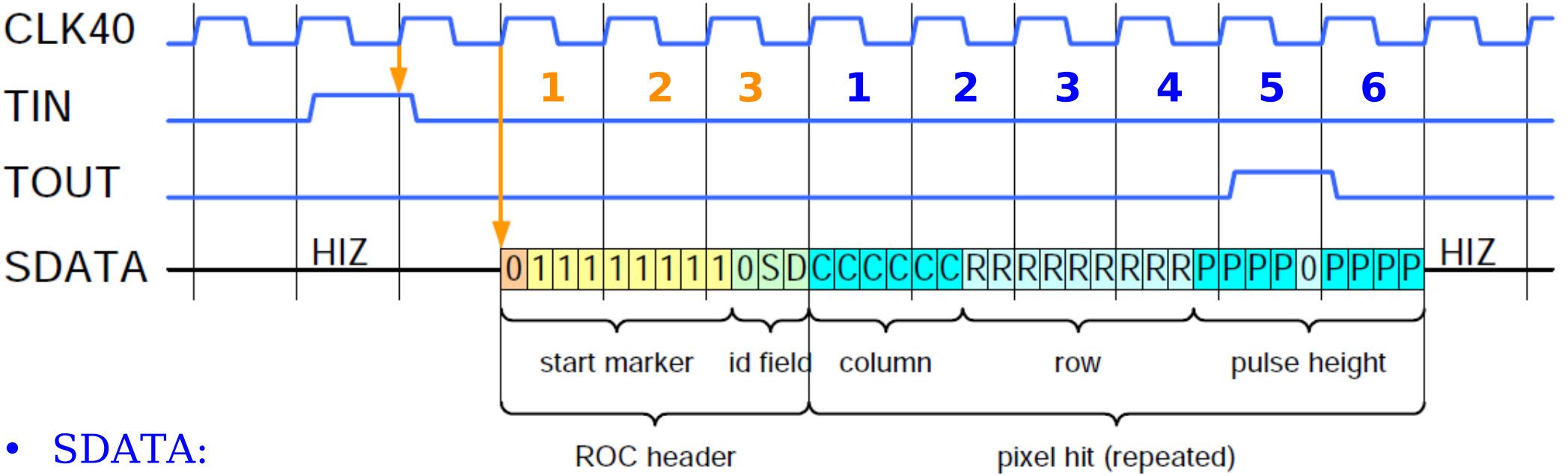


- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
  - ETH adapter card for digital 160 MHz differential signal directly into FPGA (LCDS into LVDS)
- 64 MB memory

digital ROC data format



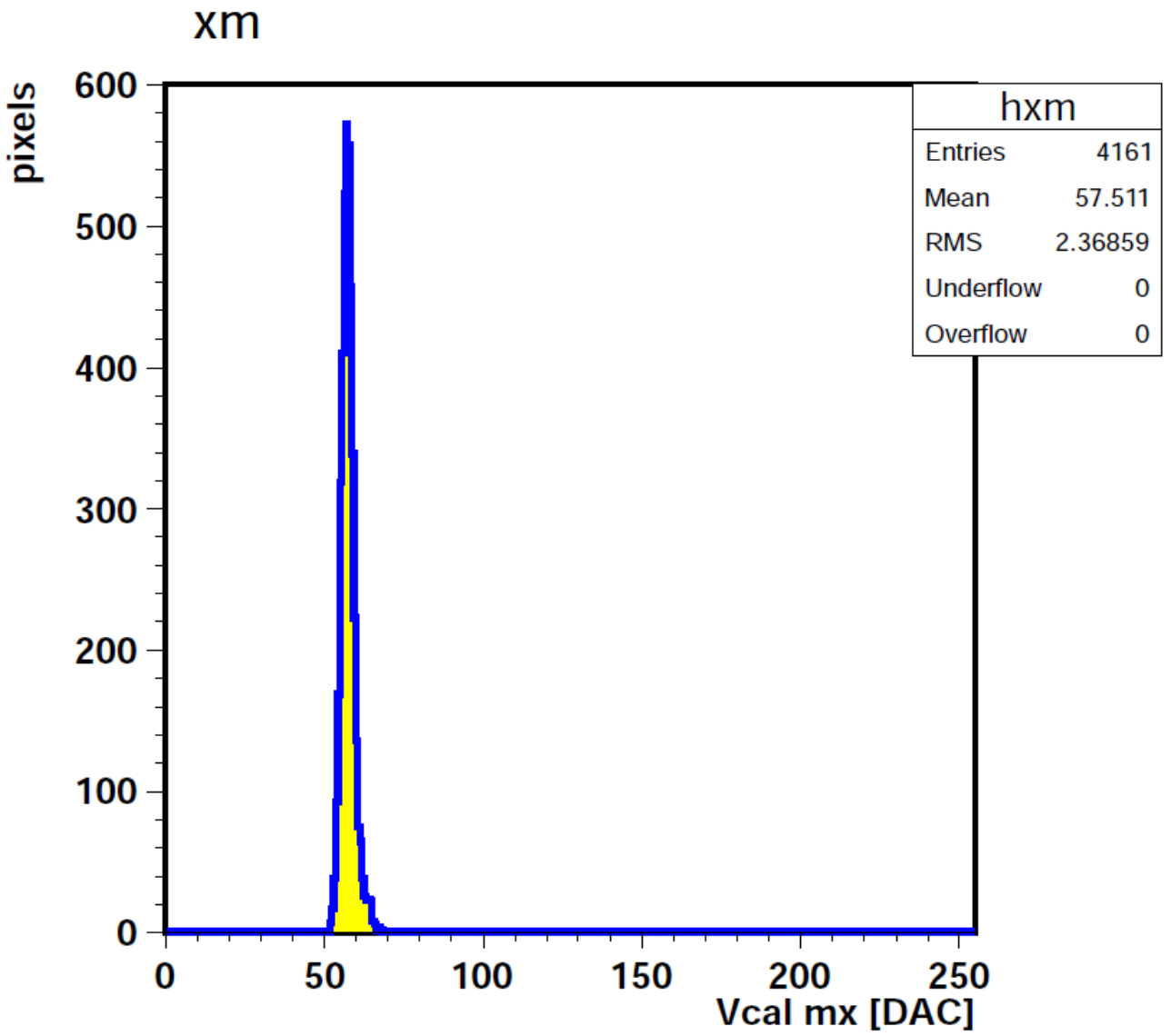
digital ROC data format



- SDATA:
  - 160 MHz
  - 4 bits per 40 MHz clock cycle
- FPGA FIFO:
  - 4 bits stored per data word (2 bytes)
  - (will be packed better on new digital tb)
- empty ROC:
  - 3 header words
- per pixel hit:
  - 6 data words

thanks to Simon Spannagel (KIT) for the digital decoder

xm distribution (Vcal CtrlReg 4)



- Digital Chip 39
  - Ia 25 mA
  - trim 29
  - with sensor, -90 V