(Virtual) Detector Laboratory

Bonn

Overall structure of the LAB

- semiconductor detectors: SiLAB
  → pixels/strips
- gas filled detectors: TPClab
  → TPC with GEMs/Micromegas/InGrid
- „spin-offs“
  → biomed, XFEL a.o.

ASIC and
electronic system dev.

Professoren/Arbeitsgruppen: Brock/Desch
Büscher/Wermes

New personnel financed by HHA

- ✓ Head of HHA Lab: Hans Krüger (1.1.2008)
- Technical Physicist (TPClab) → (1.1.2009)
- IC Designer (1.1.2008): search ongoning
- IC Designer → (1.1.2009)

Present LAB personnel (w/o CERN)

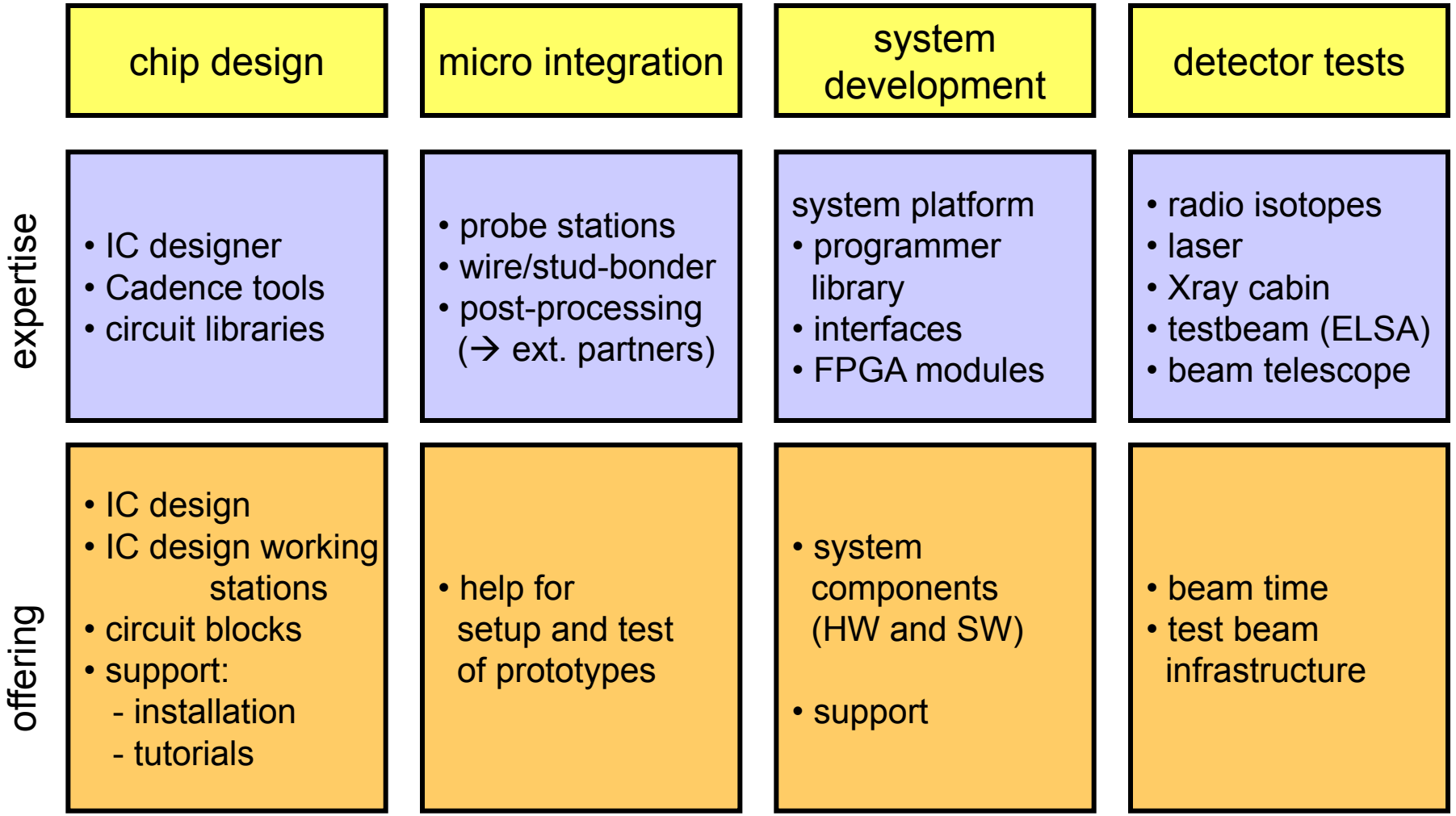
- 2 + 1 permanent scientists (H. Krüger, F. Hügging, NN_{HHA})
- 6 postdoctoral scientists
- 5.5 engineers (2.5 electronics + 3 mechanics) + 1 technician (electronics)
- 10 PhD students (CERN not counted)
- 6 diploma students + 3 FH-diploma students (el. engineering)

existing IC designers are included (→ see later)

current projects

- **sLHC** (pixel upgrade)
  - chip development
    - FE-I4
    - Chip-testsystem environment
  - new module concepts
    - include serial powering
    - new bonding and 3D integration concepts
    - new sensor materials (3D Si, pCVD und sCVD diamond)
- **DEPFET** pixels for ILC (or other?) vertex detector (GLD or SiD)
  - main focus: DEPFET - „system“, R/O, DAQ, chip and sensor tests, testbeams
- **EUDET**, involved in testbeam infrastructure for ILC detector components
- **CIX,** chip and system development for medical X-ray-imaging (Philips)
- **XFEL**, chip development for a pixel Xray-detector for XFEL experiments
- **LCTPC**/gaseous detector-development:
  - PixelTPC: prototypes for Pixel-based TPC-readout (Timepix)
  - EUDET: pixel-based GEM-module for LCTPC Large Prototype (with FR)
  - Timepix-FPGA-readout-system (with MZ)
  - Modules + electronics for LCTPC Large Prototype (with DESY, Si, Lund)
  - dev. of Timepix-successor chip + InGrid (with CERN,NIKHEF, in prep.)

for HHA: infrastructure organigram



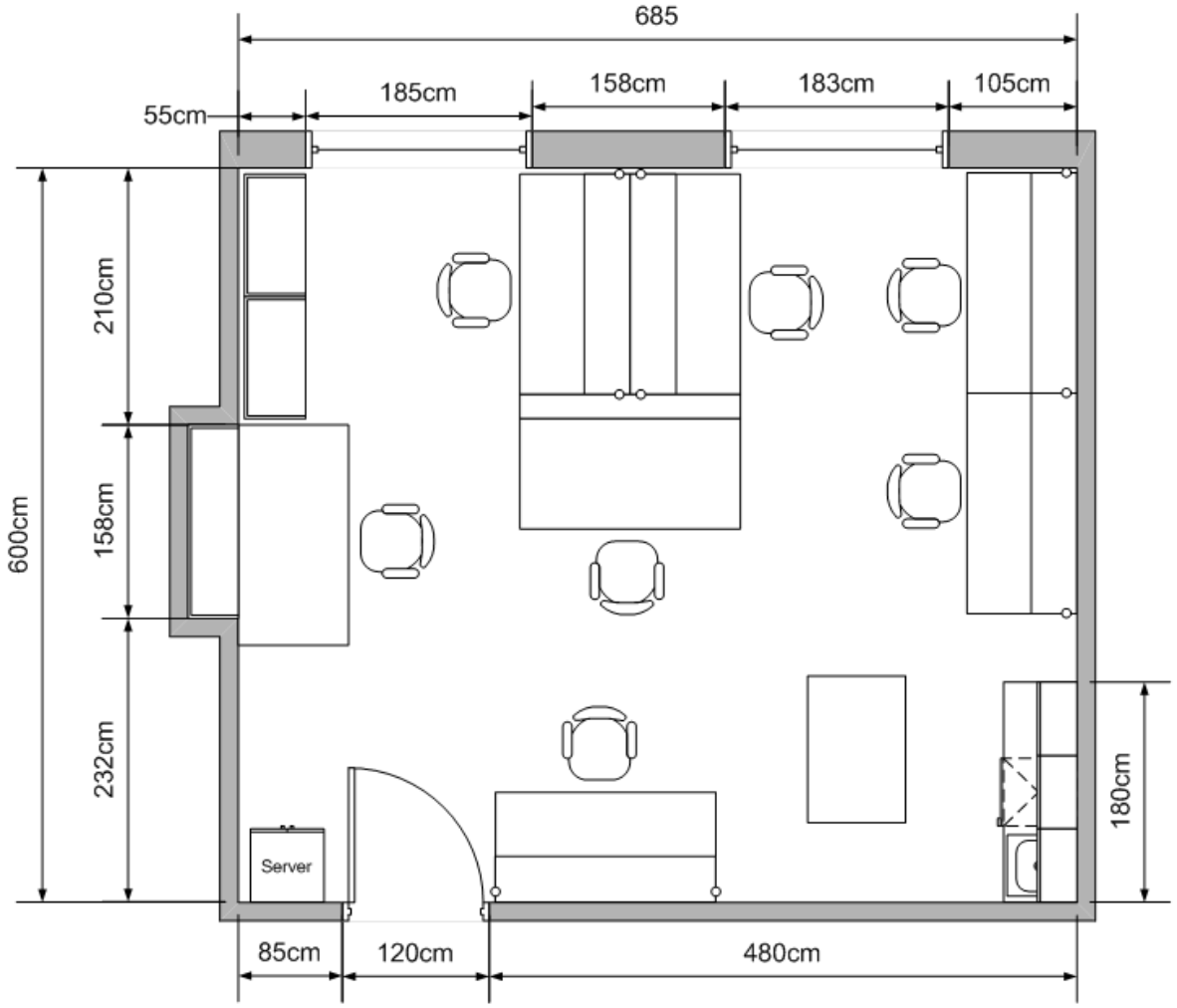
… see following slides

Status: chip design infrastructure

- 2 server LINUX/HP-UX (4 CPUs, 6 GB RAM, RAID storage)
  plus cluster of an arbitrary number of LINUX Clients
- licences
  - 7 Cadence,
  - 10 Mentor Graphics (Calibre, Eldo, Modelsim)
  - 1 Synopsys Analog Simulation & Modelling (HSPICE)
- design kits:
  - AMS 0.35µm C35B4
  - TSMC 0.25µm
  - UMC 0.18µm und 0.13µm MM/RF
  - IBM 0.25µm, 0.18µm und 0.13µm (CMRF8SF LM & DM)
- IC design personnel:
  - system administrator/designer (Michael Karagounis, sLHC)
  - 2 IC - designer / PhD students (Tomasz Hemperek[1)], Riccardo Mazzocco)
  - 3 E-Tech. FH-Studenten (6-month diploma thesis)
  - NN: IC - designer (HHA as of Q3 2008)
  - NN: IC - designer (HHA as of 1/2009)
  - 5 physicists with design background (Dr. H. Krüger, Dr. M. Barbero, M. Koch, C. Brenzina, E. Kraft)

[1)] on HHA position

Status: IC design office space



new office/lab

- 41 m^2
- 7 people
- very close to testing labs
- ready in 1 month

Note on IC designer search

2 positions (1/08 und 1/09)

- competition from industry and other labs world wide
- 1st round
  - all HEP/IC locations contacted (FNAL, LBL, PSI, CERN, IRES, …)
  - 2 excellent candidates (HEP environment)
  - top candidate → offers also from SLAC and FNAL
  - byproduct: 2 IC designers with IC background for PhD

- 2nd round has started

Status: micro integration

- contacting of chips or 1D – detectors (eg. strips)
  - ✓ 2 wire-bonders (wedge, automated, standard)

- hybrid detectors (pixel detectors)
  - ✓ solder bumping and flip-chipping (➔ IZM)
  - ✓ gold stud bumping and FC (in-house ➔ small flip-chip assemblies)
  - ✓ micro-mechanics lab with dedicated work places
  - ✓ 2 x climate chambers (e.g. → temp. cycling)

- CMOS post processing

  (in collaboration with external partners: IZM, MPI-HLL Munich)
  - → 3D-integration (through silicon vias and more …)
  - → CMOS for TPC detectors (InGrid on TimePix …)

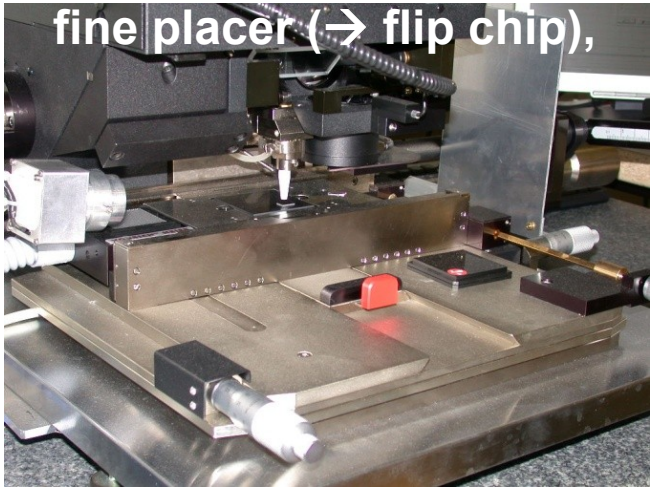
micro mechanics lab


dedicated work places

stud bonder

2 wire bonders


x1000 microscope

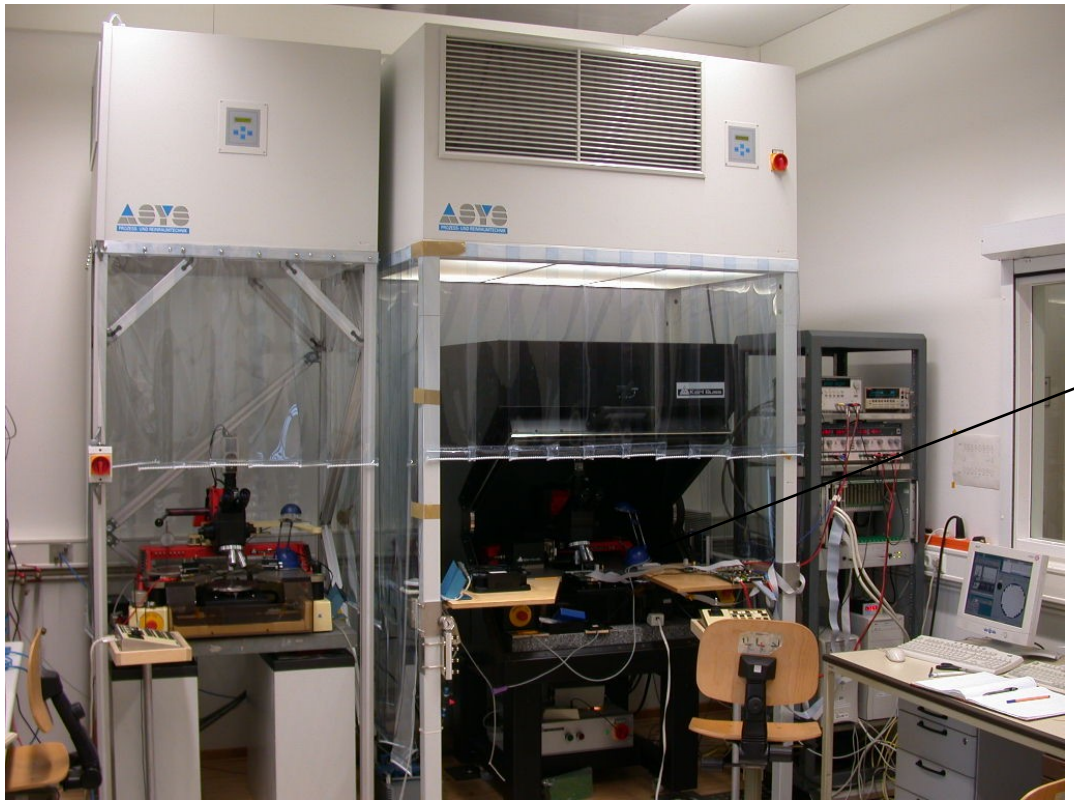

fine placer (→ flip chip),

climate chambers

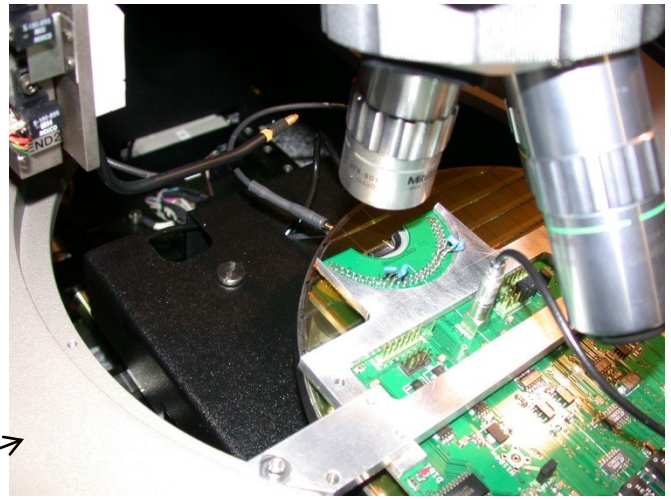
Status: testing infrastructure (chip/wafer tests)

- clean/gray room (do not want to quote a class)
- 3 x wafer-prober
  - 1 x automatic with pattern recognition → for cut wafers and chips / modules
  - 1 x automatic w/o pattern recognition → for uncut wafers / modules
  - 1 x manual → sensor tests
- several test systems for ATLAS - type chips / modules
- unique/general R/O system platform for sLHC/ILC/… pixel dev'mts

IC and wafer testing lab



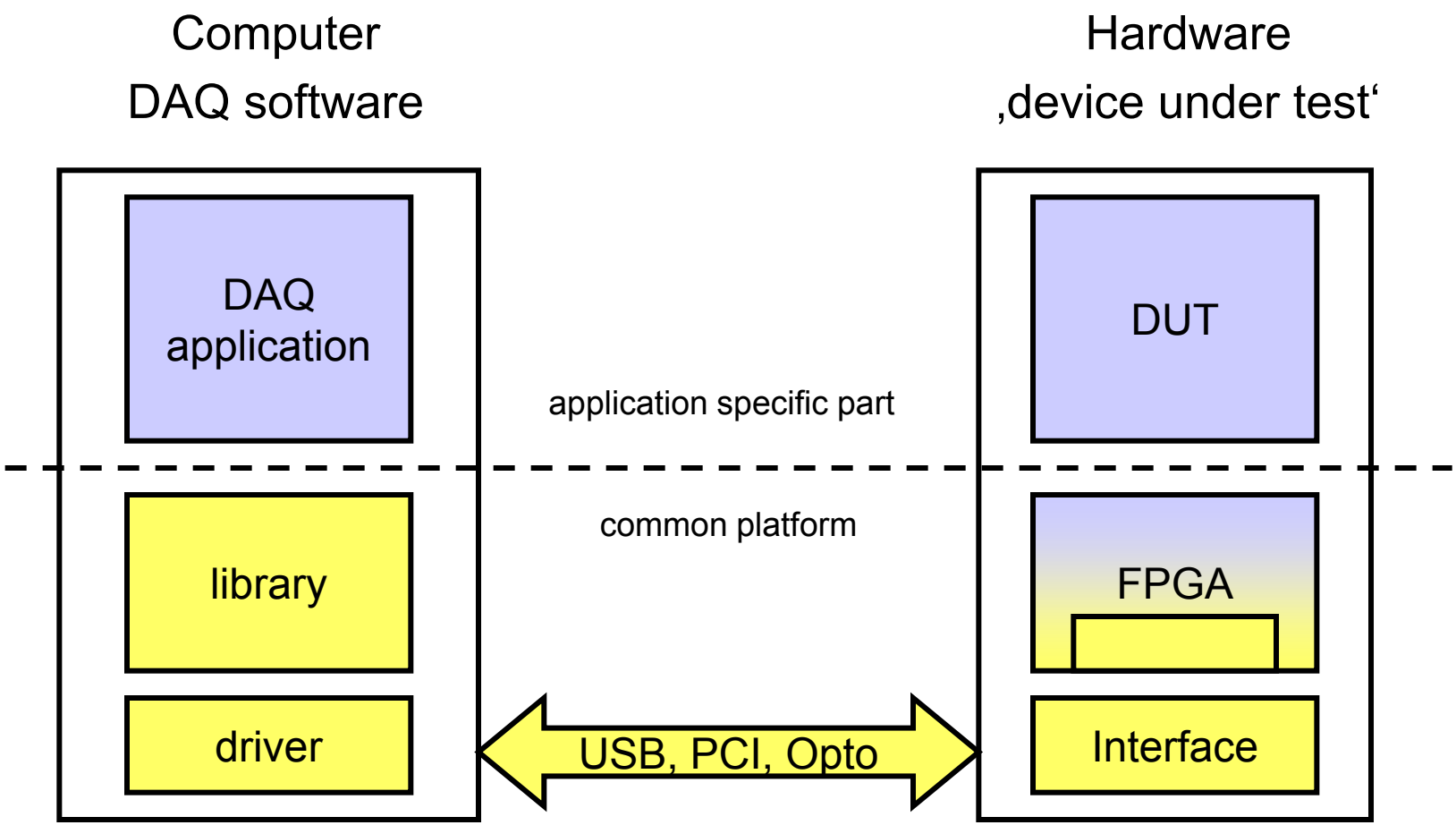
2 x automatic IC/wafer prober



manual wafer prober

system platform

A typical prototype readout/test system



Status: new system development and support

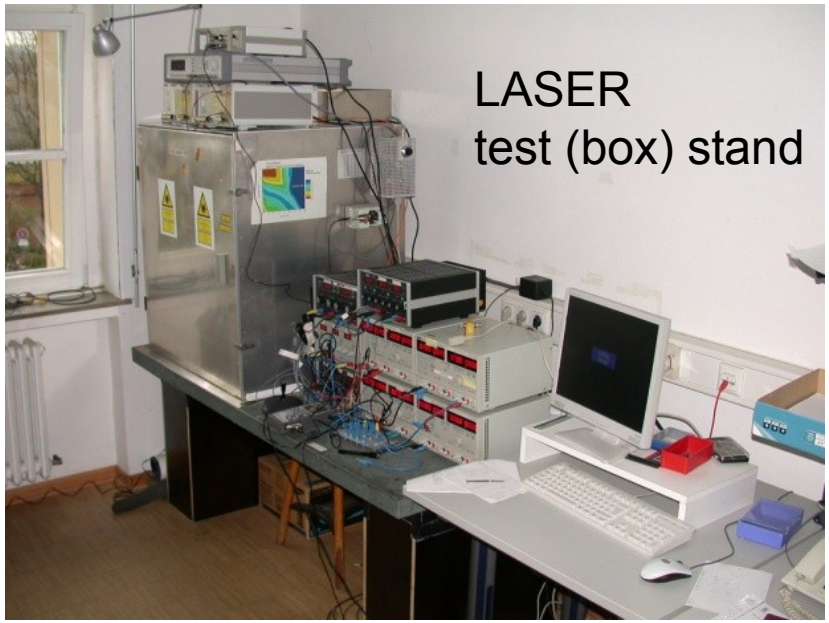
- readout system on common system platform
- many different applications
  - customers outside SiLAB:
    - ILC-DEPFET collaboration (6 institutes)
    - MPI Munich (X-ray astronomy detectors)
    - Philips Forschungslaboratorien GmbH (CiX)
    - ELSA Group (Compton-Polarimeter)
    - Crystal Barrel@ELSA (Photon-Polarimeter with ATLAS pixel detectors)
    - TimePix test system (Uni Mainz)

- HHA: access to system components
  - ✓ software (use version control system)
  - ✓ hardware (working components and design documentation)
  - ✓ support/advice

Status: infrastructure for tests of detectors

- Lab –testing possibilities

  - ✓ radioactive isotopes („alle gängigen und andere“)
  - ✓ laser (630 nm, 822 nm, 1060 nm) test stand
  - ✓ X-ray cabin (100 kV)



Status: infrastructure gaseous detectors

- operating Lab
  for gaseous detector development

- flexible cascaded HV-supply for MPGDs
- flexible gas-system (mixtures of 3 components)
- test stand with cosmic trigger
- pad-R/O electonics (ALTRO) 256 chan.
- Timepix R/O system
- test chamber for LCTPC-LP-modules
- laminar-flow box for MPGD-handling

- in preparation
  - gas-analysis
  - UV-laser-test-stand

Status: test beam infrastructure @ ELSA

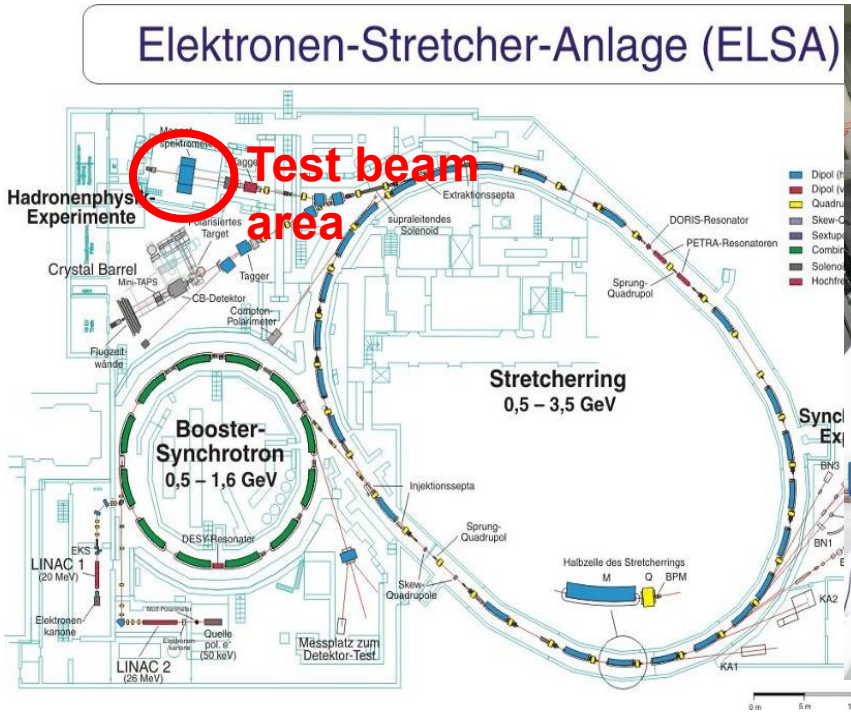
- (quasi) existing: photon test beam
  - ~cw (duty cycle ~50-80%)
  - tagging rate ~ 1 MHz
  - 1 - 3.3 GeV

- in 2008: irradiation at LINAC I with ~20 MeV electrons (pulsed)
  - 400 mA
  - 50 Hz, pulse length 1 µs

- planned (2008 ?): direct electron beam (up to 3.5 GeV)

→ 1. customer: Jenny List, Emmy-Noether Group/HH
for ILC polarimetry detector

Status: infrastructure test beam @ ELSA (3.5 GeV e^-)



Status: other test beam infrastructure

→ micro strip telescope (BAT, ~6 µm) → upgrade needed or …

→ EUDET - telescope ?

✓ experience with EUDET telescope integration (SW und HW)

✓ DEPFET telescope (3x3 mm^2 sensor area, ~2µm resolution)

→ project: new DEPFET telescope with large matrices (2010)

Chip design infrastructure – „Perspektivendiskussion“

- Angebot von Chipdesign-Arbeitsplätzen im HHA-Labor
  - ✓ Rechner-Hardware
  - ✓ Büro/Laborraum

- Support für externe Chipdesign-Arbeitsplätze
  - ✓ Zugriff auf „Standard“-Cadence/Design-Kit Installation (LINUX)
  - ✗ Remote-Administration ➔ zu aufwändig

- Entwicklung von Chips/Standard-Designblöcken
  - ✗ Entwurf und Entwicklung kompletter Chips auf Anfrage
  - → I/O Pads, DACs, ADCs, BG-Referenz, …
    → in einer Technologie → IBM CMRF8SF 130 nm)

- Training
  - → Benutzung von Cadence-Tools ➔ Entwicklung von Tutorials
  - ✗ Chipdesign-Training ➔ nein: externe Chipdesign-Kurse benutzen