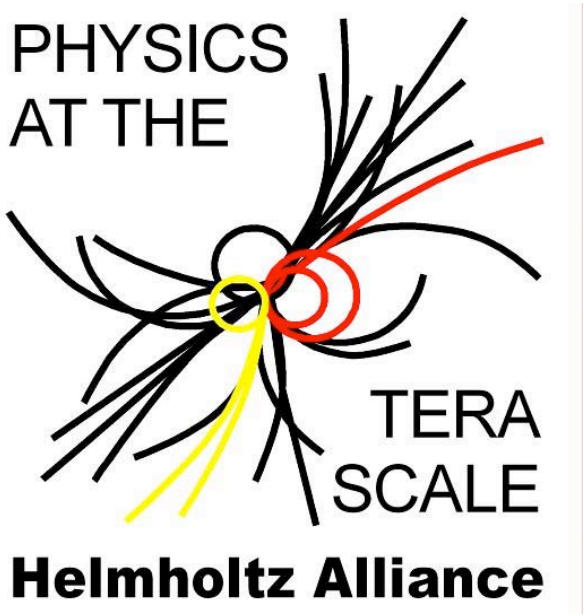
Status of VLDT Nodes Heidelberg Report

Karlheinz Meier

- Goals
- Existing Infrastructure
- Planned Developments 2008
- Current Projects



WP 1 The Virtual Laboratory for Detector Technologies

A central part of the Alliance is the formation of a Virtual Laboratory for Detector Technologies, called VLDT in the following. This laboratory will form the backbone of a network of the alliance partners formed to ensure a visible, efficient and long-lasting contribution of German groups to the future projects ILC and sLHC. The VLDT will develop, provide and maintain infrastructures and make them available to the Alliance. It will have three branches, electronics system development, sensor development and general detector test facilities. The central nodes of the VLDT will be DESY, the University of Bonn and the University of Heidelberg. Additional infrastructure will be made available to the Alliance by Aachen, Hamburg and Karlsruhe. As the project develops other institute might contribute infrastructure as well. All Alliance partners involved in detector design and construction will profit from the VLDT.

WP 1.1 The Electronics System Development Laboratory

HD Contribution :

KIRCHHOFF-
INSTITUT
FÜR PHYSIK

Within the Helmholtz Alliance Initiative the Heidelberg group plans to upgrade its research and development facilities in order to extend training and support to the German particle physics community. For that purpose it is planned to acquire laboratory (clean-room) workbenches including measurement equipment for five guest users, and to set up ten additional chip design and simulation workstations.

Basis : ASIC Laboratory for Microlectronics Heidelberg

- Established 1994
- Hosted by Kirchhoff-Institut für Physik
- Jointly supported by Kirchhof-Institut, Max-Planck Institut für Kernphysik, Physikalisches Institut
- Support Lab for Particle / Nuclear / Cosmic and Biophysics
- Contributions to HERA-B, HERMES, H1, ZEUS, ATLAS, LHC-b, ALICE, HEGRA, HESS, GERDA
- Current full staff : SW Engineer, Lab Engineer
- Related activities : Technical Informatics (KIP), Technical Informatics (ZITI, former Mannheim Group), International Graduate School on Intelligent Detetctors
- TASKS : ASIC / FPGA Design, Test, System Design, Simulation

Support offered to Users

- Access to Lab Equipment and S/W Tools
- Instrumentation Tutorials (Testing, Bonding, Packaging)
- Software Support (Layout, Simulation)
- Submission Support (MPW, Engineering Runs, Full Runs)
- Submission Readiness Reviews
- ASIC Designer Style Guides
- Online Tutorials

Software and Design Suites available

Mentor

22 Licences of complete Mentor EDA Suite
Supported use : DRC, LVS, LPE (Layout Parasitic Extraction) Tools, FPGA Programs

Cadence

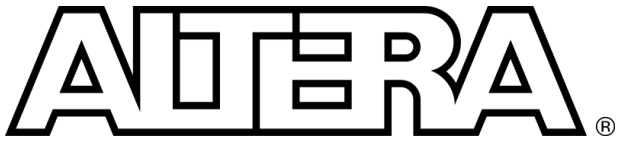
35 Licences
Supported use : Board-Layout, Chip-Layout, Simulation, Verification

Synopsys

40 Lizenzen
Supported use : Synthesis, Timingextraction, Poweranalysis

Software and Design Suites available (cont'd)

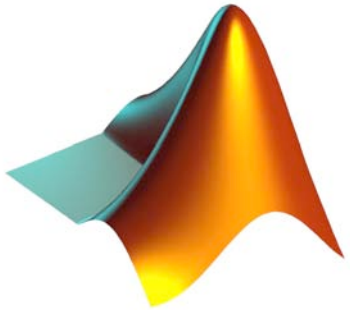
Altera
7 Licenses, FPGA



Xilinx
Institute wide Licenses

ModelSim
22 Licenses, Simulation Tool

Matlab
44 full Licences
Toolboxes:
10xSignalToolbox
2xNeural Network Toolbox
10xCurve Fitting Toolbox
10xStatisticsToolbox



Computer Hardware and Access Policies

2 SunFire 280
approx. 10 SunBlades
1 Quad DualCore AMD
1 DualCore AMD
1 DualCore Intel
1 Double DualCore Intel

Remote access for ASIC lab members and registered guest users via Portal Server :

portal.kip.uni-heidelberg.de

Running local NXClient, SGD (Sun Secure Desktop) or SSH

Selected project partners with increased access needs : VPN Access

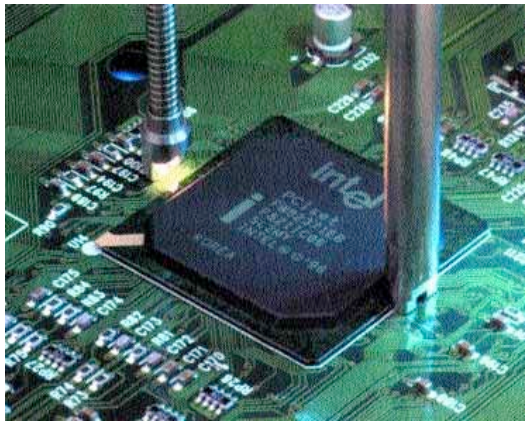
DIFFEENT ACCESS RIGHTS DEFINED BY SOFTWARE VENDORS

Laboratory : Examples for E-Measuring Equipment

Scopes	up to 2,5 GHz, 20 GS/s
Probes	up to 4 GHz, 3.5 GHz differential
LA Systems	16517A, up to 102 Channels
AWG	up to 1GSa/s 500Mh
Net./Sp. Analyzer	100kHz-1.8GHz
Param. Analyzer	1fA-100mA, 1uV-100V

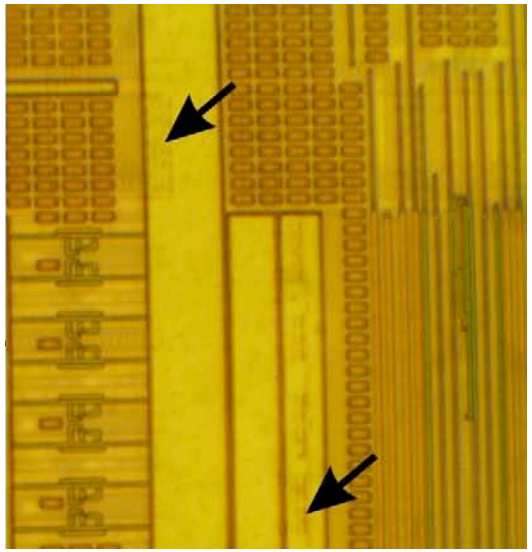
Equipment database and internal loan system :
http://www.kip.uni-heidelberg.de/~dorn/messdb/

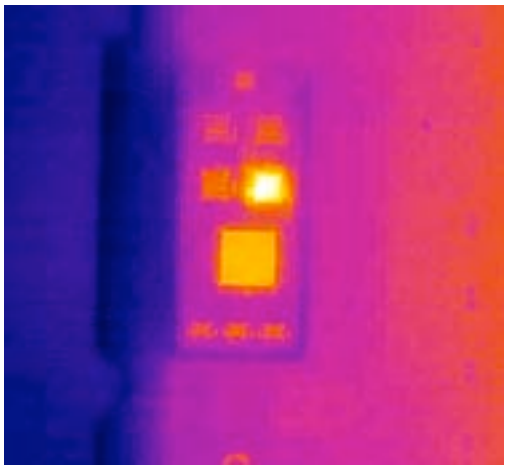
Optical Inspection Facilities



ERSA Scope optical Sub-BGA / Connector inspection system

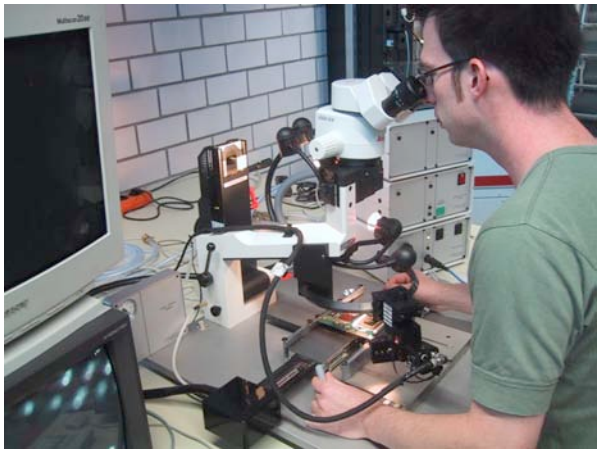
Microscopy, production fault analysis





IR Imaging, localisation of power dissipation (100 μm)

Placing / Soldering



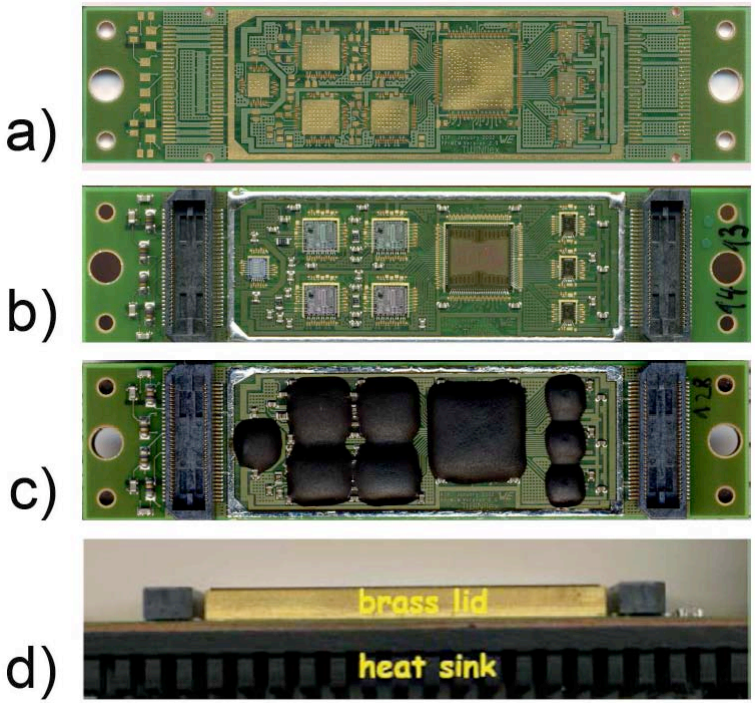
200 deg. Teflon gas soldering (9U board size)

Fine Pitch BGA placing / soldering / unsoldering / re-balling

Semi-automatic SMD placing / soldering

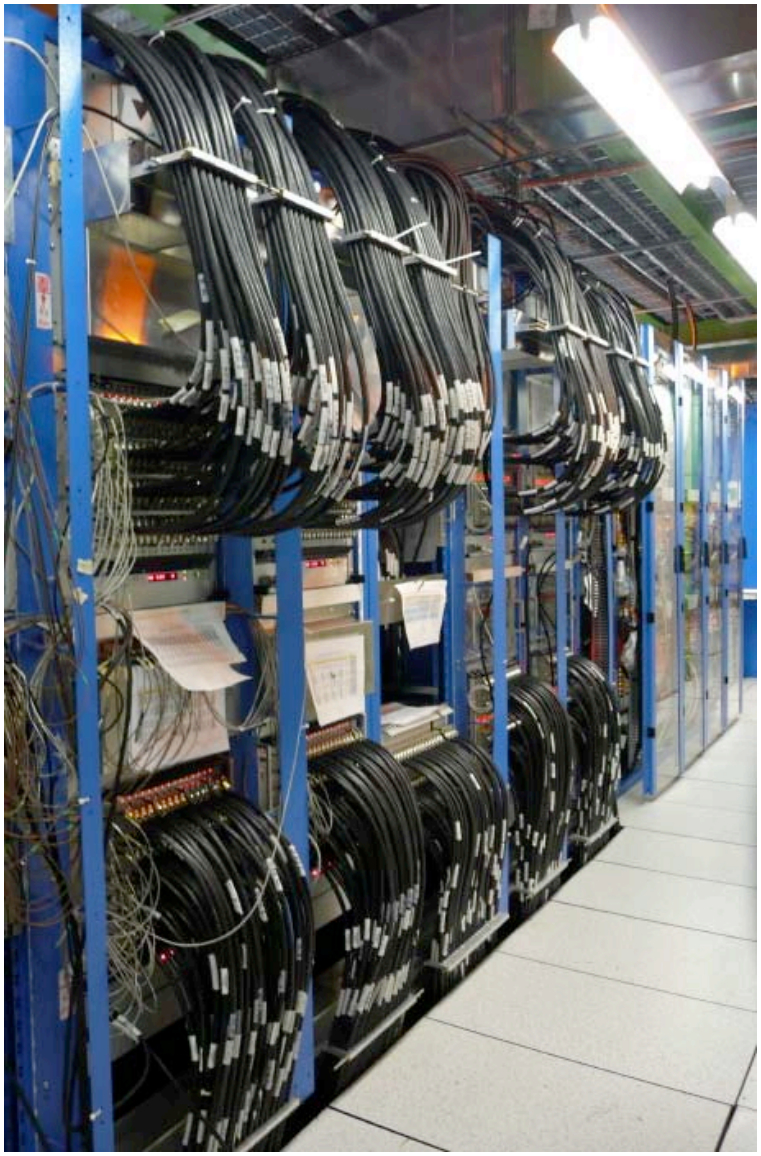
Clean Room : Test / Mounting / Storage

- 30 m^2 , approx. Class 10.000
- Probers : Suess PM5, Suess PA200
- Bonders : Delvotek 6400, MEI 1204
- Long Term N_2 Storage Facilities

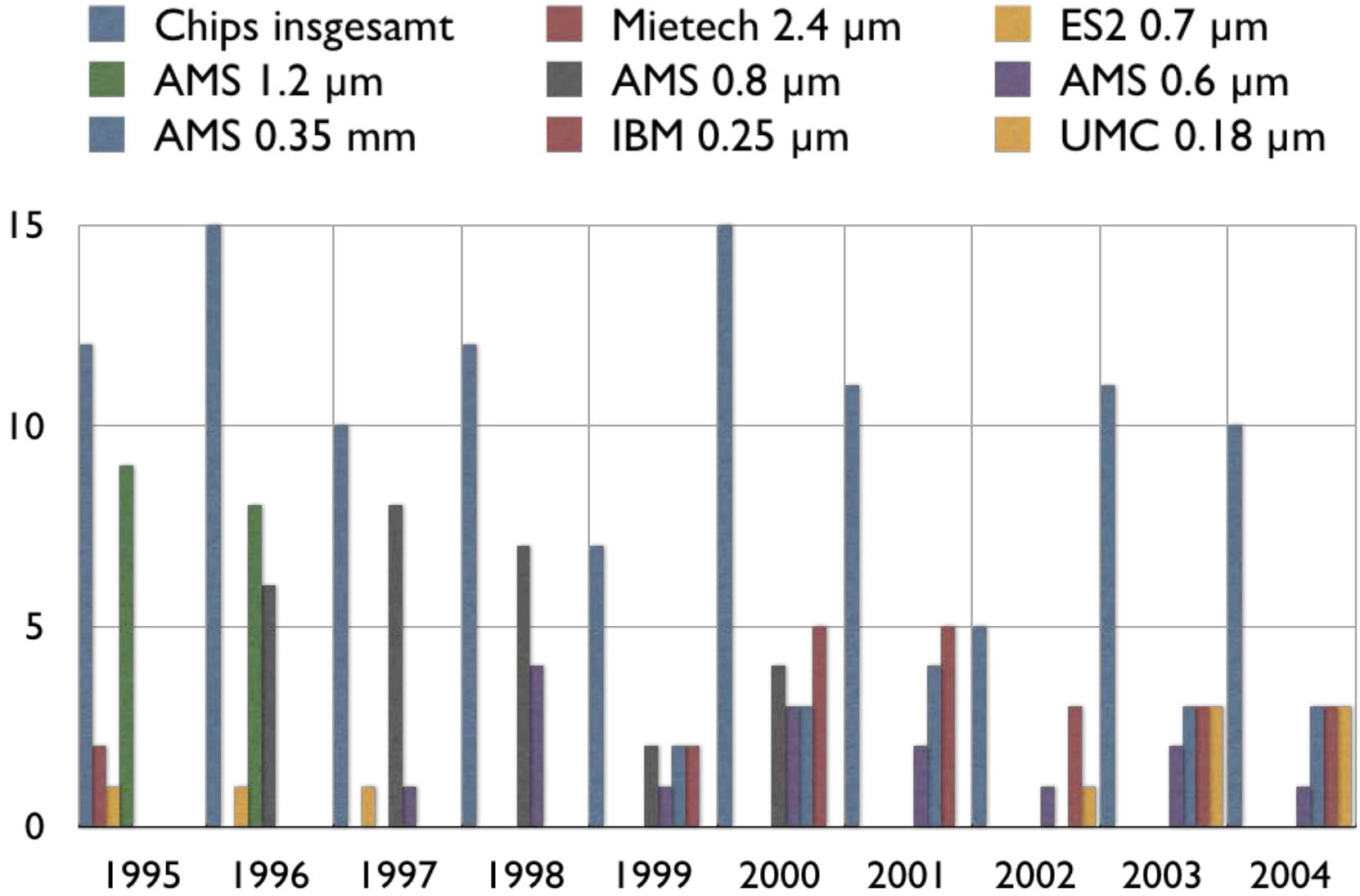


ATLAS Calorimeter Trigger
4000 MCMs produced and tested

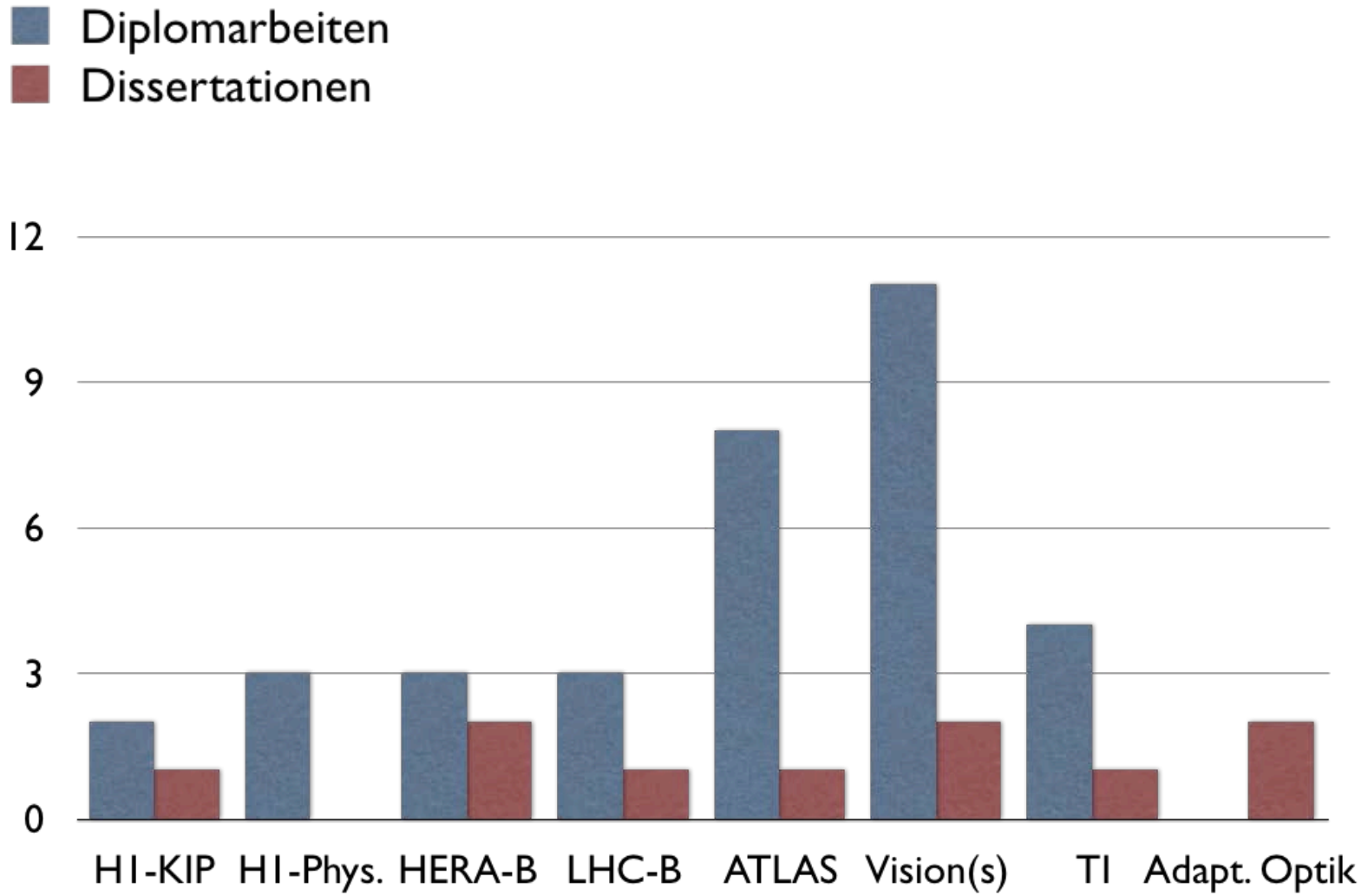
Important : System Experience (ATLAS Calorimeter Trigger)



108 Chip Submissions in 10 Years

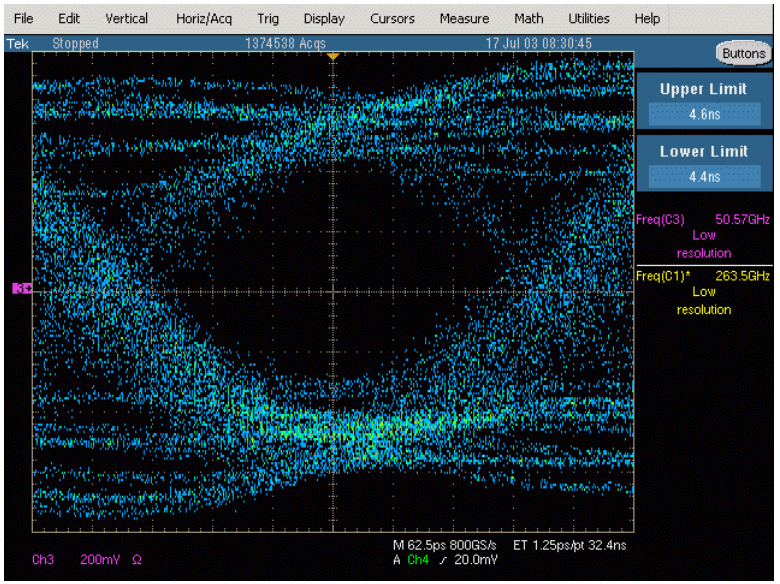


45 Chip Design Related Theses in 10 Years (2004)



Current Aquisitions with HGF Alliance (WP 1.1)

- 12 GHz Oscilloscope with active probes (approx. 100 k)
- Smaller Test and Lab Equipment
- 25 m² Clean Room Extension (Class 1000) for Wafer Handling
- Upgrade of Simulation Capacity -> requests ?



Serial MGT Links on 2.5 GHz Scope

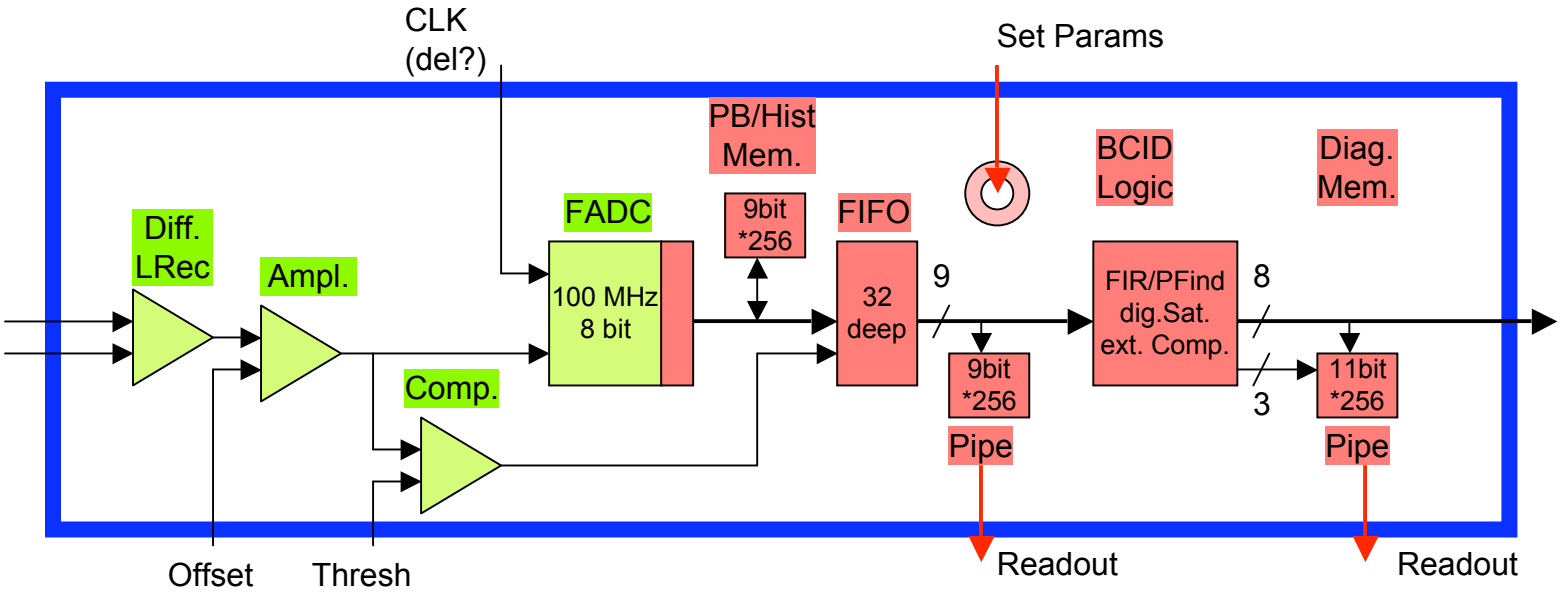
- Hiring of 2 Engineers

Problem : Salary Scale of Large Labs x1.5
Salary Scale of Industry x2 - x3

2 (safe) candidates did not finally sign

ATLAS : LVL-1 Calorimter Trigger Upgrade

Development of a calorimeter level-1 trigger frontend chip for the ATLAS detector (analog filtering, A/D conversion, digital signal filtering, serialisation)



ATLAS Level-1 Calorimeter Trigger

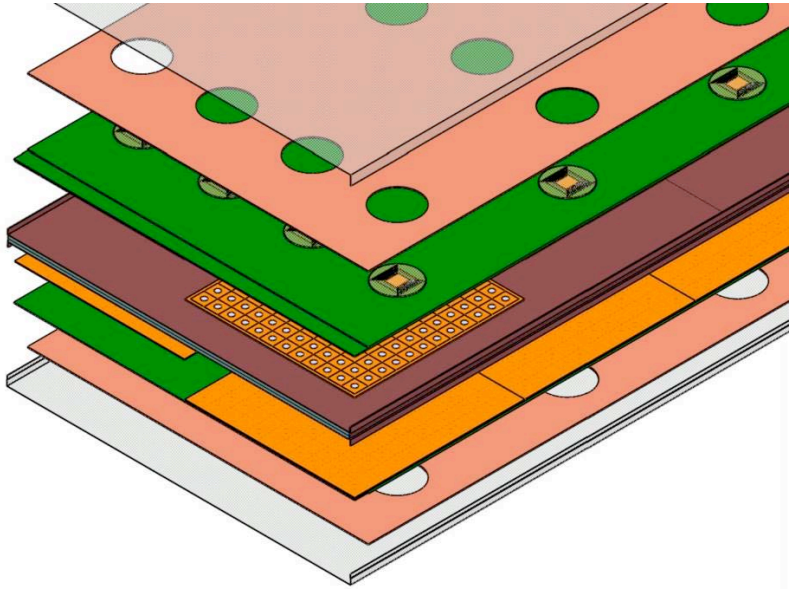
Upgrade Workshop

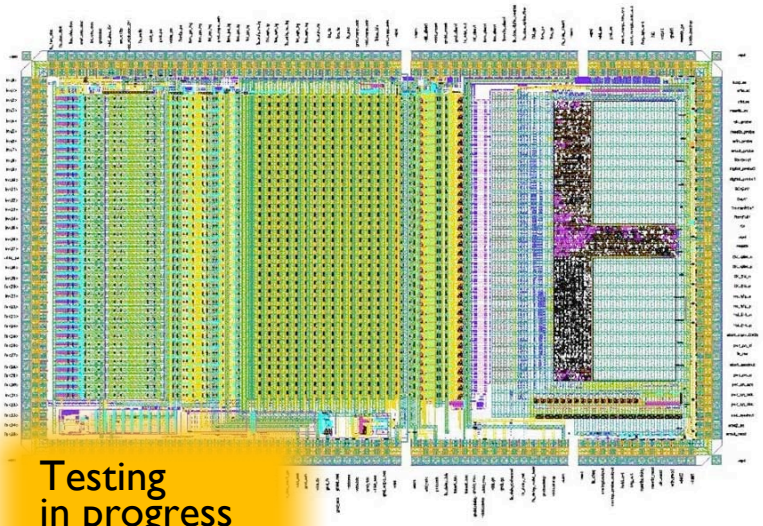
Heidelberg, 17/18 January 2008

ILC : Calorimeter SiPM r/o electronics (HCAL)

Requirements:

- Large dynamic range (15 bits)
- Auto-trigger on ½ MIP
- On chip zero suppression
- Front-end embedded in detector
- Ultra-low power : (<< 100 μW/ch)
- 10^8 channels
- Compactness





SPIROC (Orsay)

[2nd generation r/o chip]

- 36 channels
- internal ADC
- auto-trigger
- power cycling [25 μW/ch]
- ...

Further needs:

- better signal to noise for SiPMs with lower gain
- improved auto-trigger [channel wise]
- ...

- Laboratory is ready to host other users. Support limited as long as staff problem not solved

- Major upgrades of infrastructure under way (very high speed state-of-the-art signal conversion, large cleanroom facility)

- Two „Terascale" Projects currently under way locally