ATLAS Pixel Upgrade for sLHC

1st Detector Workshop of the Helmholtz Alliance
'Physics at the Terascale'

03/04/2008

Marlon Barbero - Bonn University

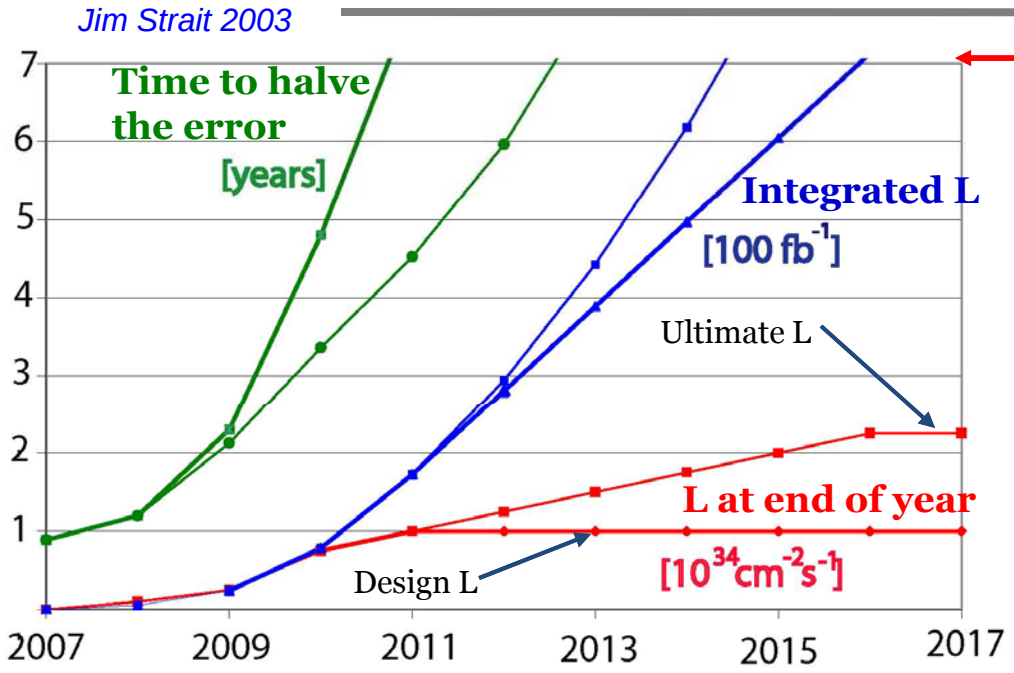
SI LAB
Silizium Labor Bonn

ATLAS Pixel Detector Collaboration

Plan

- Why sLHC & Tentative timeline.
- Strawman Inner Detector.
- On going activity in pixel upgrade collaboration:
  - Sensor: 3D, diamond, planar.
  - Powering / DCS.
  - New FE: Analog core, digital pixels / architecture, peripheric blocks.
  - Architecture concept simulations.
  - Test setup for full size FE / prototype test.
  - Thinned FE & PbSn → SnAg.
  - Modules with Through Silicon Via (TSV).

Need for sLHC upgrade

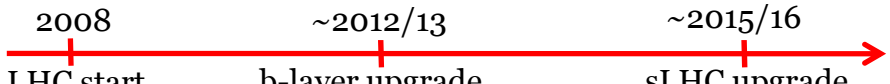


Radiation damage limit ~700 fb-1

Reasons to upgrade LHC:

- Due to the high radiation doses to which they will be submitted, the LHC IR quadrupole magnets have to be replaced after integrated luminosity of 700 fb^{-1}
- Depending on the luminosity evolution, the error "halving time" will be well above 5 years at this time

- LHC needs to do a major replacement of Interaction Region quadrupoles after an integrated luminosity of ~700 fb-1. There is still a large incertitude when it will happen (LHC has still to startup and has >1 year delay to 2003 plot).
- This would happen ~2015. SLHC upgrade has today scheduled an upgrade of ATLAS for 2015÷2016 shutdown.



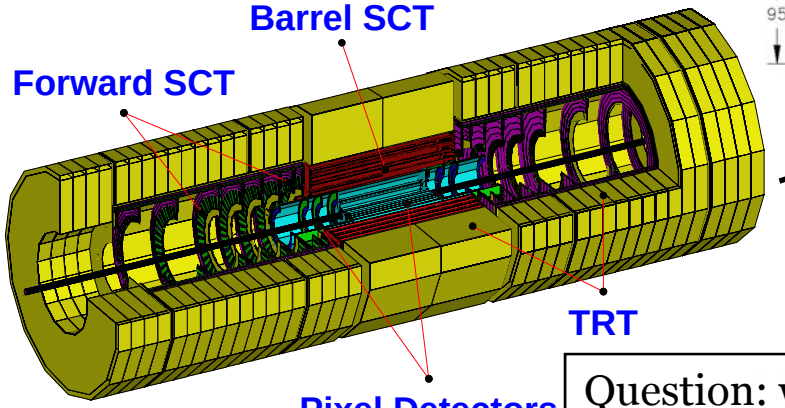
Tentative timeline for upgrades

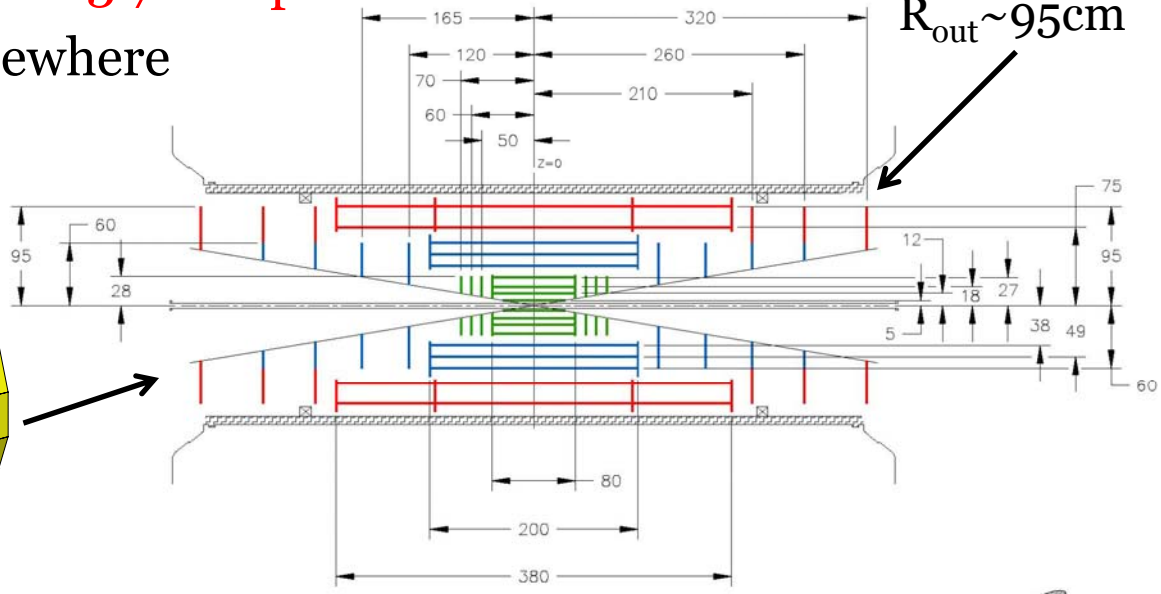
Strawman Inner detector upgrade

- 3 to 4 Pixel layers.
- 4 to 3 Short Strip (SS) layers. Length ~3cm.
- 2 Long Strip (LS) layers. Length ~12cm.

9 hits for $\eta<2.5$

- TRT out (straw occupancy already high at LHC)
- Inner radius as close as we can get! Limited by beam-pipe radius, occupancy, radiation damage. ~3.7cm option?
- Separation Strip / Pixel somewhere in the ~30cms:
- Ex: 4P+3SS+2LS.





Question: was any optimization done, Short Strips vs.Big Pixels at intermediate radii (cost, material, performance, robustness…)?

→ optimal detector???

BROOKHAVEN NATIONAL LABORATORY

Atlas Pixel Upgrade for sLHC

- Increased Lumi. at sLHC (×~10 wrt LHC HL?) → FE redesign.
- New sensor technology to cope with higher radiation levels.
- A pixel detector "at least as good" as the current one:
  - Potential reduction of b-layer radius.
  - Smaller pixel size (50×400μm→ 50×250/200μm).
  - Material reduction; influence on b-tagging efficiency:

WH120, L2044

	60%	70%
2D	195 ±13	53 ± 2
Z	32 ±1	10± 0.2
3D	440 ±46	93 ± 4.4
SV1	1110 ±180	210 ±15
SV2	1090 ±174	182 ±12

	60%	70%
2D	109 ± 5	36 ± 1
Z	25.8 ± 0.7	9.4 ± 0.1
3D	234 ±18	60 ± 2.2
SV1	730 ± 95	140 ± 8
SV2	635 ± 77	136 ± 8

~70% rejection degradation

b-tagging efficiency vs. light jet rejection

all layers ~1.2%

all layers ~2.2%

Decrease of material is useful for everything.
Effect much bigger for WH400 (higher jet $P_{\perp}$)

from V. Kostyukhin - Genova, Valencia Up. WS, Dec 14th 07

WH400, L2044

	60%	70%
2D	96 ± 3.7	41±3
Z	18 ±0.3	7 ± 0.1
3D	165 ± 8	47 ± 1.2
SV1	605 ± 58	166 ± 8
SV2	524 ± 47	150 ± 7

all layers ~1.2%

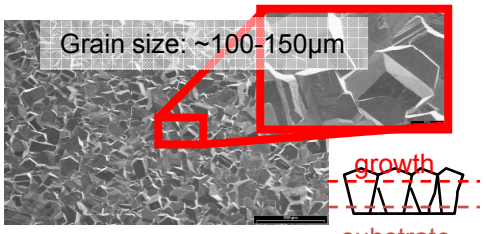
	60%	70%
2D	40 ± 1	11 ± 0.1
Z	9.7 ± 0.1	3.4± 0.1
3D	63 ± 2	16.6 ± .3
SV1	210 ± 12	49 ± 1
SV2	190 ± 10	45 ± 1

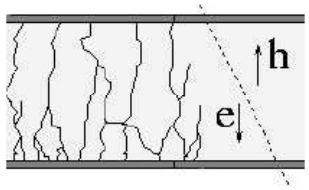
all layers ~2.2%

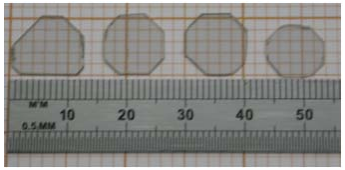
~270% rejection degradation

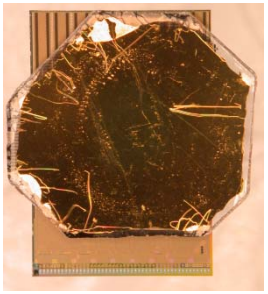
3D and diamond sensor

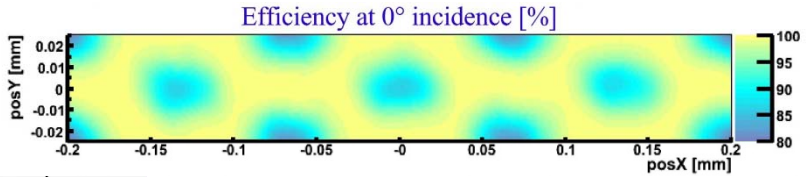
- Pixel community involved in characterization of pCVD diamond sensor, scCVD diamond and 3D. Very rad-hard. 1st results scCVD diamond w. FE-I3. 3D 99.9% eff at 15°.

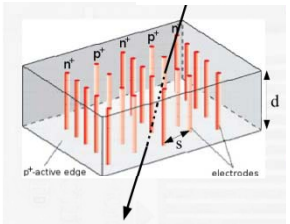


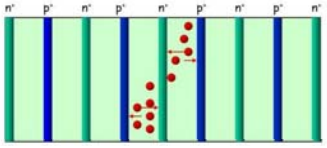


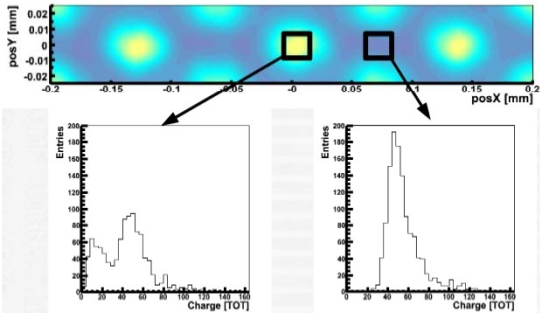










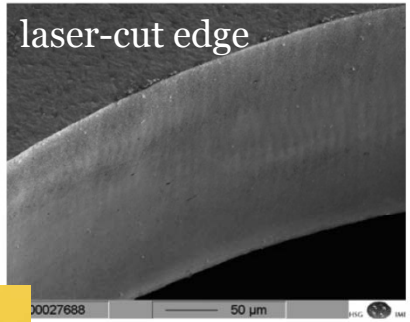


Markus Mathes, DPG
Freiburg, Mar. 5th 08

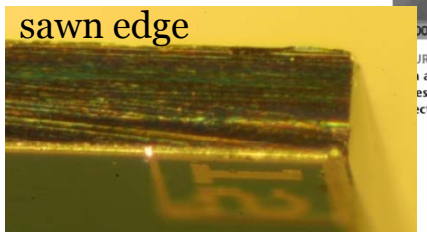
Planar Silicon Activities

- planar Si: reliable, comparatively cheap and rad-hard to beyond 10^{15} n_{eq}/cm^2
- an R&D collaboration is forming, proposal currently being circulated
- the proposal focuses on
  - performance evaluation of planar sensors up to 10^{16} n_{eq}/cm^2
  - significant cost reduction to instrument also larger radii
  - choice of bulk material n-type vs. p-type
  - edge reduction ("slim/active edges") to avoid shingling on staves; current edge width 1500µm →below 200µm? Alternative dicing methods (e.g. laser), number and width of guard rings.
  - threshold reduction to below 2000 electrons
  - better CCE, evaluate methods to reduce trapping at high fluence
- German participation:
  - HU Berlin/DESY
  - University of Bonn
  - TU Dortmund
  - Munich (MPP and MPI semiconductor laboratory)

D. Muenstermann / C. Gössling, Dortmund, Pix. Up. Meeting, Feb. 1st 08

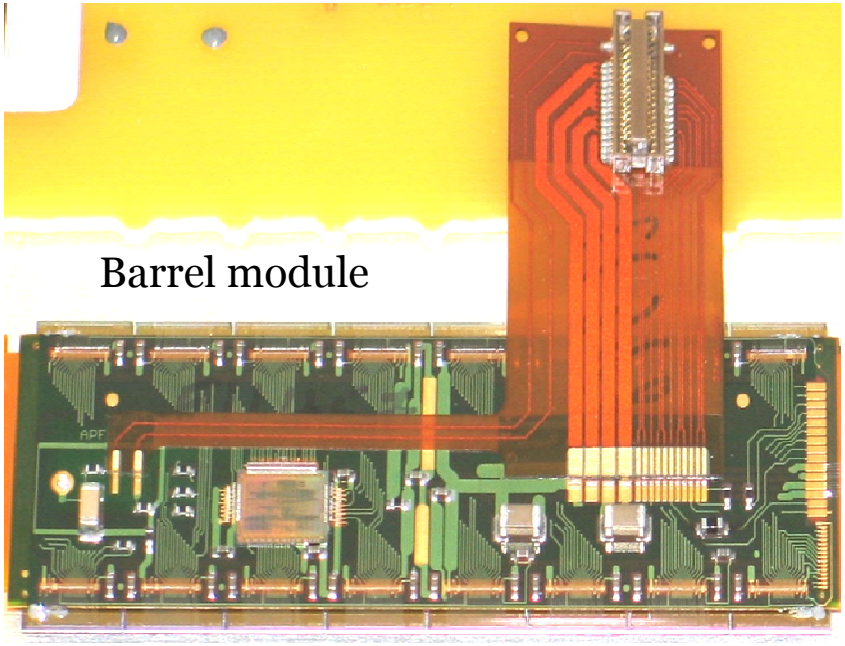


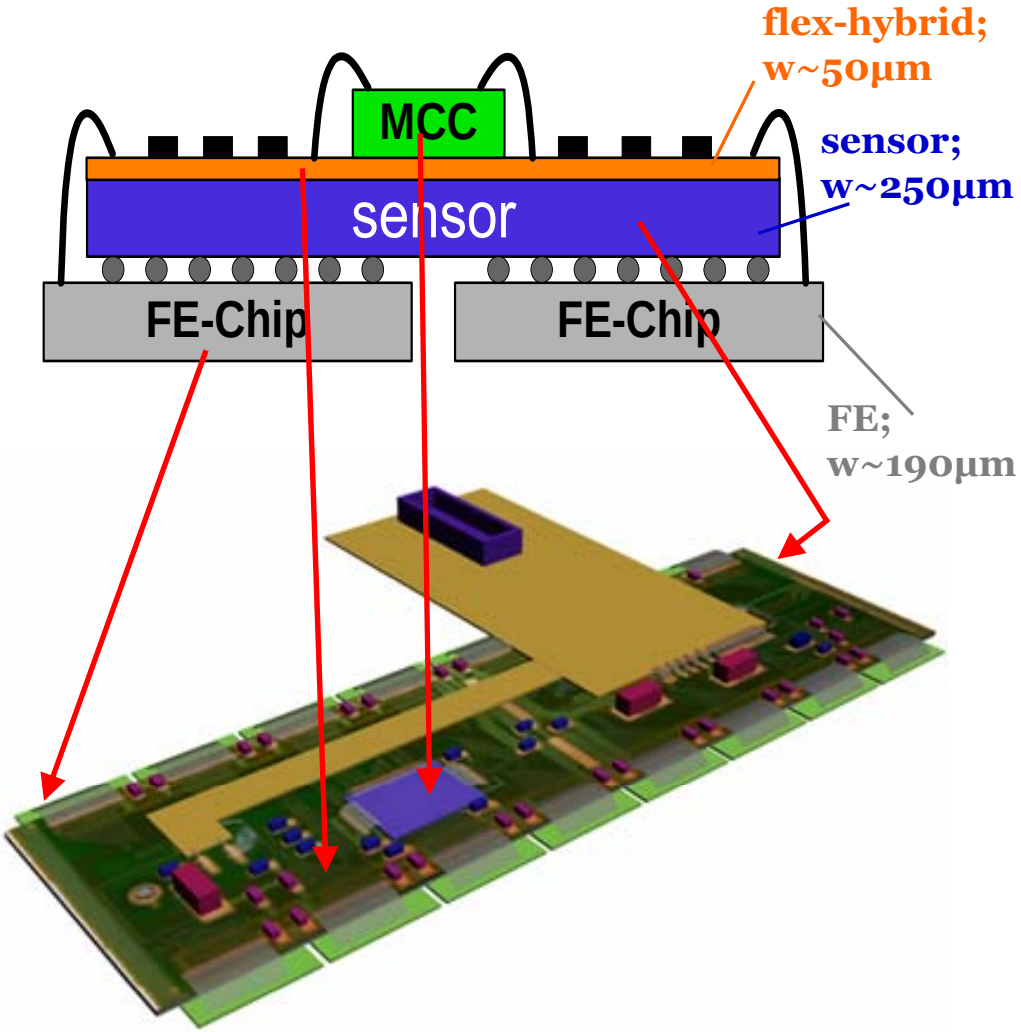
URE 2: Edge of a silicon wafer with a thickness of 300 µm cut
a high average power picosecond laser of the TruMicro
es 5000. No chipping and heat affected zone can be
cted.



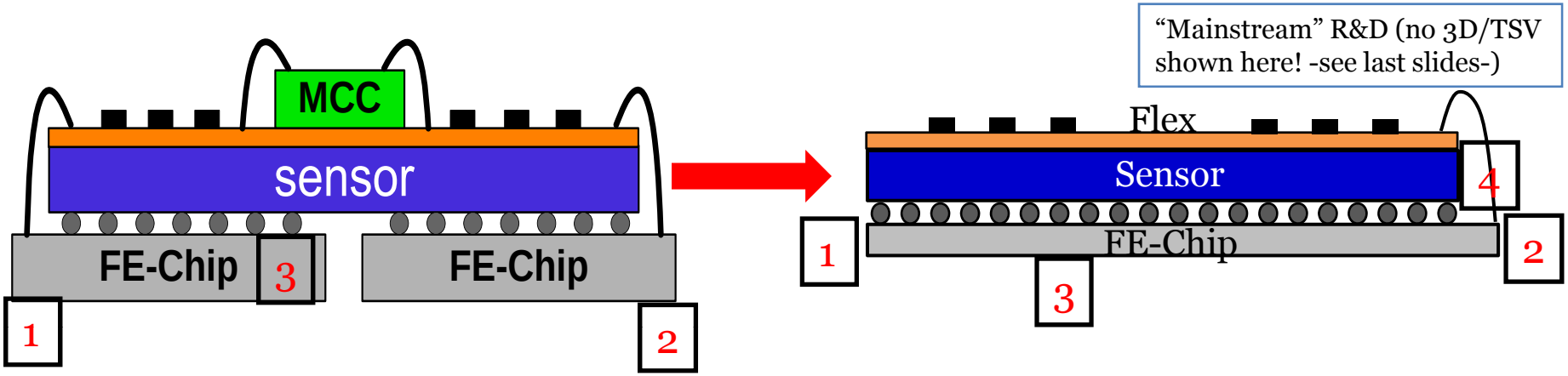
Reminder: current FE-I3 module

- 3 layers, 3 end-caps, 1744 modules

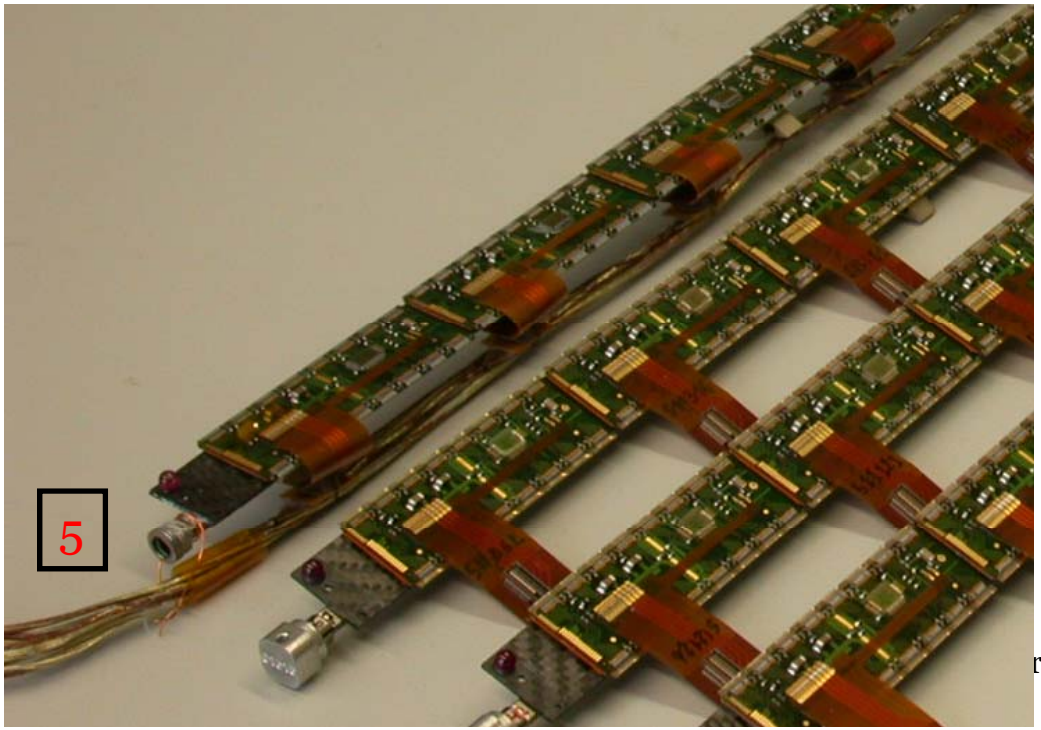




Reducing material?



"Mainstream" R&D (no 3D/TSV shown here! -see last slides-)



1 - Big chip (avoid having periphery on both sides of module).

2 - Reduce size of periphery (2.8mm→2mm).

3 -Thin down FE chips (190µm→90µm).

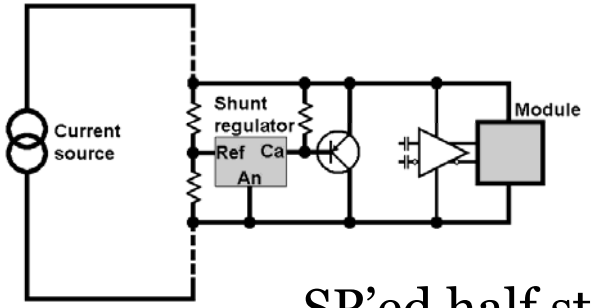
4 -Thinner sensor (250µm →200µm)

5 - Less cables (powering scheme).

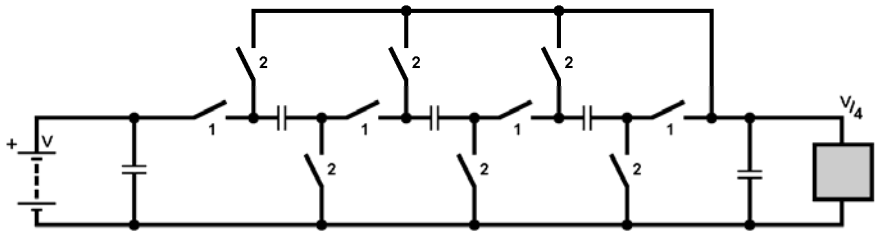
Powering activity pixels, DCS

- Serial powering and DC-DC converters

SP: recycling current, module per module



DC-DC: "high-voltage" power lines, Q pump



SP'ed half stave FE-I3

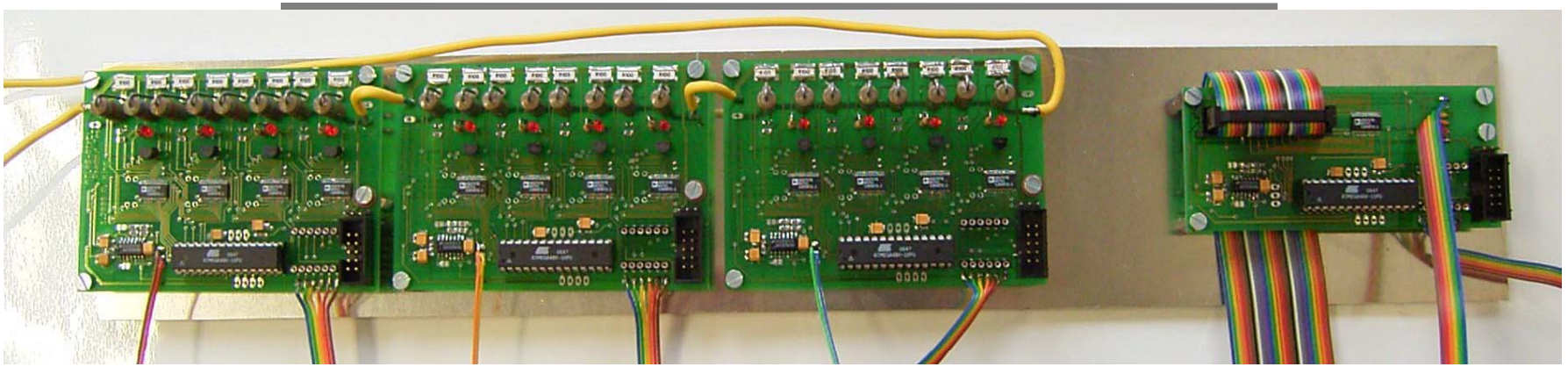
Duc Bao Ta, Bonn -2005-
(D.B.Ta *et al*, NIM A 557 (2006) 445-459)

1st proto. designed.

P. Denes, LBNL

More details about powering in L. Feld talk, later this session

Different integration schemes of the DCS chip



- Wuppertal started to study 2 different integration schemes
  - DCS (Detector Control System) chip at the end of stave
  - DCS chip on the module
  - For SP and other power schemes

Same setup is used

- DCS part in every FE chip has to be implemented:
  - need a multiplexer in every FE chip; access to 5 signals (V_{ana}, V_{dig}, I_{ana}, I_{dig}, Temp.).
  - DCS part delivers via the multiplexer the DCS monitoring values to the DCS chip
  - Disable FE through DCS
  - Acting on the optical link if at end of stave

J. Boek, Wuppertal, b-lay replacement ws, CERN, Feb. 1st 08

New Front-End for higher lumi

- Why a redesign?
  - Increased lumi + potential decrease of R_{blayer} → FE-I3 can not cope with much increased hit rate: need change of architecture.
  - Adapt to potential change of C_{sensor} (3D, diamond, planar Si)
  - Material reduction & improved active area ratio → bigger chips (7.6×8mm → 16×17 .5mm) with reduced periphery (2.8mm→2mm).
  - Better power consumption: analog design for reduced currents + decrease of digital activity by sharing digital circuits with several pixels.
- Why a new technology? ¼µm →130nm
  - Go to smaller pixel size (target 50x400 → 50x250 µm²), smaller periphery.
  - Improved radiation tolerance: linear thin gate oxide transistor sufficient (no need for Enclosed Layout Transistor -ELT-).
  - Process availability at timescale of upgrade.

Next prototype

- Collaboration: LBNL, Bonn, Genova, Marseille, Nikhef.
- 130nm, test chip already submitted and received in summer 2007.
- Focus on b-layer upgrade (as intermediate step for sLHC).
- Proto. chip being design (sub. end March 2008) + SEU + LVDS Transc.
- FE-I3: 18×160 pixels→ FE-I4: 64×350 pixels
  full proto for 'end of 2008' (very likely too tight).
- Core blocks:
  - Analog readout electronics.
  - New concept for digital pixel electronics.
  - New readout scheme for double-column.
- Peripheric blocks:
  - Bandgap reference.
  - DACs for bias/calibration.
  - Regulators.
  - LVDS Tx / Rx.
  - Slow control.

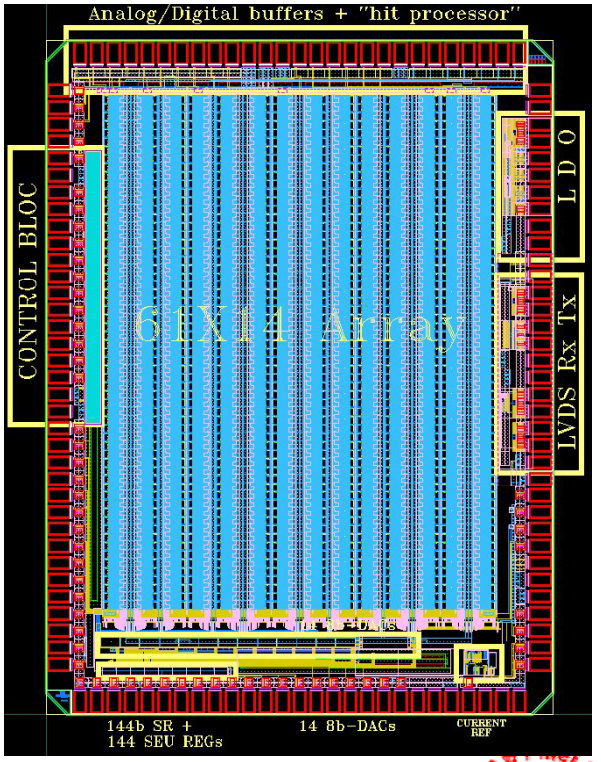
M. Moshine, CPPM

A. Mekkaoui, LBNL

R. Kluit, Nikhef

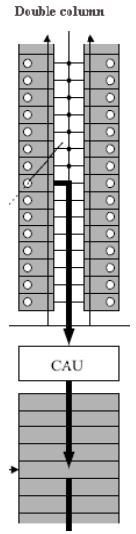
M. Karagounis, Bonn

R. Beccherle, Genova

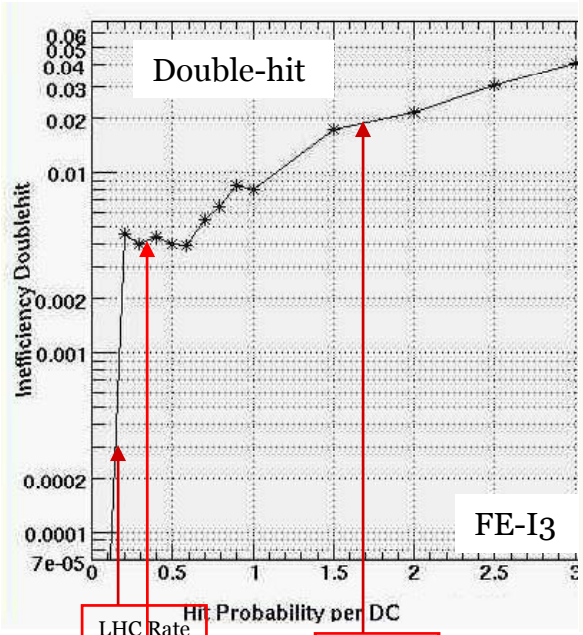


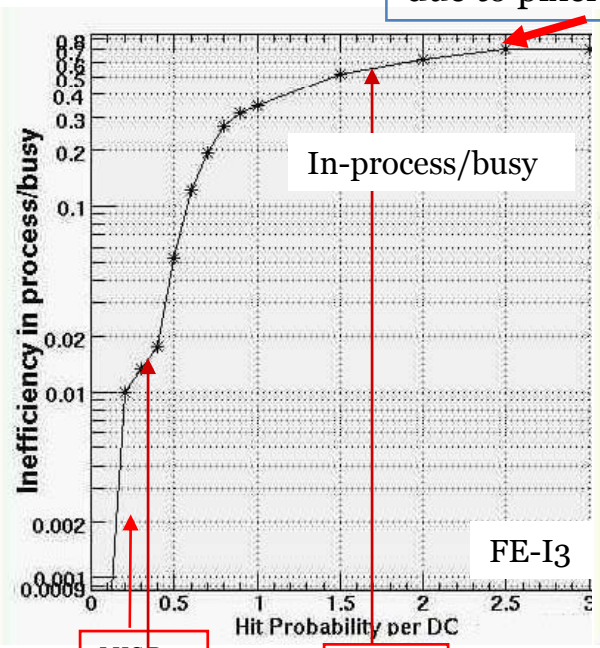
FE-I3 simulations above LHC HL

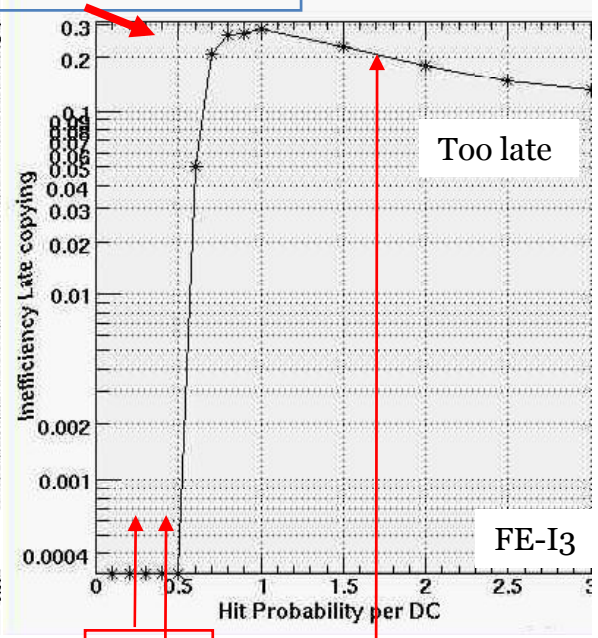
- The problem: increased luminosity, reduced pixel size but increased chip size (DC length increase), reduced radius → FE-I3 architecture with hit transferred to End of Column buffer (transfer takes time!) waiting for 1LT confirmation is too inefficient.



due to pixel →EoC transfer!





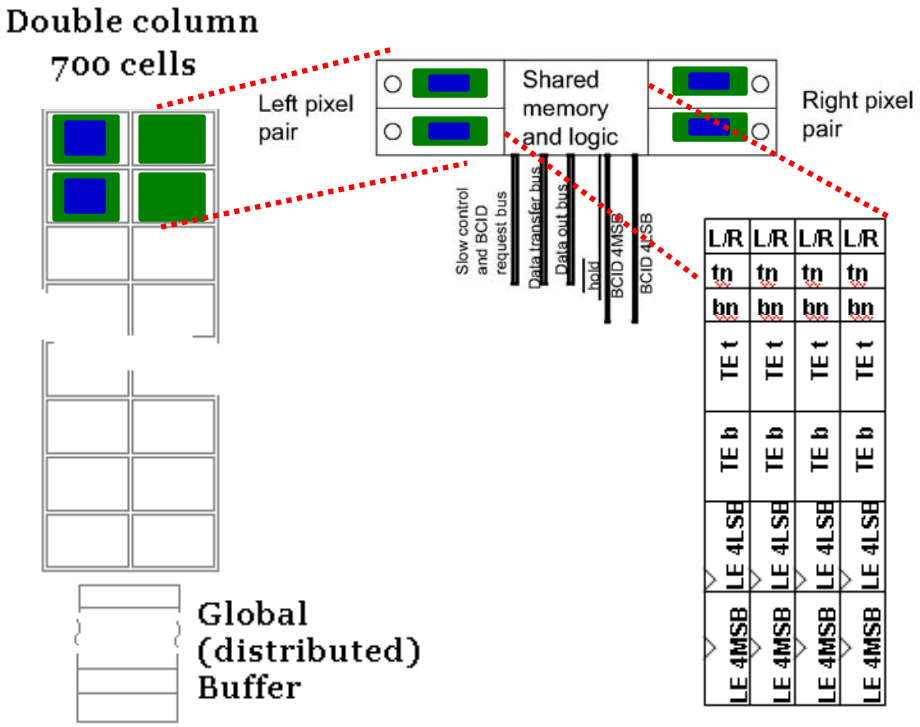


D. Arutinov, DPG Freiburg, Mar. 6th 08

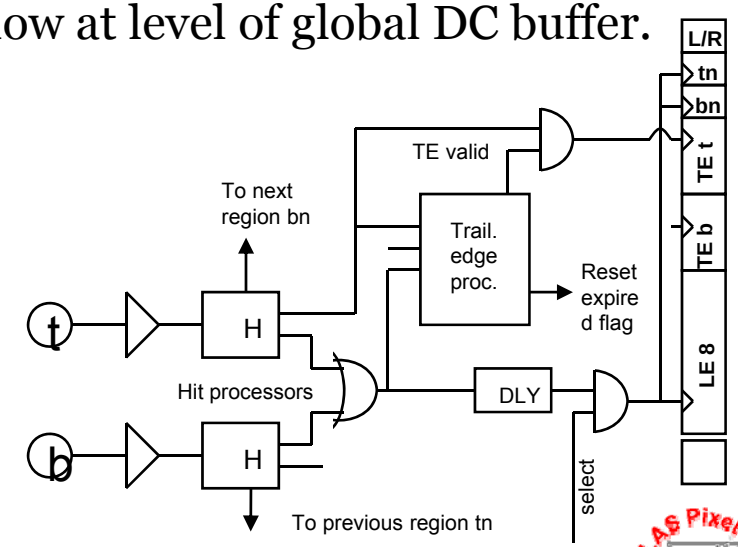
Already at 2-3 times LHC design lumi, transfer of hit to EoC might hardly be tolerable

New Architecture Concept

- Basic idea: store the hit locally in Double Column and transfer only triggered hits → regional pixel logic & regional buffer (note: can be done thanks to smaller feature size).

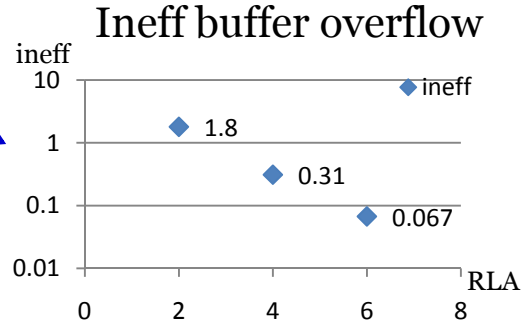


Then play with your parameters (size of pixel logic, size of regional buffer, buffer depth) and check inefficiency.
- Hit pileup.
- Overflow at level of regional buffer.
- Overflow at level of global DC buffer.



On-going studies

Ex: Buffer overflow inefficiency as a function of Regional Logic Area -RLA- (for a fixed ratio #of pixel/# of buffer cells = 1.5)



- This architecture is cluster efficient!
- For a given depth/area ratio:
  - Bigger Regional Logic Area (RLA) is better
  - Larger Logic Unit (p) is better
  - BUT: Design constraint in PUC, wire-ing, increase size of recorded event…
- Machinery is set-up in a modular way. Scan of parameter space (p, BA, d) can be done for any input.
- Outlook: Studies performed on proposed architecture continue:
  - Pythia / GEANT simulation → FE-I3 / FE-I4 (radius 3.7 cm / 5cm).
  - Truncation of first digitalization (double hit inefficiency reduction).
  - Dual threshold (a way to reduce double hit).
  - Hit erasing at L1T arrival time.
  - Transfer to DC global distributed buffer.
  - Data rate at module level.

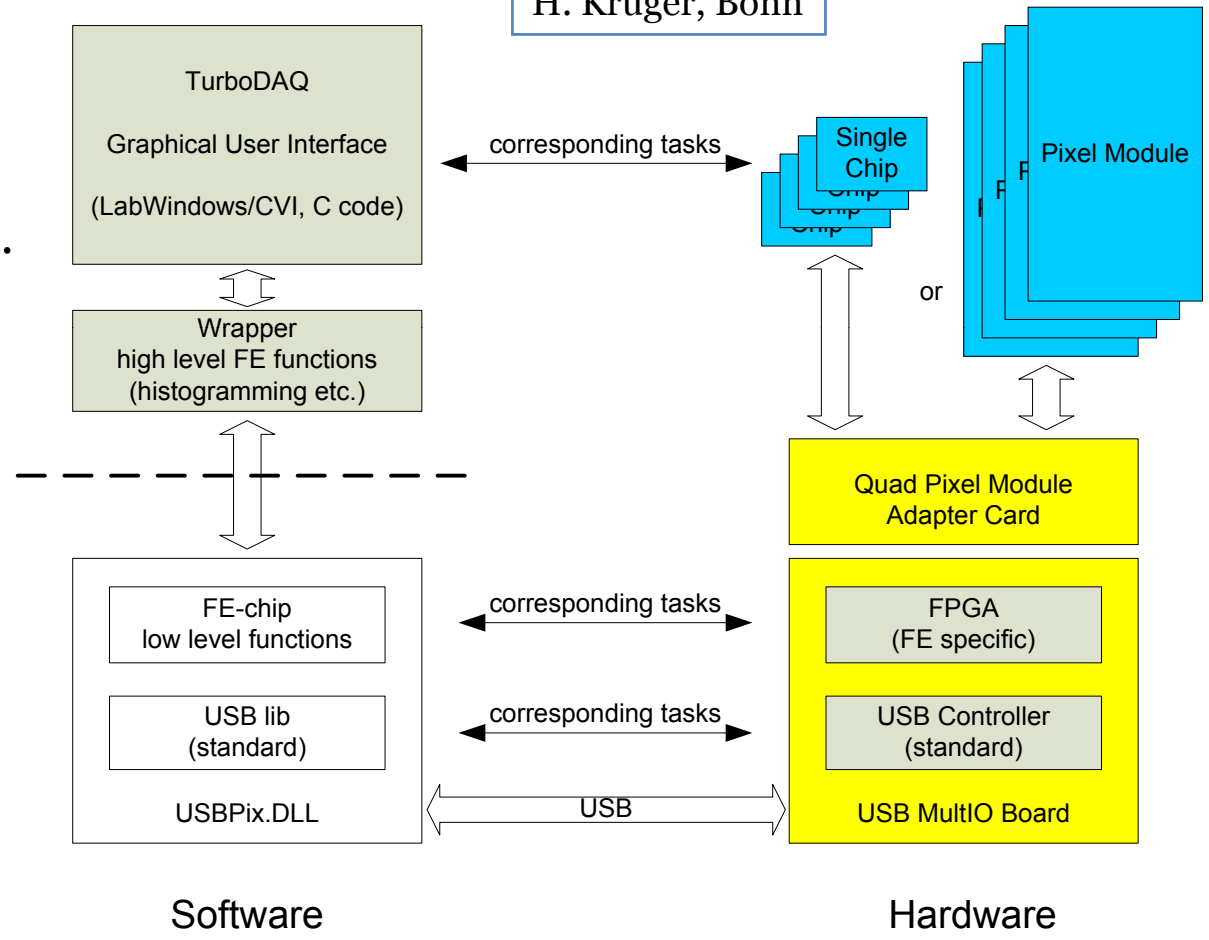
On-going! Preliminary results soon!

USB based FE Readout System - Overview

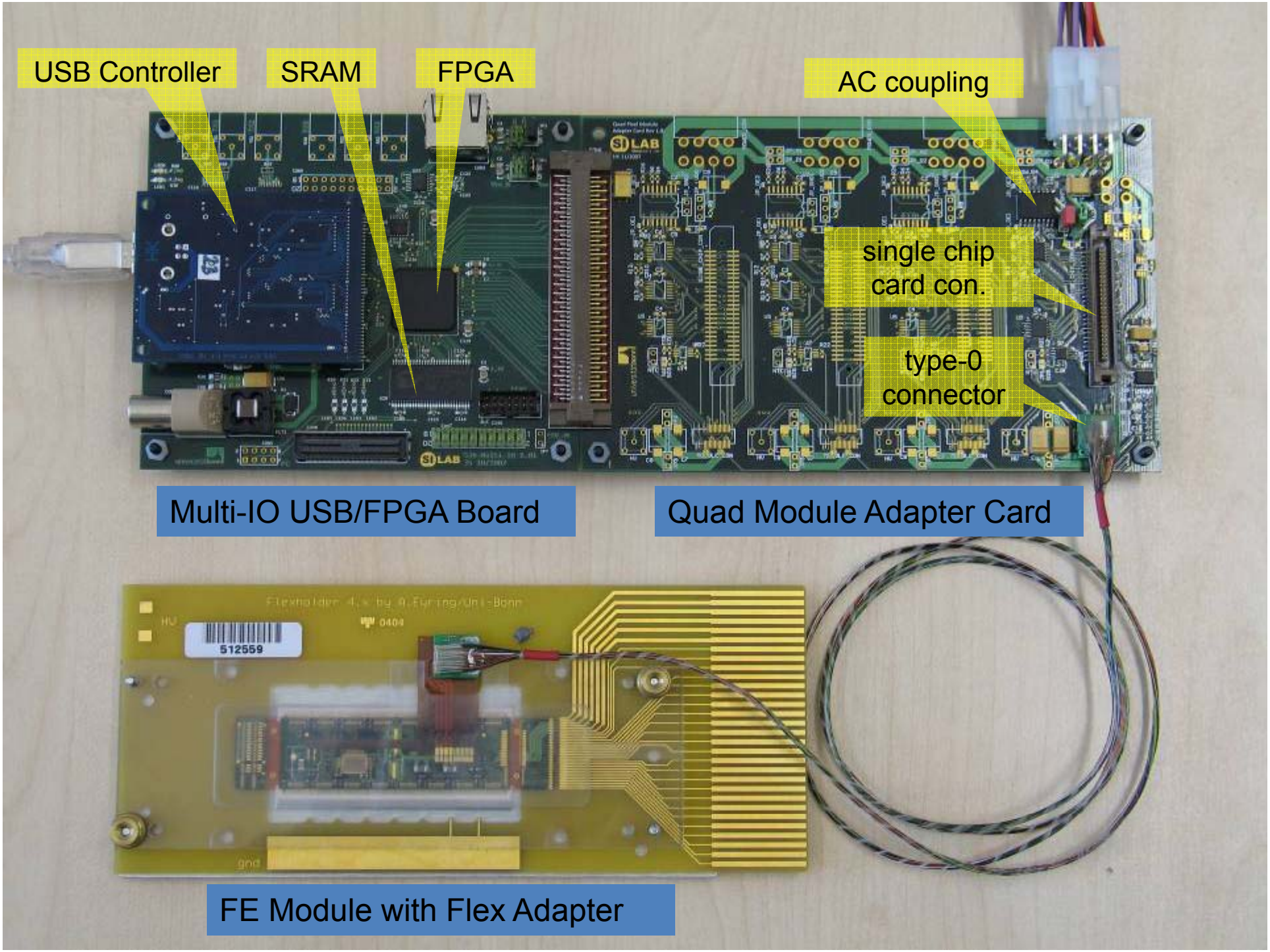
- Lightweight "Replacement" for the current read-out system: TurboPLL/PCC (designed some time ago, hard to recover for new FE).

- Hardware based on FPGA card with USB interface
- Supports up to four single chips or four FE modules
- AC coupling for SP operation of modules
- Multi-IO USB/FPGA Board
- Interface to TurboDAQ software

H. Krüger, Bonn

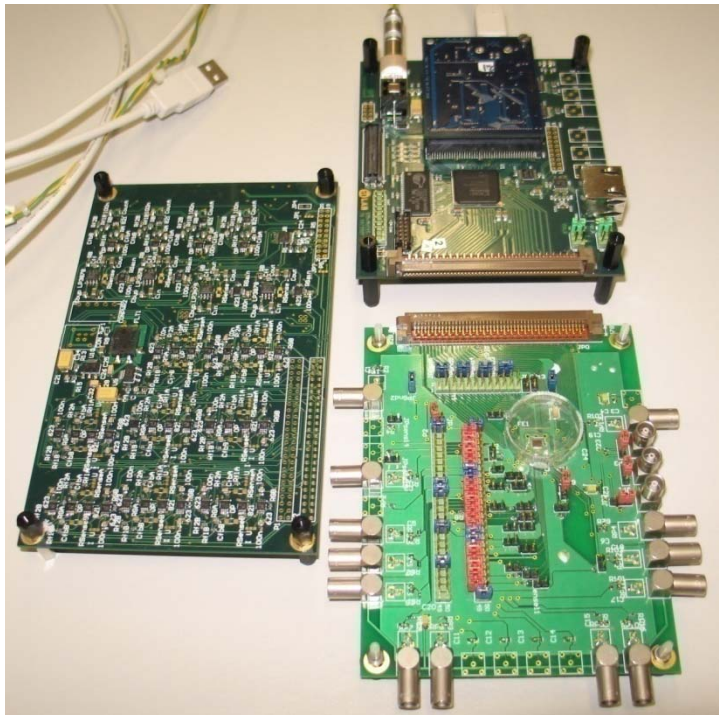


J. Grosse-Knetter, Göttingen

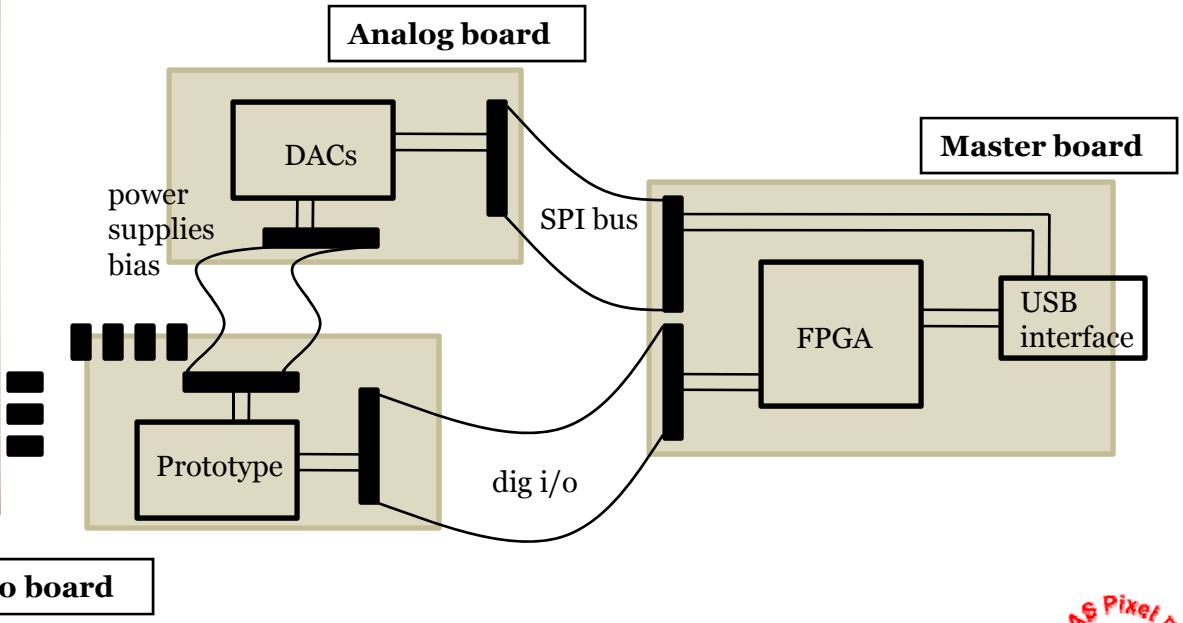

USB Controller
SRAM
FPGA
AC coupling
single chip card con.
type-0 connector
Multi-IO USB/FPGA Board
Quad Module Adapter Card
FE Module with Flex Adapter

Test Setup for Proto. Charact.

- Uses Multi I/O USB/FPGA board, interface with prototype carrier board.
- Status: prototype available for 1st proto APUP0, first tests with digital board on-going; design of test boards for next proto currently starting.



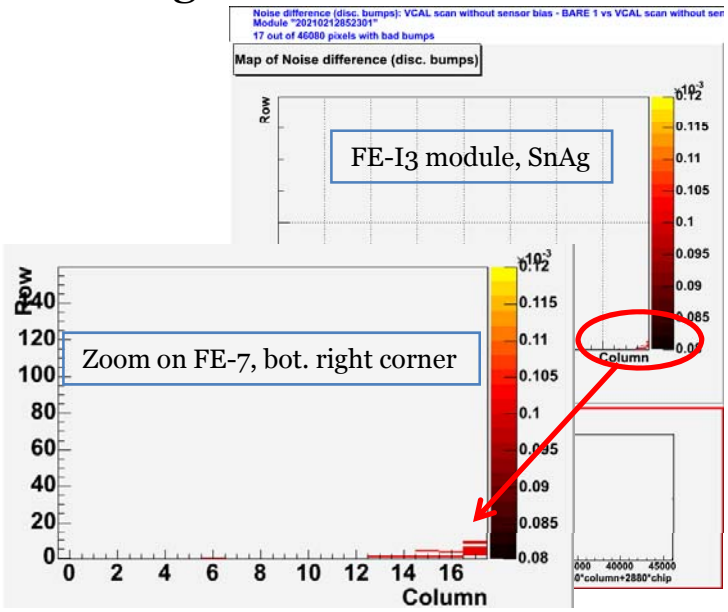
H. Junker, Bonn

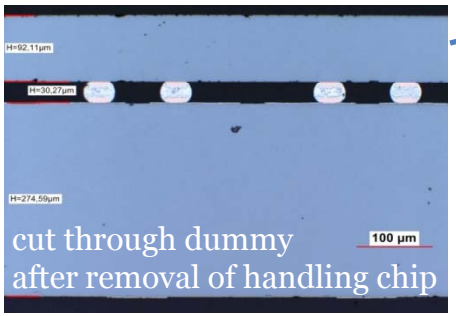


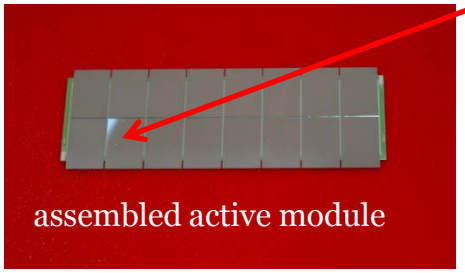
PbSn→ SnAg & Thinned FE

- PbSn→SnAg: Follow the trend of industry (Lead-free process).
- SnAg bumps less elastic than PbSn → rethink packaging/testing/handling.
- Thinned FE: For material reduction!
- Present FE-I3 (PbSn or In): 190µm → FE-I4 (SnAg) thinned to 90µm (~0.1% x/X0).
- Electrical tests of thinned FE-I2: yield ok.
- Several procedure to then bump-bond the thinned chip to the sensor, one of them being the use of handle wafer. Methods need tuning. New results available soon.

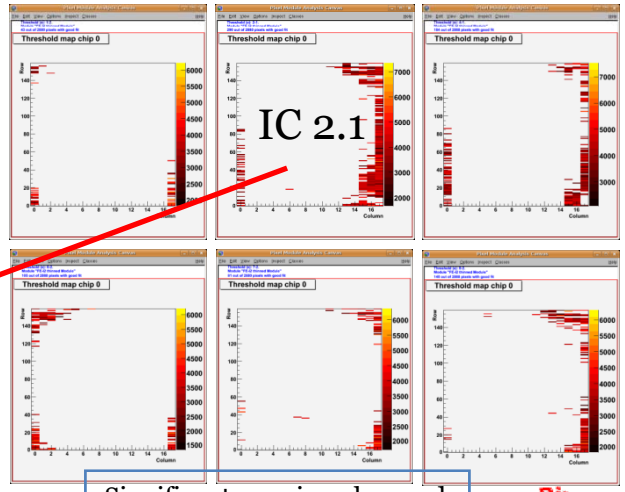
J. Allofs, Bonn







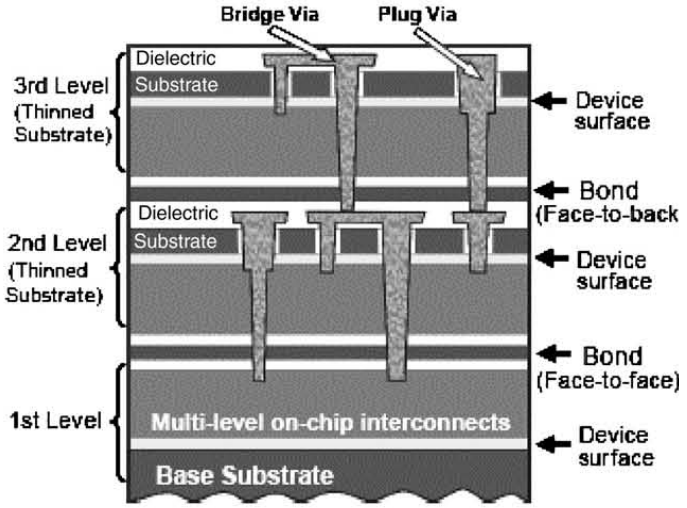
pictures IZM Berlin

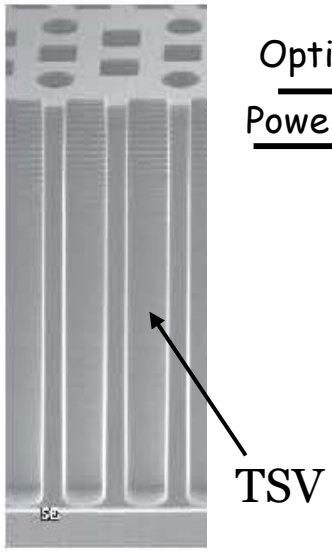


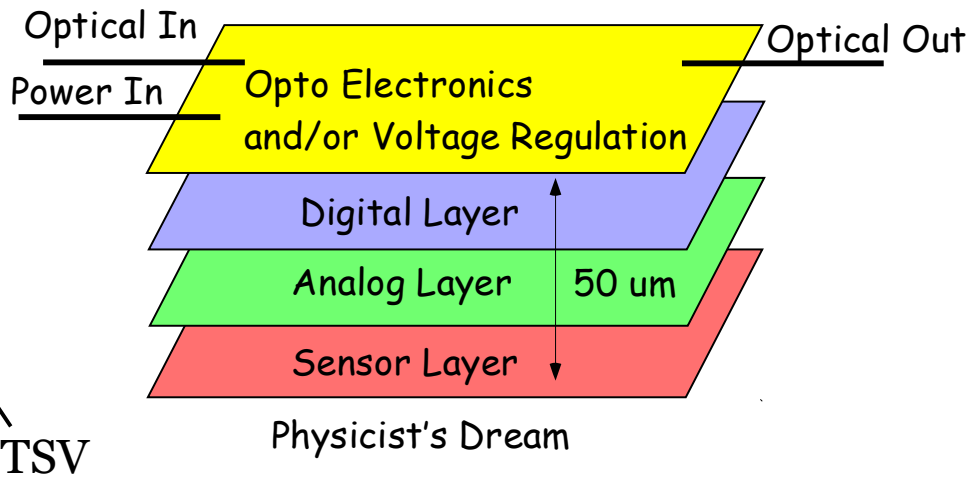
Significant warping observed

New integration techniques?

- Could the use of 3D interconnect techniques with TSV help in building up a “light weight” module?



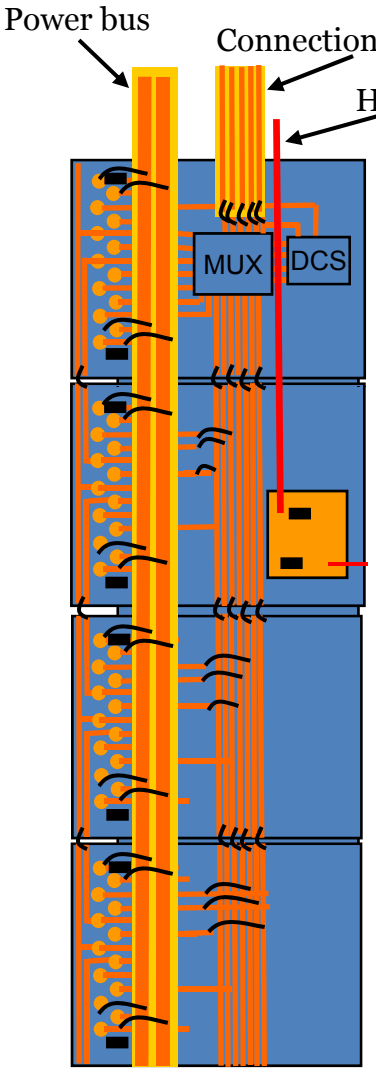


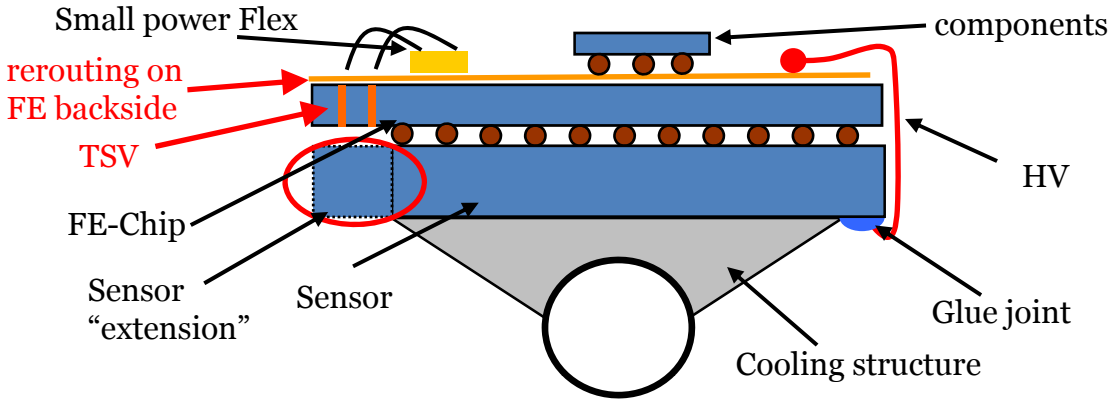


- Work has started with IZM Berlin, where 3D integration techniques are being developed.
- Note: A more ambitious project also starting with Munich group (→ 3D integrated detector).

A module concept with TSV

Bonn/IZM Berlin





Description:

TSV for all signals and power of the FE. The signals are rerouted on the FE backside →Much reduced Flex (1 for power only, 1 for signal IO). No Folded flex on back-side. Cooling structure in direct thermal contact with the sensor. Could use Flip-Chip techniques instead of Wire-bonds.

Pros:

Simple Flex. No delicate Flex on back-side. Flex accessibility. Reduced material from Flex contribution. Cooling structure to the edge of sensor. Mounting: thicker Si towards the structure. Possible to expand sensor coverage (+ reroute "à la ganged pixel") and provide real 100% coverage at module level.

Cons:

FE face interaction point. How to connect HV. FE chips need a structured back-side (with 1 out of 4 different from the others)

R&D for a novel pixel detector for sLHC

MPI/IZM München

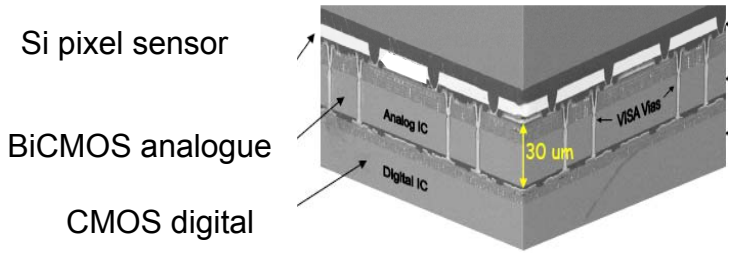
R&D on thin (75 -150 mm) FZ silicon detectors:

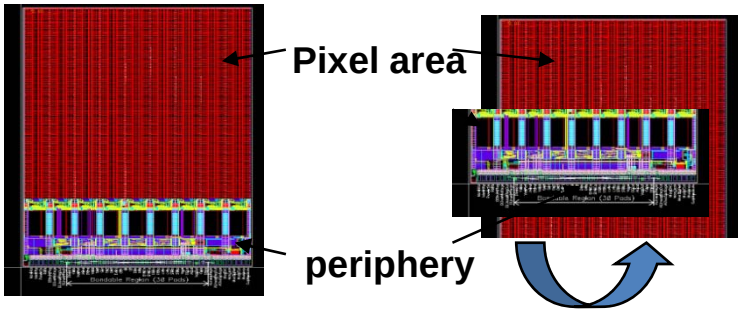
Based on well known pixel sensor technology.
Can be operated at 10^{16} n/cm² (V_{dep}, I_{leak}, CCE).

talk H.G. Moser tomorrow

3D interconnection (sensor – electronics; electronics – electronics):

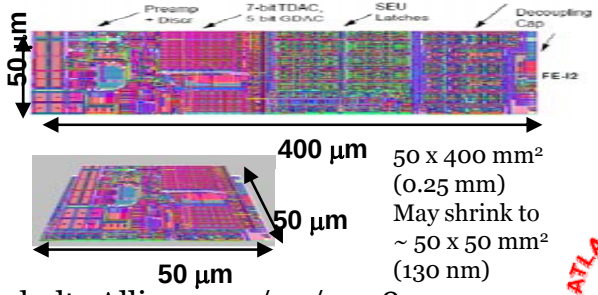
Alternative to bump bonding (fine pitch, potentially low cost?)
New ASIC architecture (multilayer, size reduction).
Optimization of rad. hardness, speed, power.
Ultra thin ASICs, top contact, 4-side buttable.





Can lead to an advanced module design:

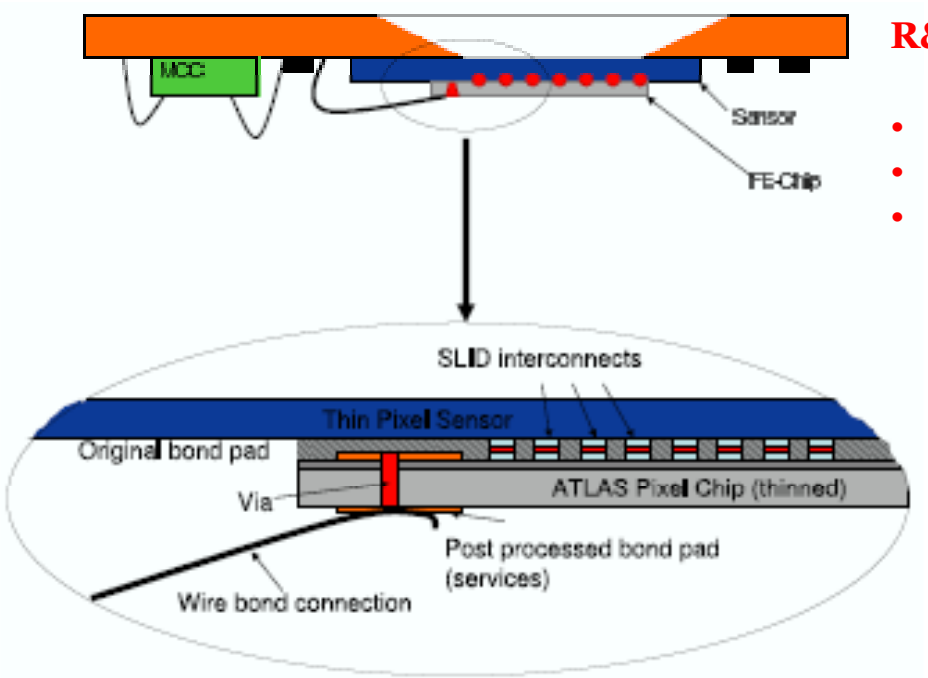
-> no dead space.
-> simpler module layout.
-> larger modules.
-> low material budget.



50 x 400 mm² (0.25 mm)
May shrink to ~ 50 x 50 mm² (130 nm)

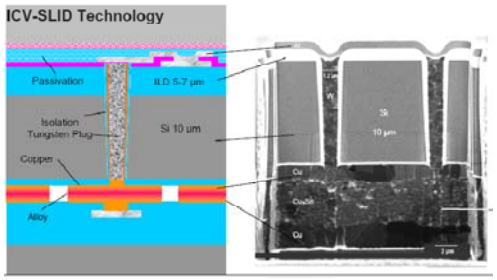
Proposed R&D Program

a) Test interconnection process with diode test structures
b) Build demonstrator using ATLAS pixel chip (FEI2) and pixel sensors made by MPI (single chip module)

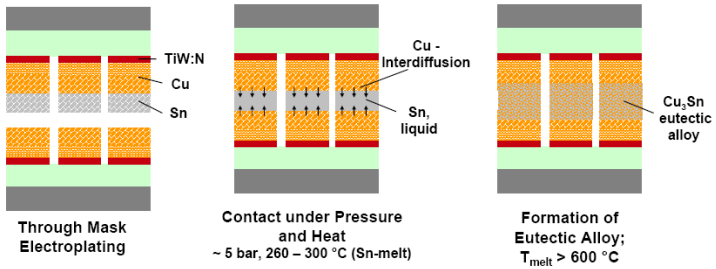


R&D goals:

- **Test thin detectors**
- **Thinning of FE chips**
- **Practice SLID and ICV**



Metallization SLID (Solid Liquid Interdiffusion)



SLID: A low cost alternative to bump-bonding?

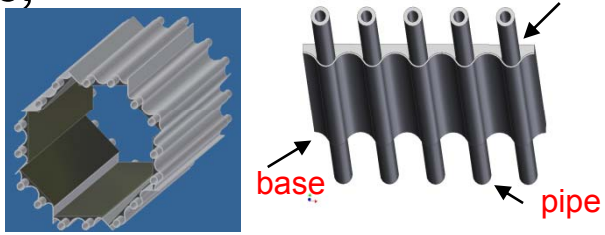
Main Work Packages (with a lot of hidden details!!!):

Design and production of thin sensors at MPI HLL → production started
Design of a dedicated r/o chip for test sensors - Interon, Uni Oslo → almost finished
Post-processing of the sensor wafers (SLID prep.) at IZM
Post-processing the FEI2 wafers and the Interon Chip (SLID prep. and ICV) at IZM
Interconnection of sensor and r/o also at IZM

Summary

- Why sLHC & Tentative timeline.
- Strawman Inner Detector.
- On going activity in pixel upgrade collaboration:
  - Sensor: 3D, diamond, planar.
  - Powering / DCS.
  - New FE: Analog core, digital pix. / architecture, peripheric blocks.
  - Architecture concept simulations.
  - Test setup for full size FE / prototype test.
  - Thinned FE & PbSn → SnAg.
  - Modules with TSV.
  - Lack of time → skipped opto-components / mechanics.

G. Lenzen, Wuppertal



M.Gilchriese, LBNL / G. Lenzen, Wuppertal / P. Schwemling, Paris, b-lay replac. ws, CERN, Feb. 1st 08

K.K.Gan, Ohio, b-lay replac. ws, CERN, Feb. 1st 08

T. Flick, Wuppertal

BK

- BACK UP

BK: Various

- Various

Physics case

- Expend the potential of LHC (measures / discoveries) to 2020 and more, in complement to the future 500-800 GeV e^+e^- ILC. Even with the advent of the ILC, only sLHC can pair produce particles with masses ≥ 0.5 TeV.
- 3 categories for the physics case -for a LHC with 10 x more data-:
  - Precision measurements -standard model physics-:
    - Higgs coupling
    - Trilinear / quadrilinear gauge boson coupling
    - Rare top decays through FCNC
  - Extended mass reach for new particles (by ~0.5 to 1TeV):
    - Heavy Higgs
    - Extra gauge boson
    - Extra dimensions
    - SUSY particle (if heavy)
  - Light SUSY (if light, already discovered at LHC):
    - Complete the sparticle spectrum
    - Access rare decay channel, measure BR

Azuelos *et al*, hep-ex/0203019

x/X0% breakdown

last update 12/13/2007

Material comparison of several module designs											
		x/X0%									
		B-layer present		B1 layer serial pwr r=37mm,16 mod Type = Standard		B1 layer serial pwr r=37mm,16 mod Type A		B1 layer serial pwr r=37mm,16 mod Type C		B2 layer serial pwrl r=49mm, 20 mod. Type = Standard	
Cables (Al 99.9% +polyurethane)		0.285		0.045		0.045		0.045		0.048	
Pigtail flex		0.056		0		0		0		0	
PCB Type 0 cable		0.066		0		0		0		0	
solder		0.009		0.01		0.01		0.01		0.01	
connectors Pigtail + type 0		0.151		0.02		0.02		0.02		0.02	
Total electrical services		**0.567**		**0.075**		**0.075**		**0.075**		**0.078**	
Flex + Components		0.395		0.330		0.230		0.213		0.316	
Sensor		0.27	(250µm)	0.21	(200µm)	0.21	(200µm)	0.21	(200µm)	0.21	(200µm)
FE I3 Chip (bumps)		0.24	(180µm)	0.12	(90µm)	0.12	(90µm)	0.12	(90µm)	0.12	(90µm)
Total Module		**1.471**		**0.736**		**0.635**		**0.618**		**0.724**	
Stave		1.08		0.43		0.43		0.43		0.43	
Global support		0.384		0.082		0.082		0.082		0.082	
Total		**2.935**		**1.248**		**1.147**		**1.130**		**1.236**	

Material	x0 [g/cm2]	x0 [cm]
Al	24,01	8,9
Si	21,82	9,36
Cu	12,86	1,43
Kapton	40,56	28,6
Al2o3	27,94	7,04
Teflon	34,84	15,8
Polyurethane	43,8	

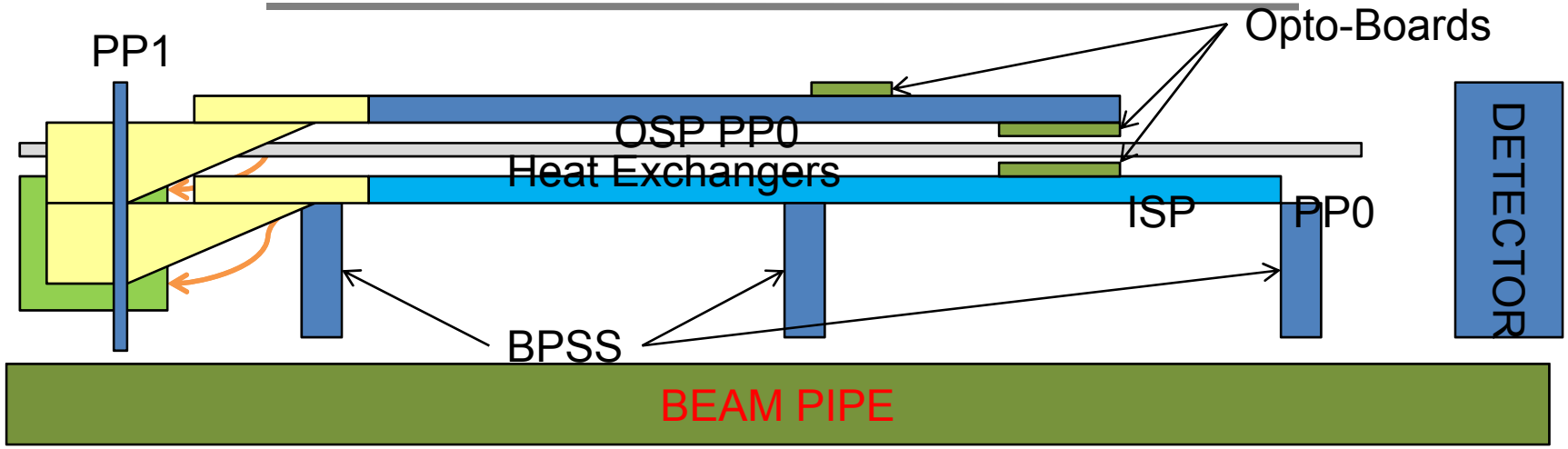
BK: b-layer upgrade

- b-layer upgrade

Why it is so difficult

- The Beam Pipe is supported at PP0 by structures that also support the Services Quarter Panel. They constitute almost *a solid cylinder* around the beam and they have to be removed (at least a part of them) to physically take out the actual B-Layer.
- The SQP's propagate the services from PP0 to PP1. Due to the number of cooling and electrical lines to be unmated (and re-mated) at PP0, the schedule is driven by the activity on the SQP's. Testing the leak tightness of the fitting at PP0 and the electrical part have taken a large amount of time during the integration phase.
- The *beam pipe flange at PP1 has almost the radius of the actual BLayer envelope* (R44 vs. R43) making rather difficult to extract the beam pipe without disassembling the B-Layer. For this reason it has been foreseen to cut one of the two beam pipe flanges in case the actual BLayer will not be kept in. → contamination issue.
- Without disassembling the services *the access from PP1* to the BLayer has a radius of ~R53mm with the beam pipe in it of 36mm [gap of 17mm].

More deeper



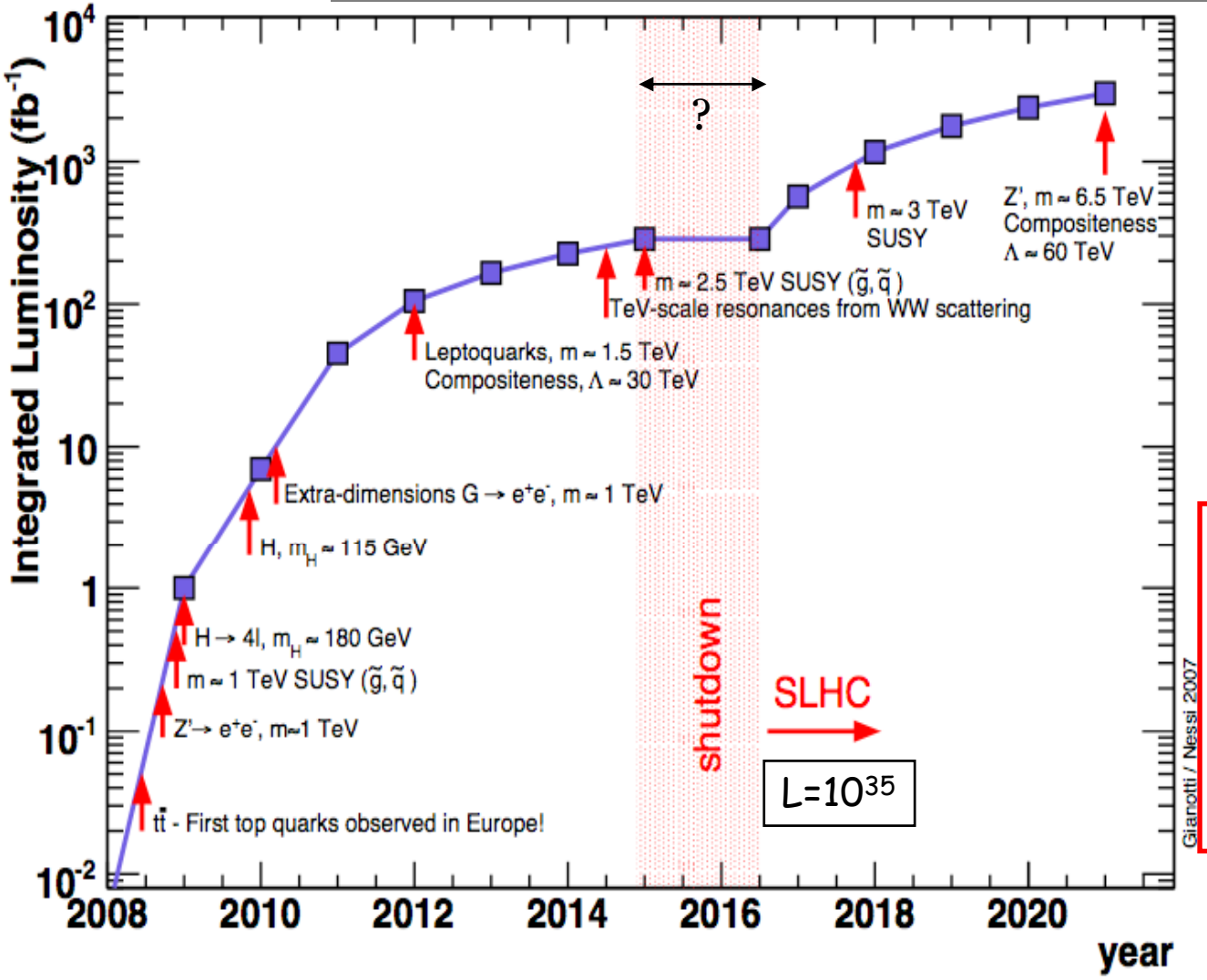
- Removing and reinstalling the SQP's is the most time consuming operation.
- *Case A needs* : to remove 3 SQP's (2 on A +1 on C).
  set an extra PP0 position for the new BL.
  provide 6 extra cooling lines (may get 6 of them from disk lines).
- *Case B needs*: to remove all the SQP's and the BPSS on the both side (no cutting)
  no extra cooling lines are needed.
  no extra PP0 position.

LHC delivery (guess!)

Parameter	Phase A	Phase B	Phase C	Nominal
k / no. bunches	43-156	936	2808	2808
Bunch spacing (ns)	2021-566	75	25	25
N (10^{11} protons)	0.4-0.9	0.4-0.9	0.5	1.15
Crossing angle (μrad)	0	250	280	280
$\sqrt{(\beta^*/\beta^*_{nom})}$	2	$\sqrt{2}$	1	1
σ* (μm, IR1&5)	32	22	16	16
L ($cm^{-2}s^{-1}$)	**$6x10^{30}$-10^{32}**	**10^{32}-10^{33}**	**$(1-2)x10^{33}$**	**10^{34}**

Year ? (present schedule)	2008	2009	2009-2010	> 2010
∫ Ldt ? (guess)	up to 100 pb^{-1}	1-few fb^{-1}	O(10 fb^{-1})	O(100 fb^{-1})

LHC vs time!? (An even wilder guess!)



An obvious fact; any extended shutdown must be agreed on with:

-Overall ATLAS community.

-CMS & LHC communities.

2 scenarios

parameter	symbol	25 ns, small β*	50 ns, long
transverse emittance	ε [μm]	3.75	3.75
protons per bunch	N_b [10^{11}]	1.7	4.9
bunch spacing	Δt [ns]	25	50
beam current	I [A]	0.86	1.22
longitudinal profile		Gauss	Flat
rms bunch length	σ_z [cm]	7.55	11.8
beta* at IP1&5	β* [m]	0.08	0.25
full crossing angle	θ_c [μrad]	0	381
Piwinski parameter	$\phi=\theta_c\sigma_z/(2*\sigma_x^*)$	0	2.0
hourglass reduction		0.86	0.99
peak luminosity	L [10^{34} cm^{-2}s^{-1}]	15.5	10.7
peak events per crossing		294	403
initial lumi lifetime	τ_L [h]	2.2	4.5
effective luminosity ($T_{turnaround}$=10 h)	L_{eff} [10^{34} cm^{-2}s^{-1}]	2.4	2.5
	$T_{run,opt}$ [h]	6.6	9.5
effective luminosity ($T_{turnaround}$=5 h)	L_{eff} [10^{34} cm^{-2}s^{-1}]	3.6	3.5
	$T_{run,opt}$ [h]	4.6	6.7
e-c heat SEY=1.4(1.3)	P [W/m]	1.04 (0.59)	0.36 (0.1)
SR heat load 4.6-20 K	P_{SR} [W/m]	0.25	0.36
image current heat	P_{IC} [W/m]	0.33	0.78
gas-s. 100 h (10 h) τ_b	P_{gas} [W/m]	0.06 (0.56)	0.09 (0.9)
extent luminous region	σ_l [cm]	3.7	5.3
comment		D0 + crab (+ Q0)	wire comp.

early separation (ES)

large Piwinski angle (LPA)

challenges

injector upgrade

Scenarios with 12.5ns & 75ns bs are gone!

aggressive triplet

Pile-up events

Sub-detector upgrade?

Cost Document (USG + EB) **ATL-P-MC-0001** v.**1 (1/2/2006)** as submitted to POFPA – Physics Opportunities for Future Proton Accelerators.

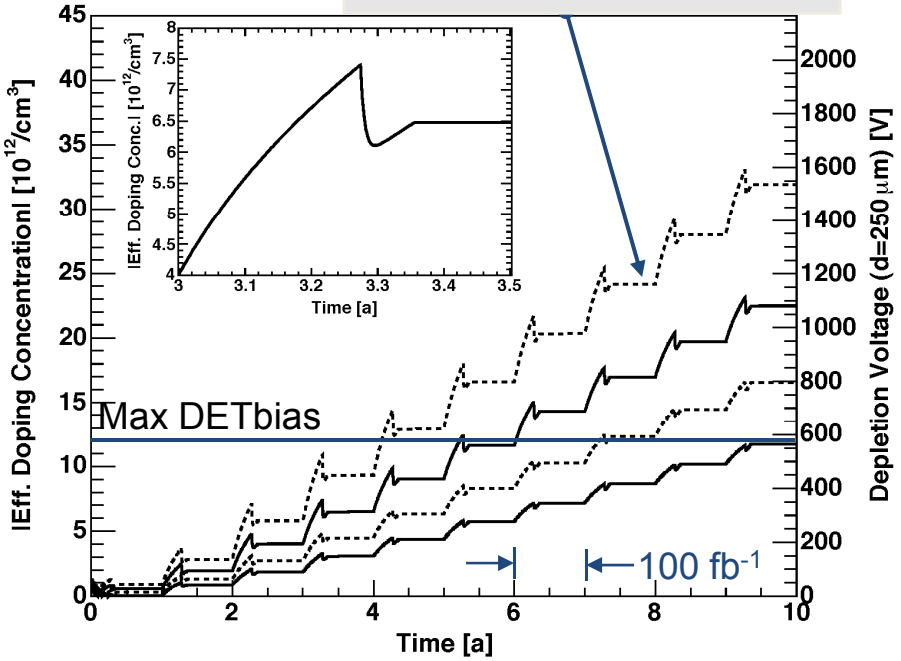
- Some upgrading needed for:
  - Shielding (5 MCHF)
  - LAr Calo (25.5 MCHF)
  - Tile Calo (10 MCHF)
  - Muons (2 MCHF)
  - Trigger / DAQ (10 MCHF)

- Major upgrade needed for inner detector:
  - Pixel + SCT + TRT → all Silicon, Pixel (3/4 layers?) + SS + LS.
  - Pixel (32.5-34 MCHF)
  - SS +LS (105 MCHF -20 MCHF assembly)
  - Installation (10 MCHF -mostly ID)

Why is b-layer upgrade needed?

- Sensor and Electronics are the two most radiation sensitive elements.
  - 1 year of nominal LHC luminosity (100 fb^{-1}) corresponds in the B-layer (5.0 cm) to a NIEL fluence of 2.4× 10^{14} n_{eq}/cm^2 and a Ionizing dose of 12 Mrad (in Si).
- Effect on Sensors
  - Type inversion, Neff increase, Vdepletion rises.
  - Leakage current (noise).
  - Charge trapping → lower charge collected, lower efficiency
- Effects on Electronics
  - Transistor V_T shift due to charge trapping in the gate oxide (Ionizing Radiation). FE and MCC tested to 50 Mrad.
- Studies on n-in-n sensors (BL Workshop) show that BL can operate sometime more than the 3 years foreseen at LHC nominal Lumi. But less than 700 fb-1. More studies needed.
- There is a large incertitude in all the above; only with experience from the running detector we will be able to predict the pixel detector lifetime.

B-layer bias voltage:
T = 0ºC operation,
T = -20ºC no operation,
T = 20ºC for short accesses
+ 50% headroom uncertainty



Not only irradiation

- There are several other events that could degrade significantly the efficiency of the detector:
  - Period of time at higher than foreseen operational temperature of the modules.
  - Leaks in the detector that would force to shutdown a cooling loop (26 modules lost = 10% of b-layer if it occurs there!). Hard to know probability of such event without operating.
  - Failure in the optoboard that serve a significant number of modules (6/7 modules lost = significant loss for the 286 -module b-layer!).

Two scenarios studied

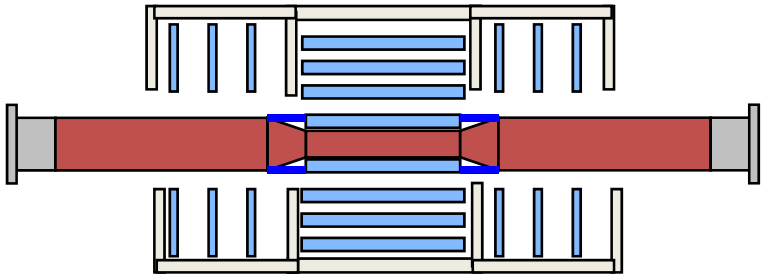
– *CASE A*:

A new B-Layer is *inserted* into the existing one.

The beam pipe carries the B-Layer and it acts as an installation tool.

It does not need to disassemble significantly the detector.

The *con* is the old B-layer stays there adding unnecessary material.

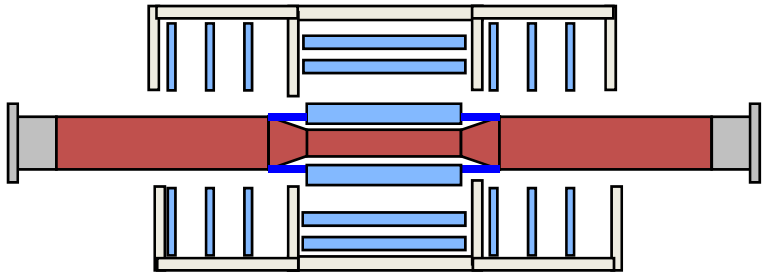


CASE A

– *CASE B:*

The old B-layer is *removed* and a new one is inserted.

This scenario implies a deep disassembling of the detector that has a significant impact on the time scale.



CASE B

Both “A” &”B” requires to move the complete pixel package out of the pit.

Time Estimate Summary

Considering T_0 the time at which we will have *the access to PP1* (i.e. Calorimeter Endcap opened with ~10m clearance on the C-side):

- Limited access: CASE A: 5.5 months
- Barrel access: CASE B: 9.5 months

} In both cases, you need to remove, reinstall and work on the SQP (a very time consuming operation).

- + Some weeks are needed to *open ATLAS* up enough to remove the Pixel detector:
  - Put the ECT in the parking position.
  - Open the EC calorimeter.
  - Setting up the working area:
    C-Side need clear from IDEP to the Shaft C (~ 10m)
    A side needs a gap (~1m)
- *+ 8 weeks for installing and re-connecting* the detector (and this is an aggressive estimate!)
- + the complication of the activation.

The two options studied (CASE A and B) *do not fit into the 6 months time shut down*.

Note that two alternatives semi-exists:
-"in-pit" replacement, not removing the Service Quarter Panel -main time driver- & find some way to work around them: qualified of "desperate" by mechanical people.
-Build a brand new pixel detector with even a limited number of layers waiting to be installed as soon as the old one gets out → cost issue.

- Extended shut-down? Of Atlas and CMS for 1 pixel-layer?

What to do Next - ATLAS Task Force

- An ATLAS task force will be nominated with the mandate to review the situation and present to the collaboration an updated plan for the B-layer and Pixel system evolution in ATLAS (in a 6 months timescale). The task force will be established at EB level and reports at TMB/EB level - and also as appropriate in ID, Pixel and Upgrade meetings.

- The task force should consider the following points:
  - The expected lifetime of the PIXEL system and critical components that might change the lifetime
  - Machine upgrade plans and expected luminosity profiles
  - Time estimates, risks, procedures for, and activity levels related to changing/adding layers for the Pixel system. This included compatibility with INB regulations and concerns both work in situ and on the surface.
  - Simulations studies for extra layers or changed layouts
  - Interfaces to and compatibility with a complete ID upgrade
  - Time scales and costs
  - Possible changes to the central beampipe
  - Key issues to study during initial running (physics, operational issues) that can provide guidance for future upgrades of the Pixels.
  - Other points as deemed necessary

Task Force (2)

- Several options must be considered, and their feasibilities studies, keeping in mind the points above for each of them:
  - Replacing the current B-layer with a similar layer (current baseline)
  - Adding a new layer inside the current system
  - Replacing the entire PIXEL system with a new system as ambitious as possible
  - Keeping several options open but defining a plan (in time and identifying key issues) that can guide us towards a decision in the coming years.
  - Permutations/derivations/ developments of the above.

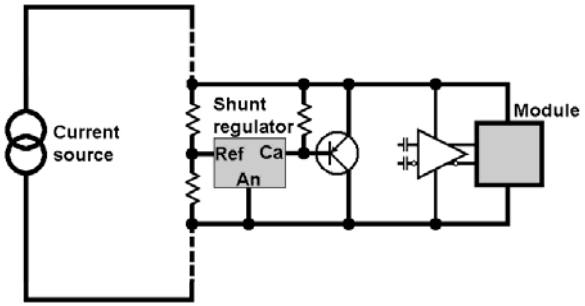
- Practical constraints:
  - Basic R&D for the Pixel upgrade must be encouraged to continue during this process and as part of the revised plan.
  - The b-layer replacement budget line in M&O must be kept open, in all scenarios there is a well-defined inner layer that will be a focus for development and early change.
  - The PIXEL upgrade community must be kept together working on a common framework as a result of any new plan.
  - In absence of a replacement plan we have no flexibility in the vertexing system (B-layer is a kind of unique layer in the B-tagging). On the other way CMS has simple mechanical replacement. The unbalance situation of the two experiment has to be corrected.

BK: Powering

- Powering / DCS

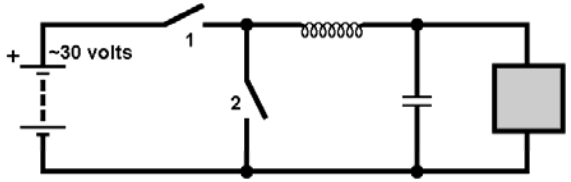
How does it work?

Minimize current through cables by
a) recycling current (SP) or b) "high-voltage" power lines (DC-DC)



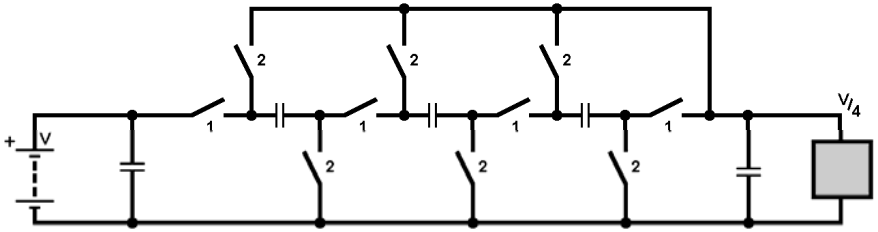
Serial powering

Talks by Wladek, Mitch, Michael, Giulio and Jan



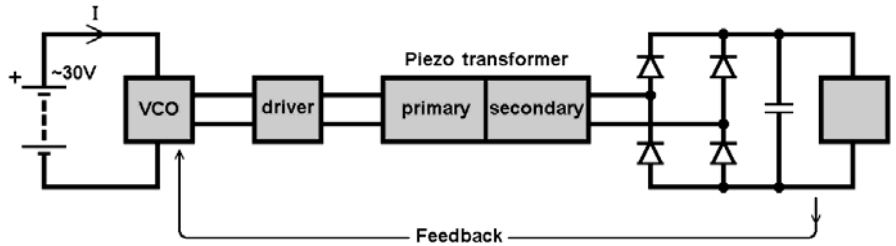
DC-DC buck converter

Talks by Federico and Satish



DC-DC charge pump

Talk by Maurice



Piezo transformer

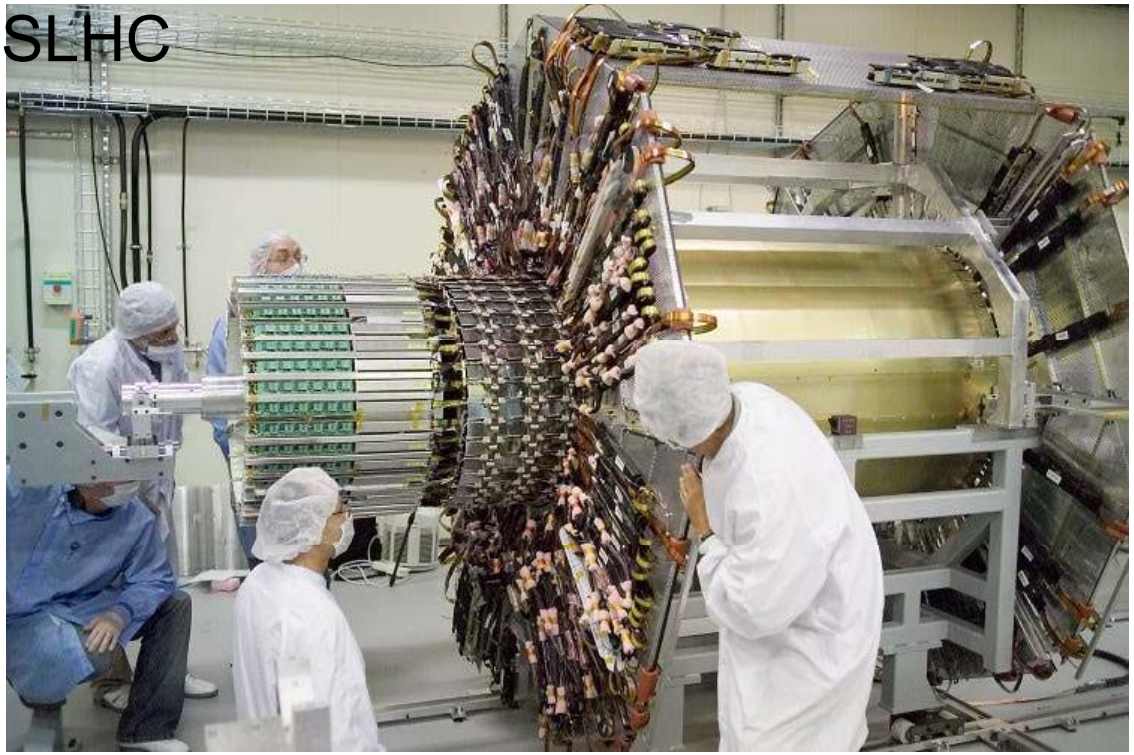
Talk by Masatoshi

Why independent powering fails at SLHC ?

Current per chip ~ constant, but many more channels

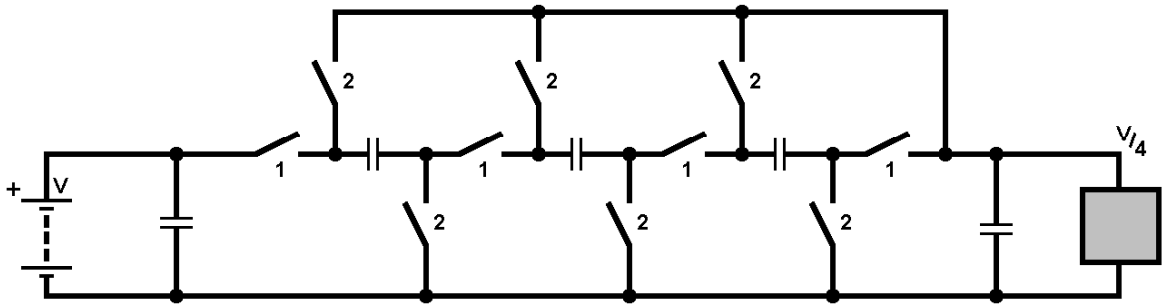
1. Don’t get 5 or 10 times more cables in
2. Power efficiency is too low (50% ATLAS SCT ⇔ ~15% SLHC)
3. Cable material budget: 0.2% of R.L. per layer (barrel normal incidence) ⇔ 1% or 2% SLHC
4. Packaging constraints

Each reason by itself is probably sufficient for a No-No

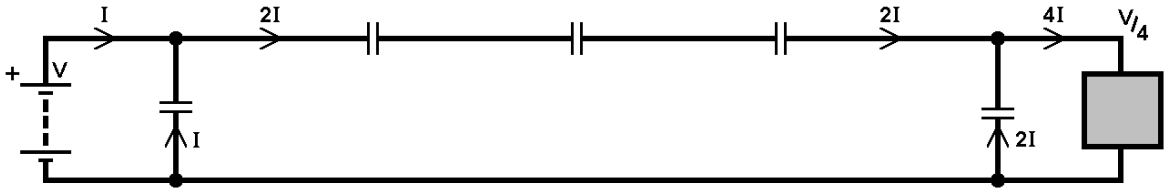


DC-DC conversion with switched capacitors

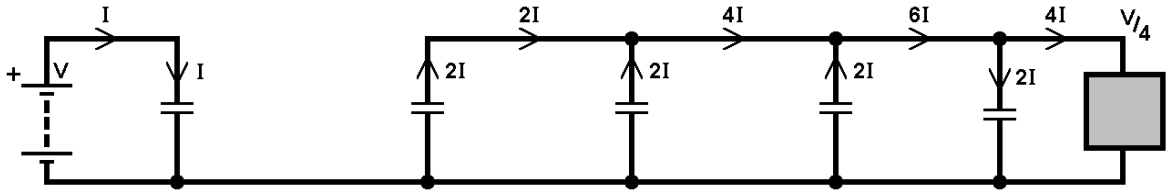
Example: divide by 4 stack: 5 capacitors – 10 switches



Phase 1 - Charge



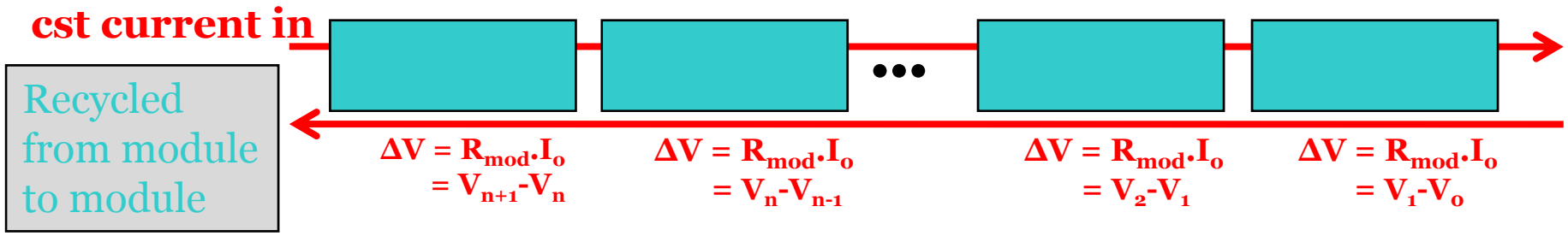
Phase 2 - Discharge



Charge and discharge different arrangements of capacitors to convert "high" input voltage to low module voltage

Challenge is design of switching chip and to supply sufficient current

Using SP

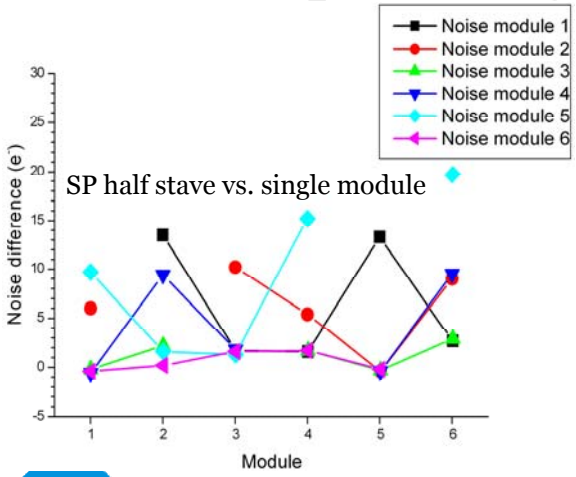


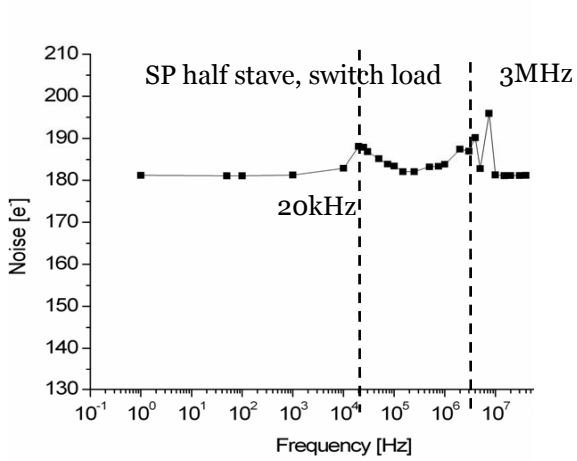
- Fight cable congestion.
- Increase power efficiency.
- Less power dissipation in cables.
  - Reduction factor 20-30, despite 20-30% more in the modules.
  - PP4 – PP2: 91W per stave → 3.4 W; PP2 – PP1: 22 W → 0.8W
- Reduce material in active area.
  - Factor < 1/10 X_0 of present cable/connectors.

Proof of principle

- Serially Powered half-stave with FE-I3 modules.

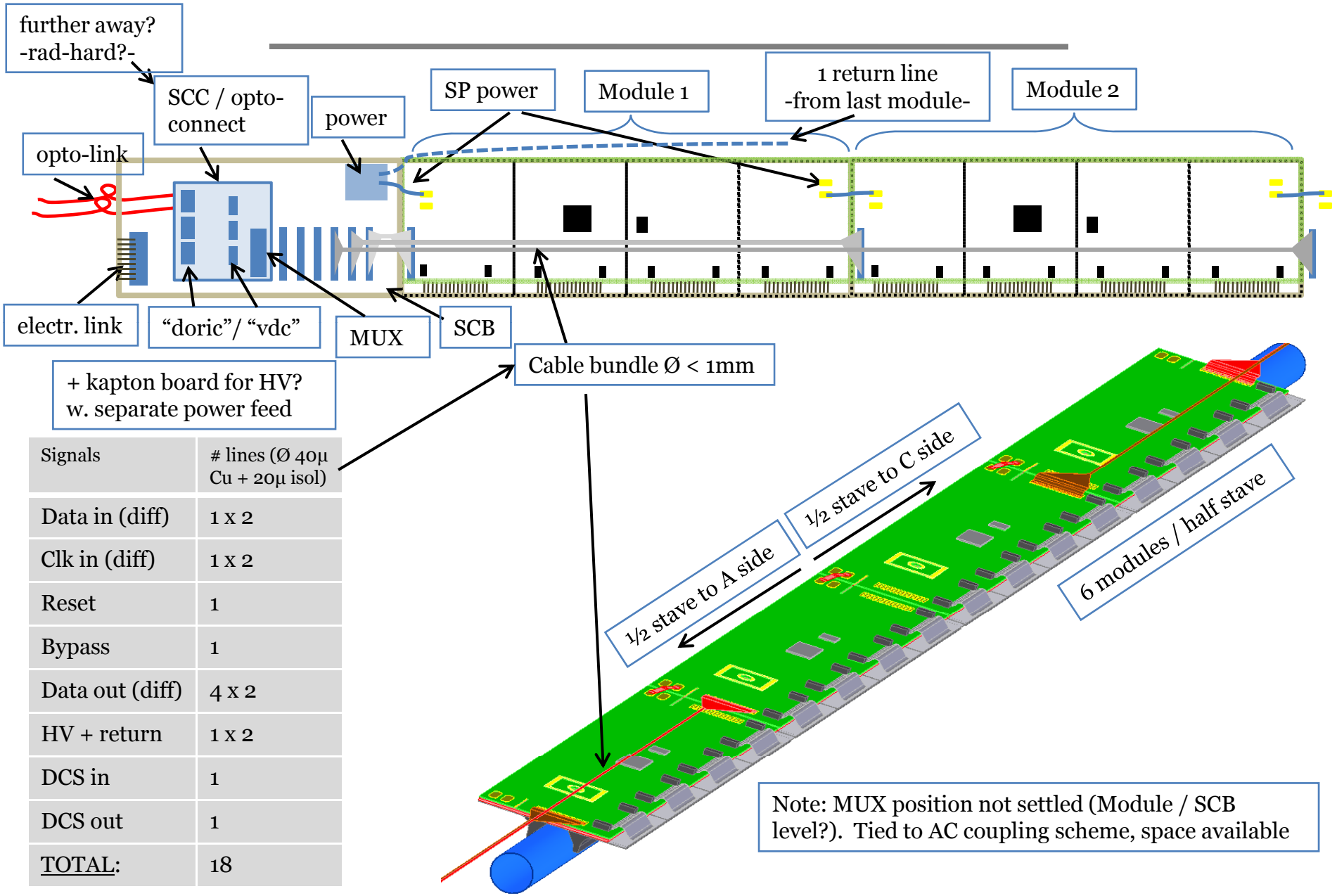
- Could show that there is no performance degradation due to the powering scheme, in particular wrt noise pickup.





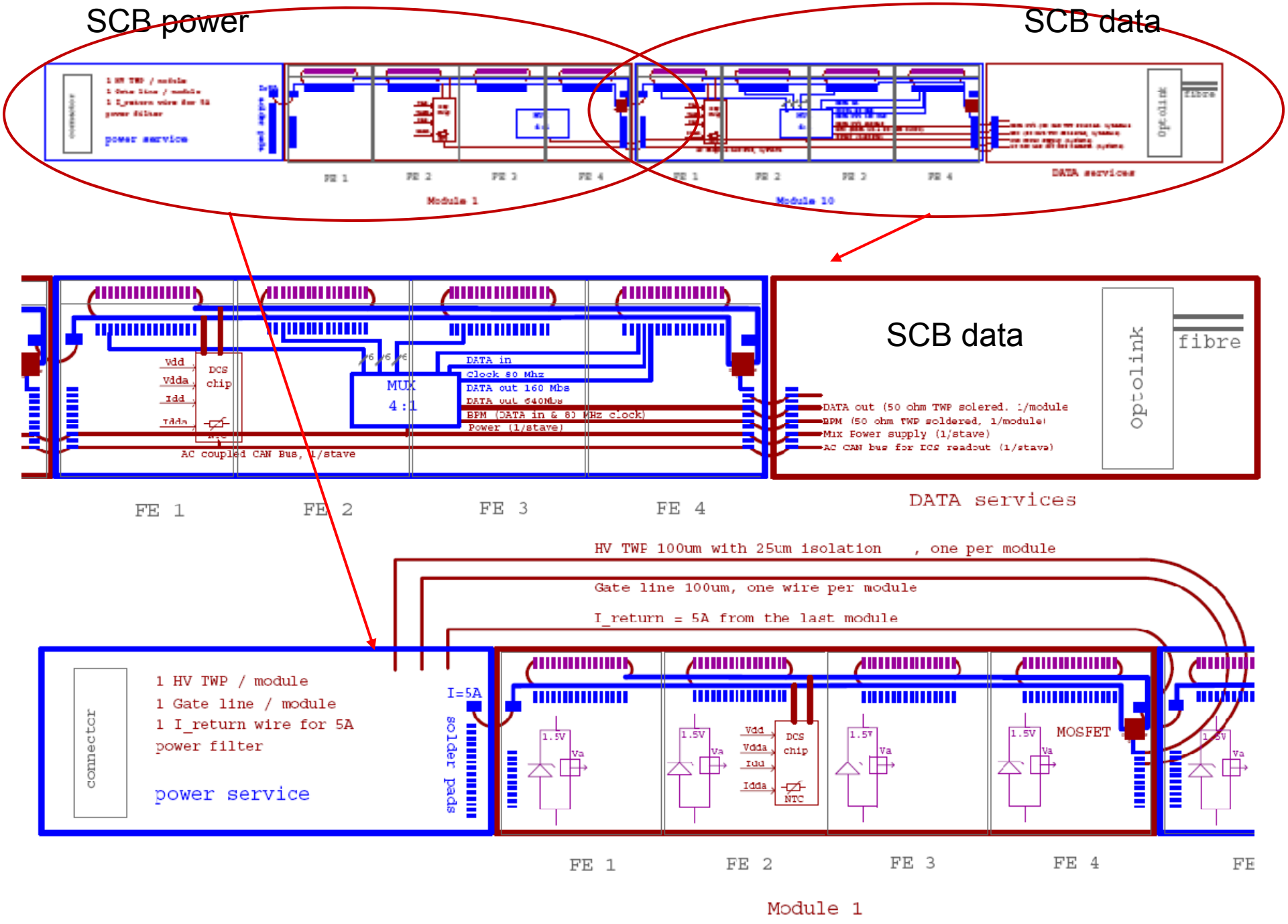
Duc Bao Ta, Bonn -2005-
(D.B.Ta *et al*, NIM A 557 (2006) 445-459)

Stave



Signals	# lines (Ø 40µ Cu + 20µ isol)
Data in (diff)	1 x 2
Clk in (diff)	1 x 2
Reset	1
Bypass	1
Data out (diff)	4 x 2
HV + return	1 x 2
DCS in	1
DCS out	1
TOTAL:	18

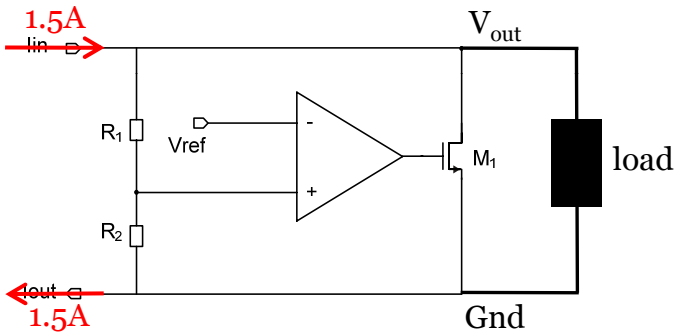
Note: MUX position not settled (Module / SCB level?). Tied to AC coupling scheme, space available


SCB power
SCB data
power service
Module 1
Module 10
DATA services
optolink
fibre
Vdd
Vdda
Idd
Idda
DCS chip
MUX 4:1
DATA in
Clock 80 Mhz
DATA out 160 Mbs
DATA out 640Mbs
BPM (DATA in & 80 MHz clock)
Power (1/stave)
AC coupled CAN Bus, 1/stave
DATA out (50 ohm TWP solered. 1/module
BPM (50 ohm TWP soldered, 1/module)
Mix Power supply (1/stave)
AC CAN bus for DCS readout (1/stave)
FE 1
FE 2
FE 3
FE 4
HV TWP 100um with 25um isolation , one per module
Gate line 100um, one wire per module
I_return = 5A from the last module
connector
1 HV TWP / module
1 Gate line / module
1 I_return wire for 5A
power filter
power service
I=5A
solder pads
1.5V
Va
Vdd
Vdda
Idd
Idda
NTC
MOSFET
Module 1

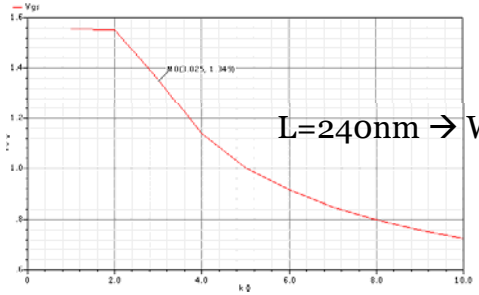
Shunt regulator in FE-I4

- 1st feasibility studies, IBM 130nm.
- Shunt and load.
- 4-5 A at module level (4FE/module).

Michael Karagounis



- Transistor area???
- ΔV~1.6V→ Vgs<=1.4-1.3V (keep amplif. output stage saturated)



A_{trans}=3mm*(240nm + 2*550nm)= 4000μm²

- Electromigration rules???
- At pad level: pad for next FE not yet developed → use standard IBM pad for estimate:

Pad Cell	Metal Stack	Width(um)
PAVDD	M2/M3	30.1
PAVSS	M2/M3	34.64

$I_{max} = 3.12mA.\mu m^{-1}(W - 0{,}06\mu m)$

$I_{max\,PAVSS} = 216mA$ ← Also ok for wire-bond!

pads: 8 VDD, 7 VSS

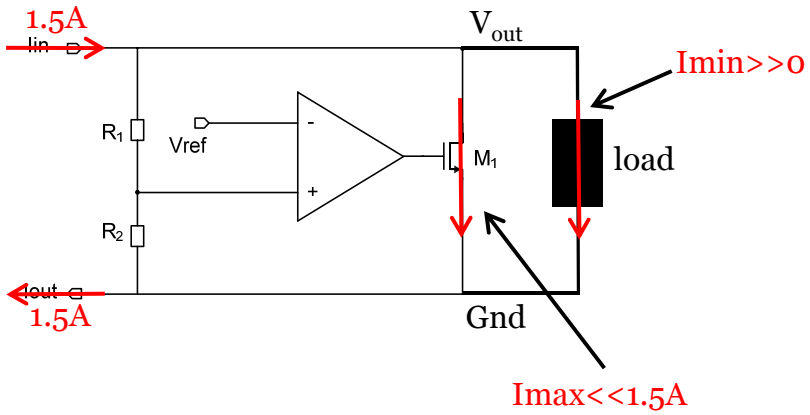
$I_{max\,PAVDD} = 187mA$

Refining what the shunt regulator should be

- Could handle special conditions: over current protection (better power-up conditions), fine reference correction (uniformize currents in // placed shunts).

Wladyslaw Dabrowski

- Shunt transistor could be distributed. Take care of properly dissipating power.
- Should not have to handle the complete current of the load! Load should be in an already controlled state by pre-setting DACs.



experience from the past

examples:

- **wrong powering of the module → MCC does not work correctly → cause a data transfer error**
  - DCS powering information helps to detect the not working MCC
- **problems with module configuration or clock signal → no data acquisition**
  - incorrect module configuration or clock signal cause a characteristic digital current consumption
  - DCS current data give information about the reason of the broken data acquisition
- **optoboard receives no light → noisy DORIC**
  - high oscillation of digital and analogue current
  - DCS information necessary to find out the broken pin diode
- **high voltage broken → noisy module**
  - cause a higher digital current and a higher temperature
  - HV modularity 6/7 → only DCS current and temperature information can detect the noisy module

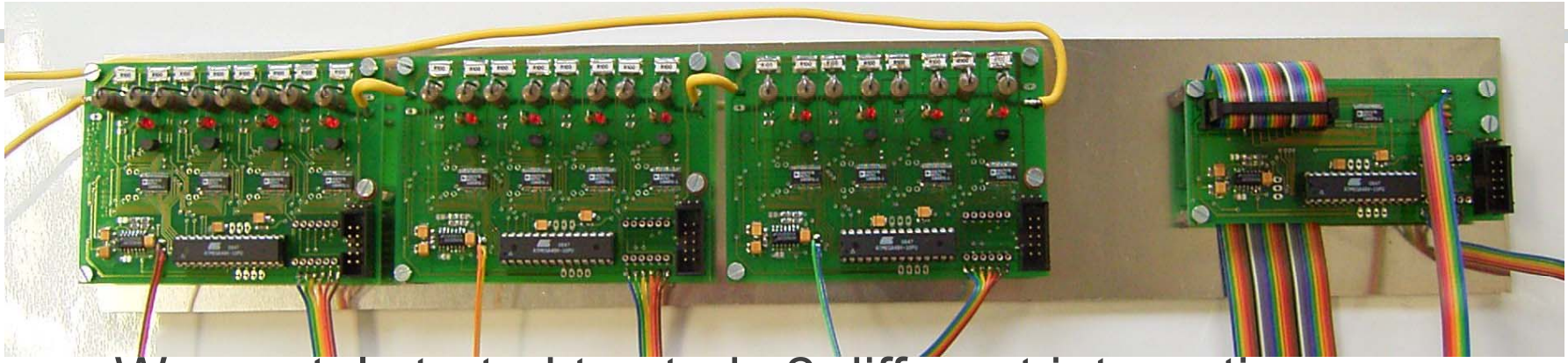
→ DCS data important to get information about a problem!

DCS specifications

- independent DCS data path fundamental to identify problems
- reduce the radiation length
- high granularity → in case of a broken DCS component keep as much DCS information as possible
- separate disabling of each FE chip → DCS part of the FE chip should remain working
- DCS data of each front end chip:
  - analogue voltage
  - digital voltage
  - 2 currents (for analogue and digital part)
  - temperature

} 5 signals per FE

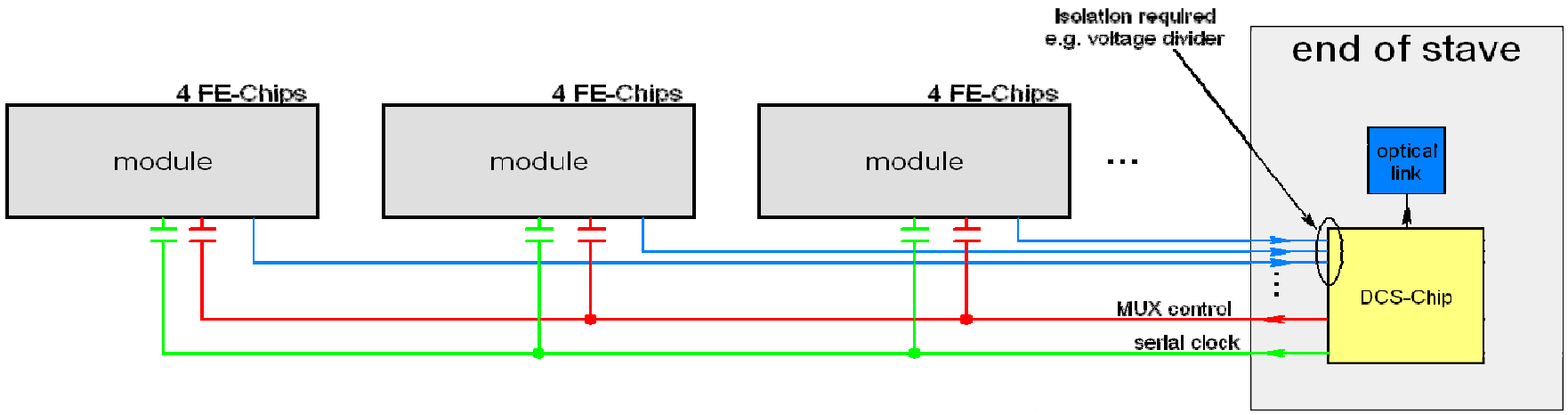
Different integration schemes of the DCS chip



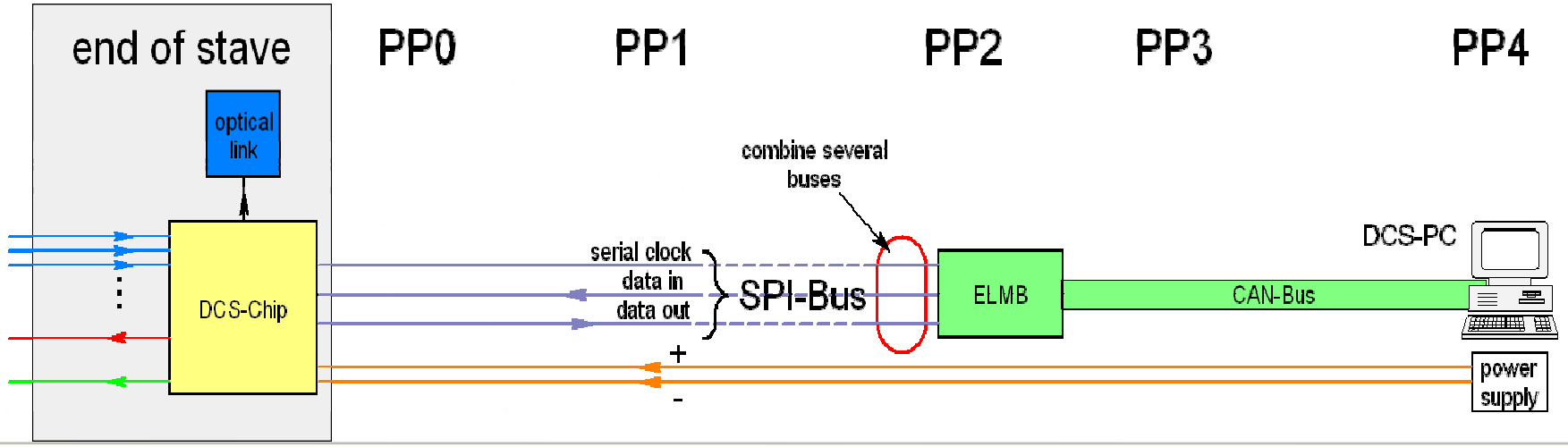
- Wuppertal started to study 2 different integration schemes
  - DCS chip at the end of stave
  - DCS chip on the module

Same setup is used

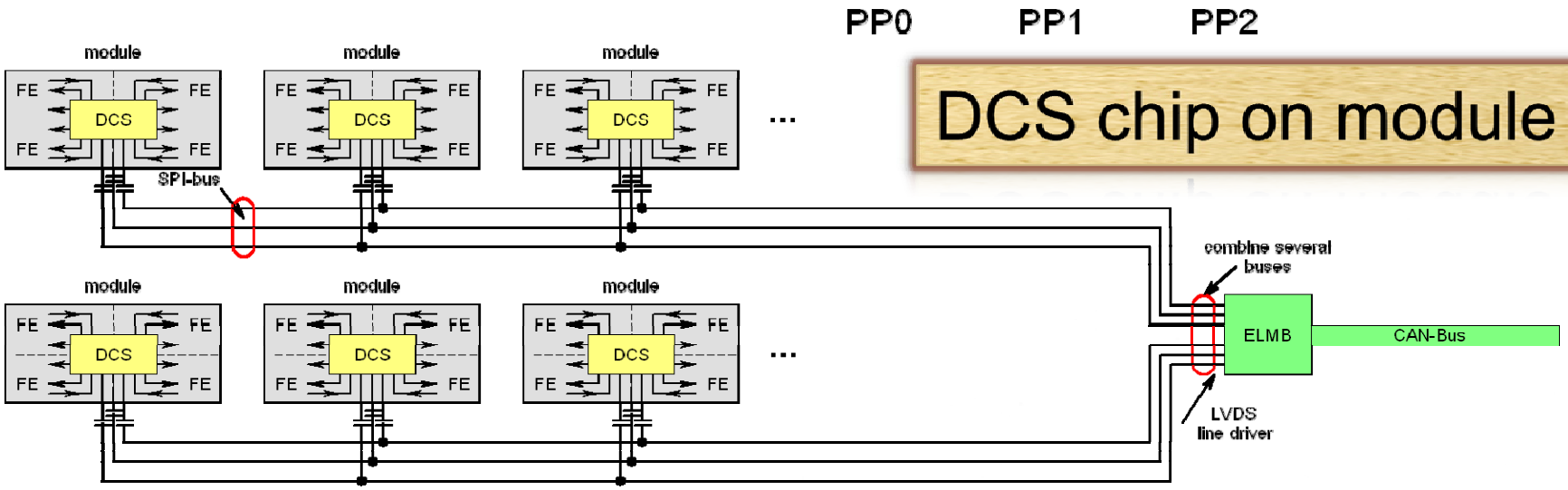
- DCS part in every FE chip has to be implemented:
  - need a multiplexer in every FE chip
  - DCS part delivers via the multiplexer the DCS monitoring values to the DCS chip
  - Acting on the optical link if at end of stave



DCS chip at end of stave



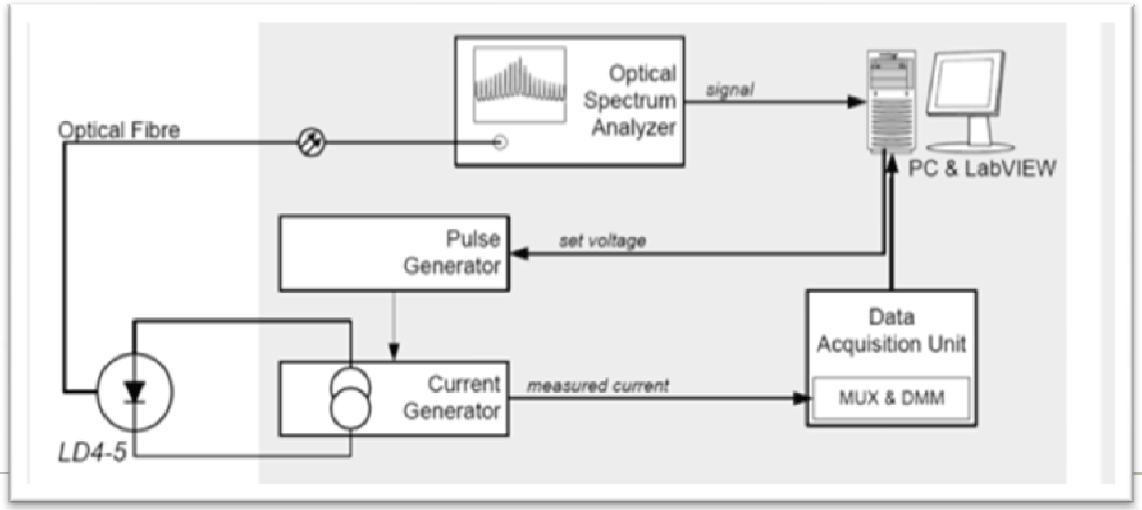
DCS chip on module



- per FE chip 5 wires (differential voltage measurement, MUX address, disable FE)
- per stave bus system
- broken DCS chip → no DCS data of one module
- broken bus cable → no DCS data of one stave
- additional material → DCS chips + cables
- independent DCS data path

Optical Link

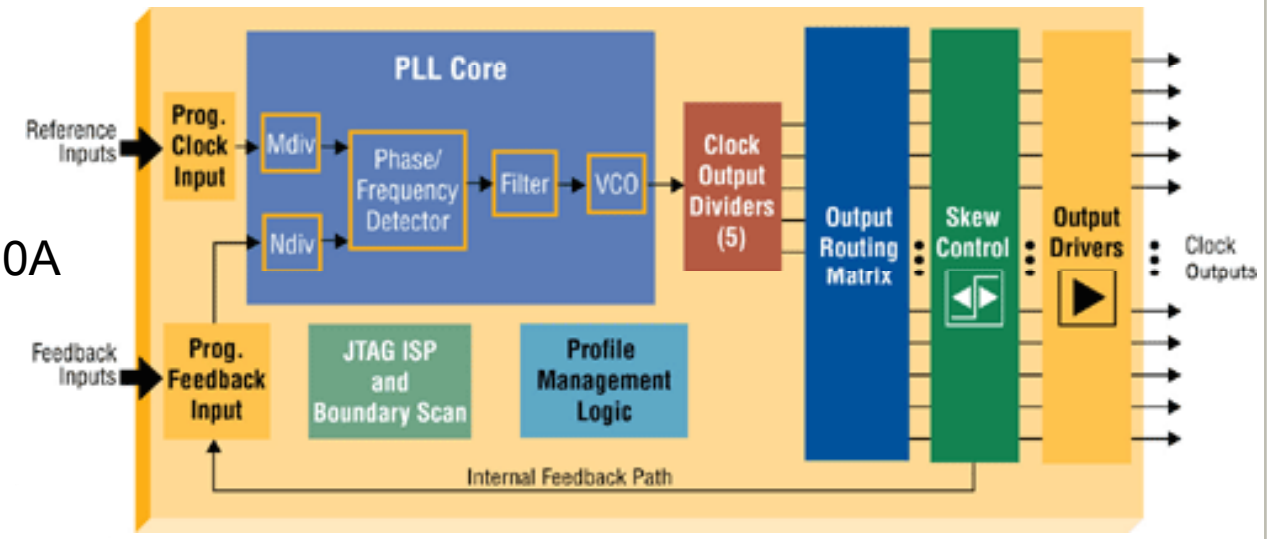
- A new optical link has to cover a much higher bandwidth for data transfer (step from 160 Mb/s to 640 Mb/s)
- Studies concerning the optical components are under preparation
  - Radiation hardness of lasers
  - Thermal conductivity and heat sink optimization
  - Speed of the link (laser switching speed, data recovery, etc.)
  - Properties like wavelength, single mode or multi mode fibres etc.



Optical Readout Hardware

- Studies on the electrical side for the new readout hardware are on the way
  - Tests of new clock chips and clock distribution strategies
  - Faster signal encoding under test, using Lattice CPLDs

ispClock5600A



conclusions & future plans

- overview about the different schemes for the DCS chip
  - DCS data aquisition via the optical readout system
  - DCS chip at the end of the stave
  - DCS chip on the module
- DCS chip on the module seems to be the prefered option → minimal radiation length, high modularity
- next step is to run the Wuppertal test setup and to concretize the schemes (e.g. bus system, decoupling…)

BK: Pixel Layout vs Physics

- Pixel Layout vs. Physics

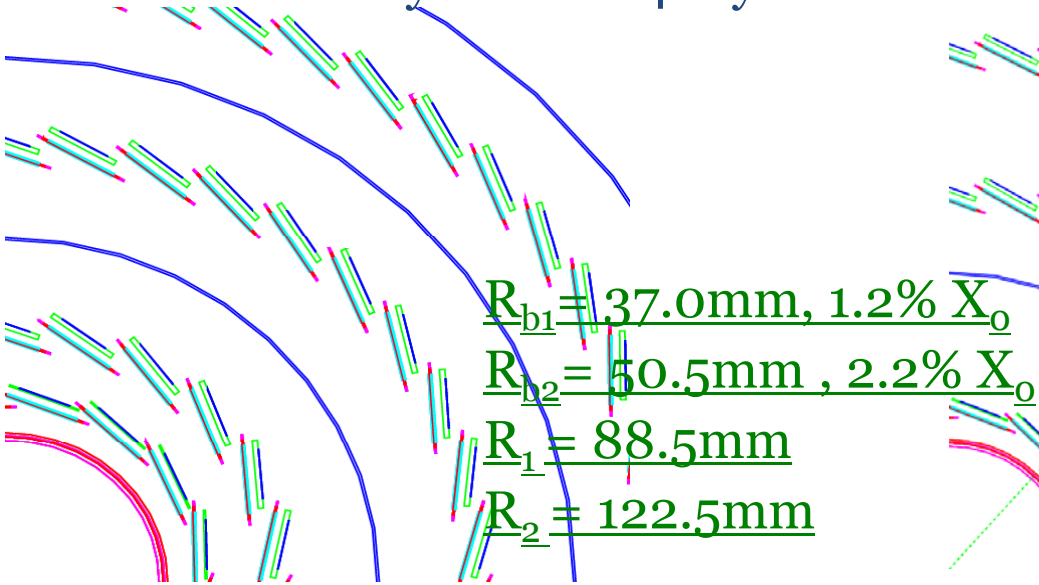
(slides from Vadim Kostyukhin, Genova, shown at Valencia Upgrade Workshop)

3 vs 4 Pixel Layer

From the B-Layer Workshop there are indications (more studies required):

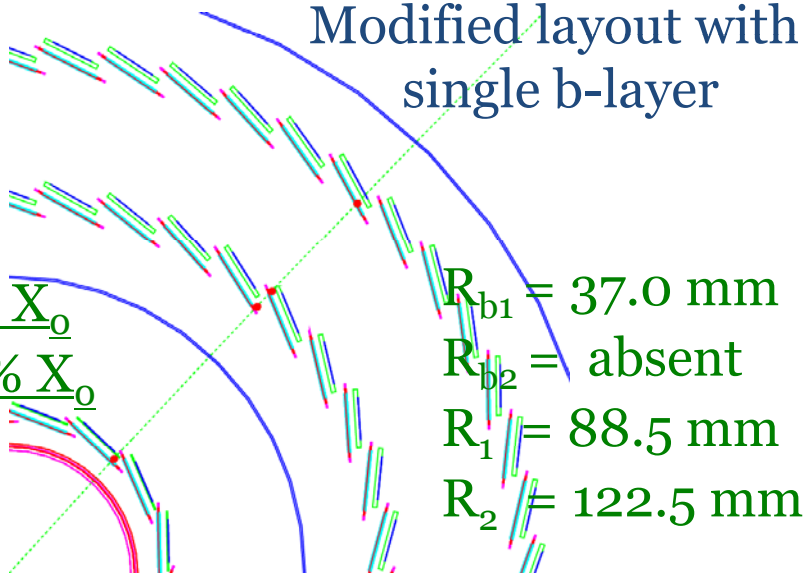
- Adding a fourth layer barely resume the initial Pixel detector performance. Material is a critical issue, smaller pixels (250 μm in Z) help, what happens with dead (or low efficiency) existing BL has to be studied.

Layout with 4-layers



R_{b1} = 37.0mm, 1.2% X_0
R_{b2} = 50.5mm , 2.2% X_0
R_1 = 88.5mm
R_2 = 122.5mm

Modified layout with single b-layer



R_{b1} = 37.0 mm
R_{b2} = absent
R_1 = 88.5 mm
R_2 = 122.5 mm

A surprise: Reduction of material is probably more important than reduction of radius & 4 working pixel layers might have worse performances than 3 working ones!

Some (preliminary) conclusions

1. To improve low $P_{\perp}$ jet rejection B-layer should be moved closer to interaction point.
2. To improve high $P_{\perp}$ jet rejection amount of material should be decreased.
3. Change of Z pitch of other pixel layers (not B one) doesn't have big influence on b-tagging performance at 0 luminosity limit. Should be much more important at 10^35.
4. Double B-layer doesn't have advantages with respect to single B-layer in b-tagging. Should be checked however for very high $P_{\perp}$ jet.
5. Beam pipe has non negligible impact on b-tagging performance.

SI LAB
Silizium Labor Bonn

ATLAS Pixel Detector Collaboration

b-layer material influence

L2444 layout, B(37mm) ~1.2% thickness, others ~2.2%
Dependence on B_2(50.5mm) thickness
WH120

Type, ε_b	X_{b2}=2.2%X0	X_{b2}=1.6%X0	X_{b2}=1.2%X0	L2044 (no b2)
2D 60%	78 ± 4	122 ± 2	135 ± 8	172 ± 11
2D 70%	26 ± 1	39 ± 1	42 ± 1	46 ± 2
3D 60%	160 ± 10	244 ± 21	262± 21	351± 33
3D 70%	43 ± 1	64 ± 2	69 ± 3	88 ± 4
SV1 60%	501 ± 56	743 ± 36	774 ± 102	1176 ± 197
SV1 70%	90 ± 4	131 ± 7	155 ± 9	219 ± 16
SV2 60%	508 ± 57	750 ± 98	717 ± 92	1035 ± 165
SV2 70%	89 ± 4	124 ± 7	145 ± 8	199 ± 14

b-layer material influence

L2444 layout,B(37mm)~1.2% thickness, others~2.2%
Dependence on B_2(50.5mm) thickness
WH400

Type, ε_b	X_{b2}=2.2% X0	X_{b2}=1.6% X0	X_{b2}=1.2% X0	L2044(no b2)
2D 60%	52 ± 2	64 ± 2	57 ± 2	75 ± 13
2D 70%	20 ± 1	22 ± 1	21 ± 1	25 ± 1
3D 60%	81 ± 3	92 ± 3	90± 3	134 ± 6
3D 70%	29 ± 1	33 ± 1	31 ± 1	37 ± 1
SV1 60%	230 ± 15	258 ± 16	271 ± 17	443 ± 36
SV1 70%	77 ± 3	95 ± 4	97 ± 4	140 ± 6
SV2 60%	226 ± 14	240 ± 14	257 ± 16	424 ± 34
SV2 70%	71 ± 3	88 ± 3	87 ± 3	128 ± 6

For both WH400 and WH120 decrease of thickness of B_2 layer produces improvement in b-tagging but the best idea is to remove it completely.

Material influence

WH120, L2044, all layers ~1.2%

Eff. to find sec.vertex in uds jet(fake)	1.95%
Eff. to find sec.vertex in b jet(true)	69.9%

	60%	70%
2D	195 ±13	53 ± 2
Z	32 ±1	10± 0.2
3D	440 ±46	93 ± 4.4
SV1	1110 ±180	210 ±15
SV2	1090 ±174	182 ±12

WH400, L2044, all layers ~1.2%

Eff. to find sec.vertex in uds jet(fake)	4.60%
Eff. to find sec.vertex in b jet(true)	76.6%

	60%	70%
2D	96 ± 3.7	41±3
Z	18 ±0.3	7 ± 0.1
3D	165 ± 8	47 ± 1.2
SV1	605 ± 58	166 ± 8
SV2	524 ± 47	150 ± 7

WH120, L2044, all layers ~2.2%

Eff. to find sec.vertex in uds jet(fake)	2.78%
Eff. to find sec.vertex in b jet(true)	69.8%

	60%	70%
2D	109 ± 5	36 ± 1
Z	25.8 ± 0.7	9.4 ± 0.1
3D	234 ±18	60 ± 2.2
SV1	730 ± 95	140 ± 8
SV2	635 ± 77	136 ± 8

~70% rejection degradation

WH400, L2044, all layers ~2.2%

Eff. to find sec.vertex in uds jet(fake)	6.21%
Eff. to find sec.vertex in b jet(true)	76.6%

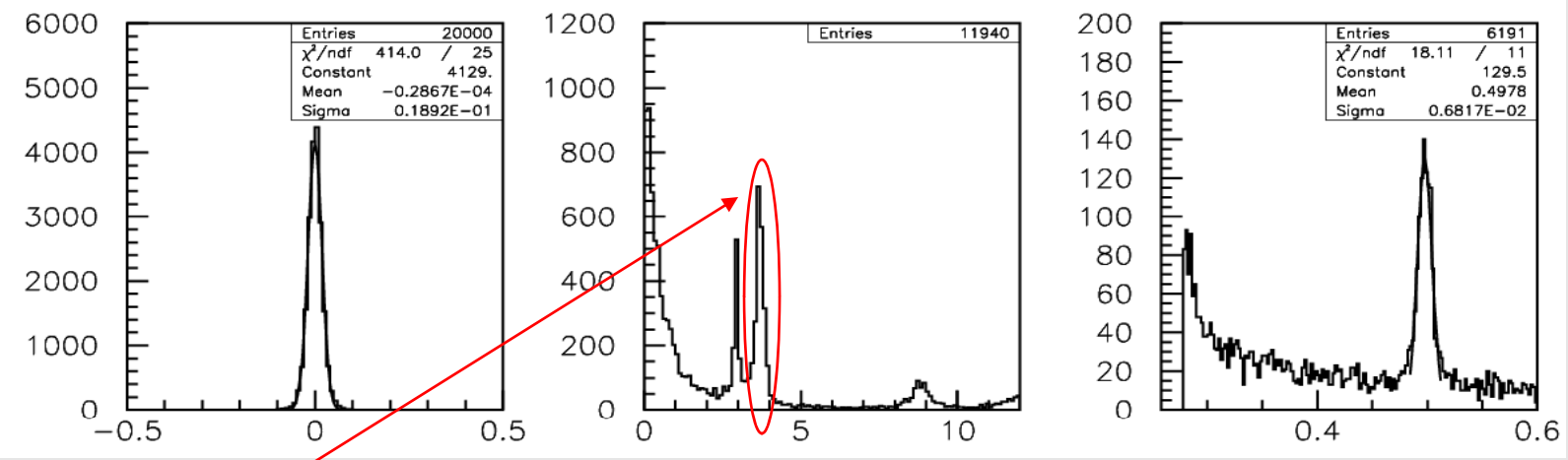
	60%	70%
2D	40 ± 1	11 ± 0.1
Z	9.7 ± 0.1	3.4± 0.1
3D	63 ± 2	16.6 ± .3
SV1	210 ± 12	49 ± 1
SV2	190 ± 10	45 ± 1

~270% rejection degradation

Decrease of material is useful for everything.
Effect is much bigger for WH400 (higher jet $P_{\perp}$)

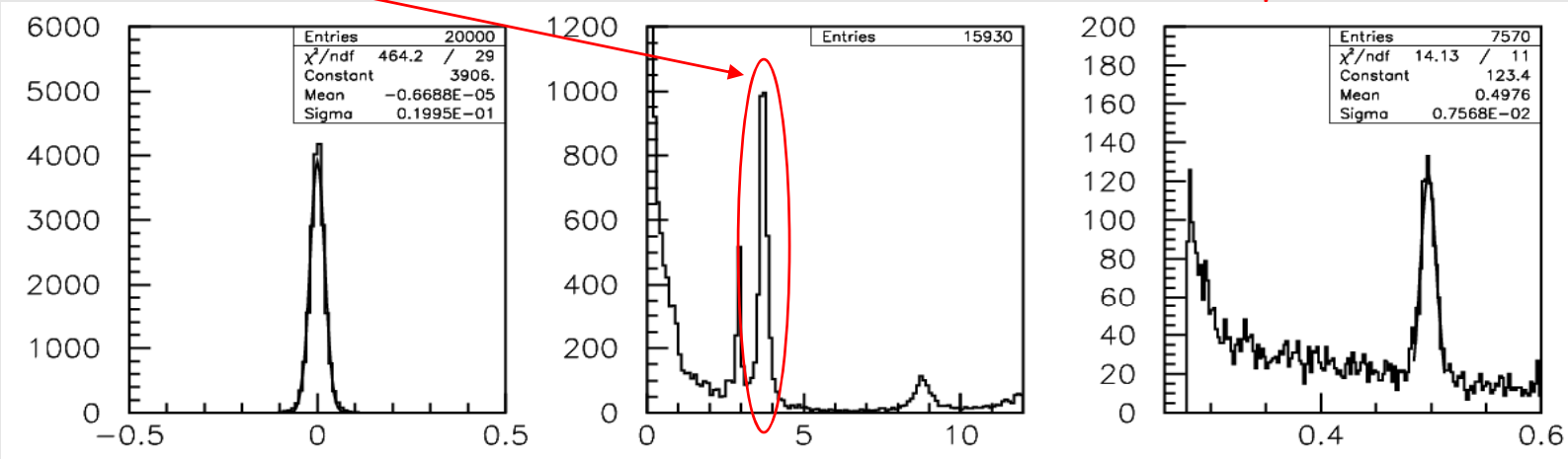
More material influence

L2044, WH400, all layers X0≈1.2%



More material is visible

L2044, WH400, all layers X0≈ 2.2%



Material increase=>

Small degradation of Z prim. vertex resolution 19μm→20μm,
small degradation of K^0 mass resolution 6.8MeV→7.6MeV,
Huge ~270% degradation in b-tagging rejection

Z pitch in L2,3(88.5mm,122,5mm) influence

L2022, WH120, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	1.81%
Eff. to find sec.vertex in b jet(true)	70.2%

	60%	70%
2D	160 ±13	52 ± 2
Z	32 ±1	11± 0.2
3D	325 ±29	82 ± 3.6
SV1	1580 ±300	214 ±15
SV2	1140 ±190	196 ±13

L2022, WH400, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	4.40%
Eff. to find sec.vertex in b jet(true)	76.4%

	60%	70%
2D	99 ± 3.8	33 ± .7
Z	19 ±0.3	7 ± 0.1
3D	188 ± 10	52 ± 1.5
SV1	619 ± 60	177 ± 9
SV2	554 ± 50	156 ± 8

L2044, WH120, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	1.95%
Eff. to find sec.vertex in b jet(true)	69.9%

	60%	70%
2D	195 ± 13	53 ± 2
Z	32. ± 0.9	10 ± 0.2
3D	441 ±46	93 ± 4.4
SV1	1110 ± 180	209 ± 15
SV2	1090 ± 174	182 ± 12

L2044, WH400, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	4.61%
Eff. to find sec.vertex in b jet(true)	76.6%

	60%	70%
2D	96 ± 4	28 ± 0.2
Z	18 ± 0.3	7.1± 0.1
3D	165 ± 8	47 ± 1.
SV1	605 ± 58	166 ± 8
SV2	524 ± 47	150 ± 7

Increase(!!!) in tracking part and degradation in track+vertex

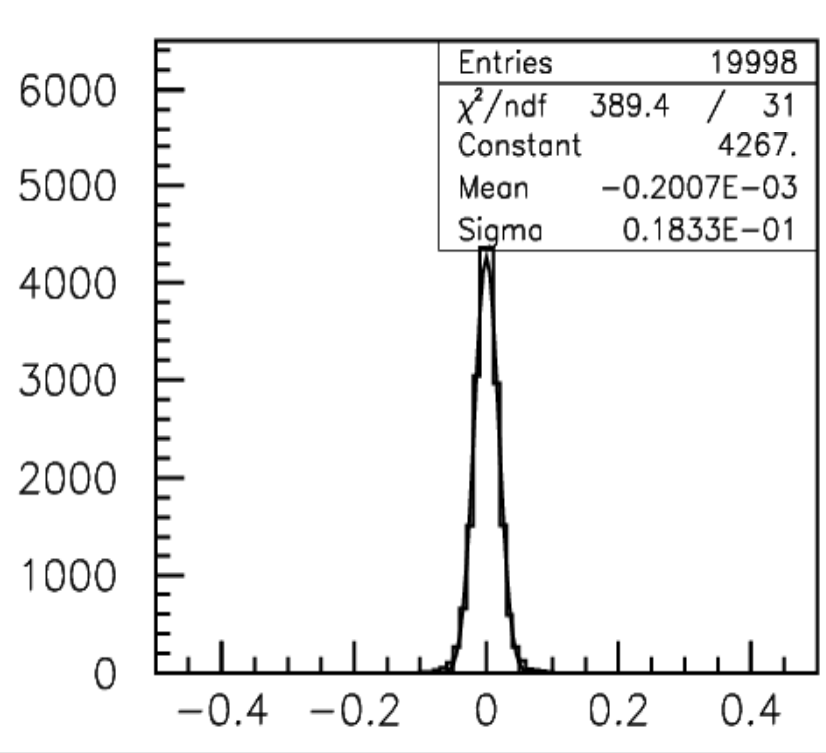
~5% degradation

Behavior is not completely clear but in any case changes are small.

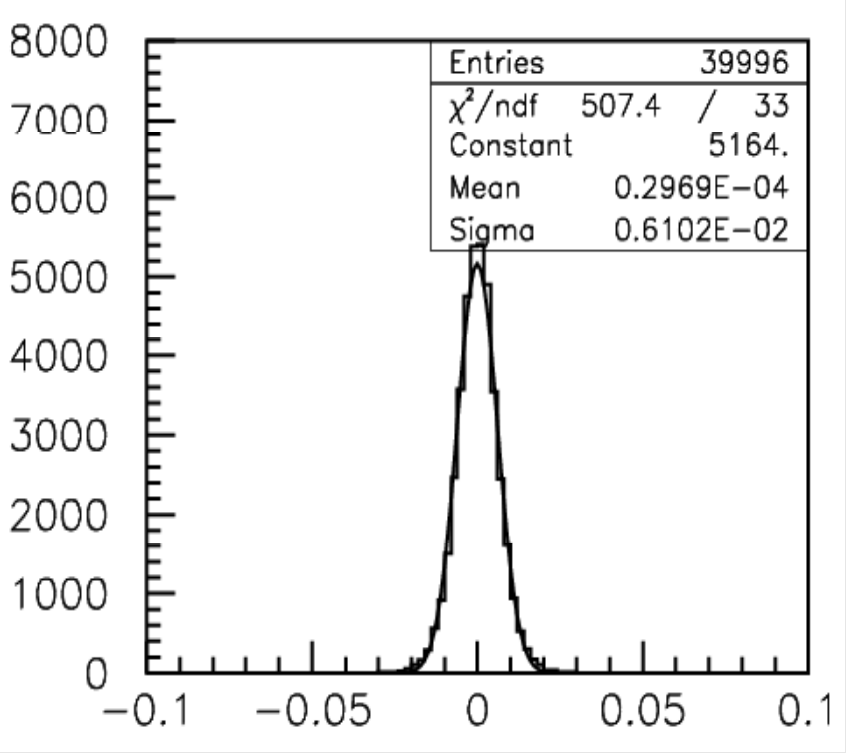
Keep in mind that this is 0 limu case!!!

Z pitch in L2,3(88.5mm,122,5mm) influence

L2022, WH400→uu
Primary vertex Z resolution



L2022, WH400→uu
Primary vertex X,Y resolution



L2044 layout has 19.4μm in Z and 6.3μm in X,Y primary vertex resolution (see above).
Improvement due to smaller Z pitch in outer pixel layers is marginal at 0 luminosity limit.
Should be studied at 10^35!!!

B-layer position influence

L0222, WH120, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	2.02%
Eff. to find sec.vertex in b jet(true)	67.0%

	60%	70%
2D	99 ± 4.7	33 ± 0.9
Z	25 ± 0.6	9 ± 0.1
3D	176 ± 11	50 ± 1.7
SV1	663 ± 82	96 ± 4.5
SV2	620 ± 74	89 ± 4

L0222, WH400, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	4.51%
Eff. to find sec.vertex in b jet(true)	75.6%

	60%	70%
2D	89 ± 3.3	30 ± .6
Z	18 ±0.3	6.6 ± 0.1
3D	142 ± 6.6	45 ± 1.2
SV1	500 ± 43	151 ± 7
SV2	480 ± 41	140 ± 6

L2022, WH120, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	1.82%
Eff. to find sec.vertex in b jet(true)	70.2%

	60%	70%
2D	160 ± 10	52 ± 2
Z	32. ± 0.9	11 ± 0.2
3D	325 ± 29	82 ± 3.6
SV1	1580 ± 300	214 ± 15
SV2	1140 ± 188	196 ± 13

~2 times increase

L2022, WH400, all layers X0≈1.2%

Eff. to find sec.vertex in uds jet(fake)	4.40%
Eff. to find sec.vertex in b jet(true)	76.4%

	60%	70%
2D	99 ± 4	33 ± 0.2
Z	19 ± 0.3	7.3± 0.1
3D	188 ± 10	52 ± 1.5
SV1	620 ± 60	177 ± 9
SV2	554 ± 50	156 ± 8

~20% increase

Change of B-layer position from 50.5mm to 37mm improves significantly performance of low $P_\perp$ jet tagging but provides only a moderate improvement for high $P_\perp$ jets.

Influence of new beam pipe

Present pixel package, but with new beam pipe (0.24 % X0) instead of old (0.47%X0),
WH400

Type, ε_b	Standard 3-layers	Standard 3-layers, new beam pipe	F(3Lnewpipe/3L)
2D 60%	61 ± 2	64 ± 2	1.05
2D 70%	21 ± 1	22 ± 4	1.05
3D 60%	99 ± 6	101± 4	1.02
3D 70%	31 ± 1	32 ± 1	1.03
SV1 60%	314 ± 21	373 ± 36	1.19
SV1 70%	88 ± 3	104 ± 4	1.19
SV2 60%	297 ± 20	340 ± 28	1.14
SV2 70%	84 ± 3	99 ± 4	1.18

~17% improvement in combined b-tagging due to new beam pipe for high $P_\perp$ jets

Influence of new beam pipe

Present pixel package, but with new beam pipe (0.24 % X0)
instead of old (0.47%X0),
WH120

Type, ε_b	Standard 3-layers	3-layers, new beam pipe	F(3Lnewpipe/3L)
2D 60%	62 ± 2	70 ± 3	1.13
2D 70%	20 ± 1	26 ± 1	1.30
3D 60%	112 ± 6	147± 9	1.31
3D 70%	31 ± 1	38 ± 1	1.23
SV1 60%	261 ± 20	386 ± 36	1.48
SV1 70%	61 ± 2	81 ± 2	1.33
SV2 60%	256 ± 19	390 ± 37	1.52
SV2 70%	57 ± 2	75 ± 3	1.32

~40% improvement in combined b-tagging due to new beam pipe for low $P_\perp$ jets

Some (preliminary) conclusions

1. To improve low $P_{\perp}$ jet rejection B-layer should be moved closer to interaction point.
2. To improve high $P_{\perp}$ jet rejection amount of material should be decreased.
3. Change of Z pitch of other pixel layers (not B one) doesn't have big influence on b-tagging performance at 0 luminosity limit. Should be much more important at 10^35.
4. Double B-layer doesn't have advantages with respect to single B-layer in b-tagging. Should be checked however for very high $P_{\perp}$ jet.
5. Beam pipe has non negligible impact on b-tagging performance.

BK: USB based system

- USB based FE readout system

USB based FE Readout System – Some Specs

- Multi-IO USB/FPGA Board
  - 15 Mbyte/sec USB/FPGA system transfer speed
  - 2 Mbyte SRAM
  - Xilinx XC3S1000 FPGA
  - LVDS and TTL IOs (for trigger, TDC etc.)
  - Drivers for Windows XP and Linux available

- Module Adapter Card
  - four channels support single chip cards or modules
  - serial powering option for modules
  - current and (individual) voltage measurement for SP

- "Lightweight"/low-cost replacement for TPLL/TPCC
  - limited FPGA resources (possibly no HW histogramming?)
  - no dedicated, programmable delay lines
  - FPGA internal de-skewing with 5 ns resolution

- Status:
  - prototype HW available
  - FPGA / DLL programming under way
  - Interface to TurboDAQ software

H. Krüger, Bonn

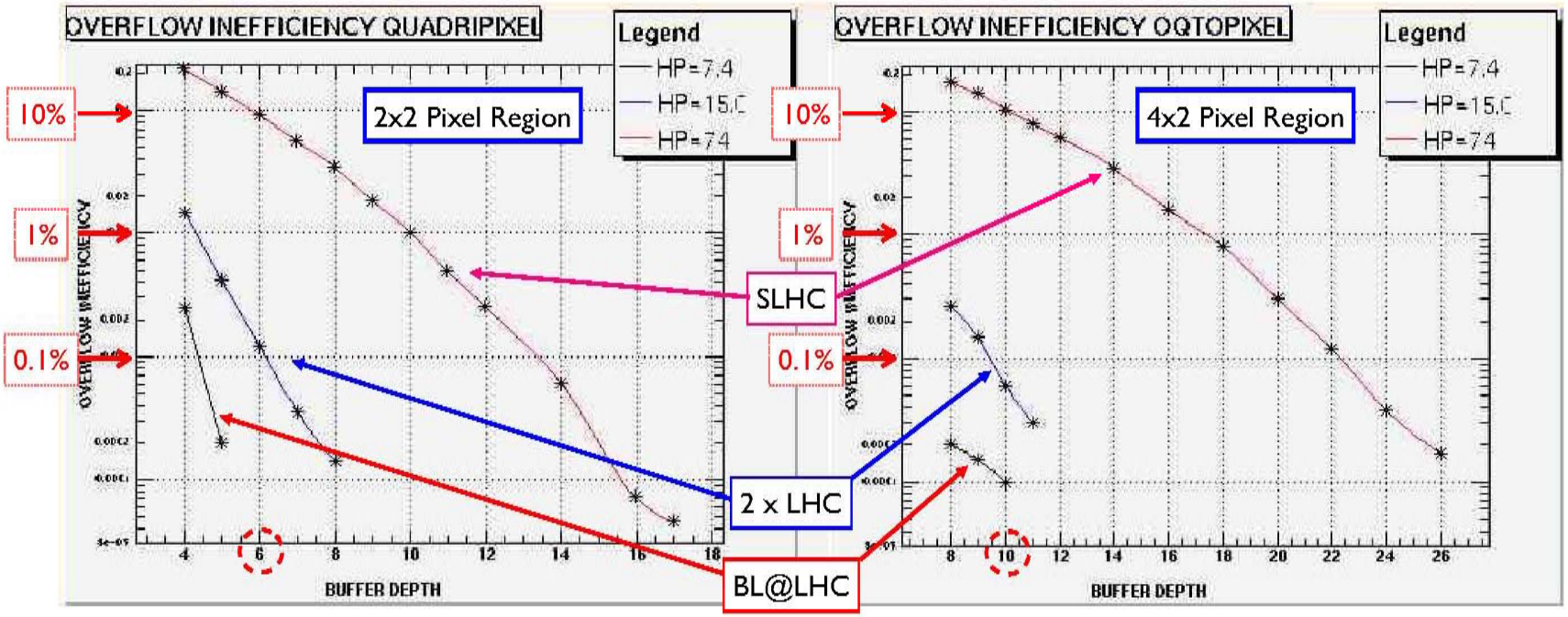
J. Grosse-Knetter, Göttingen

BK: Archi. Concept Simul.

- Architecture Concept Simul.

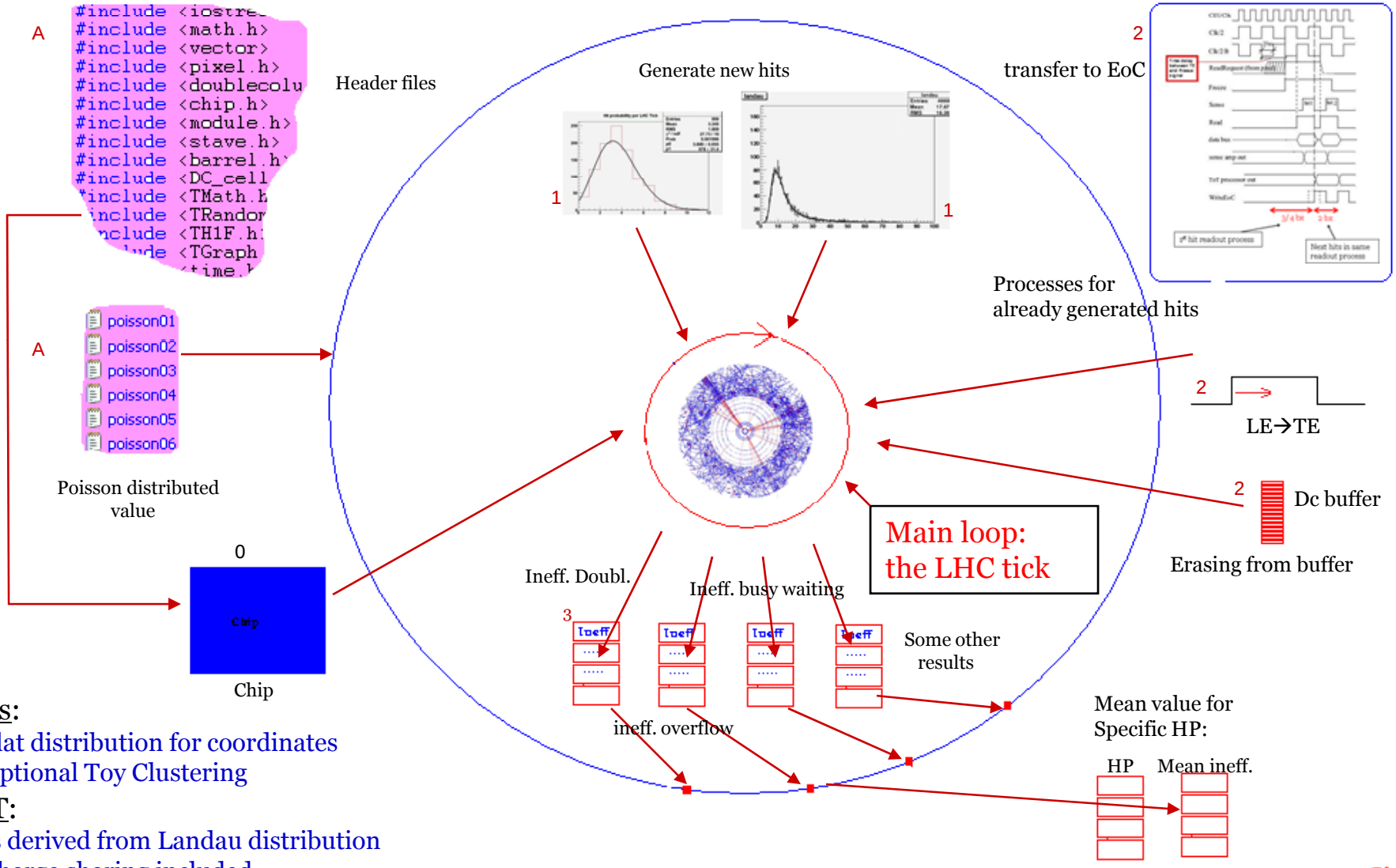
New Architecture Concept

- Basic idea: store the hit locally in DC and transfer only triggered hits → regional pixel logic & regional buffer (note: can be done thanks to smaller feature size).



Also check for consequences of change of logic: increased event size (transfer rate), buffer depth, routing at regional buffer level (implementation in layout)…

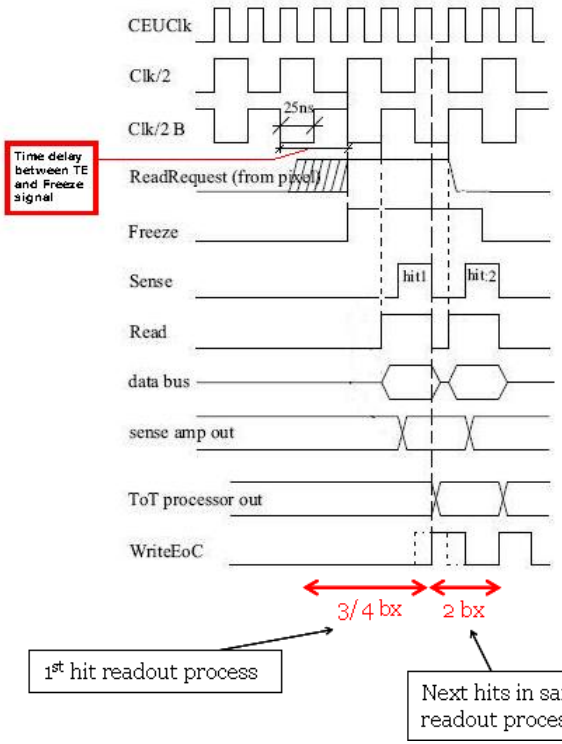
Time-driven simulation



Hits:
→Flat distribution for coordinates
→Optional Toy Clustering

ToT:
→Is derived from Landau distribution
→Charge sharing included

2 sources of inefficiency for FE-I3



Time between TE and Read signal for first pixel in read out process vary from 1 to 3 BX

For next pixels in RO process time between 2 Read signals is 2 BX

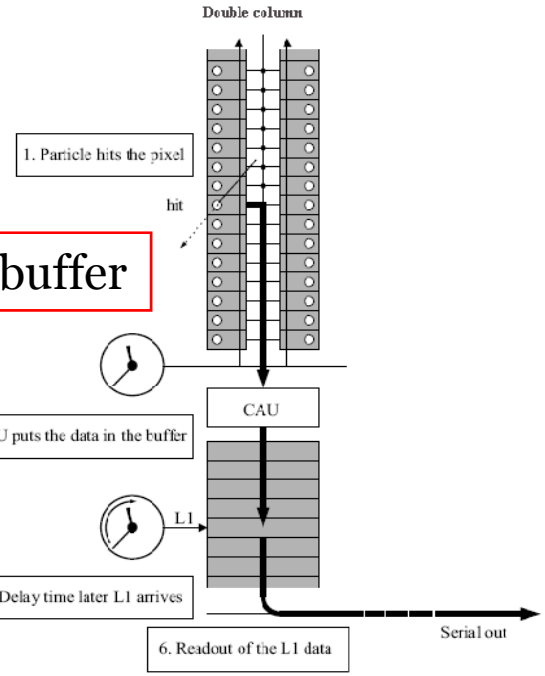
Time between Read and WEoC is 1.5 BX

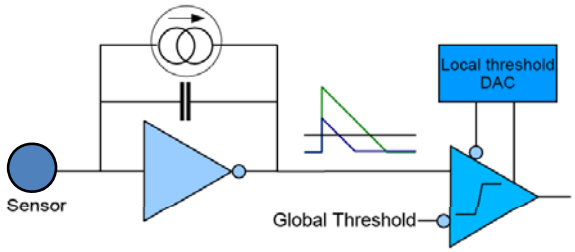
Copy to EoC buffer

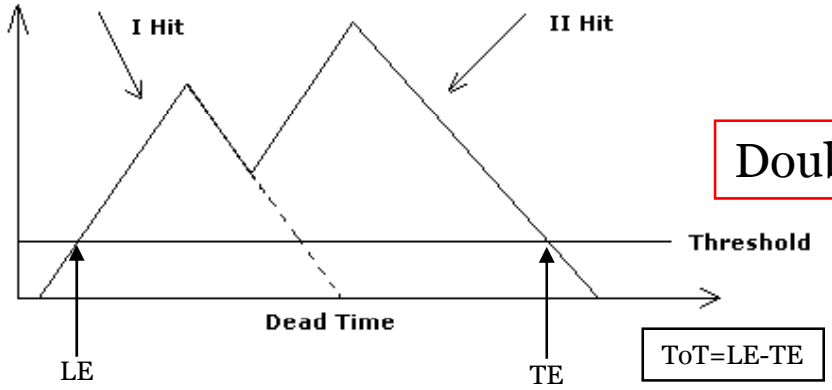
In summary, we have from 4.5 to 2.5 BX from TE to WEoC signal

In Simulation 1 BX is used for time between Read and WEoC.

And for Simulation we have 4 to 2 BX From TE to WEoC signal.





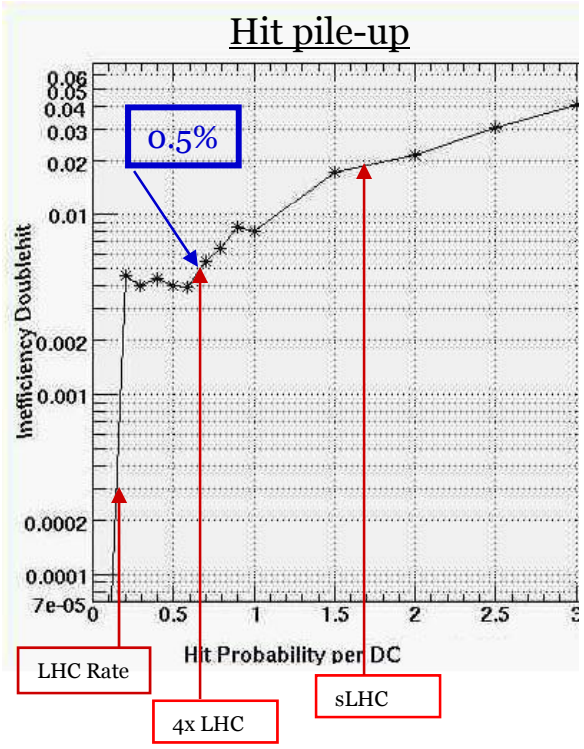


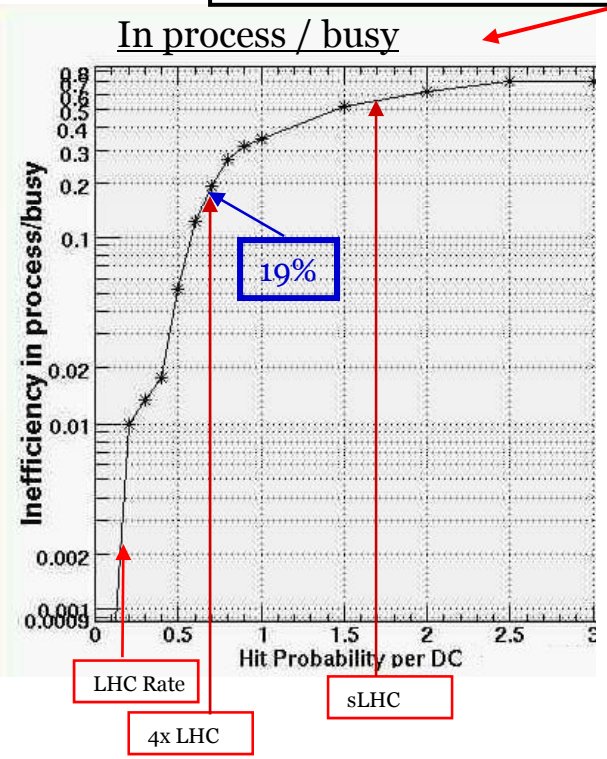
Double hit

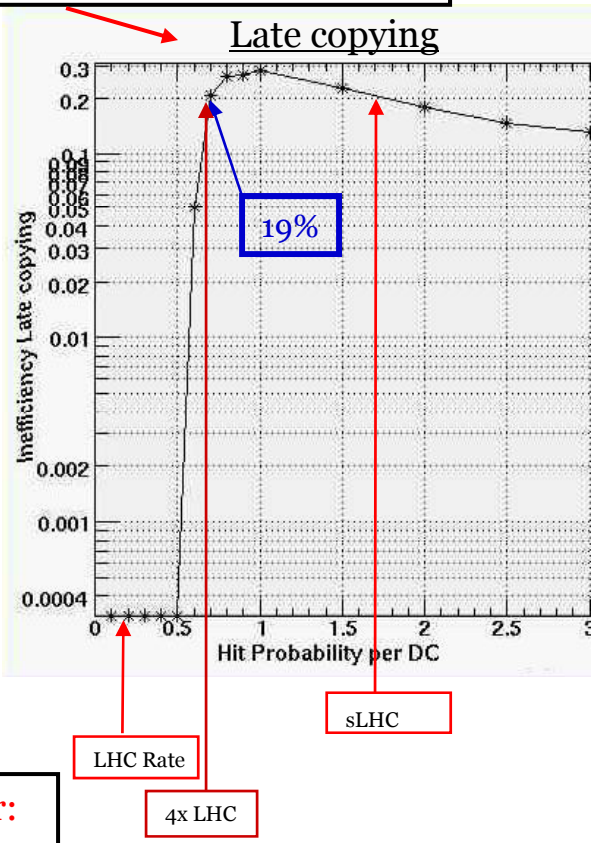
Inefficiencies in FE-I3

- Identified (note; up to DC buffer only): double-hit, wait/busy (new hit when last still pending), wrong latency (late copying), EoC full.

Both ineff. related to time consuming hit transfer







FE-I3 behaves inefficiently at high hit rate because of pixel → EoC transfer: NEW ARCHITECTURE is based on local storage of hits (à la Maurice)

FE-I3 vs 'FE-I4' (new concept)

FE-I4 :

→ In Logic Unit, pixels are tied together.
(Logic unit - inherent handling of clustered hits)

A

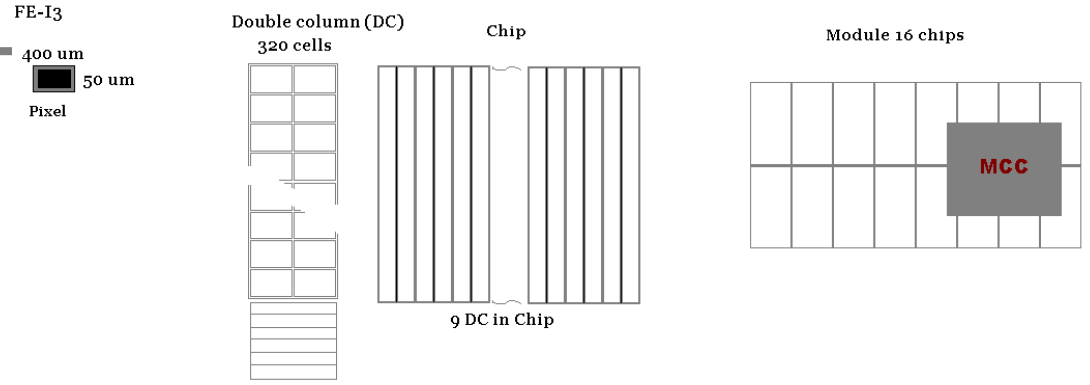
→ Logic Unit linked to Local buffer
(no time consuming hit transfer)

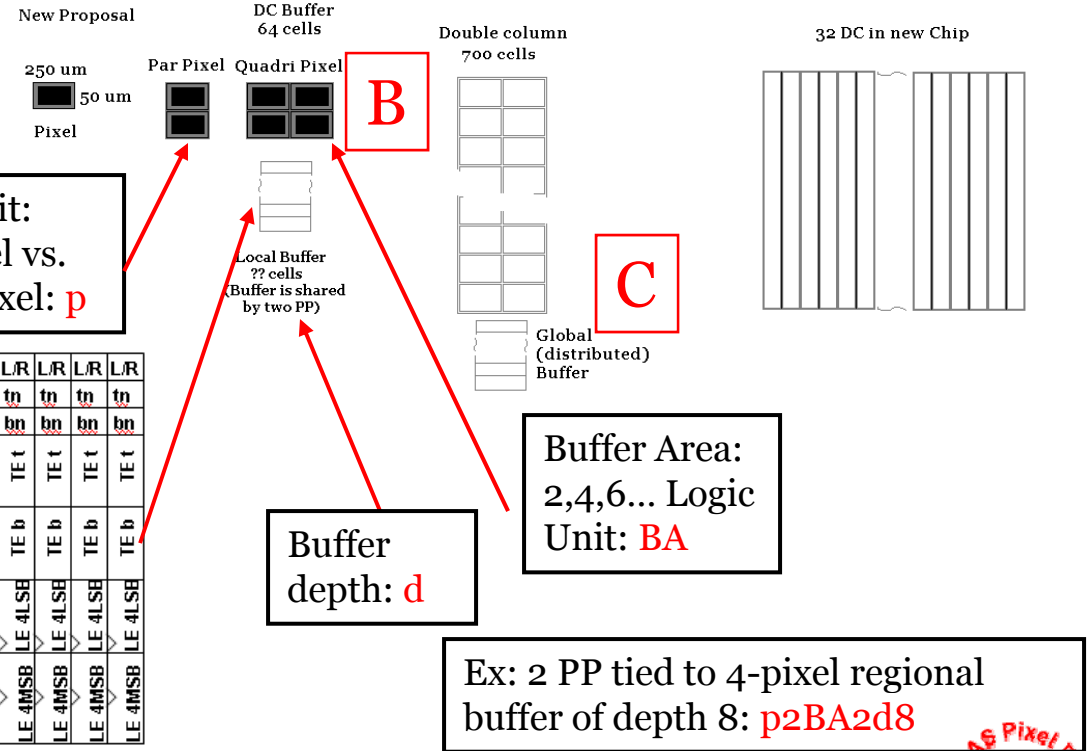
B

→ Global distributed buffer for triggered hits only!
(Hit is in local buffer till "Latency" and copied only if L1T confirmed)

C

→ local buffer depth a parameter.



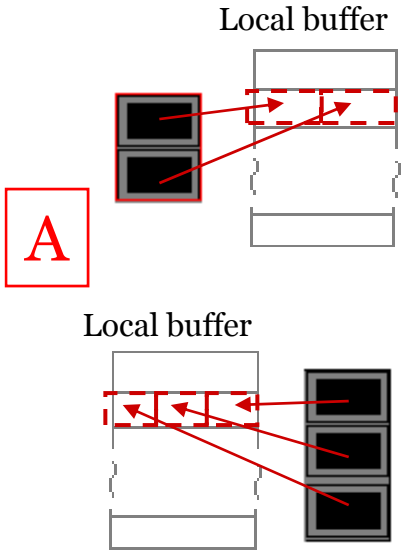


Logic unit:
Pair Pixel vs.
Triple Pixel: p

Buffer Area:
2,4,6... Logic
Unit: BA

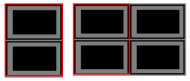
Buffer
depth: d

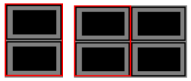
Ex: 2 PP tied to 4-pixel regional buffer of depth 8: p2BA2d8

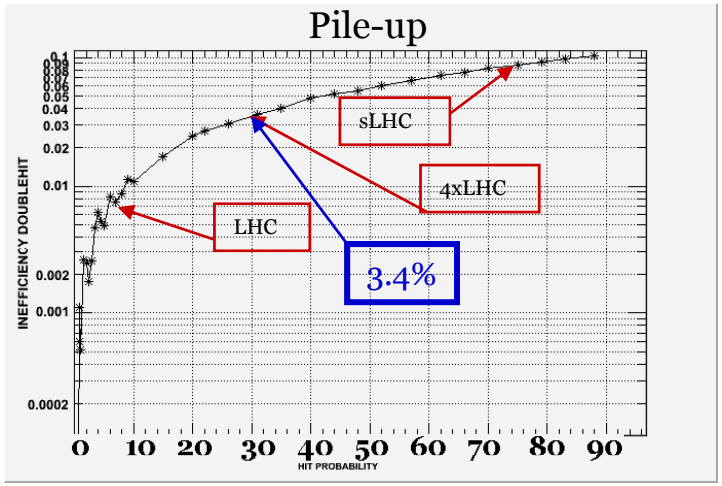


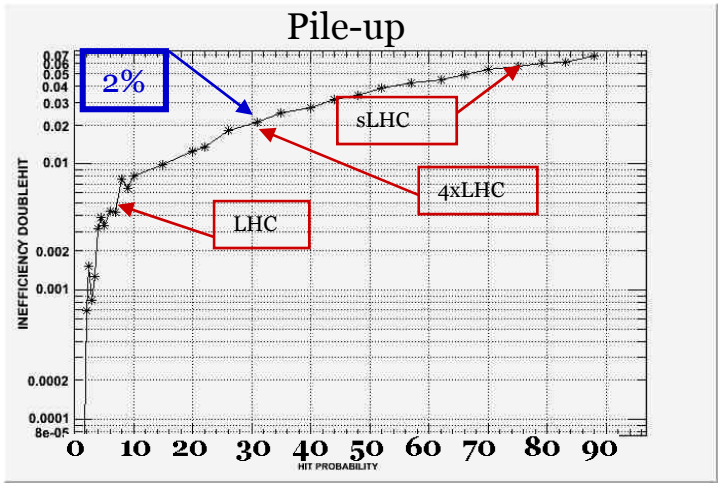
Inefficiency FE-I4 (p2BA2d4)

- Only double hit and buffer overflow inefficiency: transfer hit to local buffer very fast (& No long ToT -time-out at 16BX).


p2BA2d4 Without Clustering

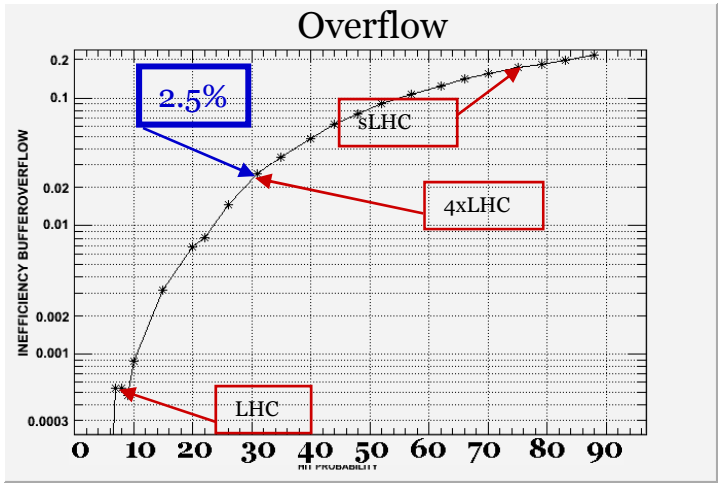

p2BA2d4 With Clustering

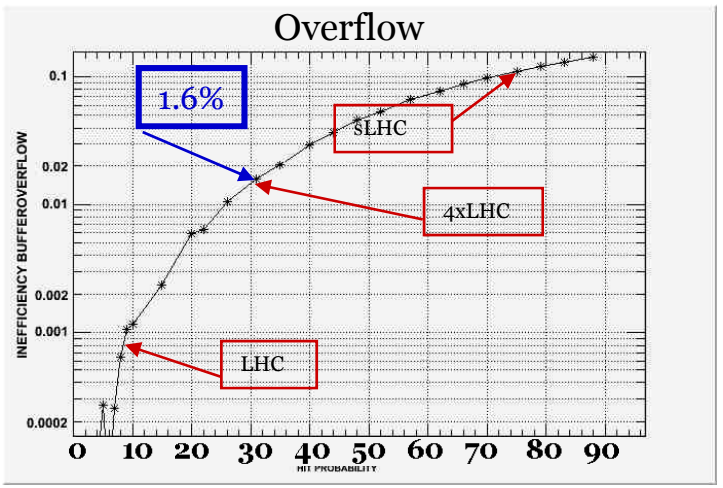




Double hit inefficiency

→ ToT tuning, truncation, double threshold

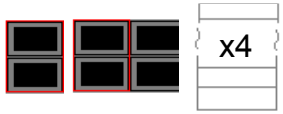




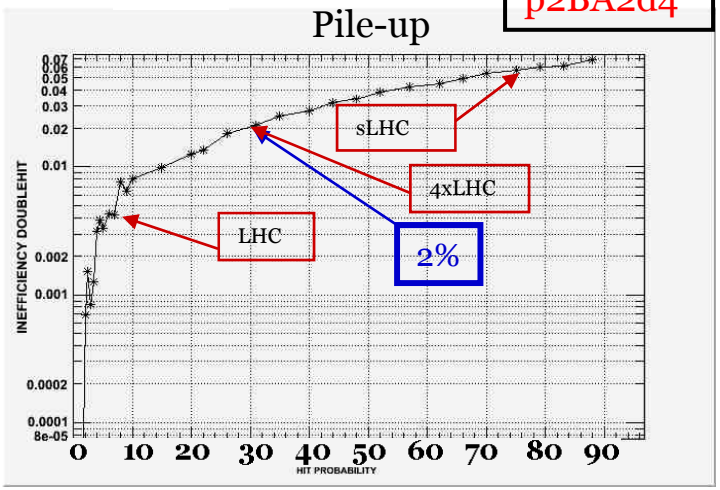
Buffer overflow inefficiency

Logic Unit more efficient for clustered hits

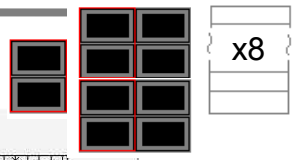
Increased Buffer Area (p2BA2d4 vs. p2BA4d8)

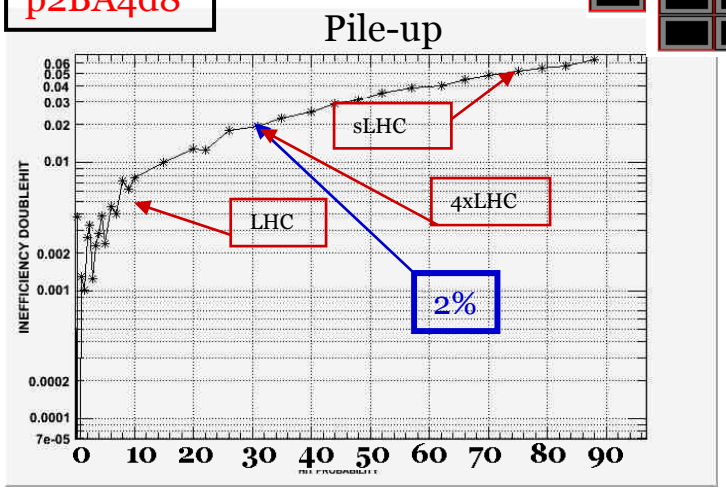


p2BA2d4



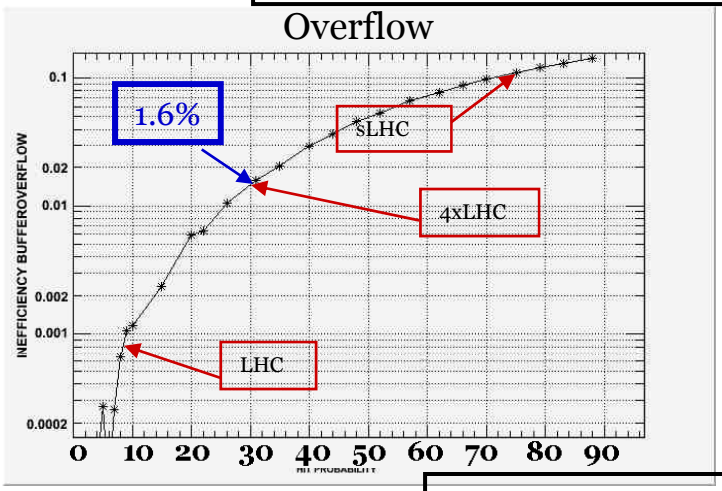
p2BA4d8

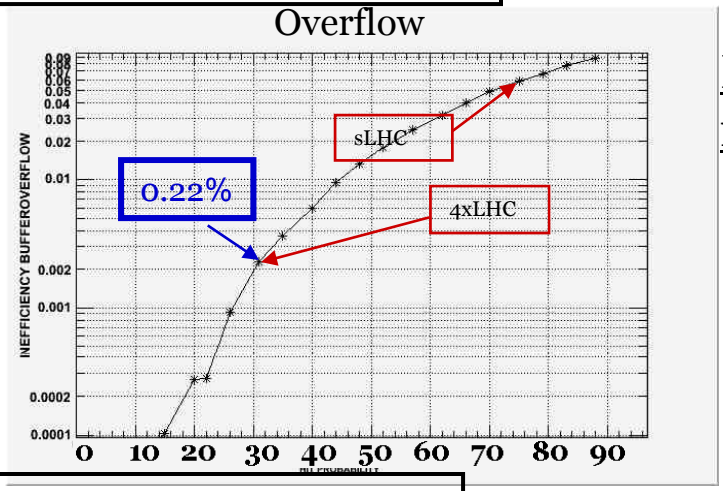




Double hit inefficiency

Same pileup inefficiency regardless of BA size

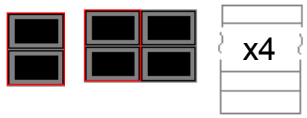




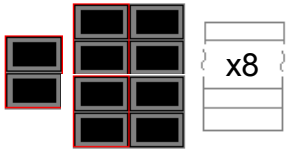
Buffer overflow inefficiency

Increased BA → buffer efficiency up

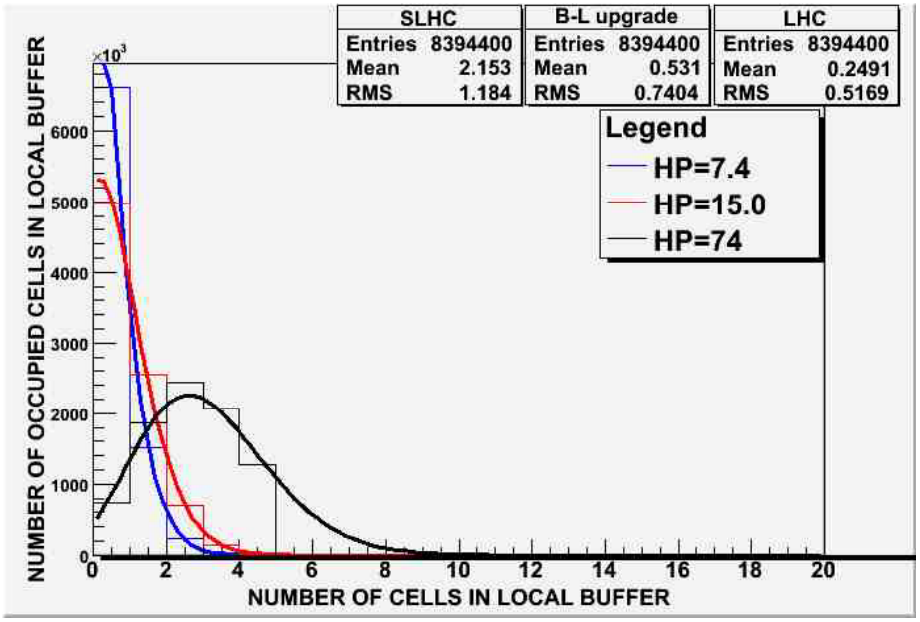
#of occupied cell in local buffer (p2BA2d4 vs. p2BA4d8)

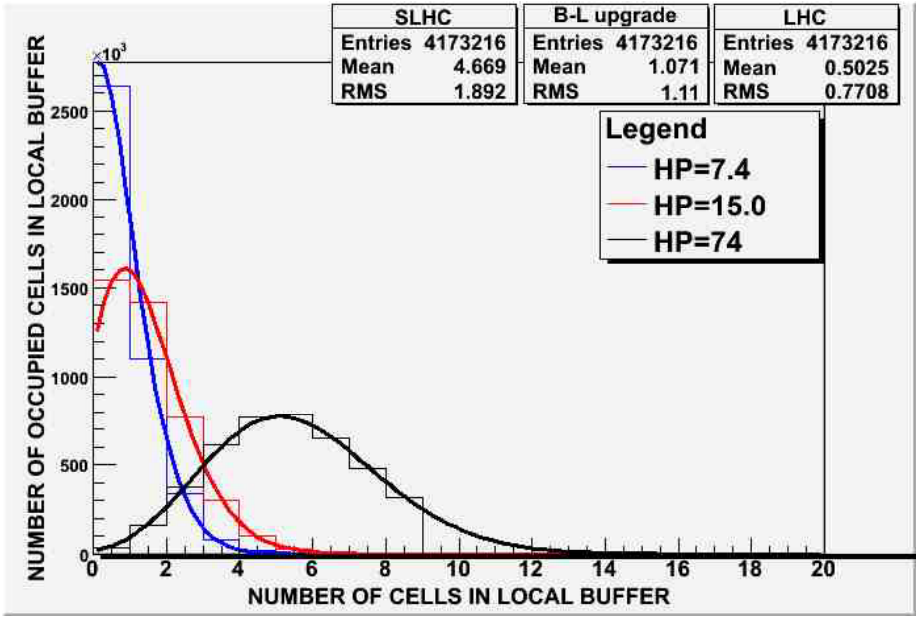


p2BA2d4



p2BA4d8

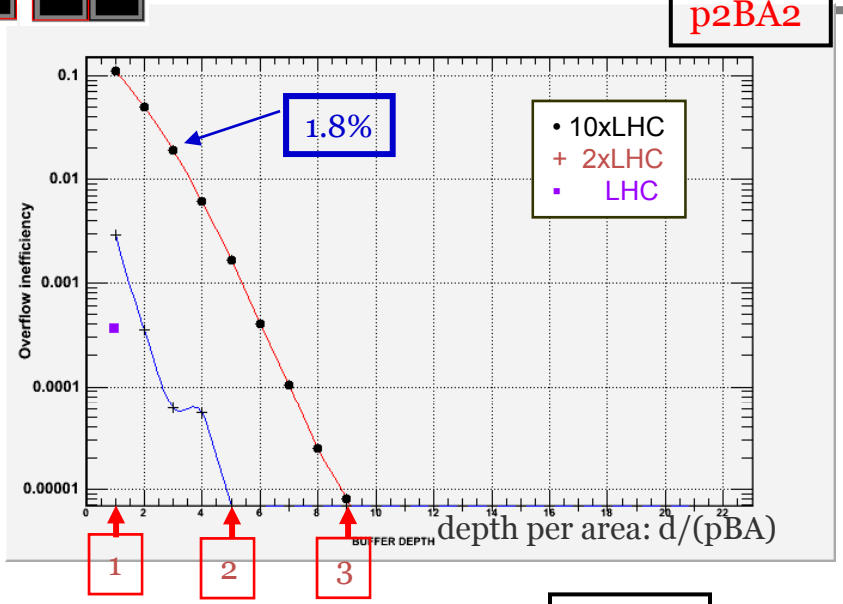




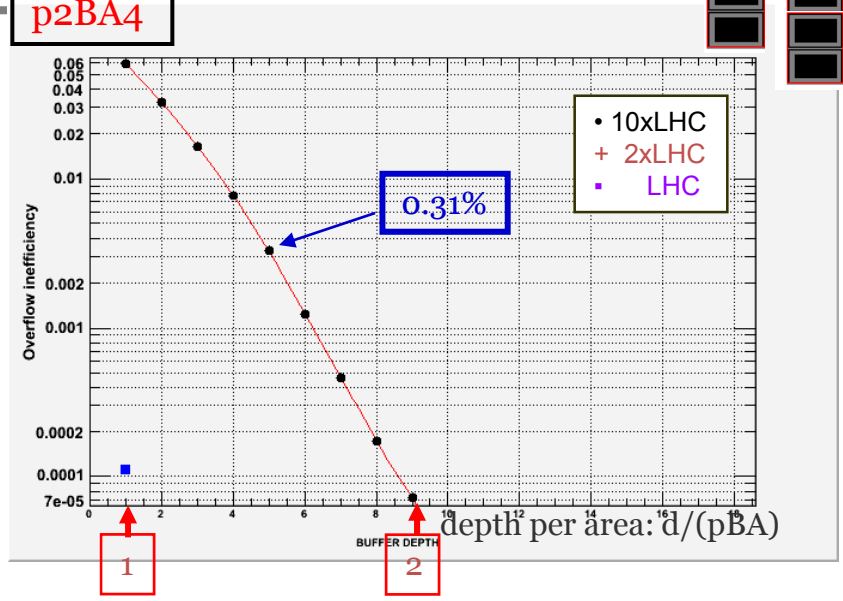
Increased BA → buffer overflow inefficiencies average out

Buffer Overflow for p2(BA,d)

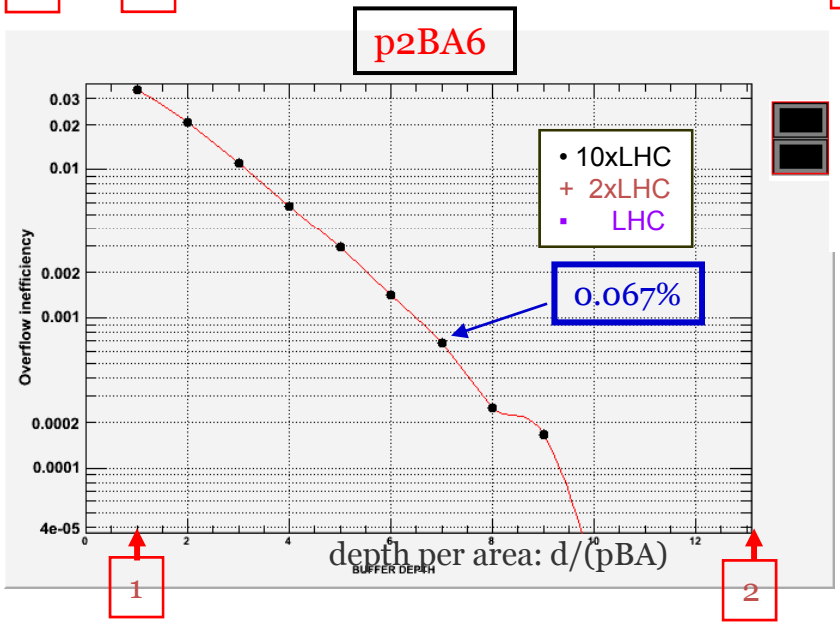
p2BA2



p2BA4



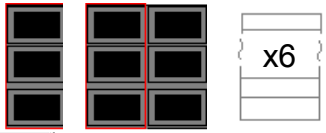
p2BA6

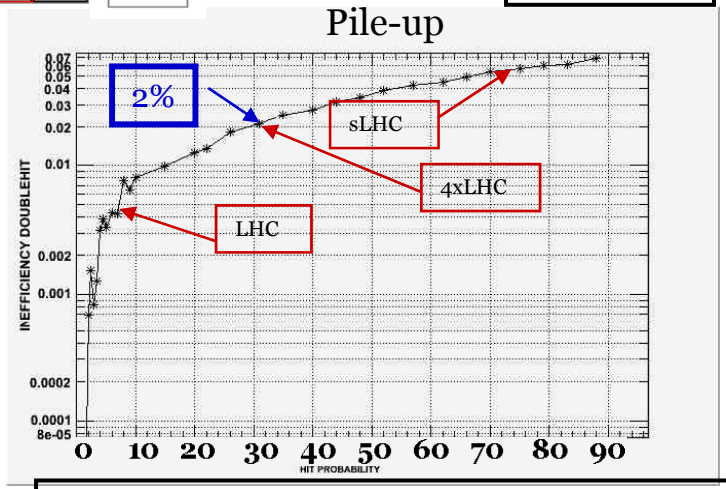


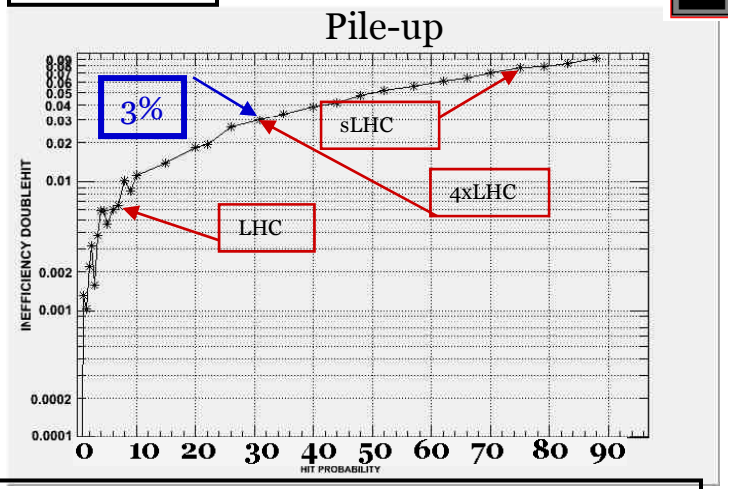
Increased BA, same depth per area ratio → buffer efficiency up

Bigger Logic Unit (p2BA2d4 vs. p3BA2d8)

p2BA2d4 | p3BA2d6

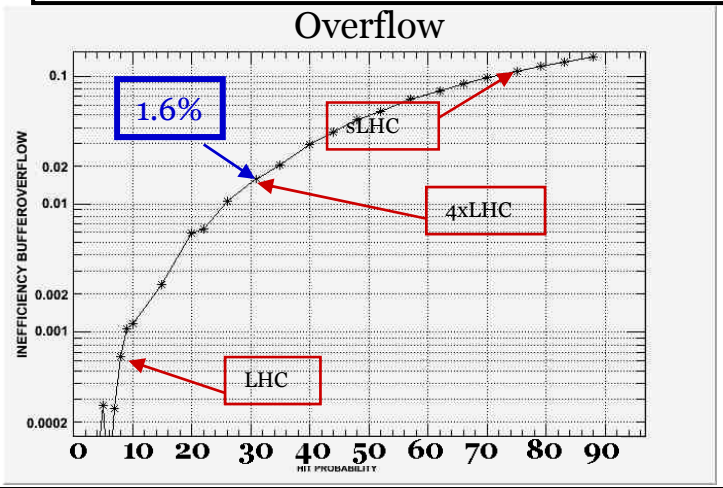


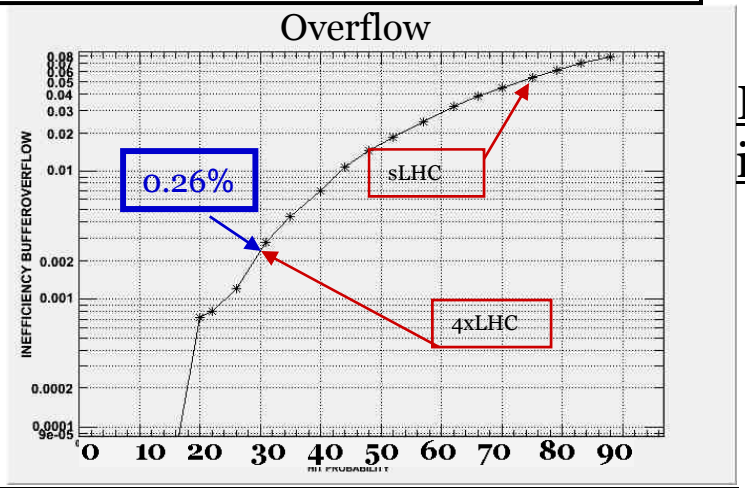




Double hit inefficiency

Increased pileup inefficiency for larger p (note: no truncation of 1st hit)

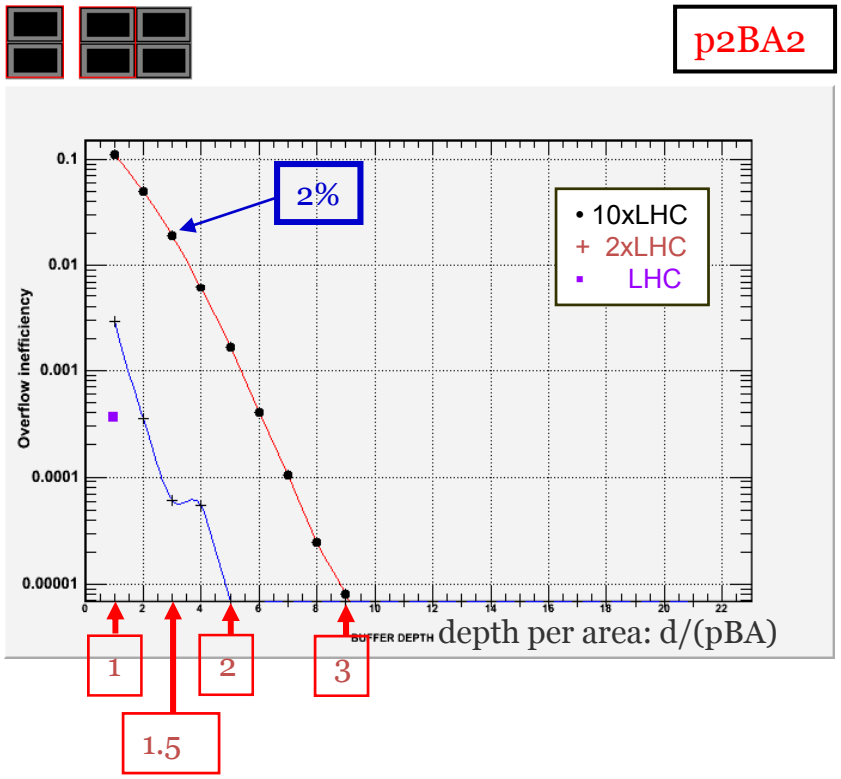


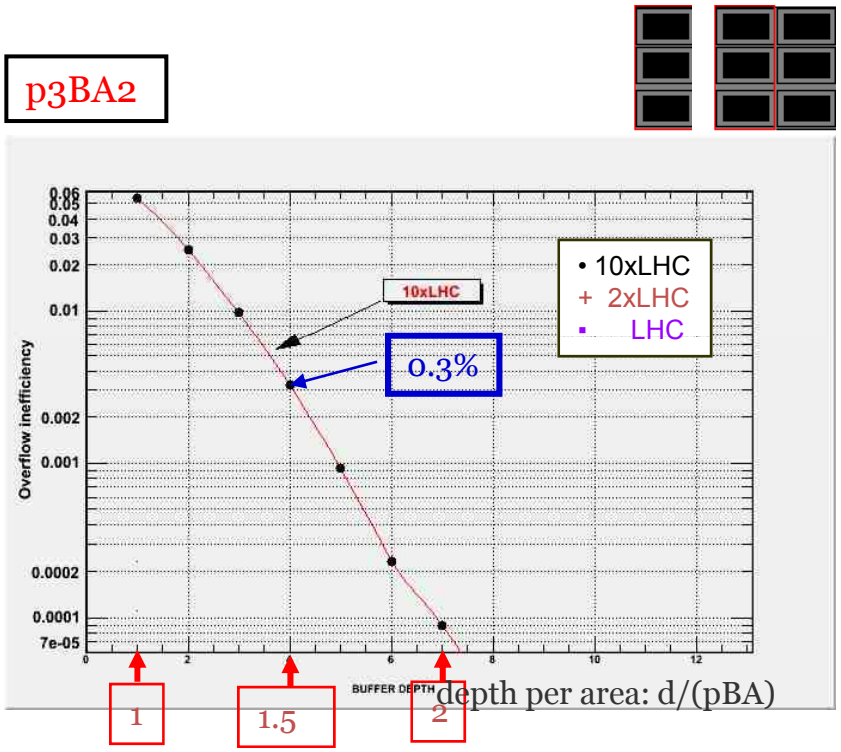


Buffer overflow inefficiency

Reduced buffer overflow inefficiency (cluster efficient & larger area)

Buffer Overflow for BA2(p,d)





For a same depth per area ratio, bigger logic unit much more efficient

Note: for p3, intrinsic increased area too

BK: SnAg & thinning

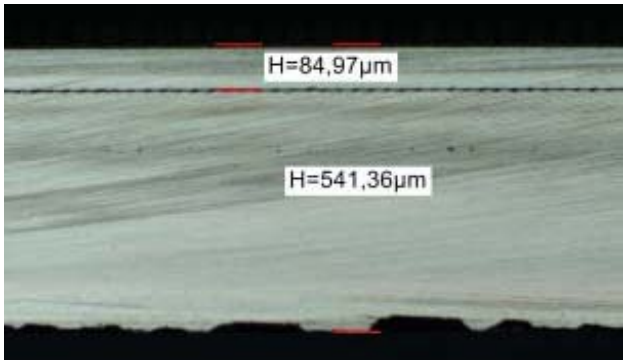
- SnAg & thinning

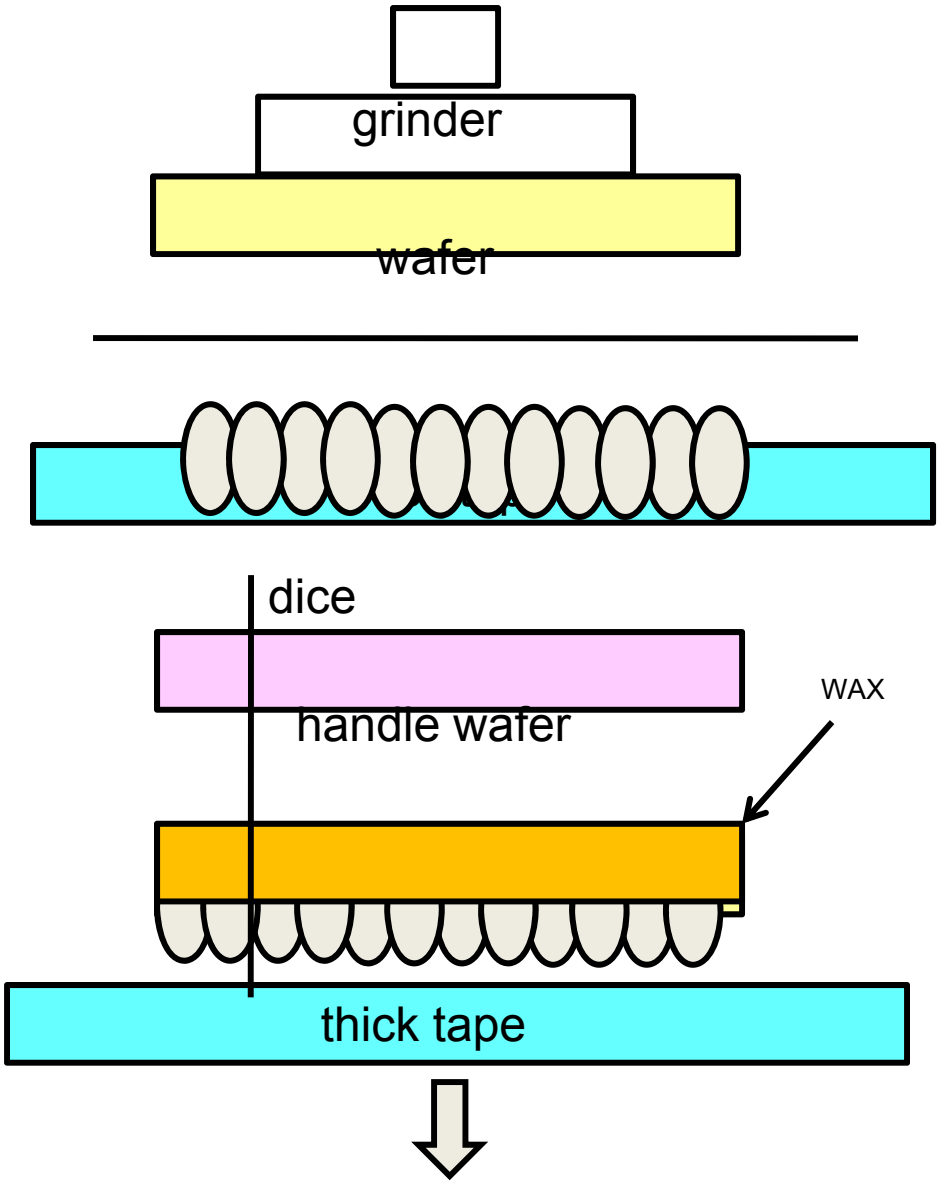
Thin chip with handle wafer

1. bump IC (SnAg)
2. bump protect by thick UV release tape
3. mechanical two-step backside grinding to 90 µm (coarse/fine)
4. thinned wafer wax-bonded to thick handle wafer
5. remove thick tape (bump protection no longer needed)
6. dice bonded wafers (handle + thin wafer)
7. (take off handle chips by heating)
8. electrical testing of chips → either thick or thin
9. flatten warp and bond to sensor
   (several secret methods !)

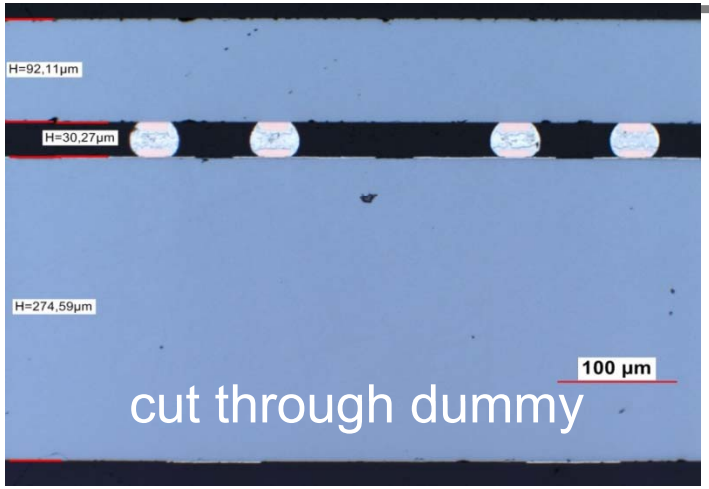
variant:

handle wafer → handle chips mounted only after the electrical testing

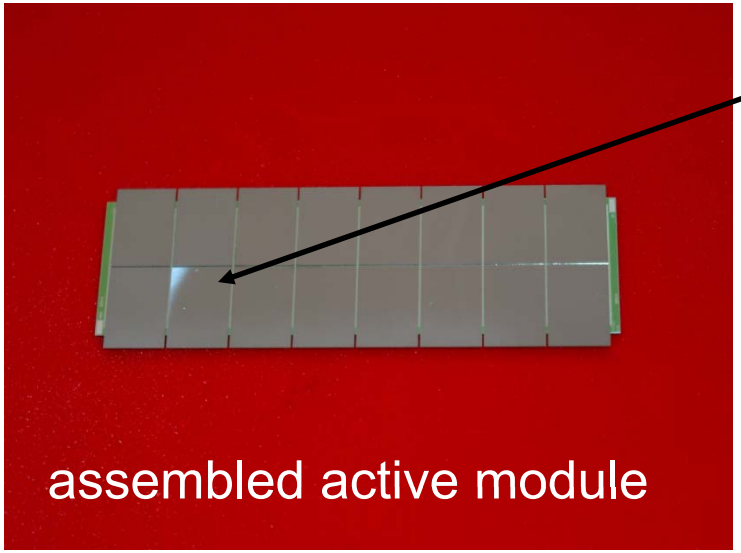


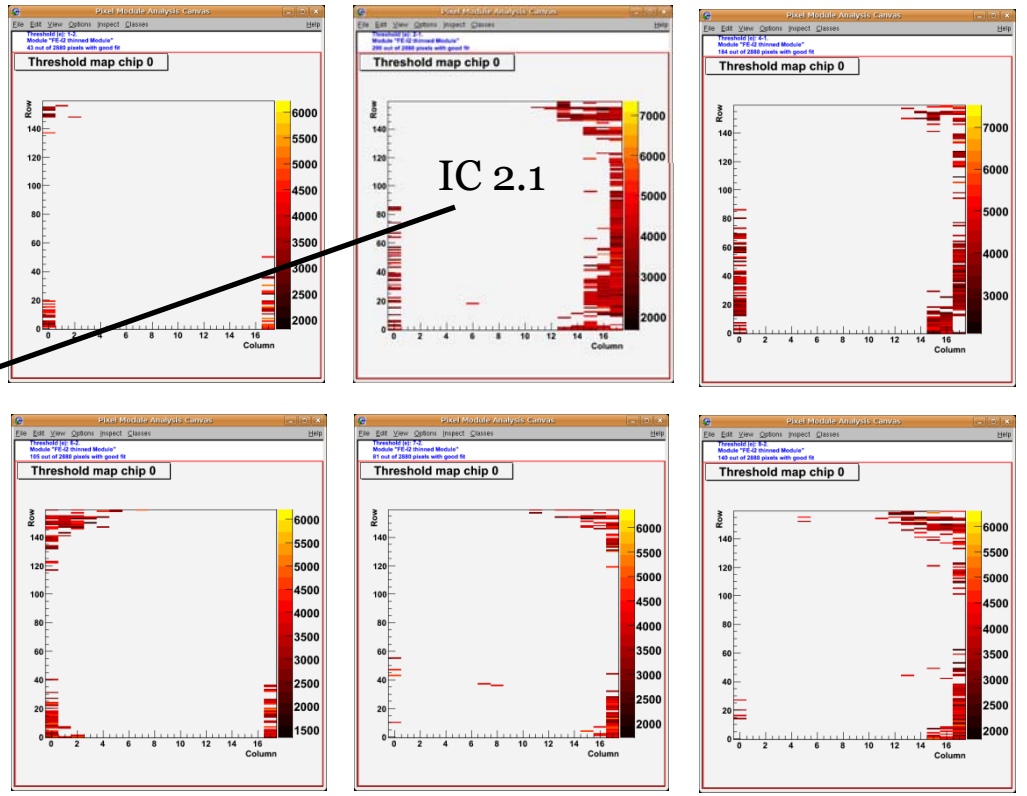


Test of bare module with 90µm thin IC

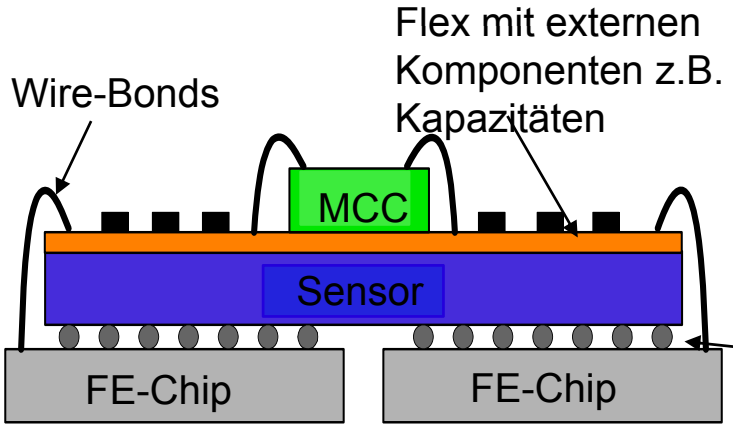


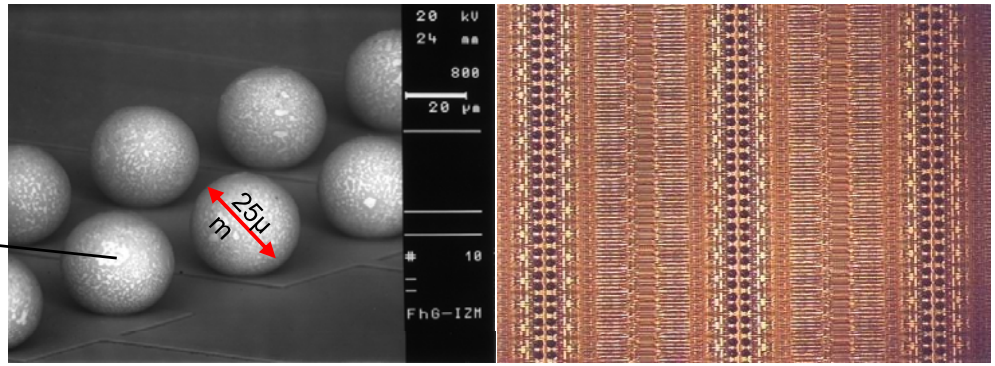
← dummy assembly after the removal of the support chip



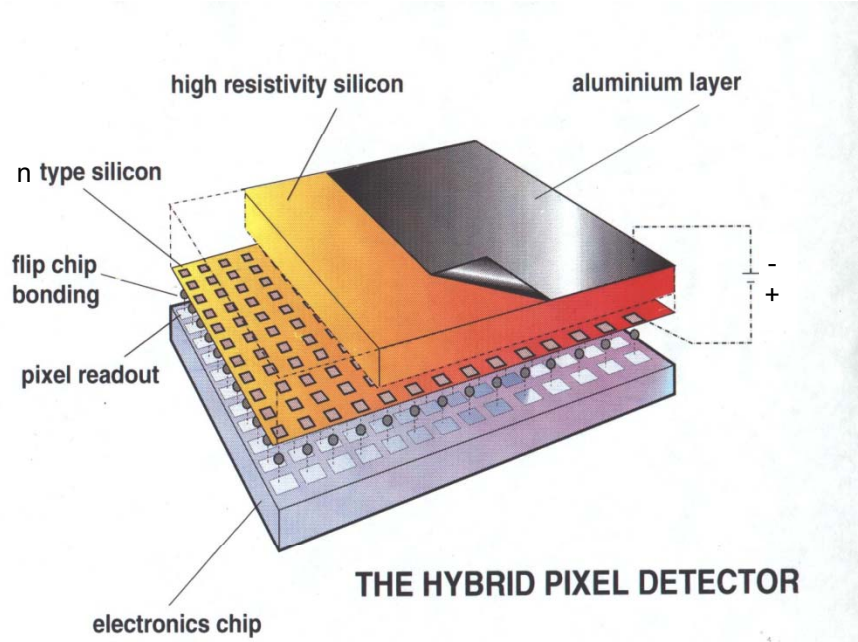


1.3 Aufbau des Moduls





Bilder von IZM Berlin

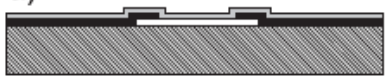


Der Sensor wird über Bump-Bonds mit dem Auslesechip verbunden.
Über Wire-Bonds werden die FE-Chips dann mit einem ModulControlChip verbunden.

2.1 Bump Bonding Prozess

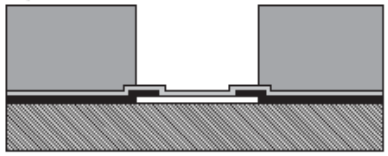
Vorbereiten der Bumps

a)



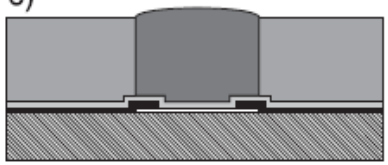
Sputtern der Oberfläche (Ionenstrahldeposition)(Ti,W), galvanisches Aufbringen einer Cu-Schicht

b)



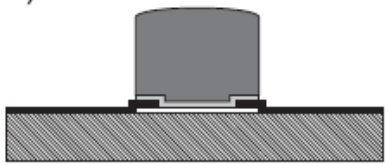
Aufbringen von Photolack (spin coating), Strukturierung des Lacks

c)



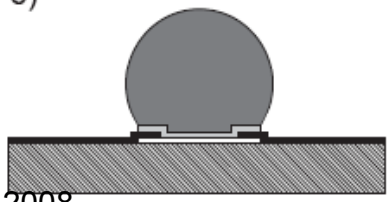
durch Galvanisieren wird SnAg an den nicht vom Photolack verdeckten Stellen aufgebracht

d)

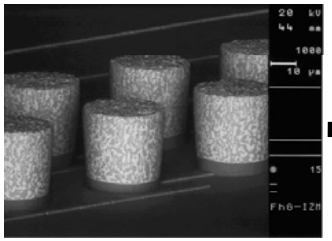


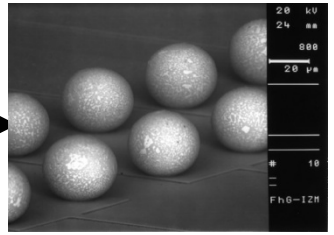
Entfernen des restlichen Photolacks durch ein Plasma. Entfernen der überstehenden Auflagefläche durch nasses Ätzen

e)



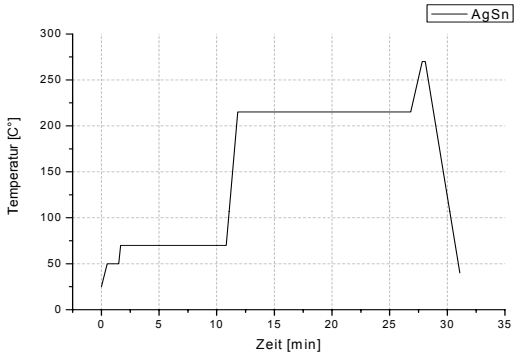
kurzzeitiges Erhitzen führt zum sog. Reflow

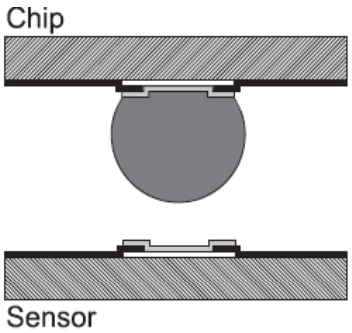


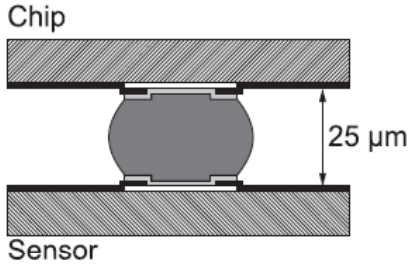


Flip-Chip-Prozess

Zum Verbinden der beiden Teile, in diesem Fall Sensor und FE-Chips, werden die Bumps in einem bestimmten Temperaturprofil erhitzt und die Komponenten unter leichter Kraftanwendung aneinander gefügt.



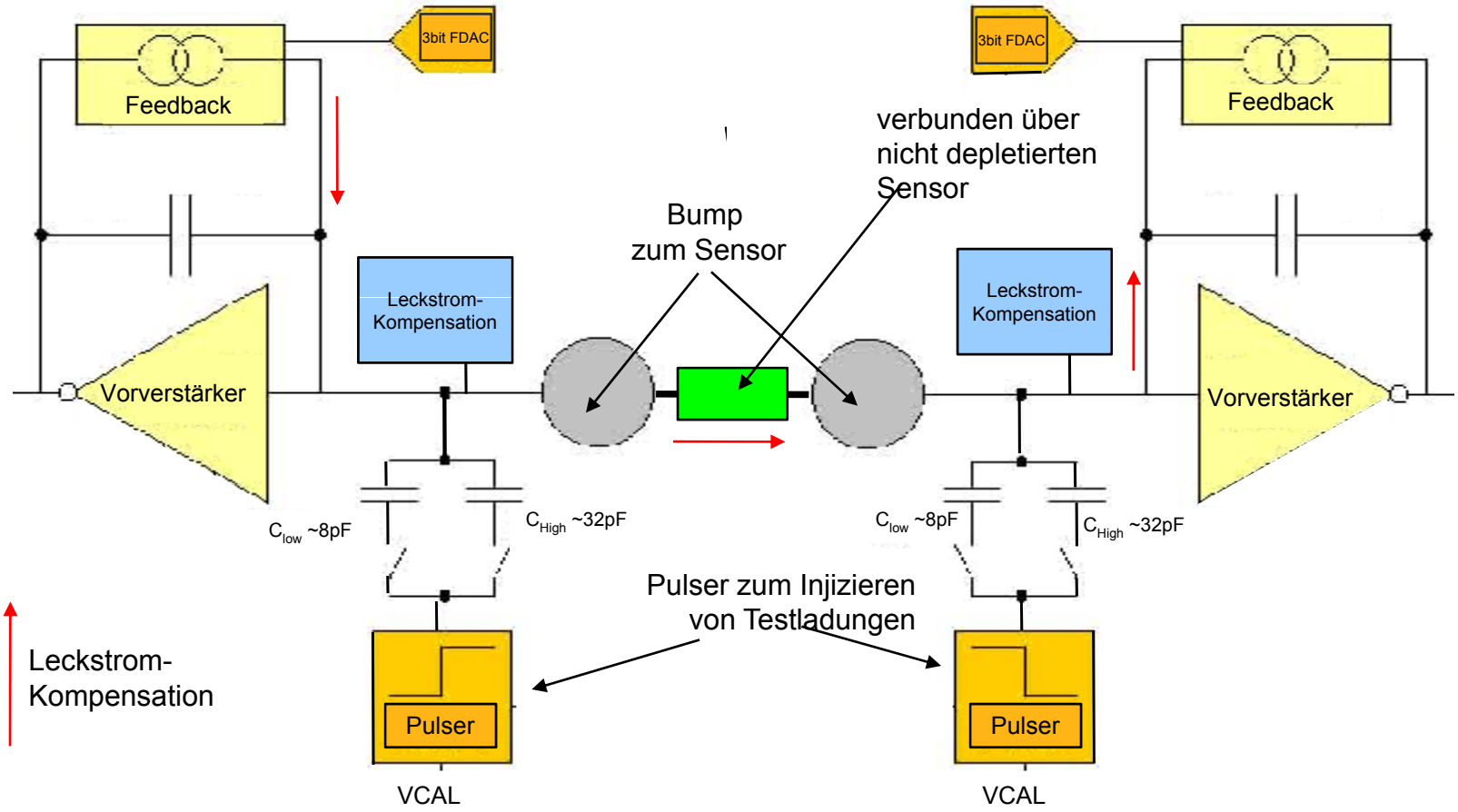




Bilder von IZM Berlin

universitätbonn

2.3 Methodik der Charakterisierung



Der linke Vorverstärker hat ein leicht höheres Eingangspotential als der rechte.

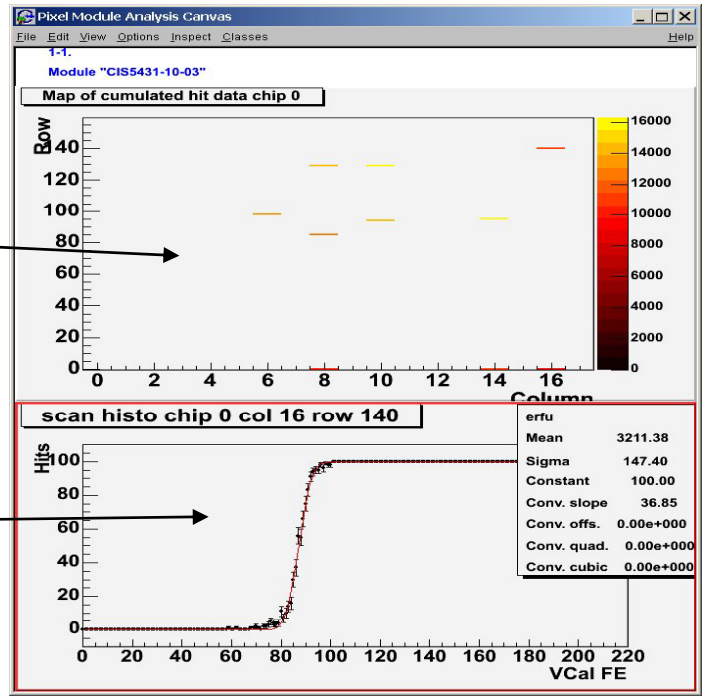
2.3 Methodik der Charakterisierung

Aufgrund von Ladungsteilung über den nicht depletierten Sensor und einen Sättigungseffekt durch die Leckstromkompensation, zeigen **an den Sensor verbundene Pixel KEINE Treffer** beim Injizieren von Testladungen.

Eine **Hitmap** zeigt einzelne Pixel ortsaufgelöst, die bestimmte Eigenschaften tragen, in diesem Fall eine messbare Schwelle im Schwellenscan. Die Schwellenhöhe ist farbkodiert.

Schwellenscan:
Es wird eine **definierte Ladung 100 mal injiziert** und aufgezeichnet, wie häufig diese Ladung einen Treffer erzeugt. Danach **wird** dies **für** eine **höhere Ladung wiederholt**.

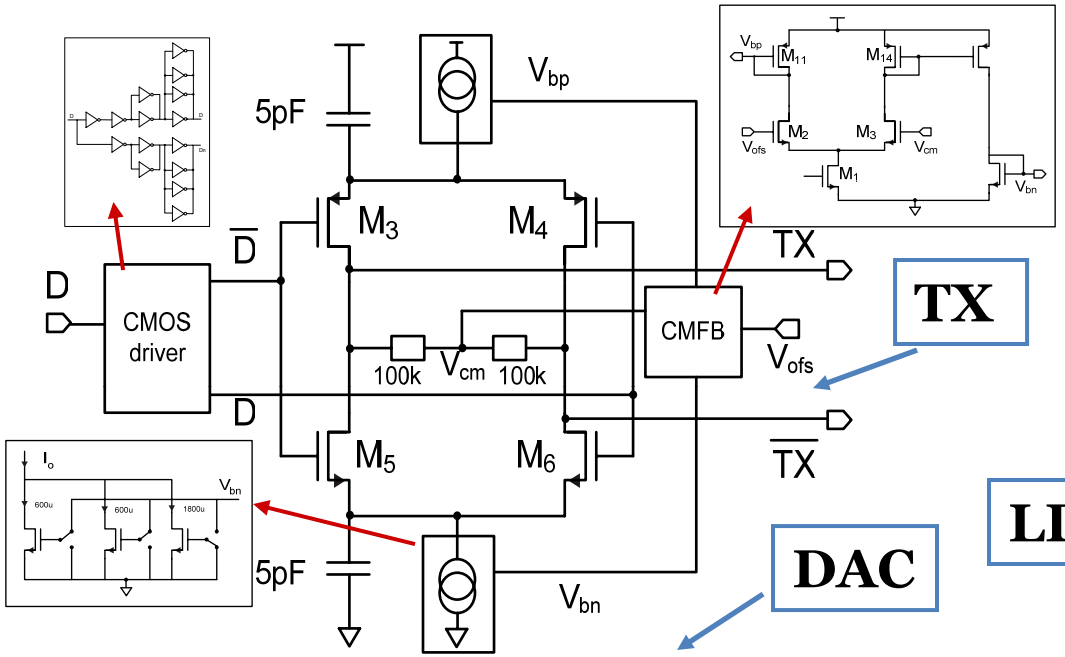
Hitmap:
Schwellenscans mit undepletiertem Sensor



BK: new FE

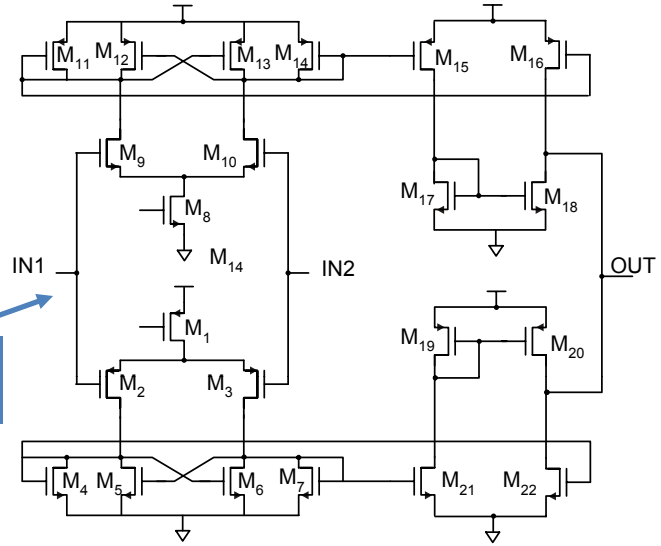
- New FE

Block design for next prototype



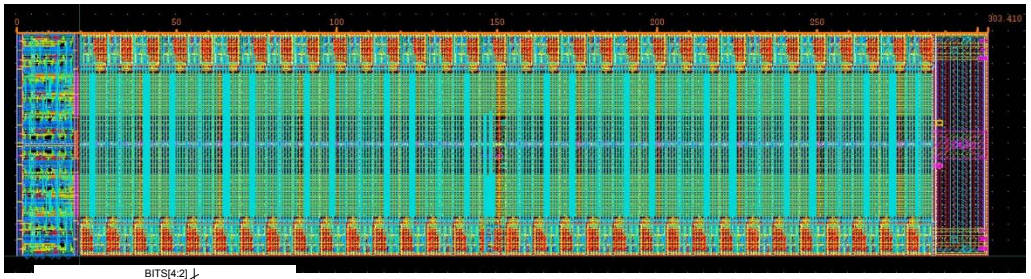
TX

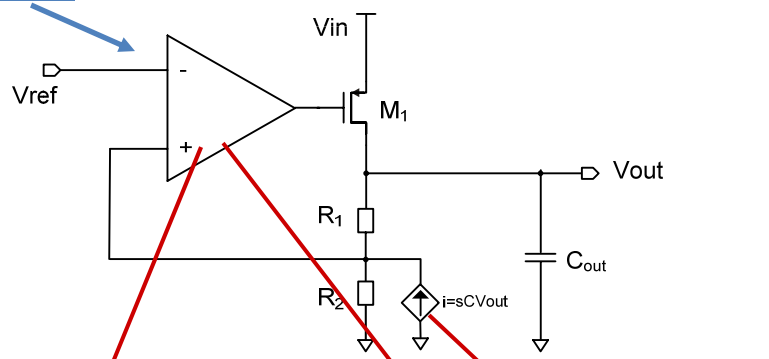
RX

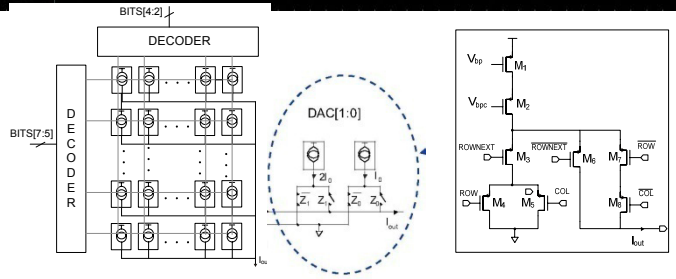


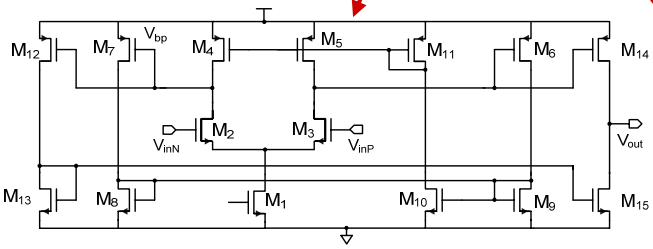
LDO

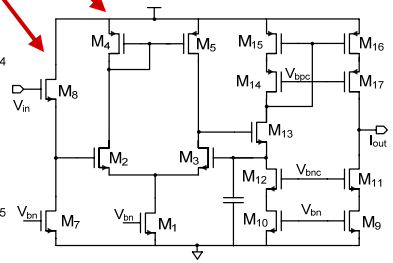
DAC







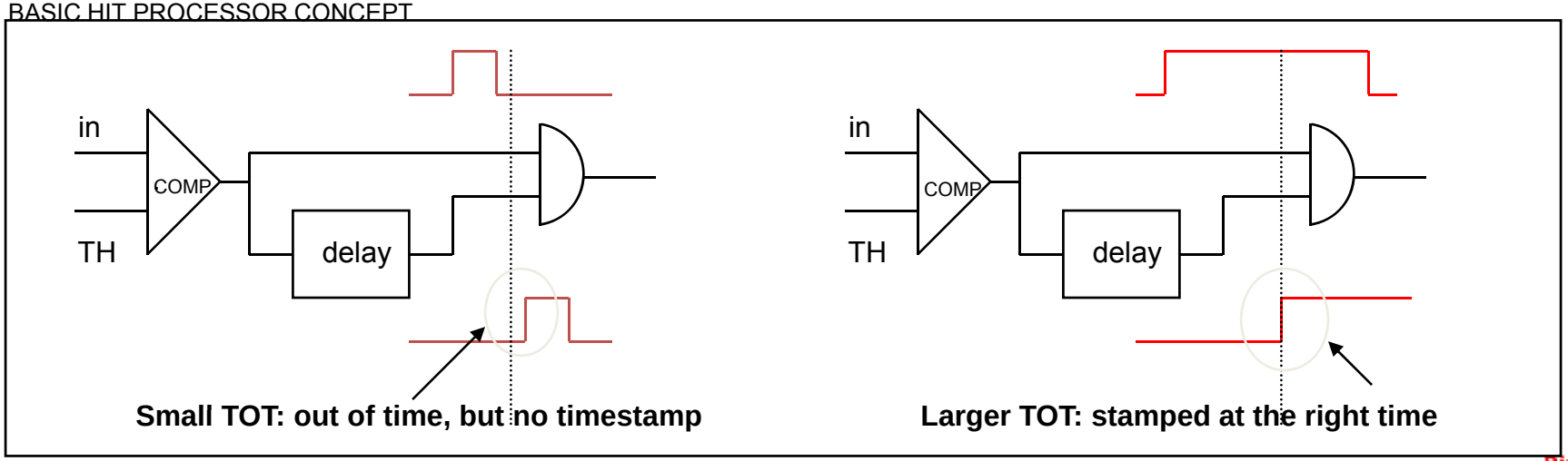




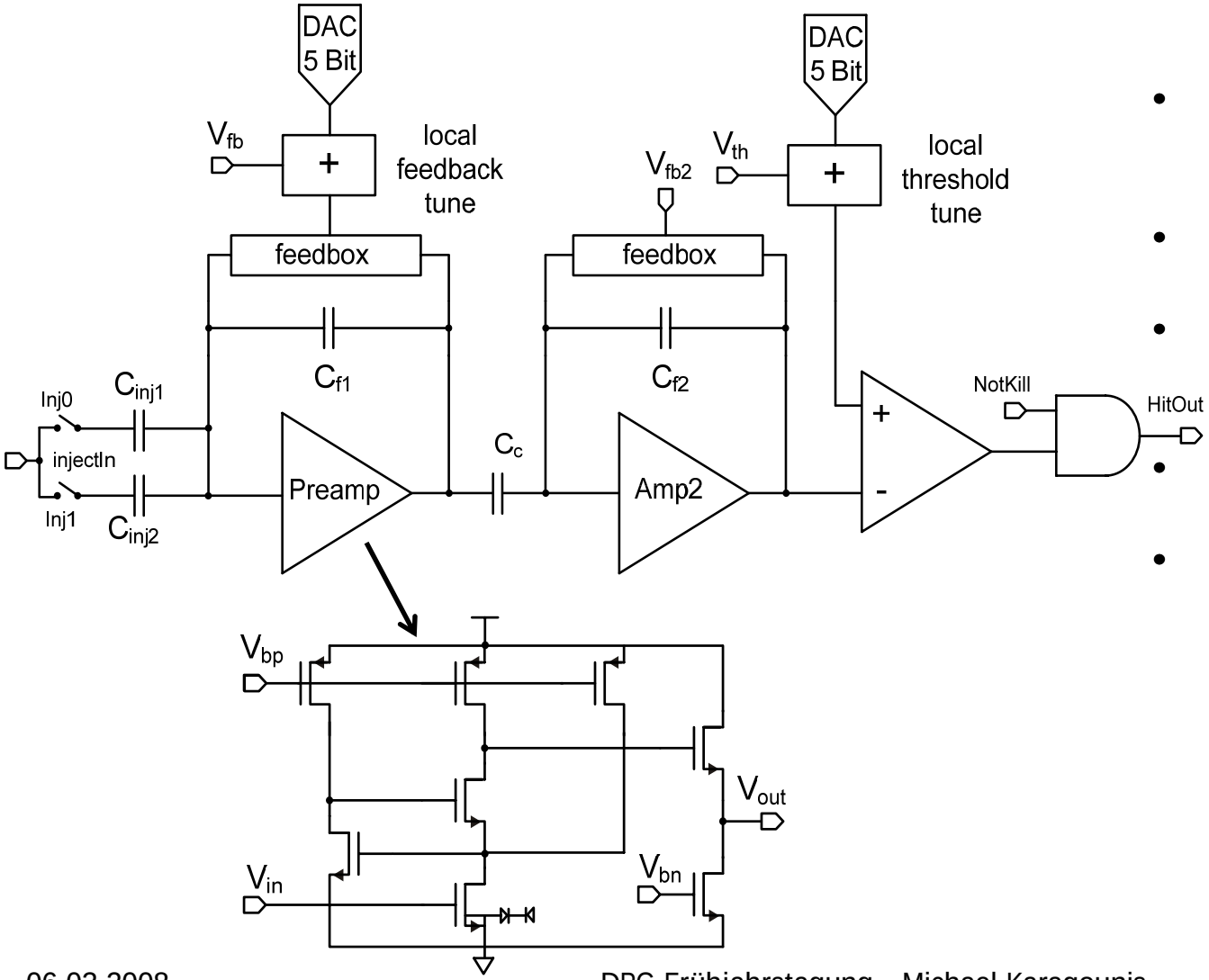
Hit Processor: a new hit discrimination concept

- Use comparator to:
  - Measure arrival time of all pulses
  - Measure charge
  - **<u>BUT NOT</u> to timestamp hits (as done now)**
- A hit ≠ a pulse
  - Use measured charge to find "big" pulses
    - Big pulses are less sensitive to noise => can work with lower threshold / higher noise
  - Use measured arrival time of big pulses to timestamp hits
    - Arrival time of big pulses has small time-walk => can accept lower analog performance.
  - No "big" pulse <=> no real hit
- See appendix for discussion and implementation options

BASIC HIT PROCESSOR CONCEPT

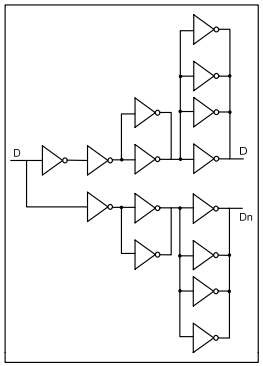


Analog readout electronics



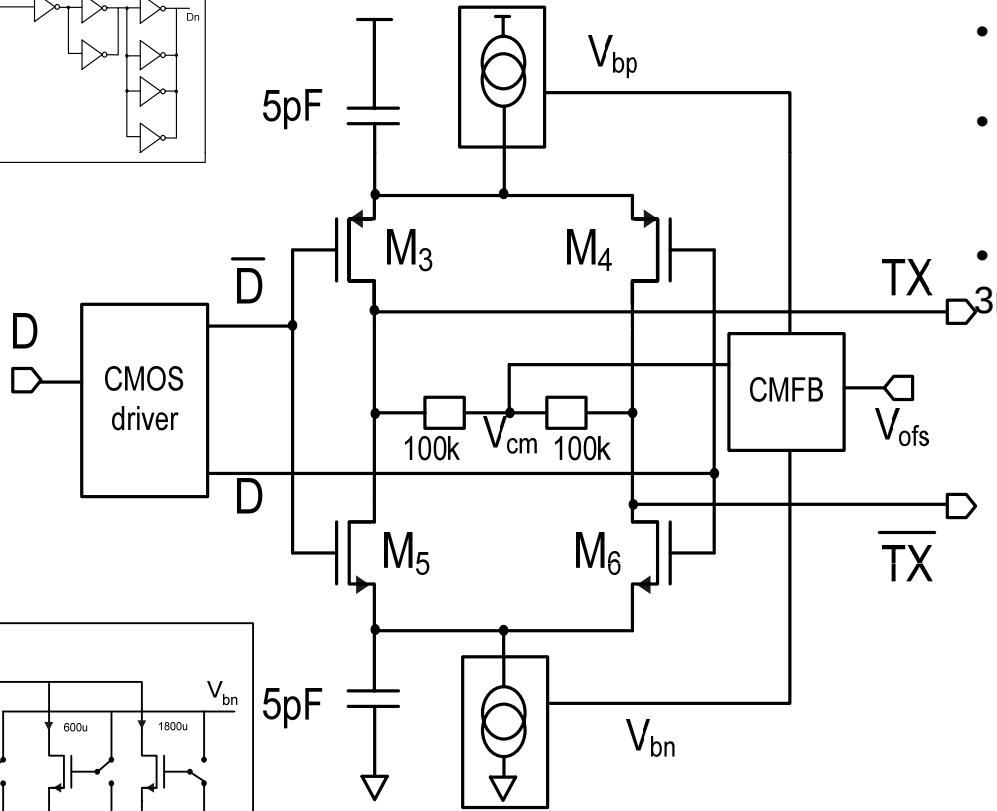
- 2-stage amplifier optimized for low power and fast rise time
- additional amplification Cc/Cf2
- decoupling from preamplifier DC shift caused by leackage
- trimable feedback current & comparator threshold
- preamp with regulated cascode and tripple-well nmos input transistor

LVDS Driver

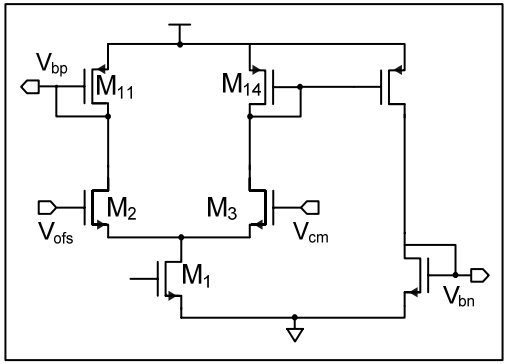


NOTE: Only thin oxide transistors for radiation hardness -> No thick oxide ECL transistors

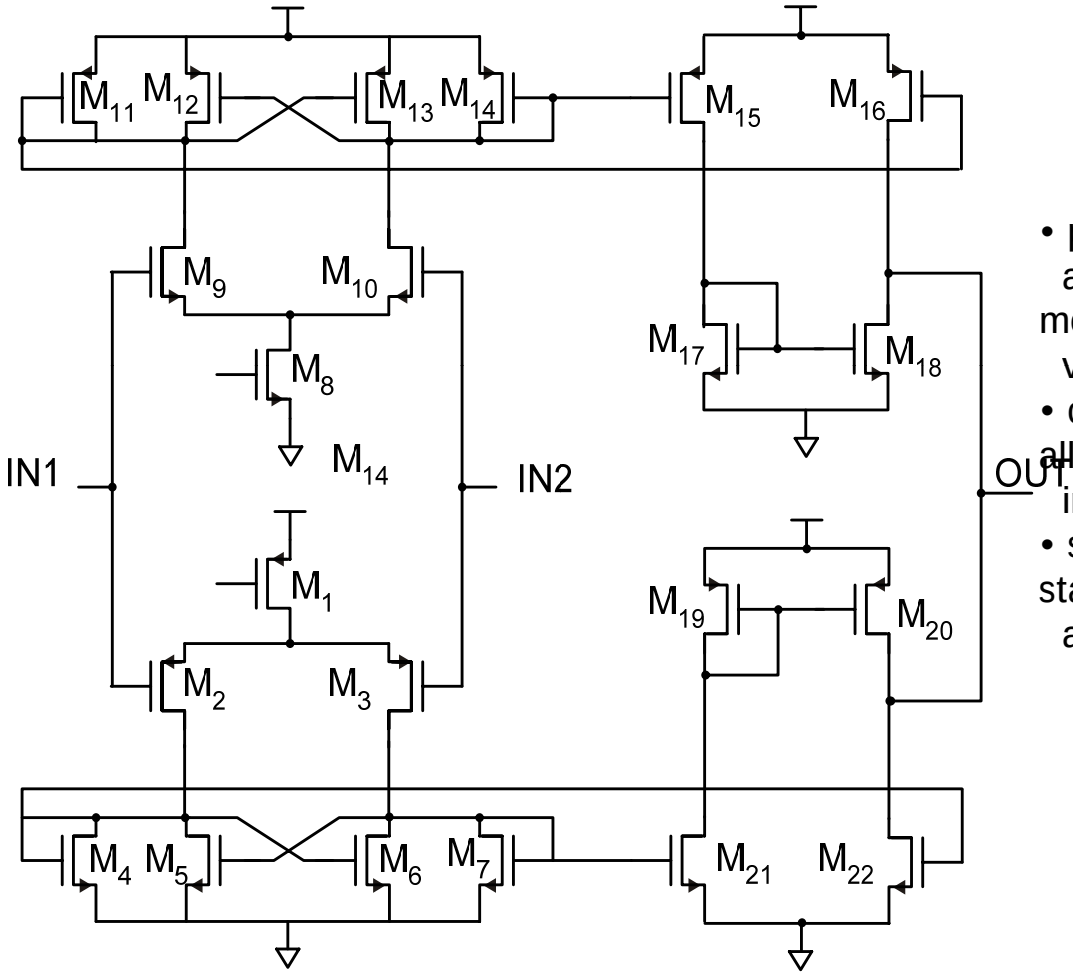
- standard LVDS architecture for 320MHz data rate and adapted to low supply voltage 1.5-1.2V
- current is routed to/from the output by four switches M3-M6
- common-mode voltage is measured by a resistive divider and controlled by a common-mode feedback circuit
- Output current is switchable between 0.6 - 3mA



Boni et al., IEEE JSSC VOL. 36 NO. 4, 2001



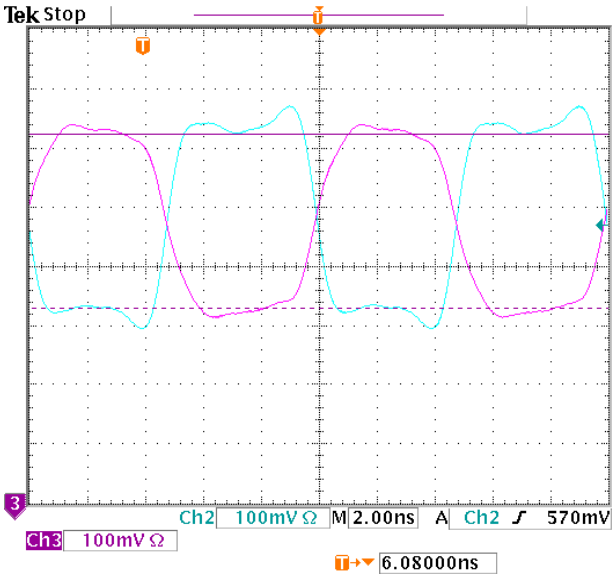
LVDS Receiver



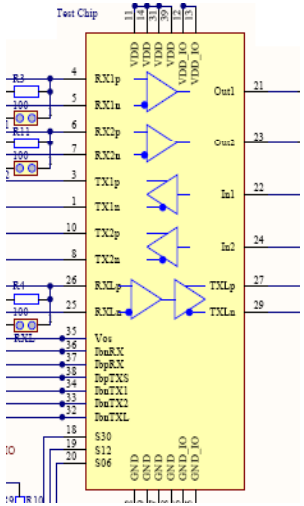
- parallel PMOS/NMOS comparator input stages allow operation in a wide range of common-mode voltages
- cross coupled positive feedback structure allows introduction of hysteresis
- second stage sums singals from both input stage and converts them to a CMOS output signal

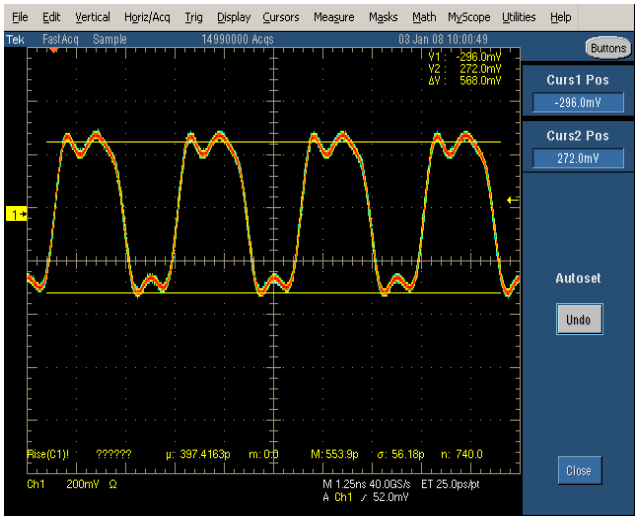
Tyhach et al., A 90-nm FPGA I/O Buffer Design With 1.6-Gb/s Data Rate for Source-Synchronous System and 300-MHz Clock Rate for External Memory Interface, IEEE JSSC, Sept. 2005

LVDS test chip & test setup



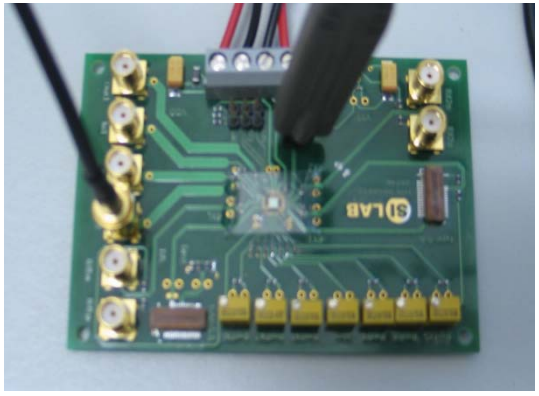
Transmitter, 100MHz
8pF probe cap.
300MHz scope bandwith



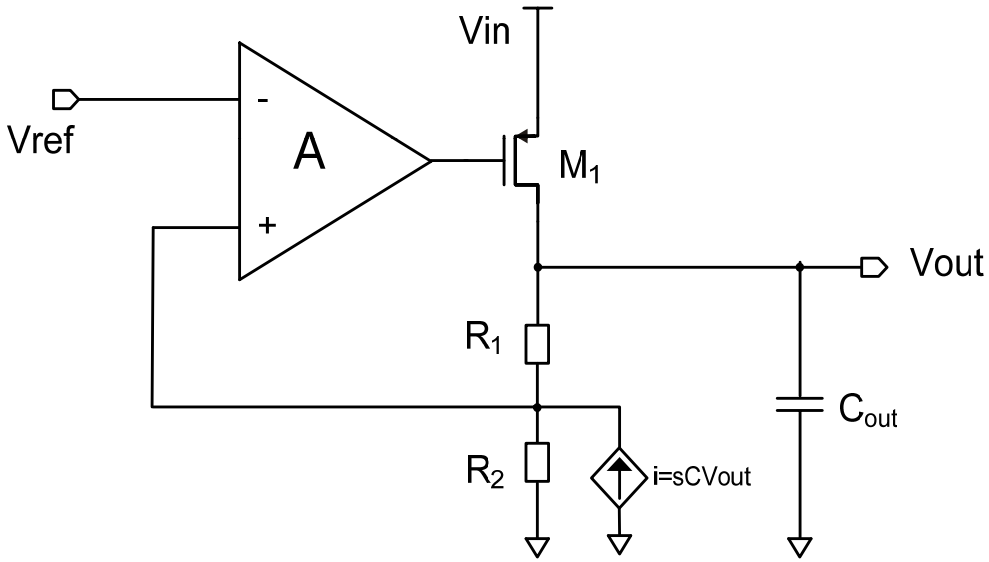


Transmitter, 320MHz
differential probe <1pF
cap.
1GHz scope bandwith
I=3mA

- A test chip submitted to UMC130nm
  July 2007
- two pairs of standalone receiver and transmitter
- One receiver in series with a transmitter. No need for CMOS signals going on/off chip
- Two type 0 cable adapter are available, to feed the output signal
  of transmitter via a type 0 cable to a termination resistor.



Low Drop Out Regulator



- LDO regulator for Vin=1.6V,Vout=1.5-1.2V
  minimum drop out voltage 100mV
- Iload=500mA
- Line Regulation:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{g_{mpt} r_{opt}}{A\beta} = \frac{5mV}{100mV} = \frac{1}{20}$$

- Load Regulation:

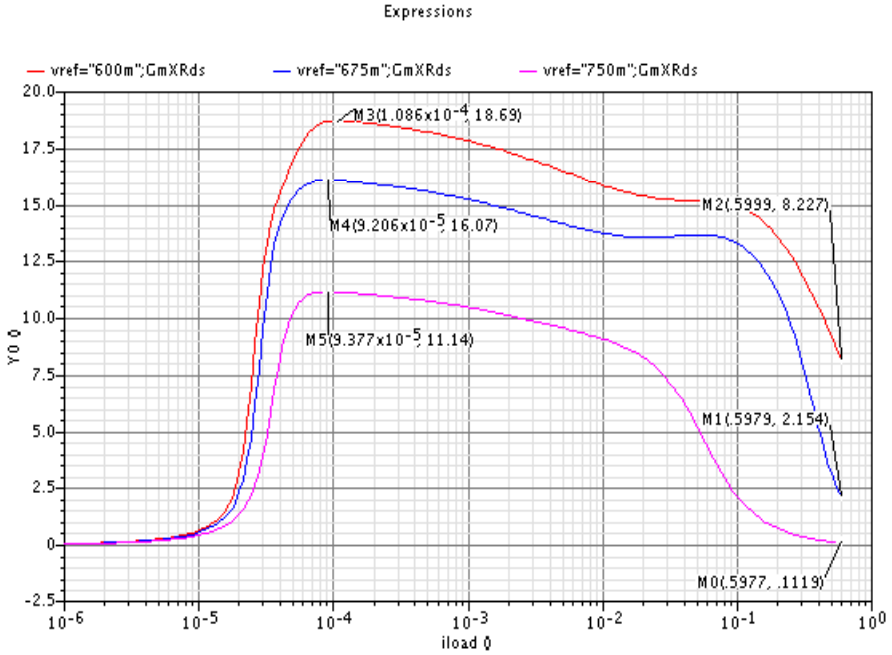
$$\frac{\Delta Vout}{\Delta I_{load}} = \frac{r_{opt}}{1 + A\beta} = \frac{5mV}{150mA} = 33m\Omega$$

- Instead of using the ESR of the output capacitance
  a zero is introduced by a special voltage controlled
  current cell.

$A\beta = 60dB$

$g_{mpt} r_{opt}$

Line & Load Regulation



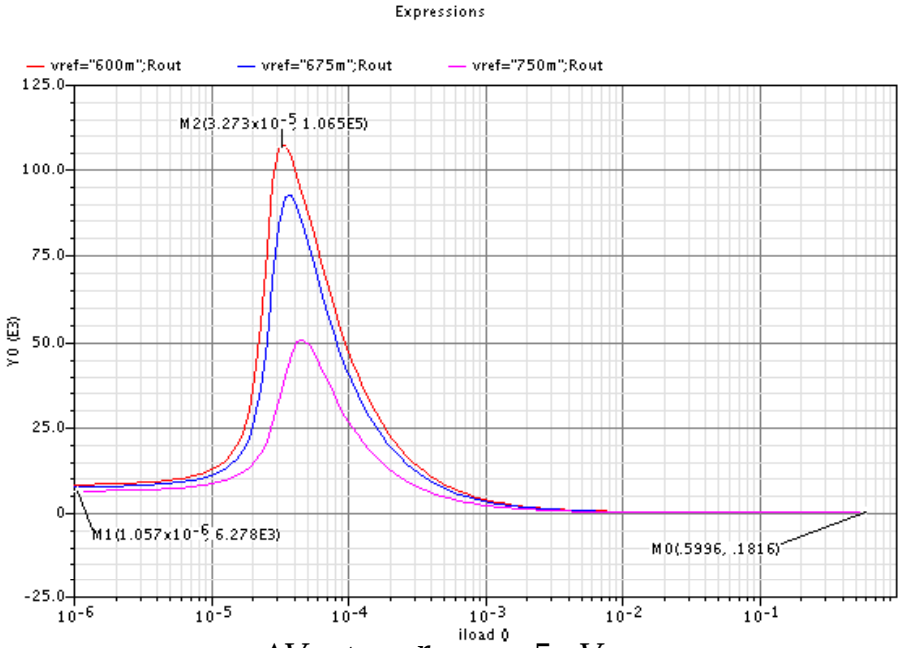
$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{g_{mpt} r_{opt}}{A\beta} = \frac{5mV}{100mV} = 0.05$$

$g_{mpt} r_{opt}$ varies between 0.1 - 19

For worst case and with $\beta = \frac{R_2}{R_1 + R_2} = \frac{1}{2}$

$$A = \frac{19}{0.05 * 0.5} = 760$$

Error amplifier with a DC gain of $A = 60dB$ meets the specs

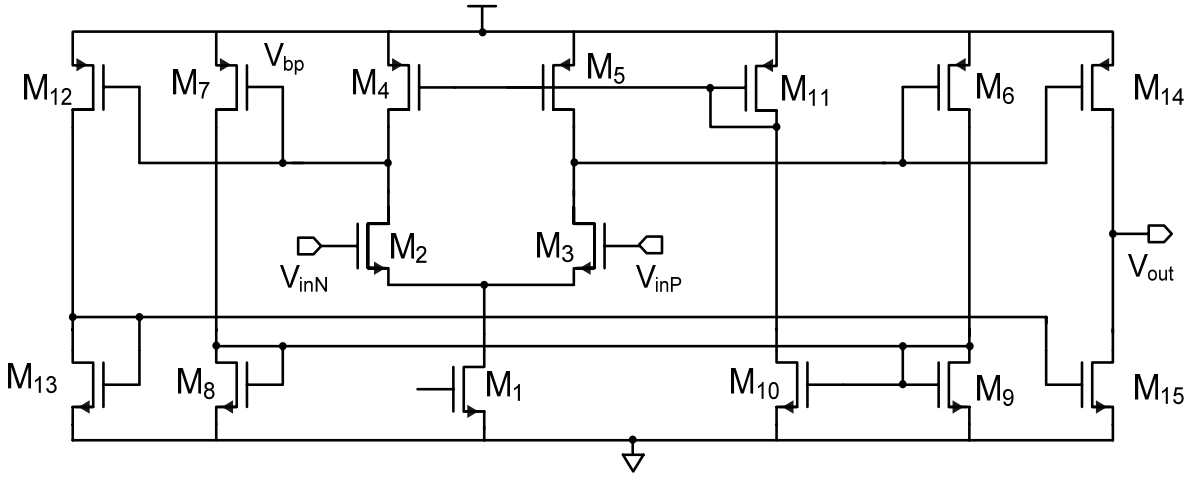


$$\frac{\Delta Vout}{\Delta I_{load}} = \frac{r_{opt}}{1 + A\beta} = \frac{5mV}{150mA} = 33m\Omega$$

Worst Case: R_{opt}=100K at I_{load}=300uA
Region of Interest I_{load} > 1mA R_{opt}< 5 Ohm

$$\frac{\Delta Vout}{\Delta I_{load}} < 10m\Omega \quad \text{with} \quad A\beta = 500$$

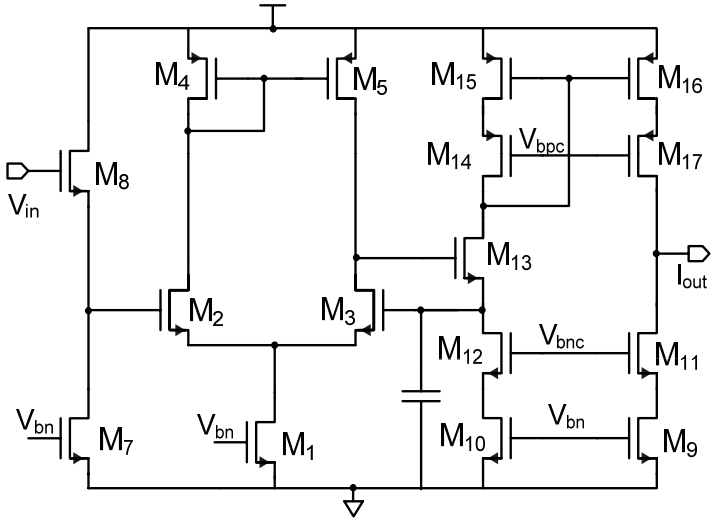
LDO error amplifier



- 2 stage error amplifier with fully-differential first stage combined with a common-mode feedforward biasing technique to have a rail-to-rail /class AB output stage and high gain at the same time.
- Conventional circuits would have transistors M4 & M5 gate-drain connected which reduces the output impedance and as a result less amplification at the first stage
- CMFF circuit: M7 & M6 sense common mode voltage. The currents of M7 & M6 are summed and averaged in M8 & M9 and than used to bias M4 & M5 via the transistors M10 & M11

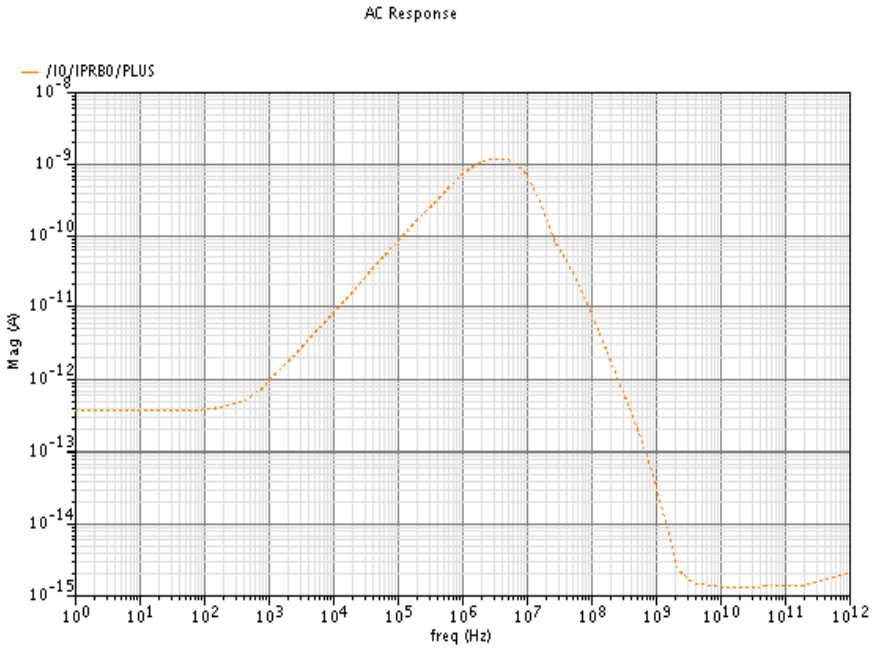
Mohieldin,Silva-Martinez,A Fully Balanced Pseudo-Differential OTA with Common-Mode Feedforward and Inherent Common-Mode Feedback Detector, IEEE JSSC, April 2003

Zero Cell for stability



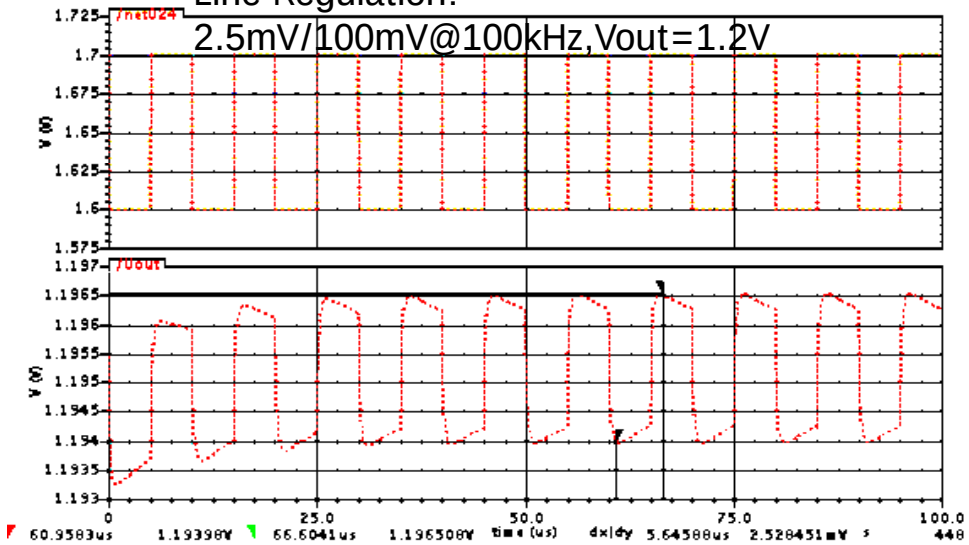
Chava,Silva-Martinez, A Frequency Compensation Scheme for LDO Voltage Regulators, IEEE Transactions on Circuits and Systems, June 2004

- stability is achieved by pole/zero cancellation. The zero is introduced by a frequency dependent voltage controlled current source.
- A frequency dependent current is flowing through the capacitor at the source of M13 which is mirrored to the output.

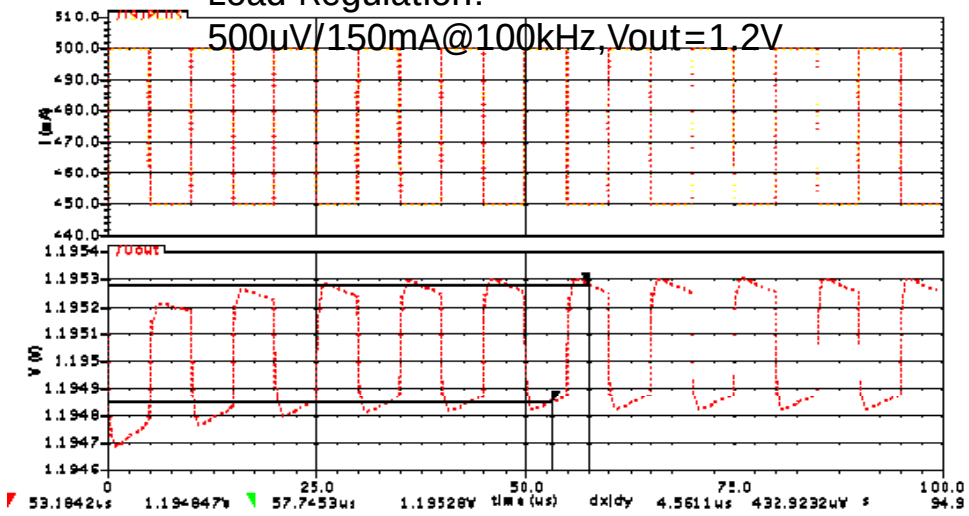


LDO simulations in frequ. & time domain

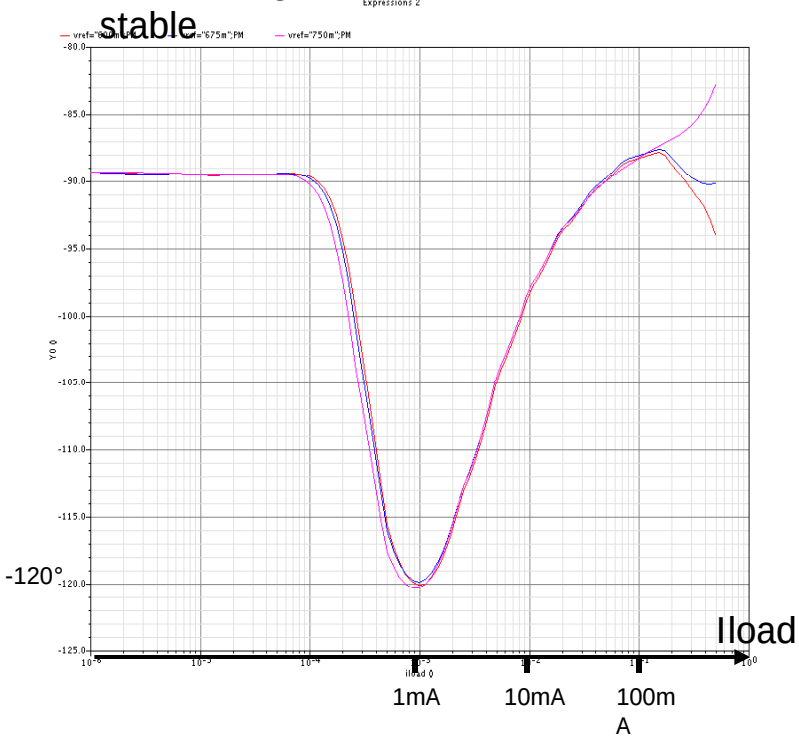
Line Regulation:
2.5mV/100mV@100kHz,Vout=1.2V



Load Regulation:
500uV/150mA@100kHz,Vout=1.2V



Vout=1.2V(red),1.35V(blue),1.5V(pink) Phase Margin > 60° -> circuit stable



BK: sensor

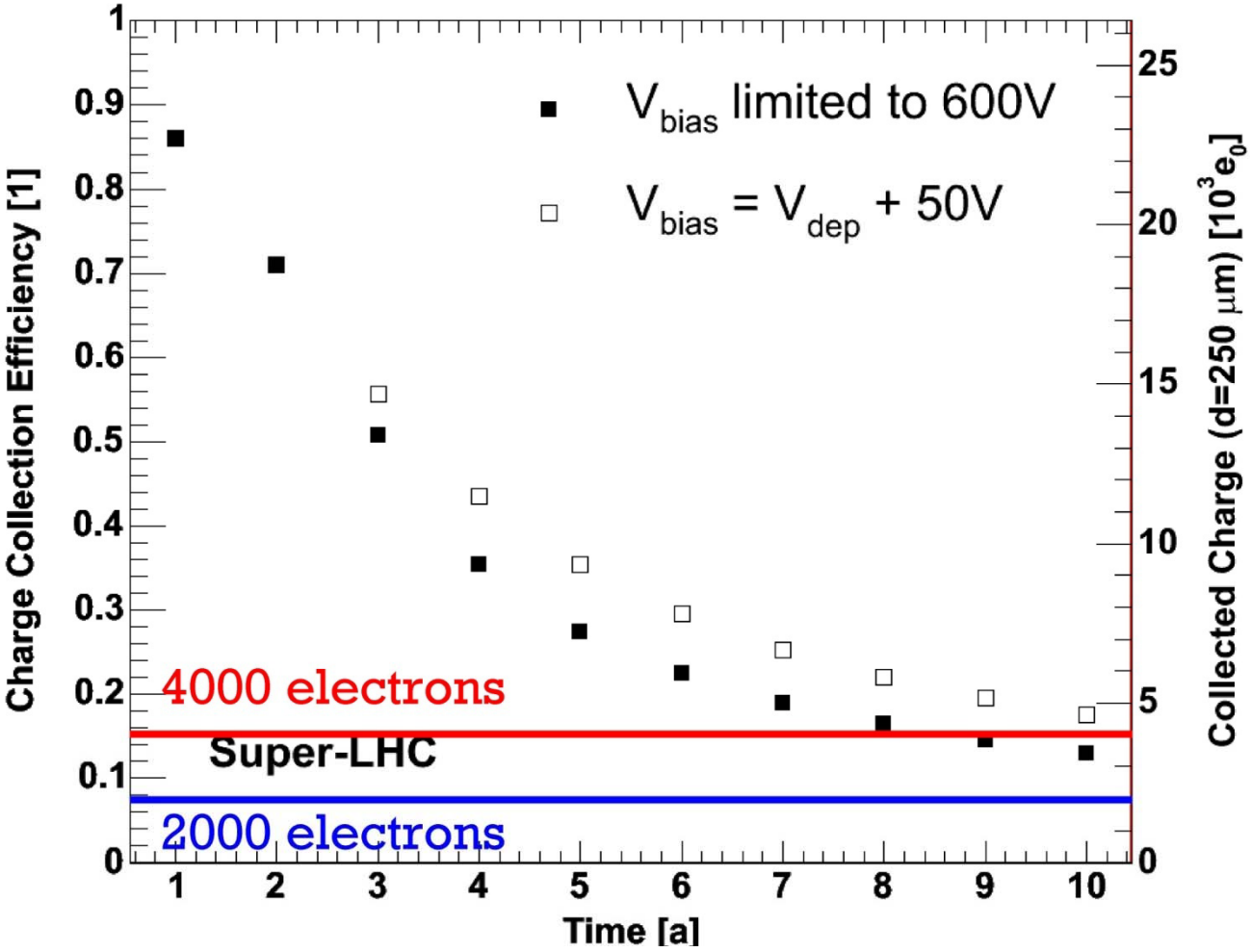
- Sensor

BK: sensor

- Planar Sensor

Low collected charge

- Scenario: current sensor, r=9cm, SLHC luminosity
- Current FE threshold: 4000 electrons
- Could the threshold be reduced to 2000 electrons?



ATLAS Upgrade

Planar Silicon Activities

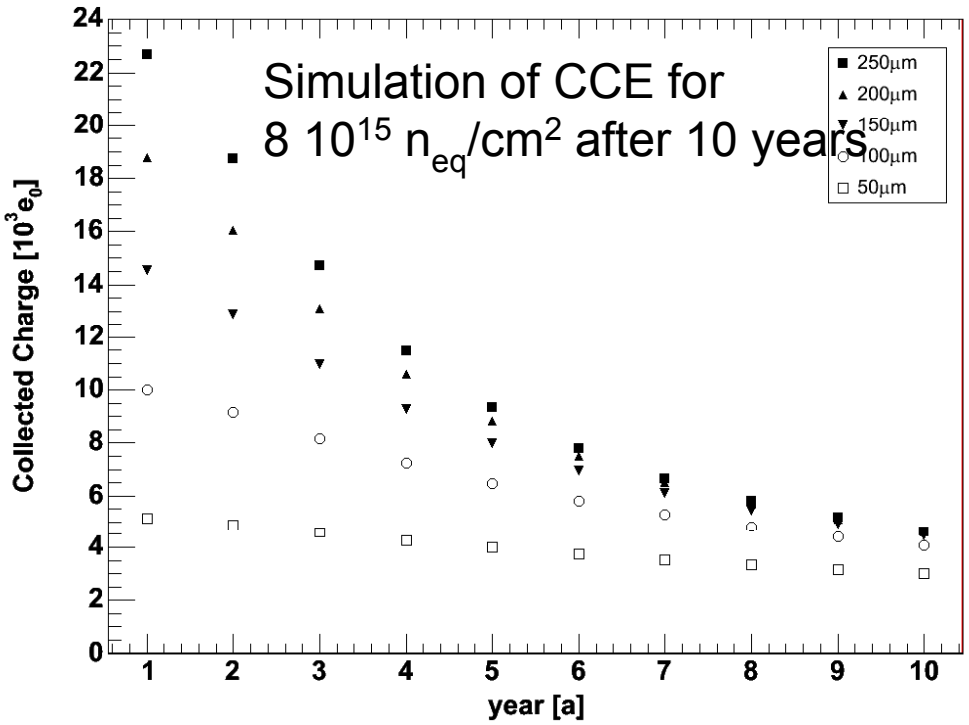
- planar silicon sensors are reliable, comparatively cheap and radiation hard to beyond 10^{15} n_{eq}/cm^2
- an R&D collaboration is forming, proposal currently being circulated
- the proposal focuses on
  - performance evaluation of planar sensors up to 10^{16} n_{eq}/cm^2
  - significant cost reduction to instrument also larger radii
  - edge reduction (“slim/active edges”) to avoid shingling on staves
  - threshold reduction to below 2000 electrons
- German participation:
  - HU Berlin/DESY
  - University of Bonn
  - TU Dortmund
  - Munich (MPP and MPI semiconductor laboratory)

The PlanarPixelProposal

- A proposal for R&D on planar pixel sensors for the ATLAS upgrade is currently being circulated
- Aim of this proposal is to form an R&D collaboration focussing on pixel sensors of planar silicon technology
- Specifically, research is proposed on
  - choice of bulk material: n-type vs. p-type
  - improvement of radiation hardness (reduction of trapping) for planar sensors at above 10^{15} n_{eq}/cm^2
  - significant cost reduction to be able to afford an increase of the instrumented area by one order of magnitude
  - edge slimming to enable staves without shingling
  - MC studies to determine the optimum pixel geometry
  - lowering the FE's threshold

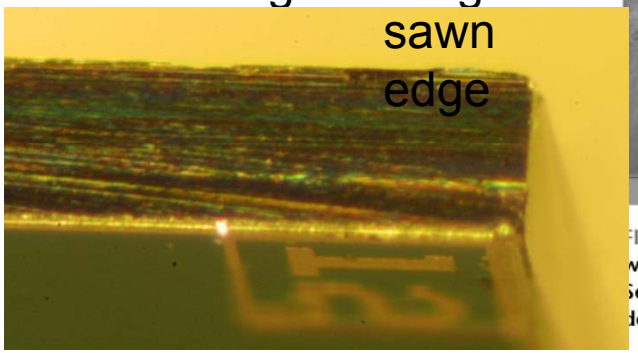
R&D in Dortmund: Radiation Hardness

- sensors must yield hits up to several 10^{15} n_{eq}/cm^2
- in this regime, deteriorated CCE due to trapping is the main concern
- Dortmund has started efforts to
  - explore the behaviour of planar sensors up to 10^{16} n_{eq}/cm^2
  - determine the fluence limits of the current sensor/FE-I3 detector
  - evaluate methods to reduce the trapping and improve the CCE at very high fluences



R&D in Dortmund: Edge Slimming

- Shingling of modules is used to avoid gaps of the hermeticity
- Shingling deteriorates the thermal performance and adds extra cost
- Stave designers strongly prefer one-sided stave concepts without shingling which requries very slim edges (< 200 µm)
- The current edge width (≈ 1500µm) is dominated by guard rings and a safety margin due to crystal defects inflicted by the dicing saw
- R&D areas in Dortmund:
  - evaluation of alternative dicing methods (e.g. laser-cutting)
  - study on the necessary number and width of guard rings
  - CCE of pixels face-to-face of the guard rings at the sensor's edge



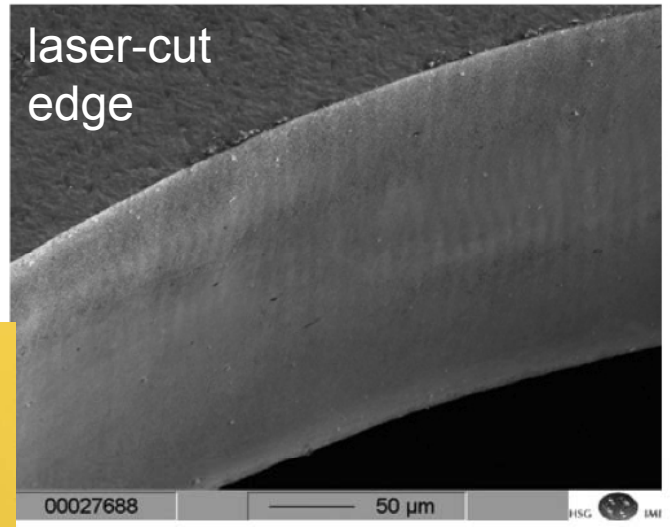


FIGURE 2: Edge of a silicon wafer with a thickness of 300 µm cut with a high average power picosecond laser of the TruMicro Series 5000. No chipping and heat affected zone can be detected.

BK: sensor

- Sensor-Diamond

Motivation for Diamond

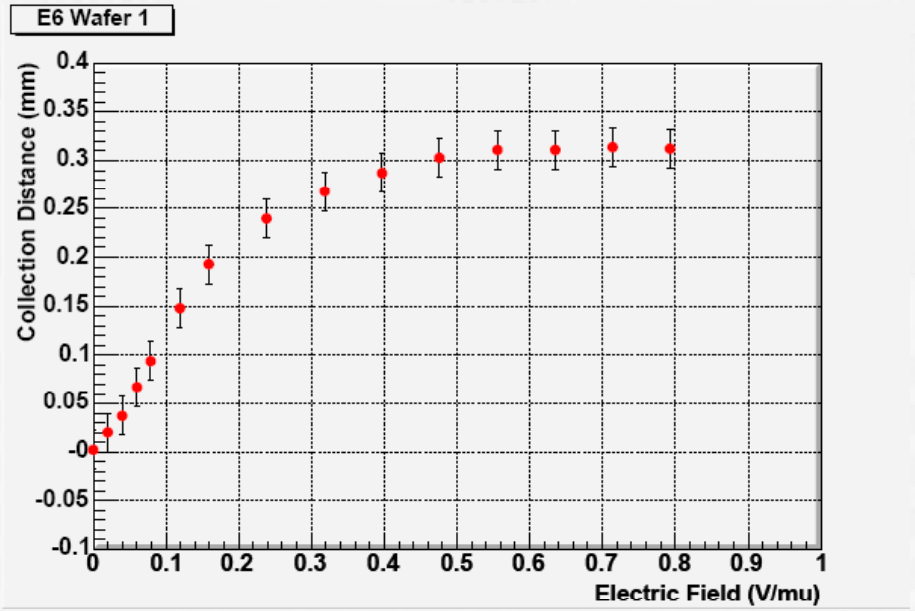
Advantages:

- High displacement threshold
- Low dielectric constant
  - Low capacitance
- High bandgap
  - Low leakage current
  - No need for p/n
- Room temperature operation
- Low readout noise
- High mobility/breakdown voltage
  - Fast signal collection
- High thermal conductance

Disadvantages:

- Less e-h pairs than silicon
  - e/h pairs per X_0 one half of silicon
- Polycrystalline material
  - Charge trapping
  - Minor inhomogenities in signal collection

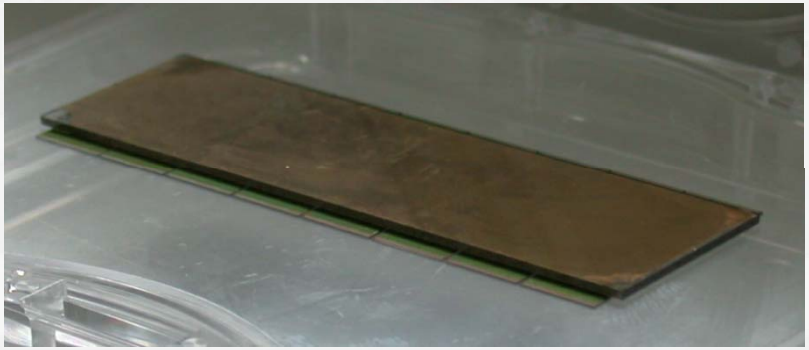
Towards a Large Diamond Pixel Module

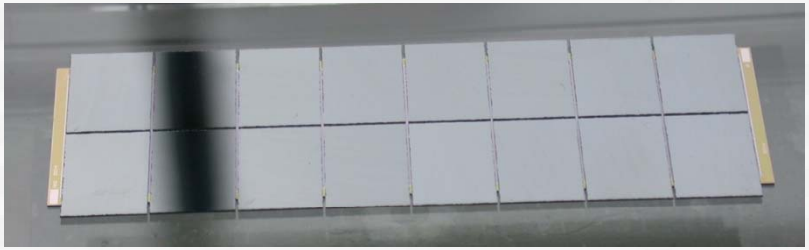


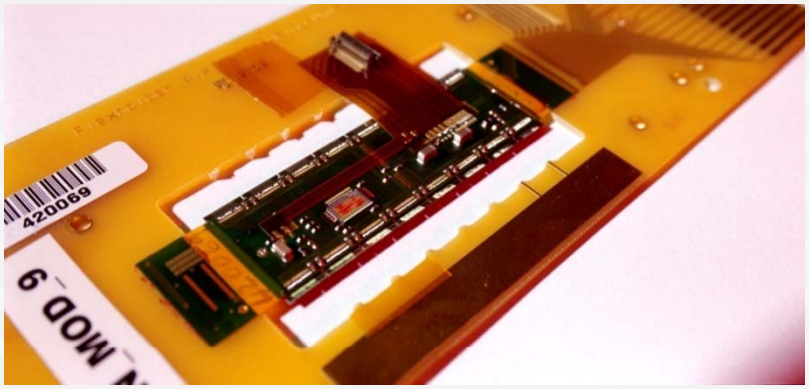
- Diamond sensor courtesy of RD42, H. Kagan, Ohio
- Material with high charge collection is essential for sensor application.
- Charge collection distance: Distance a hole and an electron move apart before being trapped.
- Collection distance of this wafer: 200µm (edge) to 310µm (center)

Diamond Pixel Module

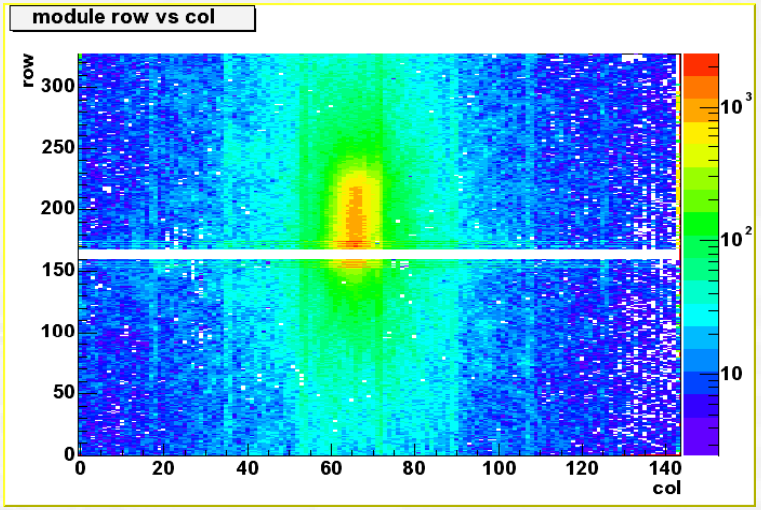
- Sensor:
  - Active area of 61x16.5mm^2
  - Thickness 800µm
  - Pixel size 400(600)x50µm^2
  - Total of 46k pixels
  - First sensor of this size
- Readout by 16 ATLAS FE-I3:
  - ATLAS pixel production chip

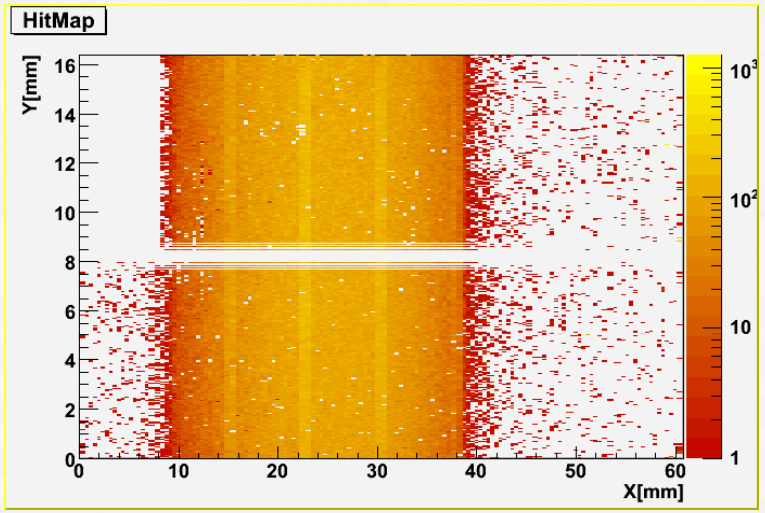






Diamond Module in Testbeam





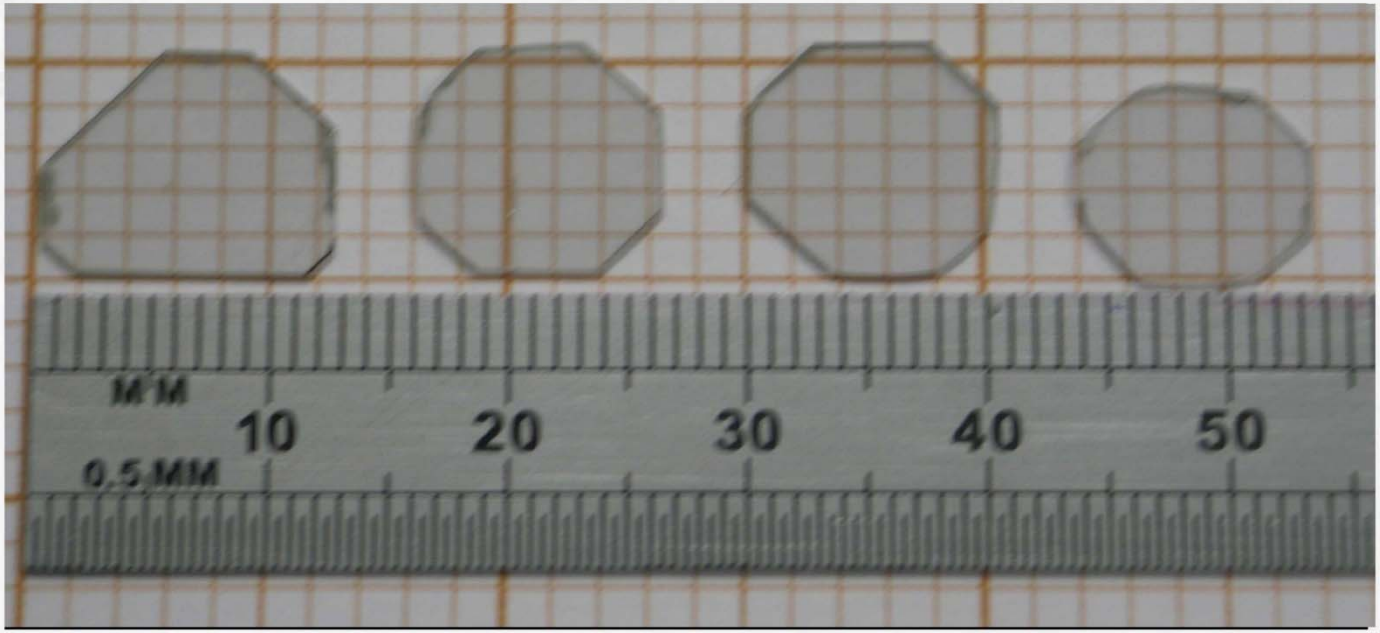
CERN

- 180GeV pions
- Only a few hours run during the last days of the CERN testbeam period in 2004
- No telescope information

DESY

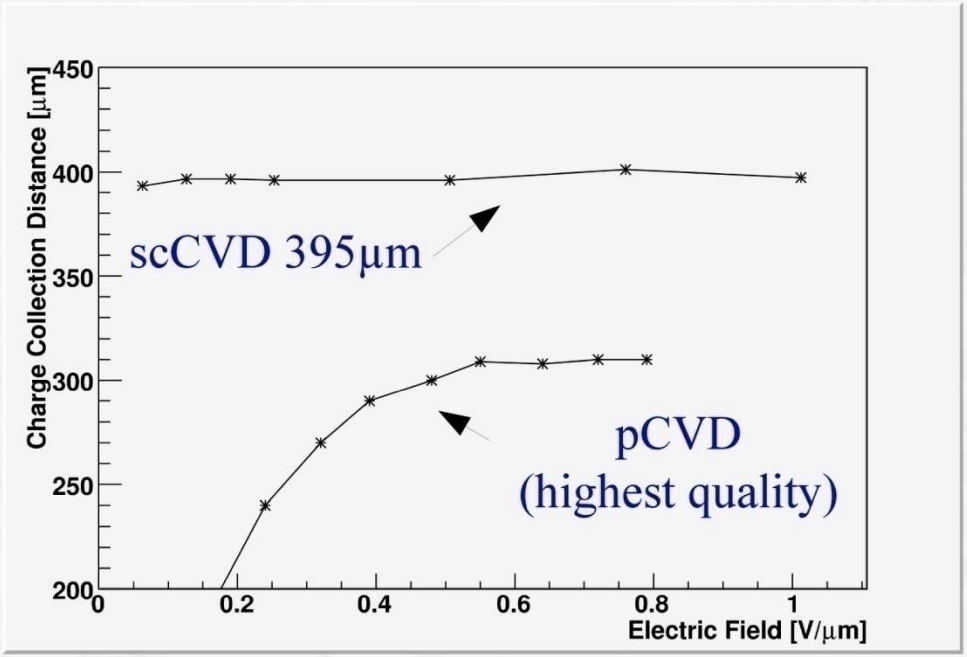
- 4-6GeV electrons
- Illuminated region given by triggering scintillator
- First one end of 2004
- Second one last week

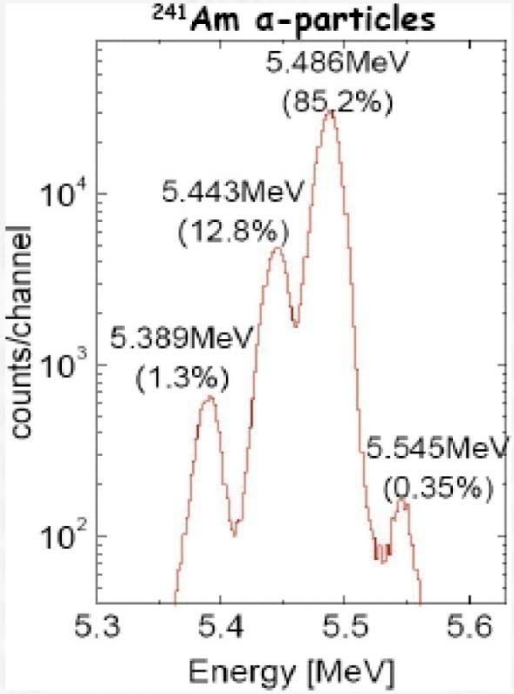
Single Crystal CVD Diamond



- pure monocrystalline material
- no grain boundaries, no charge trapping or pumping effects
- commercially available in sizes of about 1cm² (10mm×10mm)

Properties of Singe Crystal Diamond

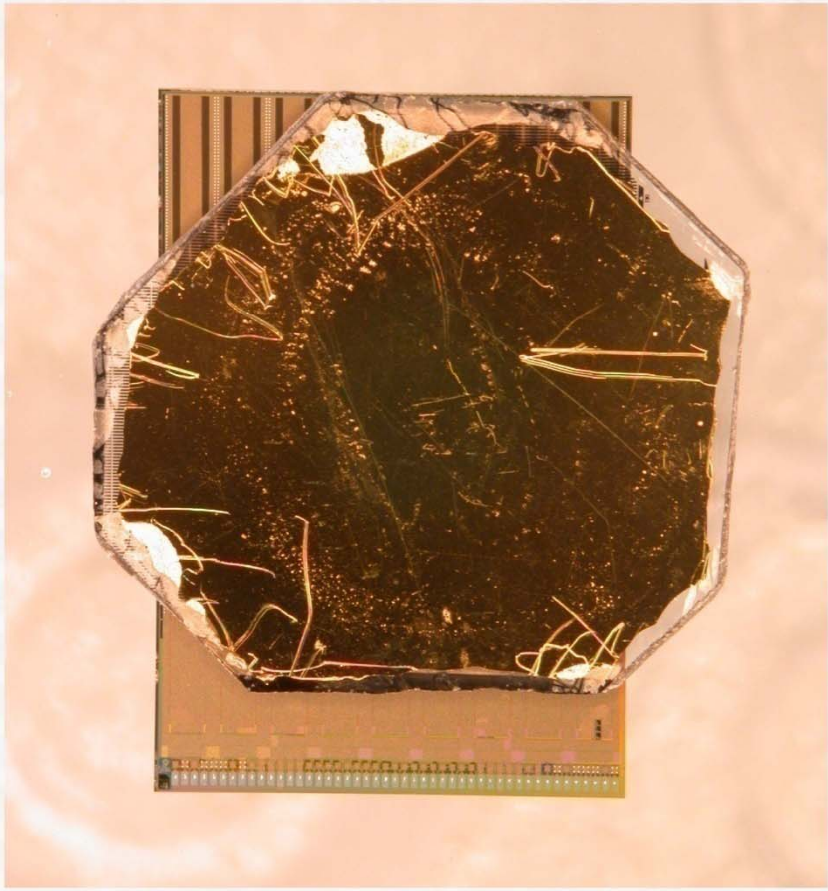




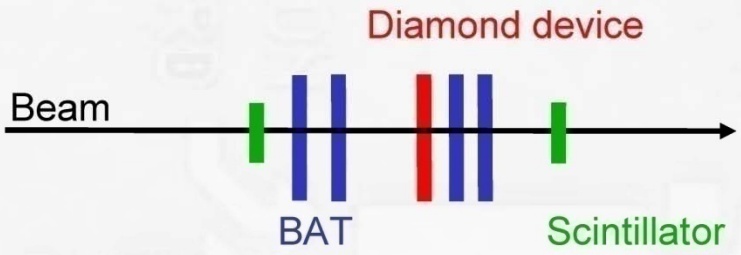
- first tested as pad detector, spectroscopic grade properties
- Charge Collection Distance:
  Collected charge expressed in terms of expected charge of a detector of given thickness D; ccd = $Q_{meas}/Q_{created}$*D
- full charge collection at fields lower than 0.1V/μm
- no pumping effects observed

Single Crystal Diamond Pixel Device

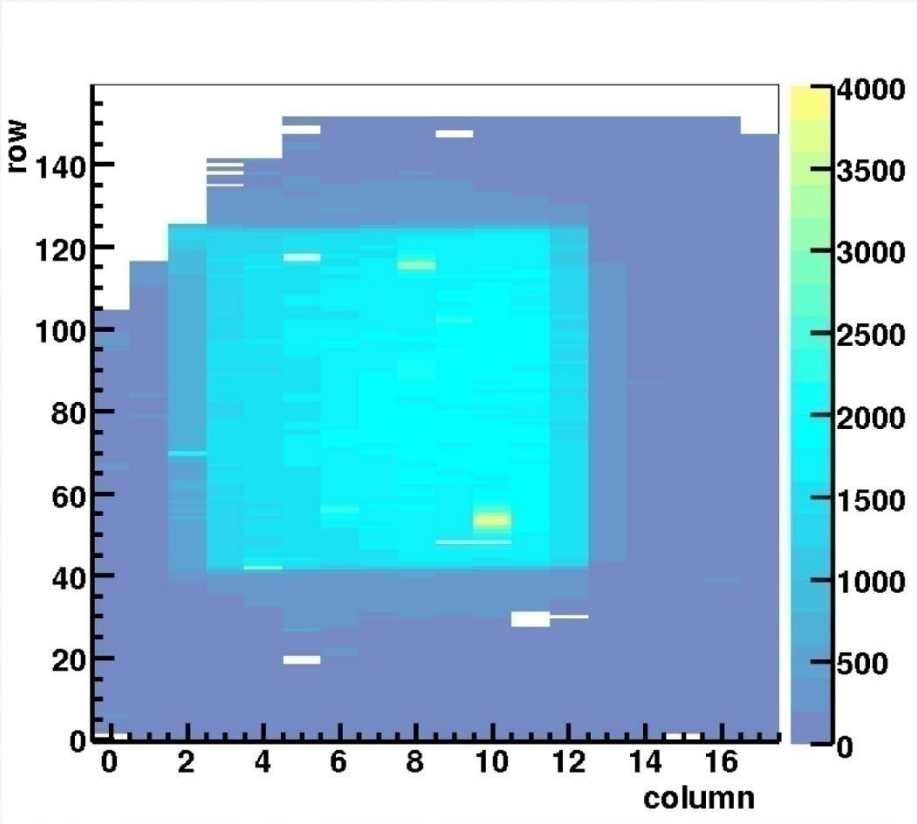
- hybrid detector: diamond sensor bump bonded using a standard wafer process (IZM) to the ATLAS-pixel readout chip (FE-I3)
- processing steps needed from raw diamond to fully working detector doable at short timescale (weeks)
- 2880 pixels of 50x400µm² size, ~400 not covered because of sensor geometry
- threshold of ~1700e at a noise of ~130e. Noise comparable to the noise of the bare electronics chip, not influenced by sensor



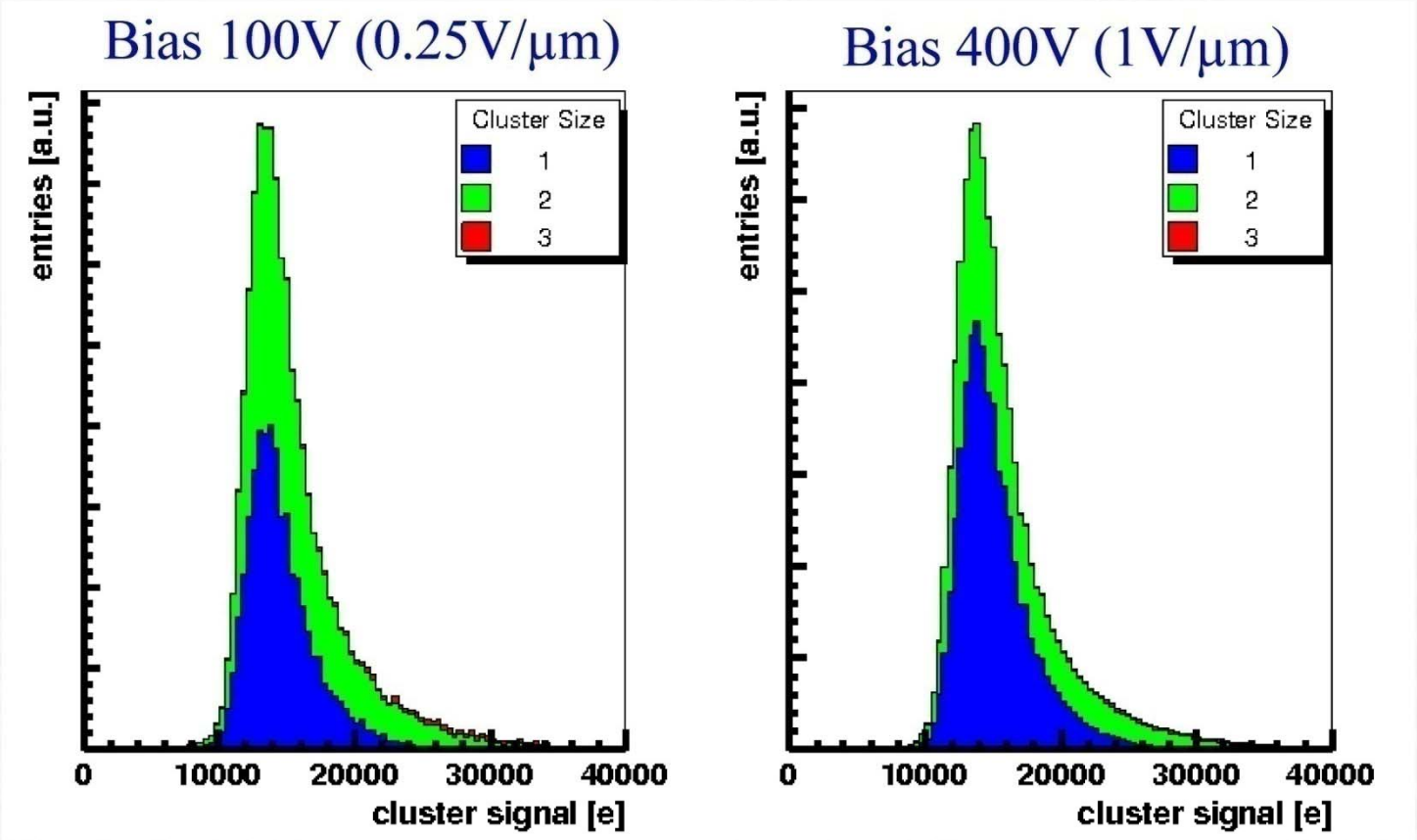
Testbeam



- In 100GeV pion testbeam in October 2006
- eight noisy and twelve bad channels caused by electronics, one by metalization
- shape of detector and trigger-scintillator visible



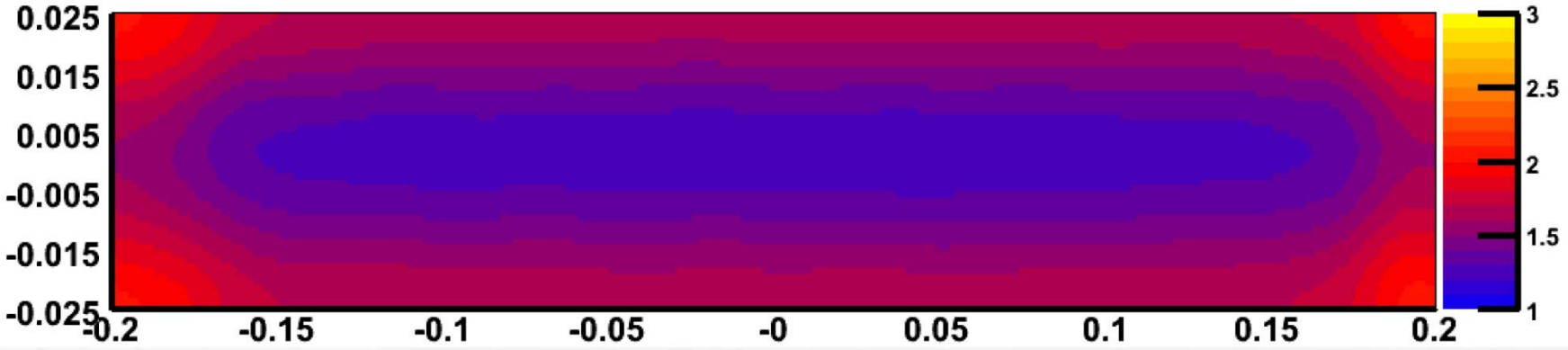
Charge Collection



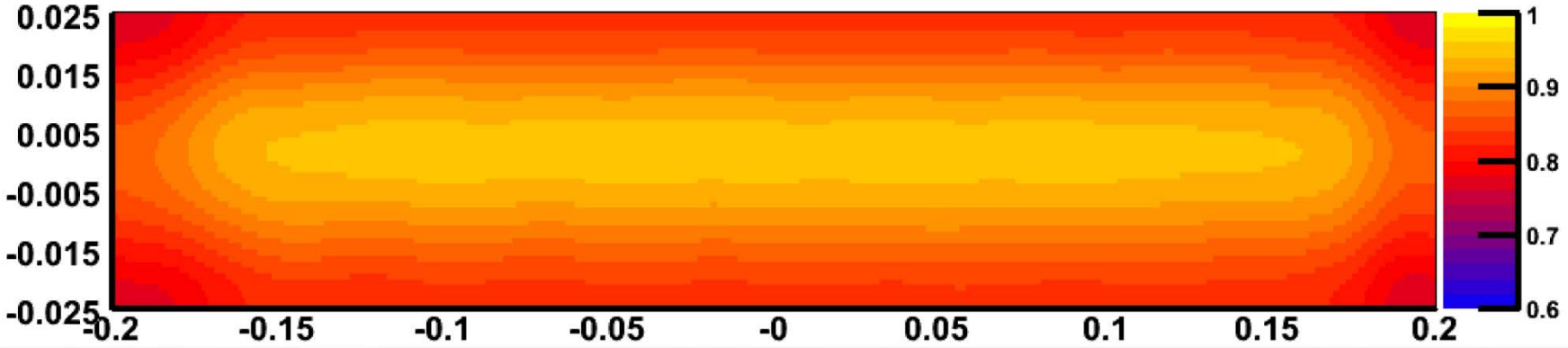
- full charge collection down to electric fields as low as 0.25V/µm
- charge carrier drift velocity and therefore cluster size adjustable by electric field

In Pixel Characteristics

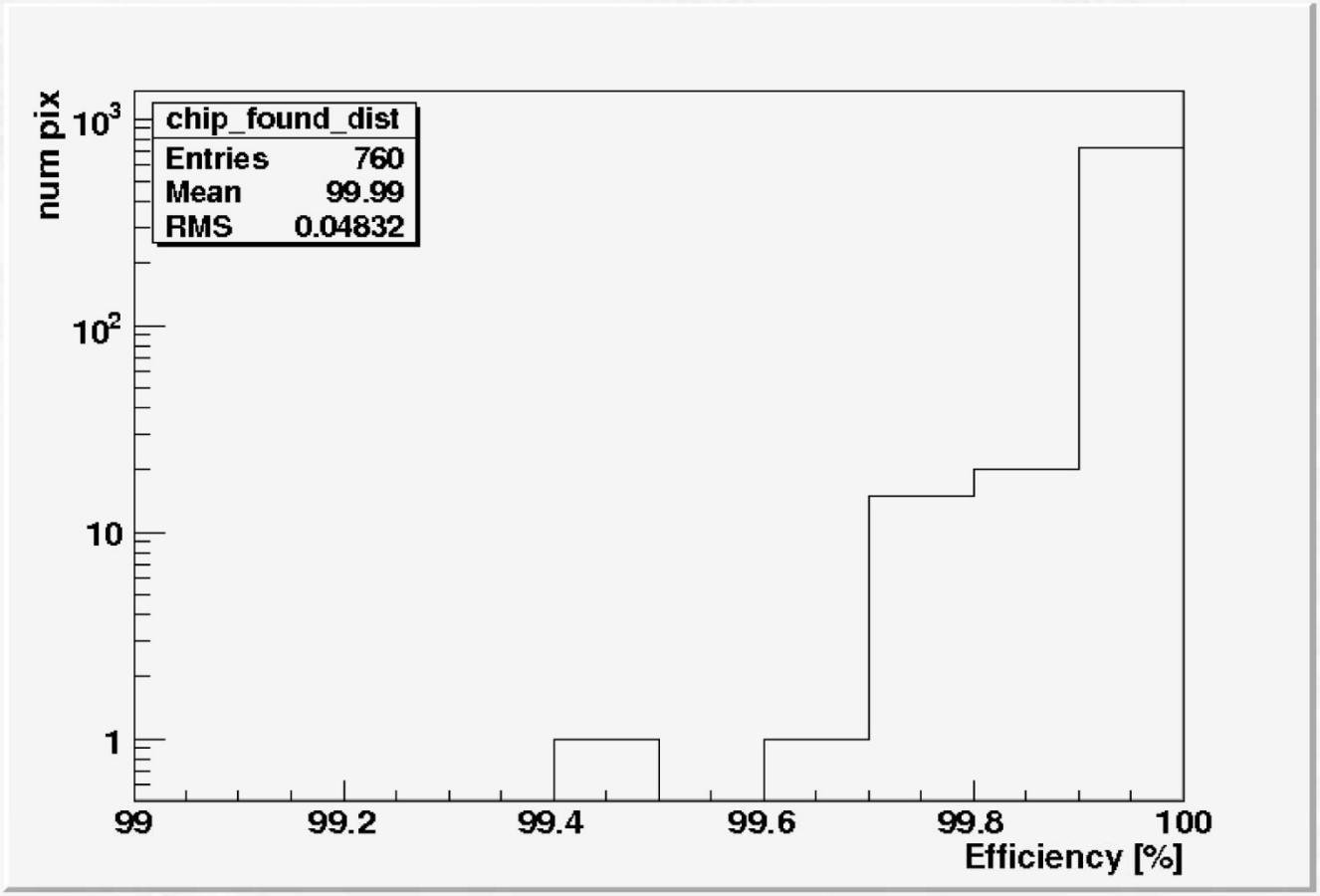
Mean Cluster Size



Fraction of signal in seed



Efficiency



- efficiency higher than 99.9% for most pixels, not finalized

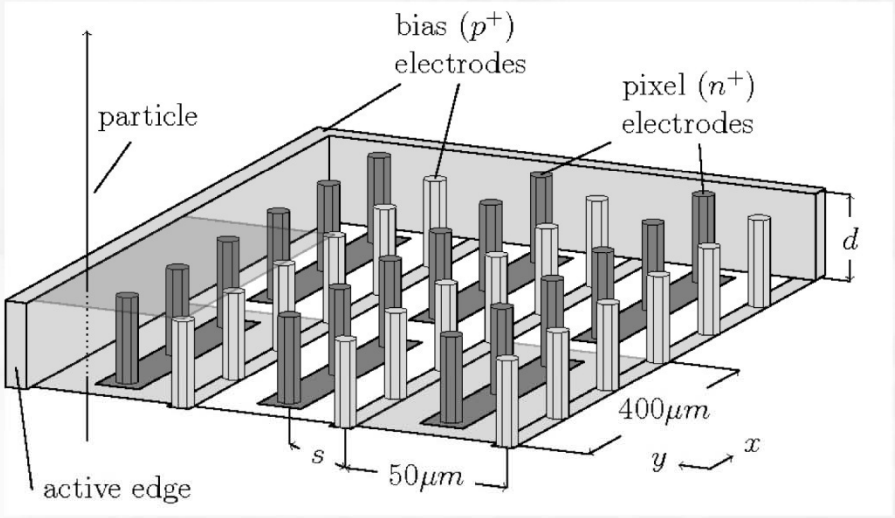
Conclusion

- Single crystal diamond is available
  - sizes of 1cm^2
  - full charge collection already at 0.2V/µm
  - no pumping and trapping effects observed
- Successful hybridisation of a scCVD diamond pixel detector
- Successfully operated in testbeam
  - efficiency of 99.9%

BK: sensor

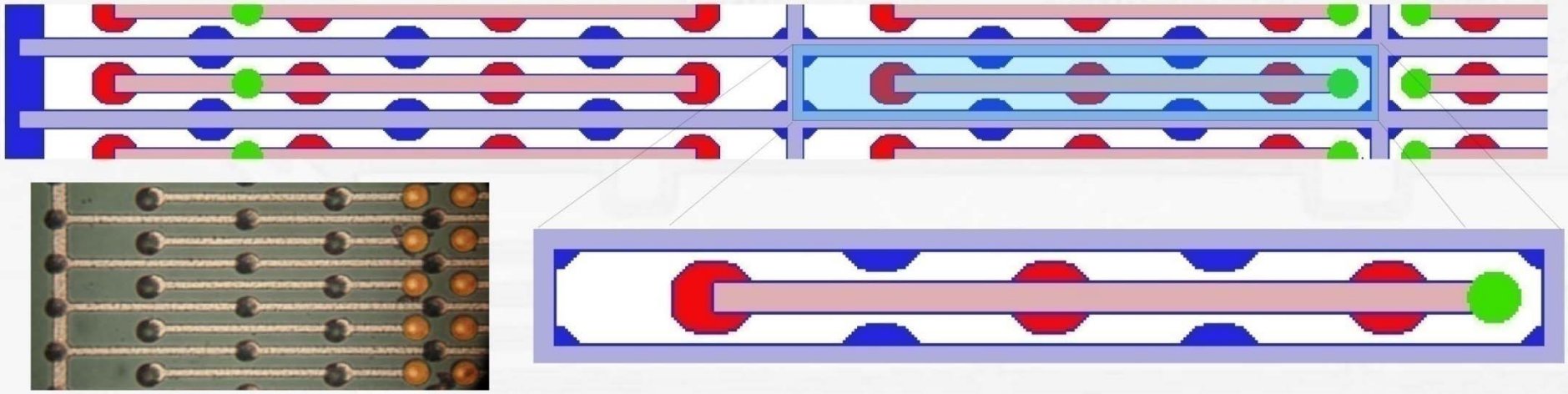
- Sensor-3D

Advantages of 3D detectors



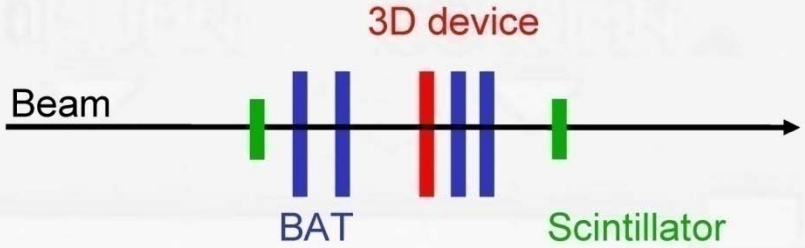
- Advantages
  - Direction of charge collection (s) is decoupled from direction of charge generation (d)
  - Lower depletion voltage
  - Edge usable as electrode. Sensor active up to it's physical dimensions
- Disadvantages
  - Electrode structure induces material inhomogeneities
  - Increased capacity

ATLAS-compatible 3D Detectors

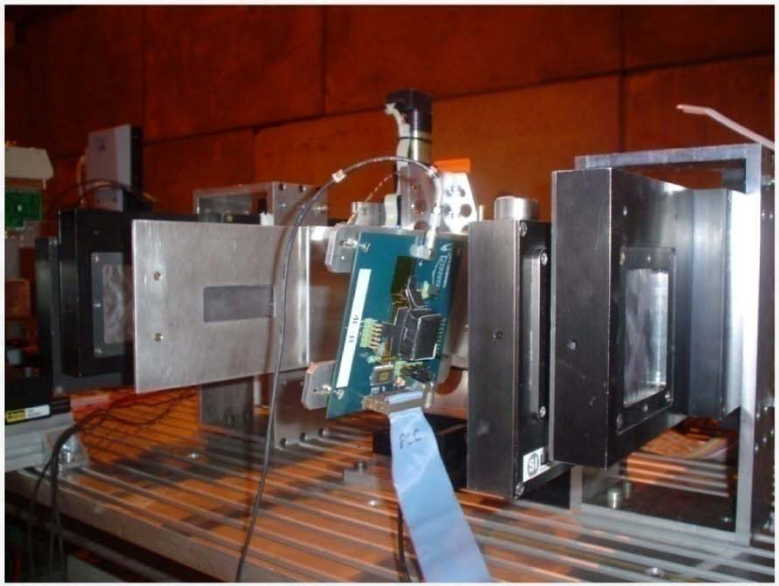


- Design adapted to ATLAS-pixel pattern
- Different electrode configurations implemented (2,3 or 4 electrodes per pixel)
- Hybrid detector: 3D-sensor bump bonded using standard wafer process (IZM) to the ATLAS-pixel readout chip (FE-I3)
- 2880 pixels, pixelsize 50x400μm^2 (edge pixels 50x500μm^2 with active edge)
- Zero supressed digital readout with a threshold of 3000e.
- Analog information via time over threshold (TOT)

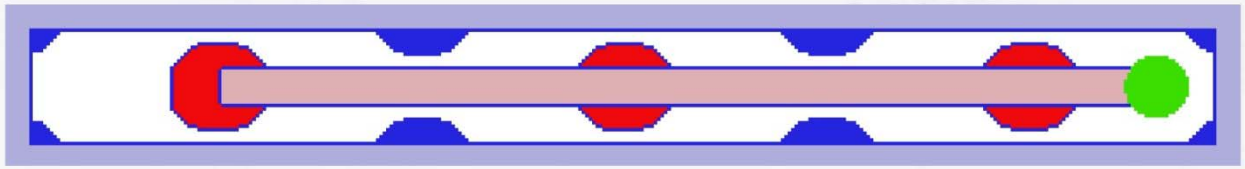
Testbeam Setup

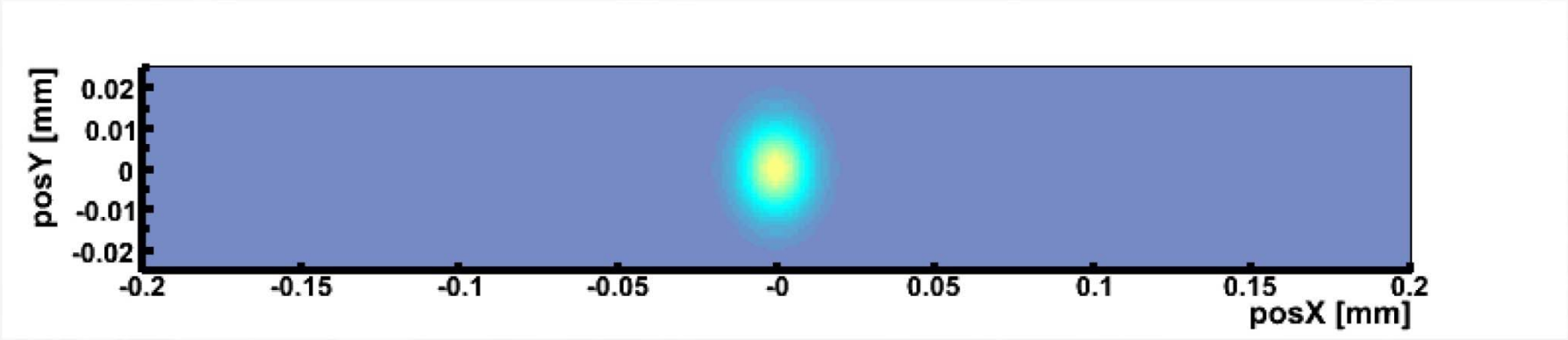


- CERN 100GeV pion beam
- Triggering scintillators
  - front and back
- BAT Telescope
  - 50µm strip telescope
  - tracking resolution of ~5-7µm
- Focus for this talk on 3D-3E
  - Threshold 3000e
  - Bias scan (5V,10V,15V,25V)
  - Angular scan (0°, 15°)



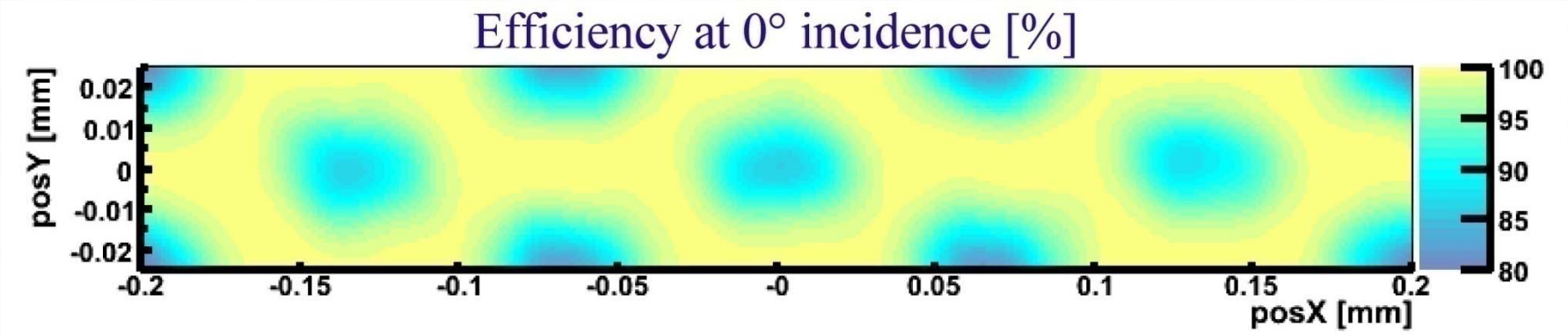
Plot Resolution





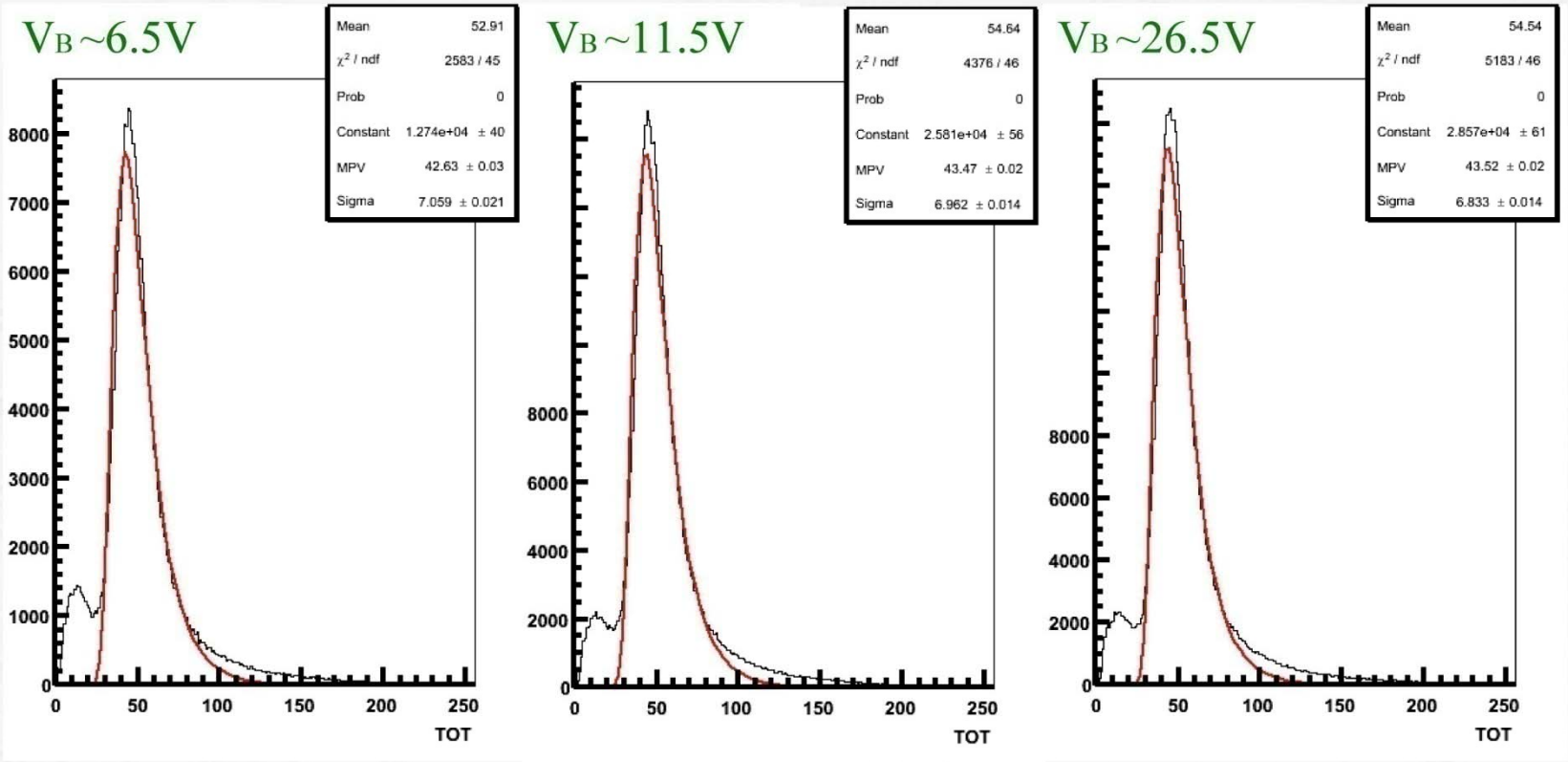
- Telescope resolution of ~6µm (in y-direction better, in x-direction a bit worse)
- Binning needed because of statistics
- Precision is limited by resolution of telescope and by statistics
- Effective resolution of ~8µm

Efficiency



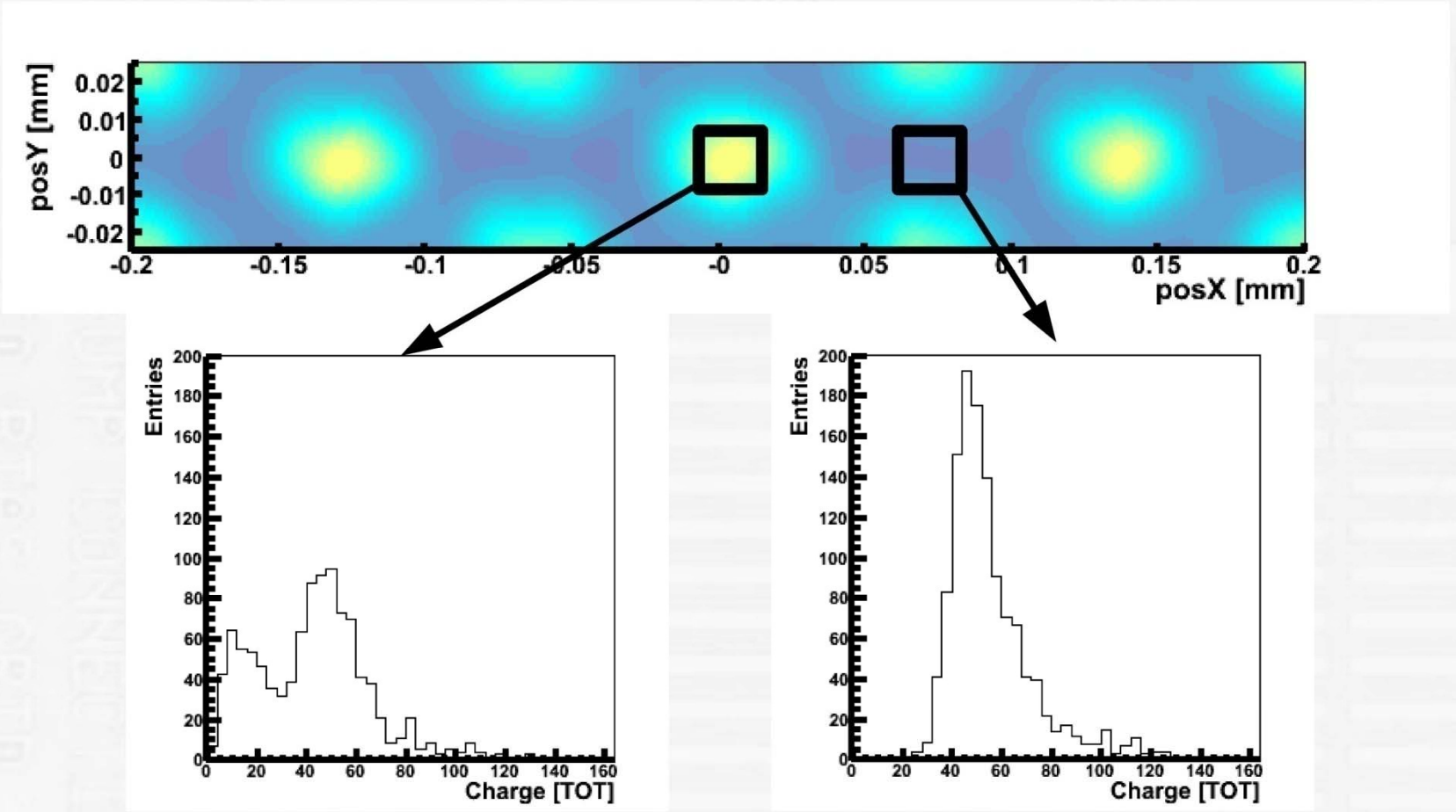
- Measured position efficiency
  (spot efficiency × telescope resolution/binning)
- Efficiency in bin depends on folding effect
- Area integrated efficiency: 96.2%±0.1%
- Assuming 0% electrode efficiency this would correspond to a diameter of 13µm
- Etched electrode diameter 17µm

Charge Collection



- Low voltage operation; cluster signal saturation expected at ~8V
- MPV 43TOT (14000e) , Mean 55TOT (18000e), Threshold 0TOT (3000e)
- Tail on the left are real events, not noise!

Charge Losses

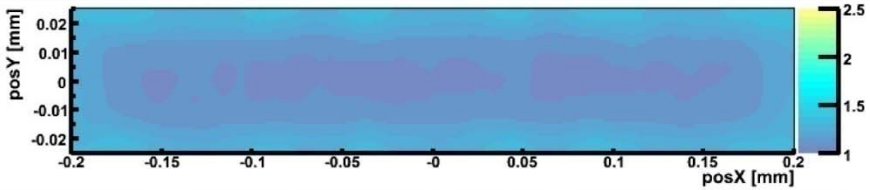


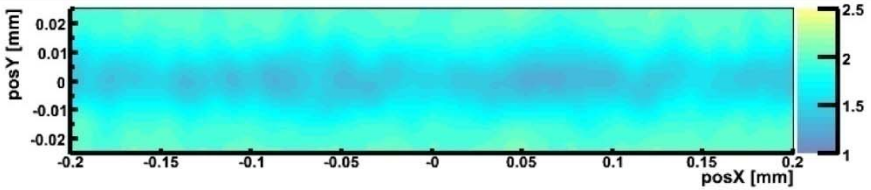
- Loss in charge collection at electrode position

Charge Sharing

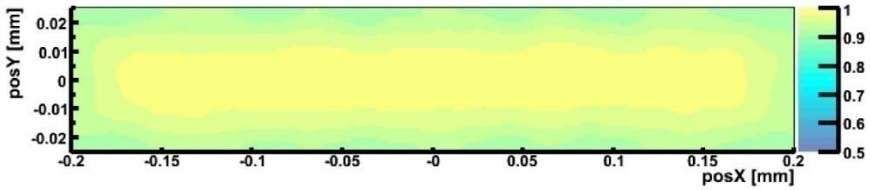
0°  15° (limited statistics)

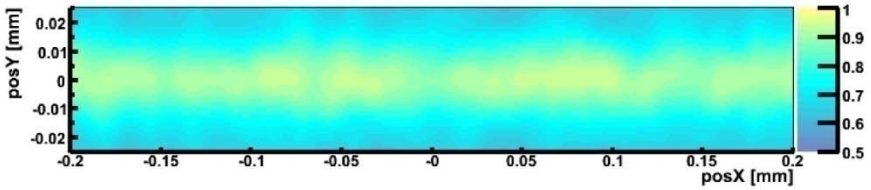
Mean Cluster Size



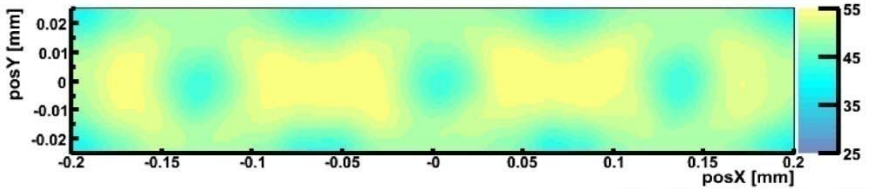


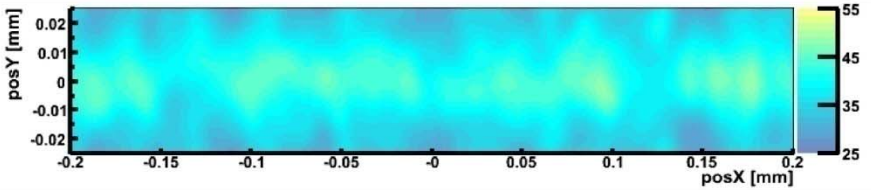
Fraction of Cluster Charge in Seed





Mean Pixel Charge





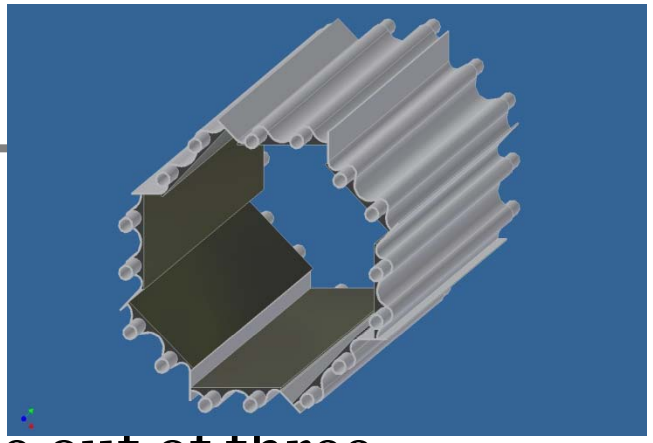
Conclusion

- First fully working ATLAS-compatible 3D devices operated in testbeam
- Efficiency of 96.2% at normal incidence in agreement with electrode structure, but dependent on used threshold
- Efficiency of 99.9% for angular mounting of 15° with “no” dependence on threshold

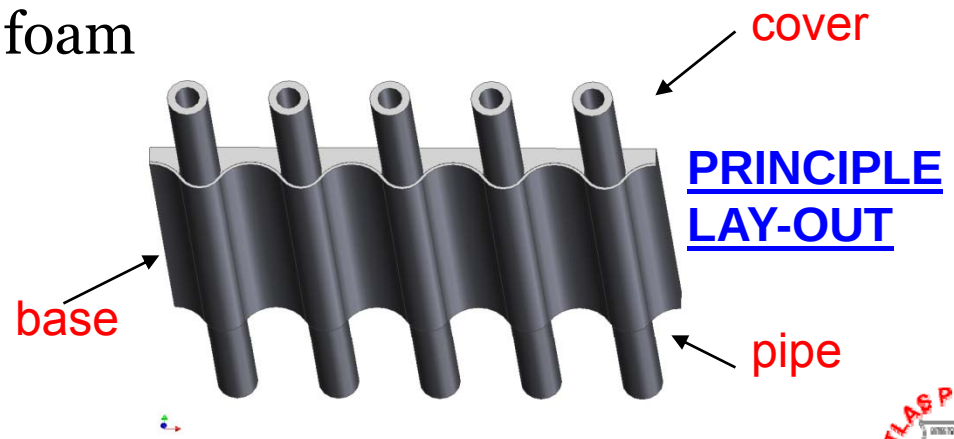
BK: Mechanics

- BACK UP: Mechanics

Mechanics

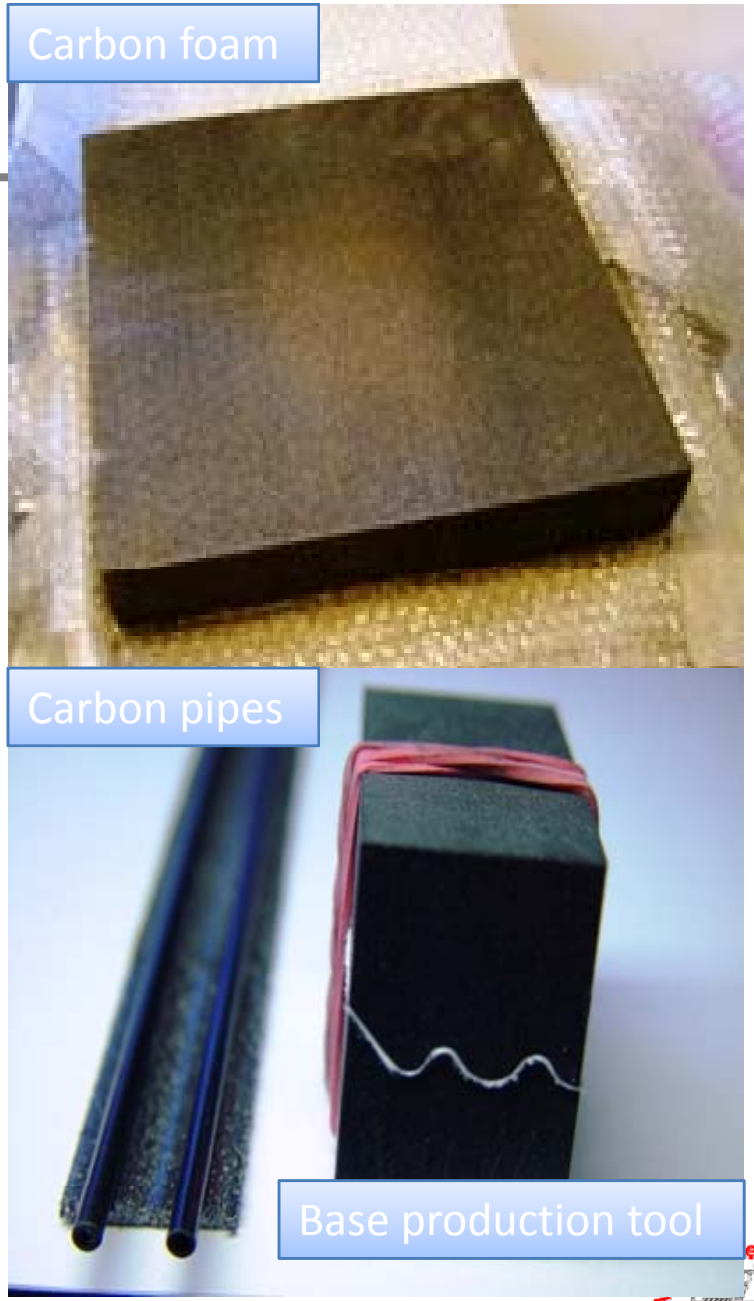


- Study of a new stave concept
- The proposed stave structure is made out of three basic components:
  - an accordian-shaped “base” made of carbon fiber composite materials
  - “cooling pipes” made of carbon
  - “cover” made of carbon foam



Realization

- Cover made from POCO foam:
  - Density: 0.4923 g/cm^3
  - Thermal conductivity:
    - 145 W/mK out of the plane (k_x)
    - 45 W/mK in the plane (k_y, k_z)
- Prototype carbon pipe:
  - A braided hose with 8 fibers 3K roving was used for the first prototype => pipe with Ø=3.0mm and thickness 250µm
- Double Ω base:
  - Pressed carbon sheet using a special tool



Status Mechanics

- Long pipes (750mm) under production 80mm prototype available and under investigation
  - Check leak tightness
  - Perform Overpressure tests
  - Optimize production procedure
- Investigate a “long” stave containing two pipes, the carbon base, and the poco foam cover
  - Heat conductivity tests
  - Stability
  - …

BK: TSV MPI

- TSV MPI

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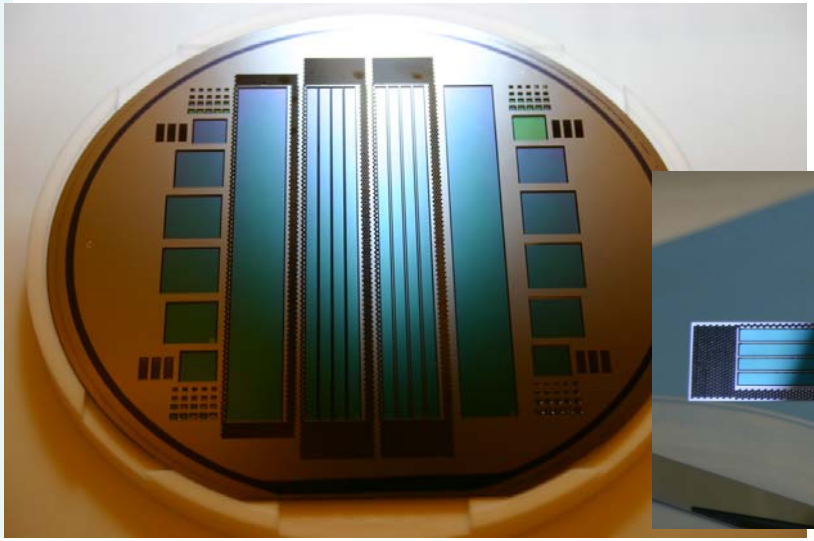
Thinning Technology

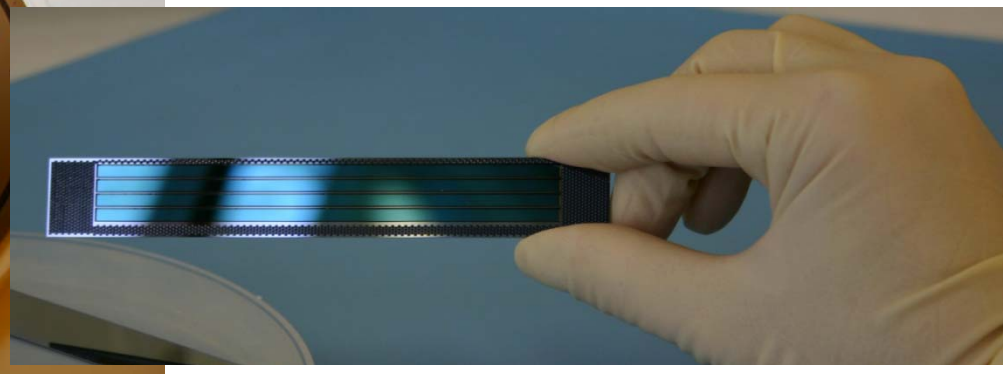
- **Sensor wafer: high resistivity d=150mm FZ wafer.**
- **Bonded on low resistivity "handle" wafer".**
- **(almost) any thickness possible**

Thin (50 μm) silicon successfully produced at MPI.

- MOS structures
- diodes

-No deterioration of detector properties, keep I_{leak} <100pA/cm²





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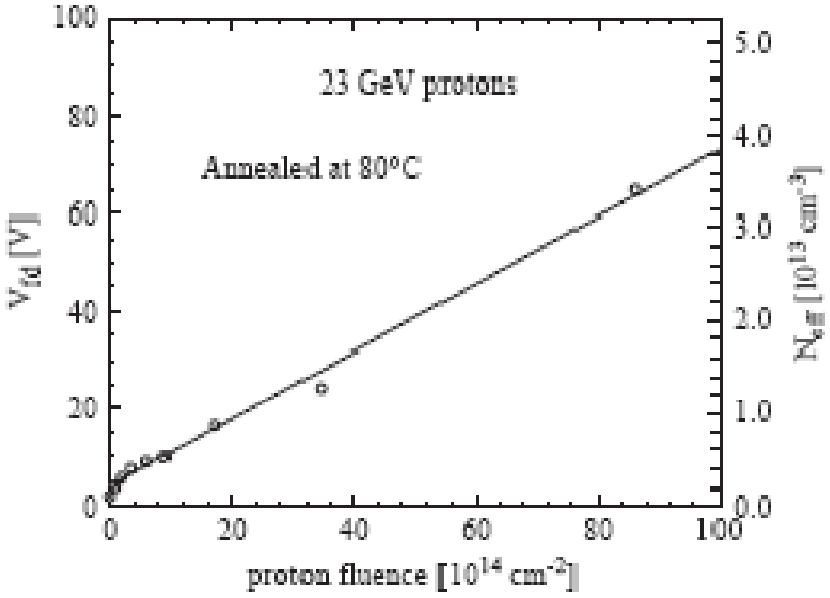
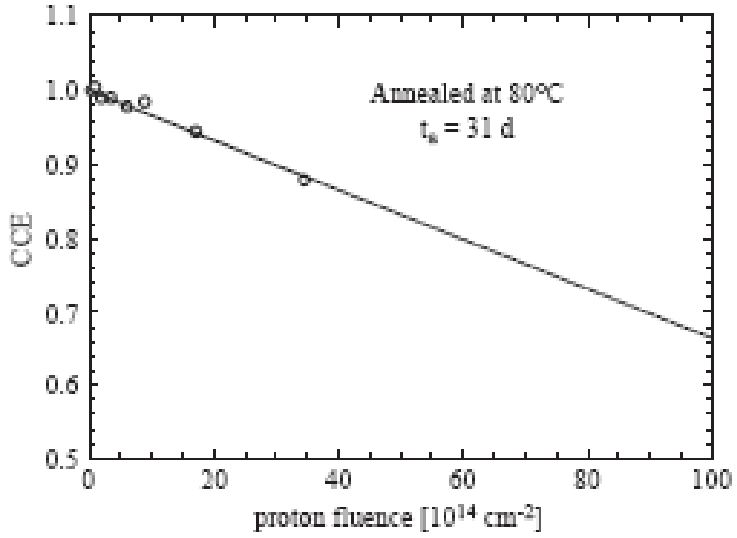
Measurements (V_{dep}, CCE)





Fretwurst et al. NIM A 552 (2005): After short term annealing:

V_{dep} < 100V at 10^{16} 1/cm^2.

However, detectors need to be kept cold (reverse annealing!).

Leakage currents:
α(80°C, 8min) = 2.4 x 10^{-17} A/cm.

CCE ~ 66% @ 10^{16} p/cm^2 (extrapolated).

Similar to results from epi-material (G.Kramberger):

3200e (62% average),
2400e (60% most prob).

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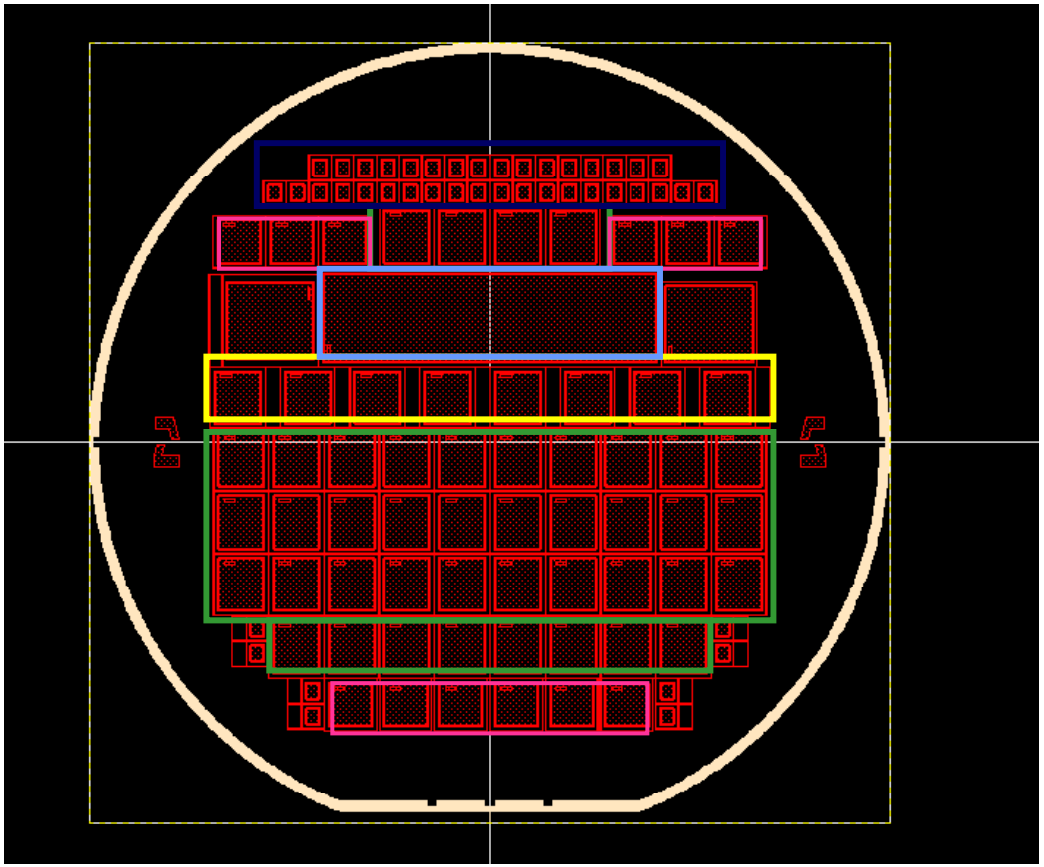
Status: Wafer Layout (6” SOI)



- 42 cells 10.5 x 11.9 mm^2
  10 different micro-strips versions + test-structures
- 12 diode cells
  10.0 x 10.0 mm^2
- 8 pixel cells – ATLAS geometry to be read out by a single FE chip – designed for SLID interconnection
- ATLAS module, to be connected to the FE with bump-bonding
- Pixel cells to be read out by a FE chip by INTERON (Norway)

Pixels follow ATLAS layout:, 160 x 18 pixel 50 x 400 μm^2 for FEI3 chip
10 x 10 pixel arrays with smaller pith (50x200, 100, 50) for special simple readout chip
Ministrips to be read by ALTAS SCT128 chip
Diodes

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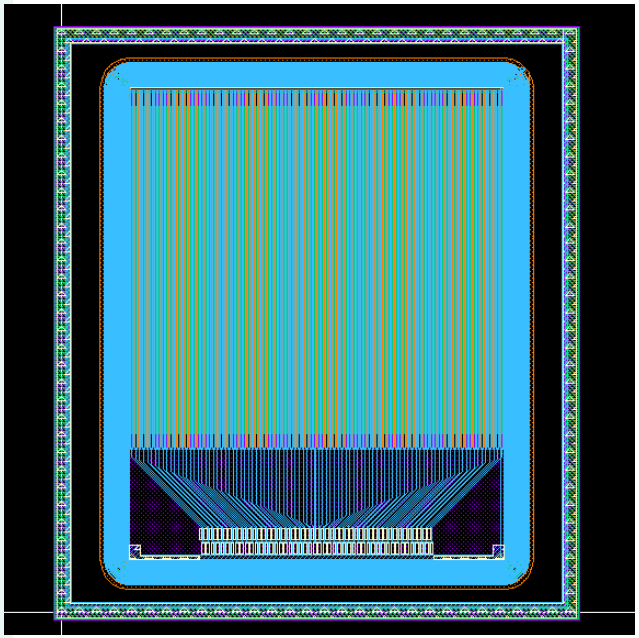
Layout of Microstrips

SOI & EPI: 4 copies/wafer

Strip pitch (μm)	n+ implantation width (μm)	p-spray moderation width (μm)
50	30	10
50	30	No
80	30	10
80	30	no

SOI: 3 copies/wafer

Strip pitch (μm)	n+ implantation width (μm)	p-spray moderation width (μm)
50	24	10
50	30	6
50	36	6
80	20	No
80	20	24
80	30	24

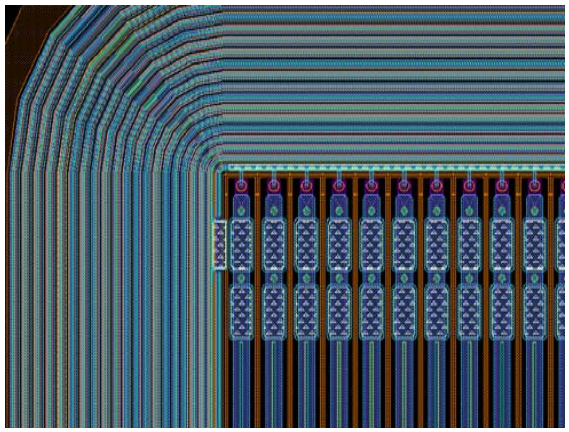


DC coupled

Punch through biasing for testing

96 strips (80 μm pitch)

L=7.5 mm



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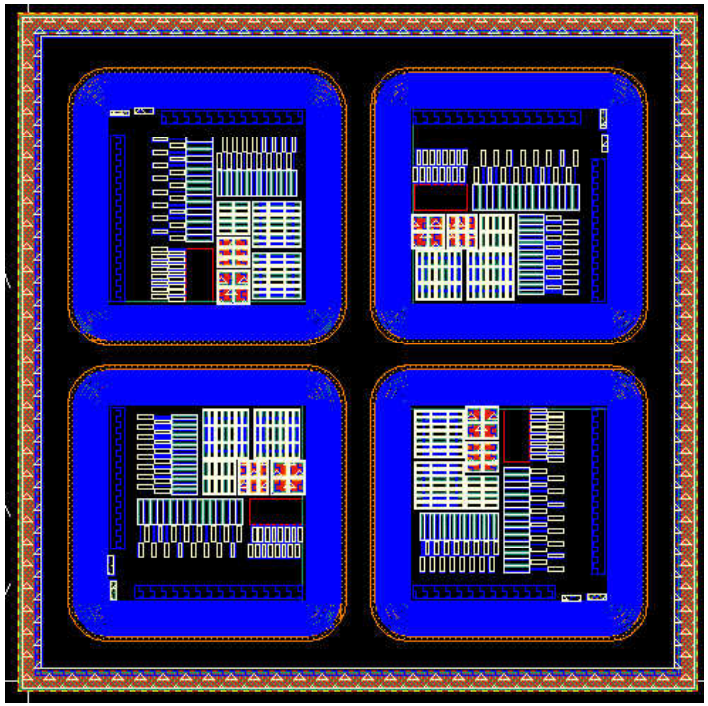
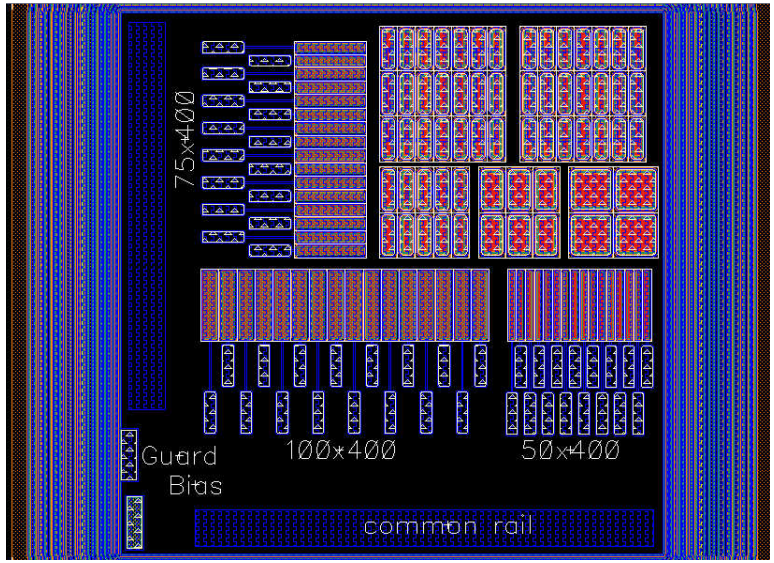
Layout of Test Diodes

16 Frames for diodes and simple structures

4 identical frames for “Ljubljana style” structures (with for variants each)

12 frames for “Hamburg style” diodes (propose 4 identical copies/wafer)





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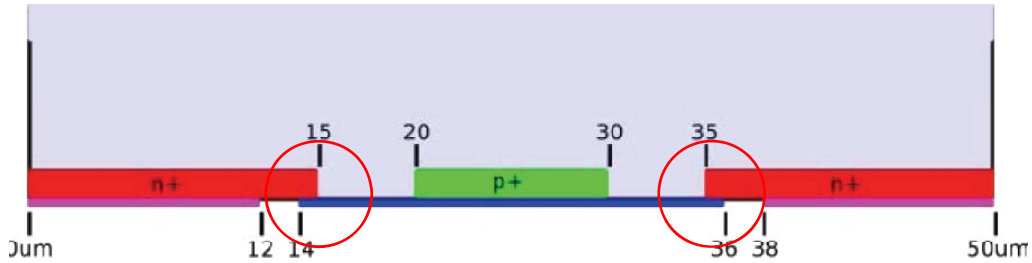
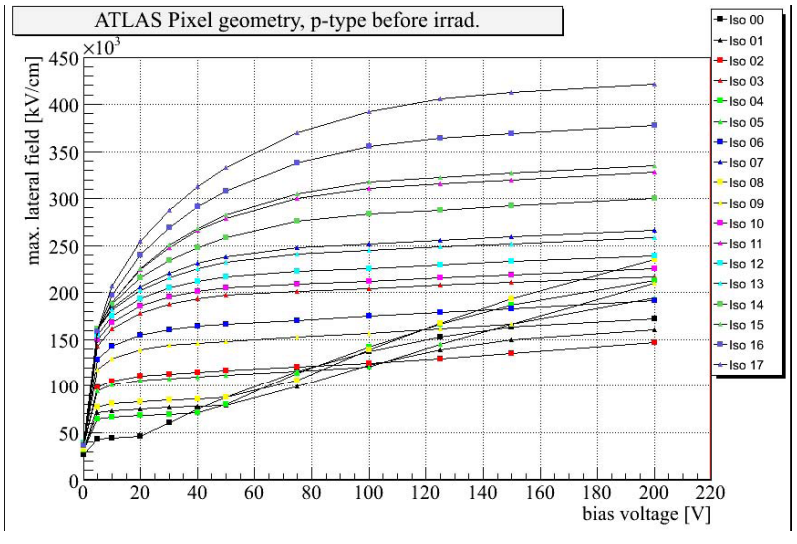
Simulations

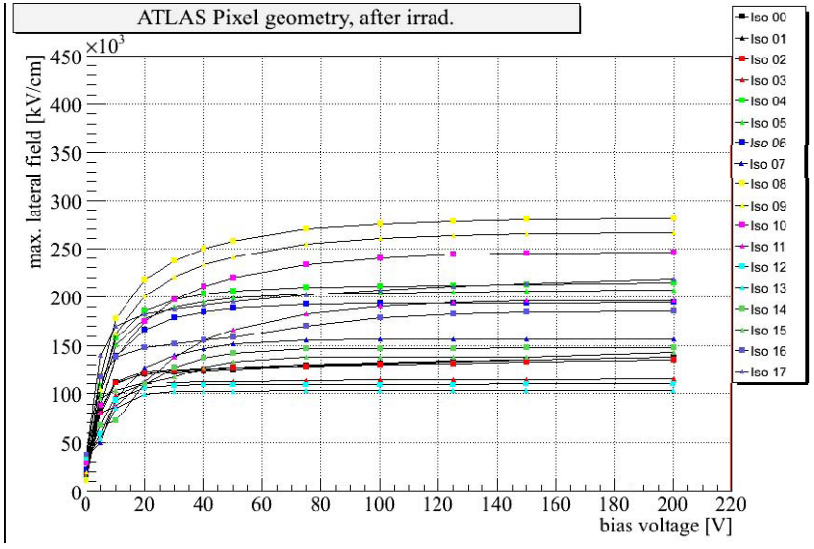
Simulation of electrical fields due to p-spray (M. Beimforte)



high fields at edges of n-implant
Depending on p-spray dose

p-substrate most critical before irradiation! -> chose two different p-spray doses





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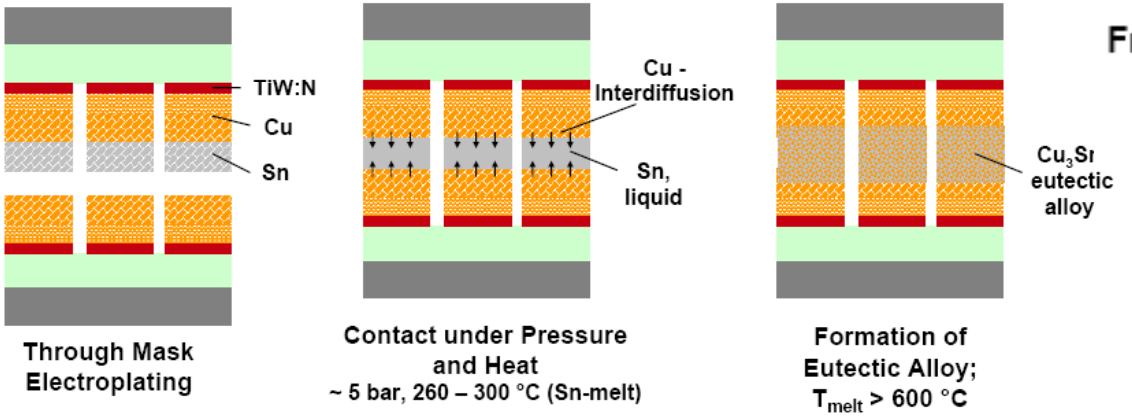
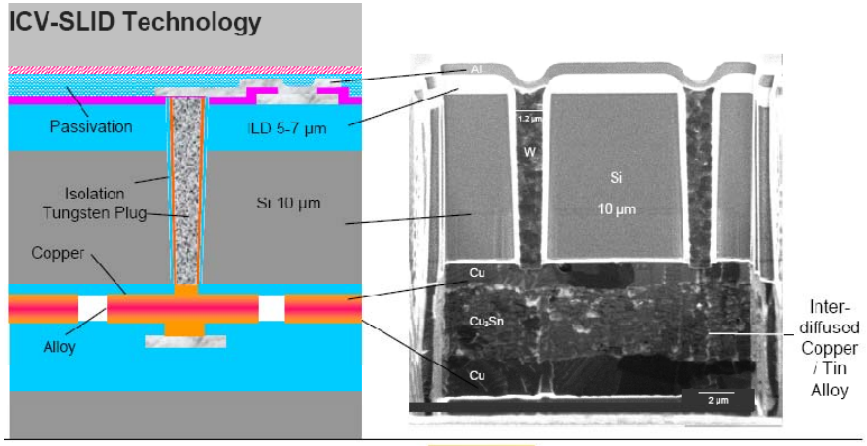
IZM SLID Process, ICV

Metallization SLID (Solid Liquid Interdiffusion)



Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

- Alternative to bump bonding (less process steps “low cost” (IZM)).
- Small pitch possible (< 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.



ICV = Inter Chip Vias

- Hole etching and chip thinning
- Via formation with W-plugs.
- Face to face or die up connections.
- 2.5 Ohm/per via (including SLID).
- No significant impact on chip performance (MOS transistors).