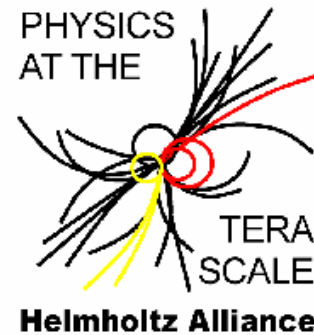


Trigger at SLHC



Stefan Tapprogge

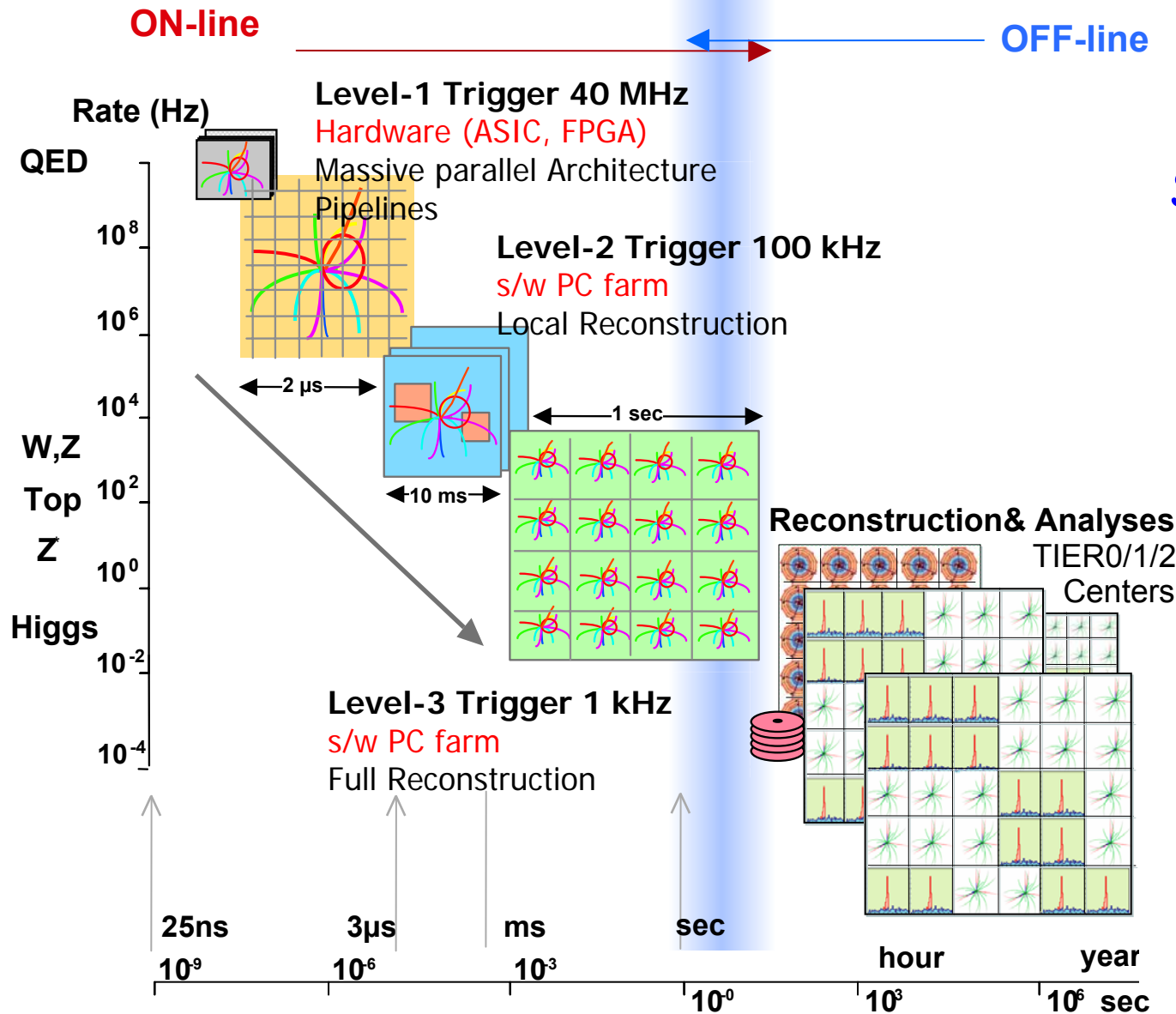
Institut für Physik

JOHANNES
GUTENBERG
UNIVERSITÄT
MAINZ

1st Detector Workshop
of the HGF Alliance
'Physics at the Terascale'

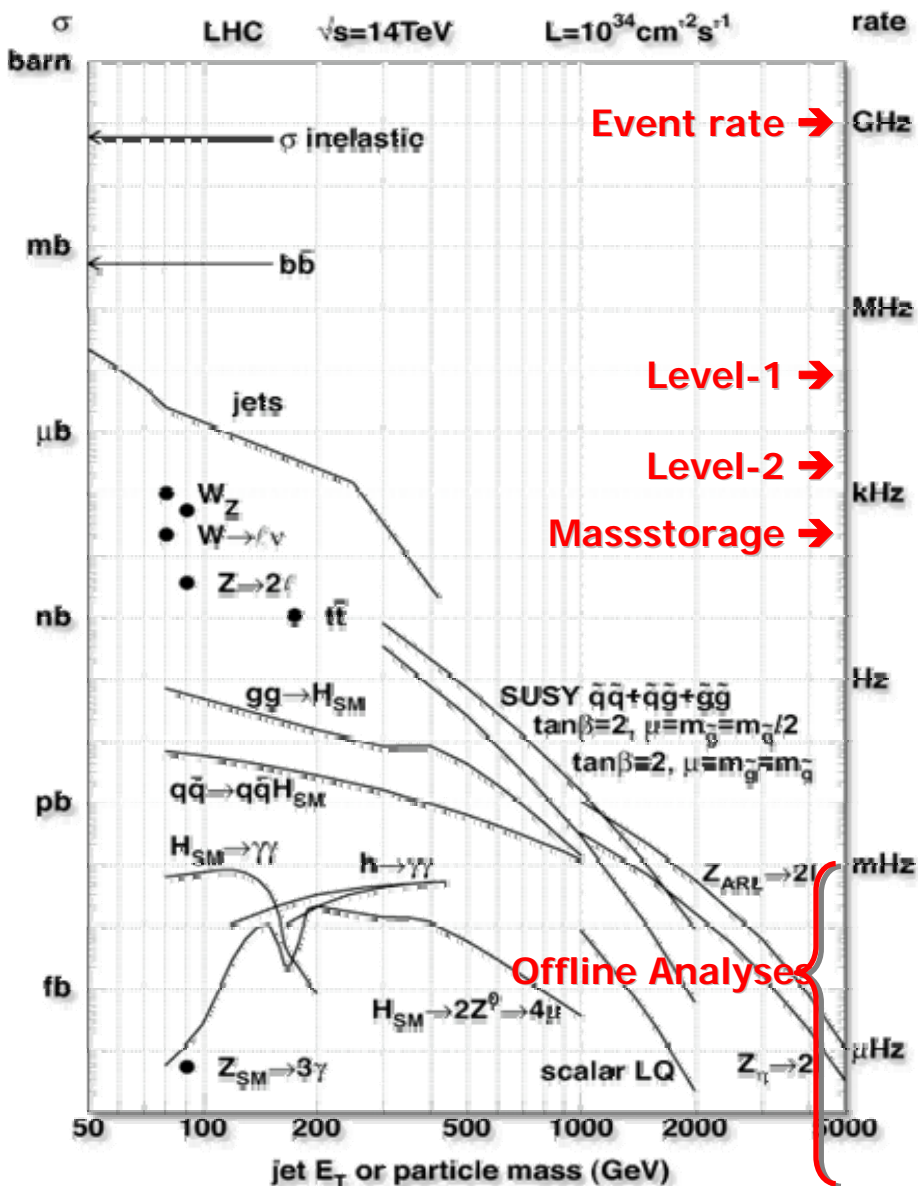
Karlsruhe

April 3rd, 2008



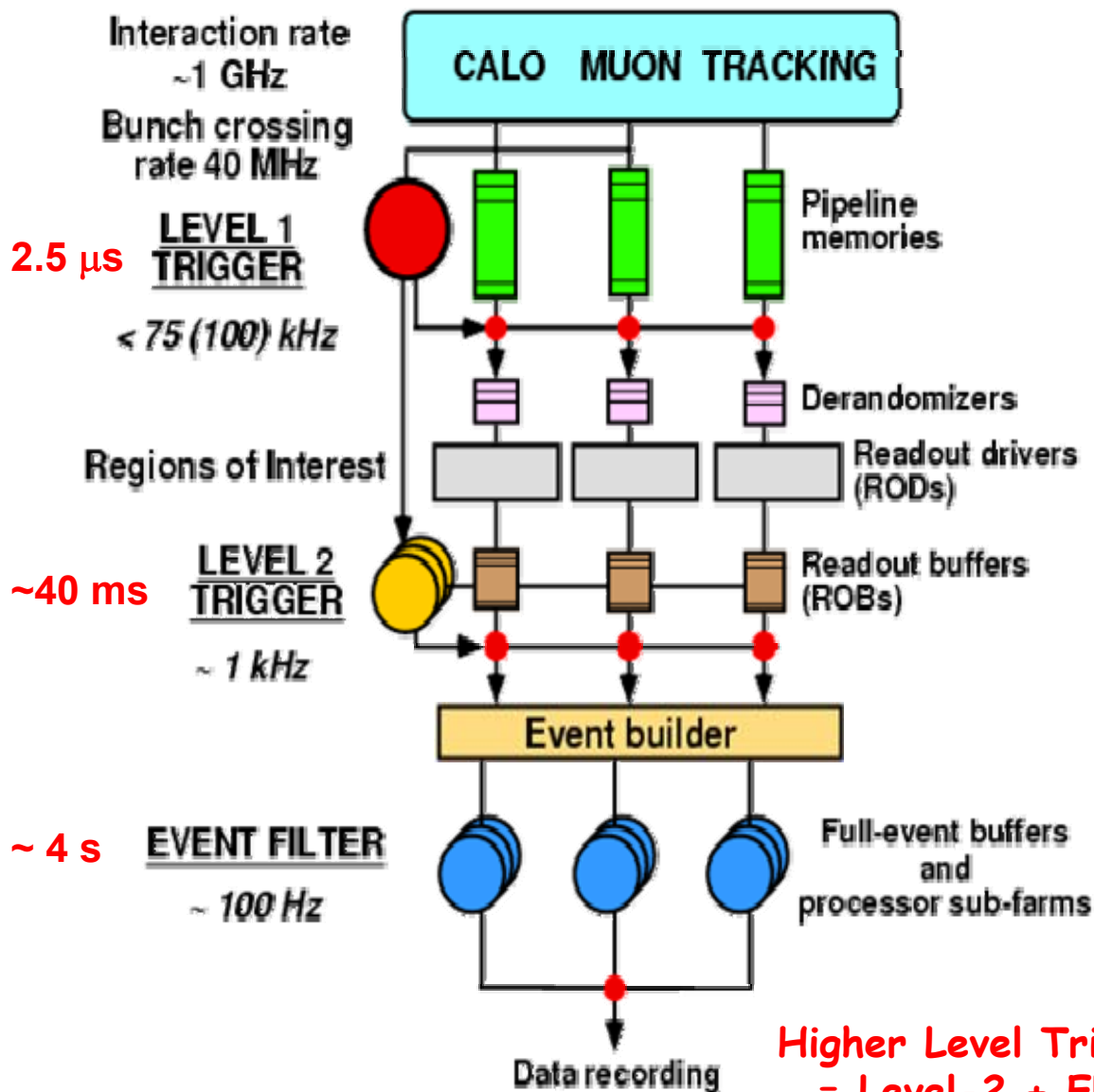
- LHC
 - challenges and trigger/DAQ architecture
- SLHC
 - physics requirements
 - challenges
- Trigger upgrade for SLHC
 - ATLAS Level-1 calorimeter trigger
 - CMS Level-1 track trigger
- Summary

LHC: the challenge(s)



- extremely high interaction rates
 - mostly uninteresting background
- many physics processes of interest happen only rarely
 - very efficient selection needed
- complex detectors
 - 10^8 electronic channels
- many simultaneous pp interactions
 - at design luminosity
- constraints from available latency, computing resources, network bandwidth, ...
- solution
 - multi-level trigger systems

ATLAS trigger & DAQ architecture



• Level-1

- coarse calorimeter data and muon trigger chambers
- buffering on detector

• Level-2

- Region-of-Interest data ($\sim 2\%$ only)
- full granularity
- all detectors
- fast rejection
- buffering in ROBs

• EF (Event Filter)

- refines selection
- latest calibration, alignment

SLHC physics requirements

- to exploit physics potential of SLHC, need
 - triggers for discovery physics
 - (very) high p_T objects (thresholds increased wrt LHC)
 - as inclusive as possible (also inclusive W/Z selection ?)
 - triggers for precision measurements
 - high p_T objects (with similar thresholds as for LHC)
 - use more exclusive / multi-object selection to control rate
 - monitor and calibration triggers
 - low to high p_T thresholds (will be pre-scaled)
- conditions at $10^{35} \text{ cm}^{-2}\text{s}^{-1}$ will impact trigger rates
 - higher rate for fixed threshold and efficiency
 - trivial increase by corresponding increase in luminosity
 - further increase due to less effective isolation criteria, increase in fake rate, ...
 - up to 400 inelastic pp interactions per crossing (on average)

TDAQ upgrade parameter space

- upgrades of the trigger and DAQ system are influenced (driven) by several constraints and requirements, from
 - physics goals
 - objects, algorithms, p_T thresholds, ...
 - machine parameters
 - bunch crossing frequency,
of simultaneous inelastic pp interactions, ...
 - sub-detector changes
 - number of channels, occupancy,
signal formats for LVL1 (analog vs. digital), ...
 - technology evolution
 - availability of performing commodity items, ...

Upgrade plans/ideas

- CMS

- increase Level-1 latency to $6.4 \mu\text{s}$
- muon and calorimeter trigger at Level-1 with finer granularity
- introduce Level-1 track trigger (see later)
- regional correlation at Level-1 with track, muon and calo trigger information (before global trigger)

- ATLAS

- discussion on new concepts have started
 - example Level-1 calorimeter trigger (see later)
- need/use of Level-1 track trigger to be determined

- boundary Level-1 to Higher Level trigger likely to be kept

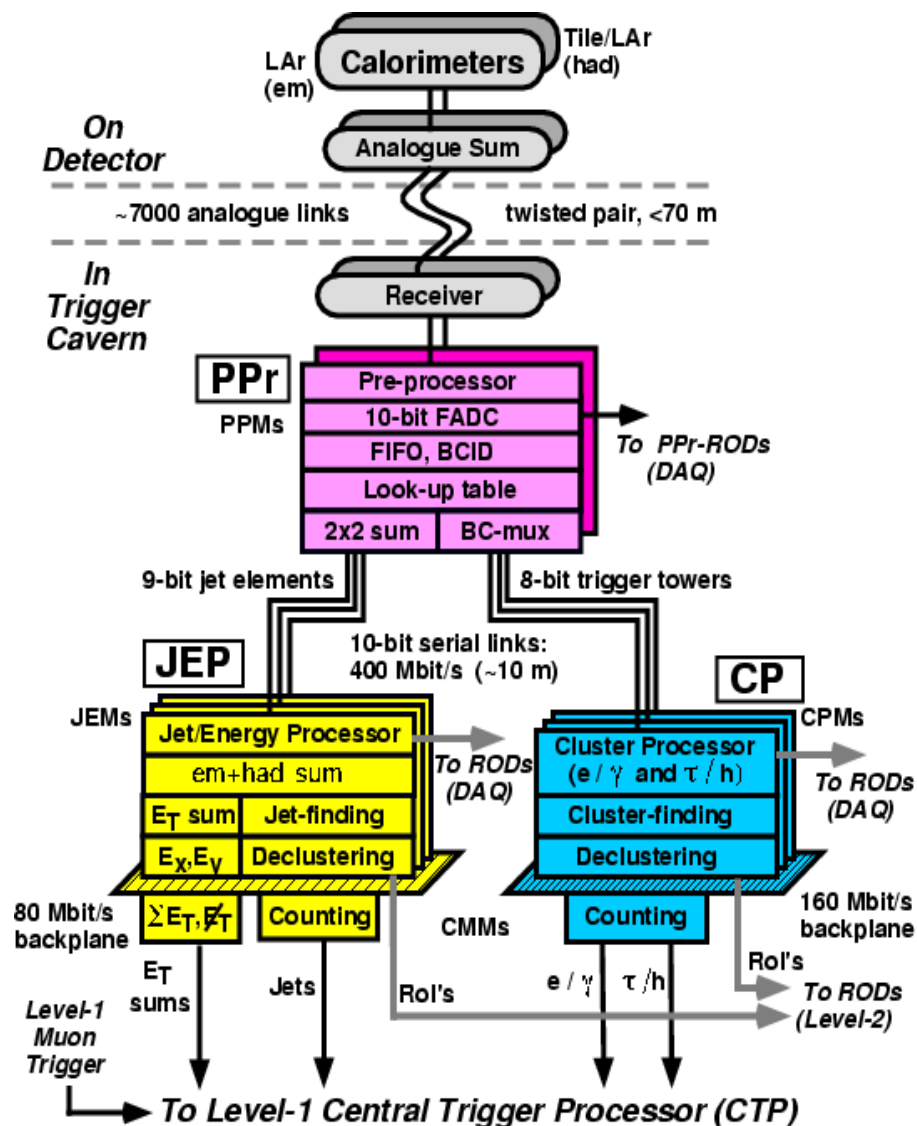
- no change in Level-1 accept rate

- mostly focusing on Level-1 issues right now

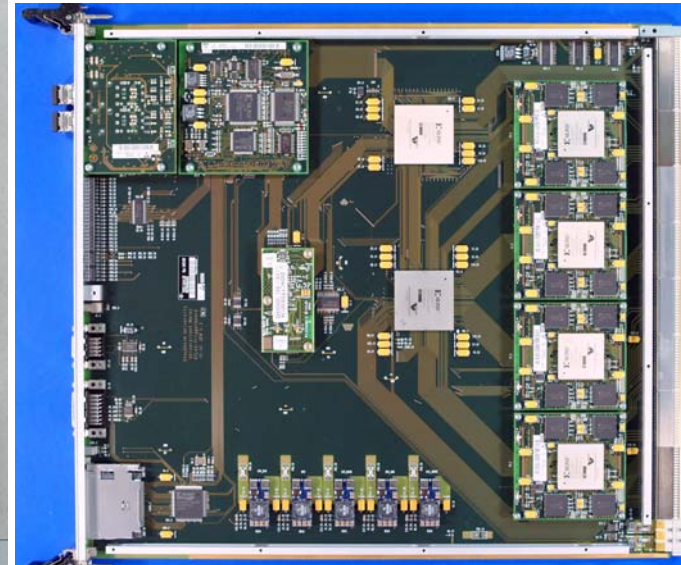
- DAQ and Higher Level trigger to profit from technology advancements (bandwidth/processing demands will increase)

ATLAS LVL1 calorimeter trigger

- analogue electronics on detector sums signals \rightarrow trigger towers
- signals received and digitised
 - \rightarrow digital data measure E_T per tower for each BC
 - E_T matrix for ECAL and HCAL
- tower data transmitted to processors (4+2 crates in total)
 - \rightarrow fan out values needed in more than one crate
 - Motivation for very compact design of processor
- within crates, values need to be fanned out between electronic modules, and between processing elements on the modules
- Connectivity and data-movement issues drive the design



ATLAS calorimeter trigger: installed



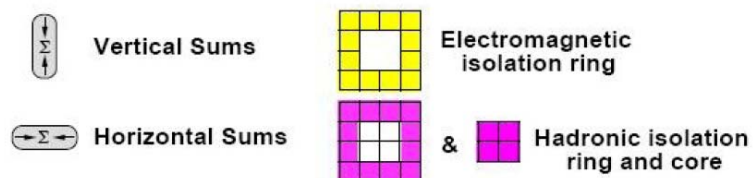
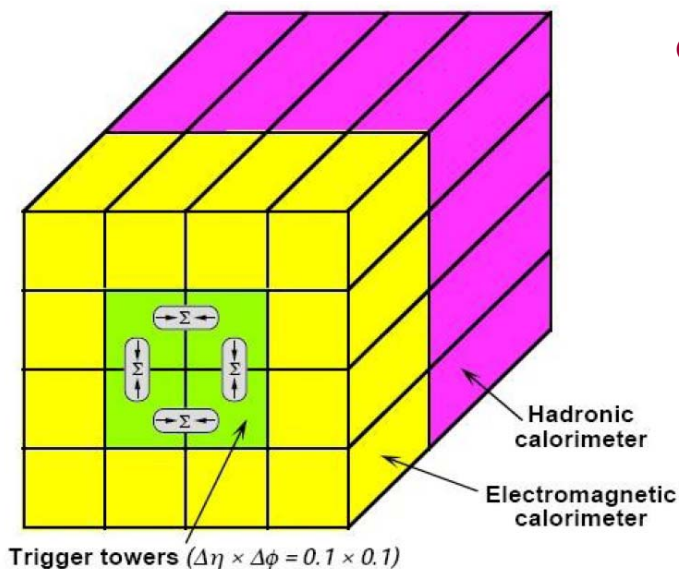
- limitations on input/output
 - stability and reliability of cable plants
- first stage (preprocessor)
 - mixed signal design
- data duplication in processor systems
 - backplane limitations

ATLAS Level-1 calorimeter trigger

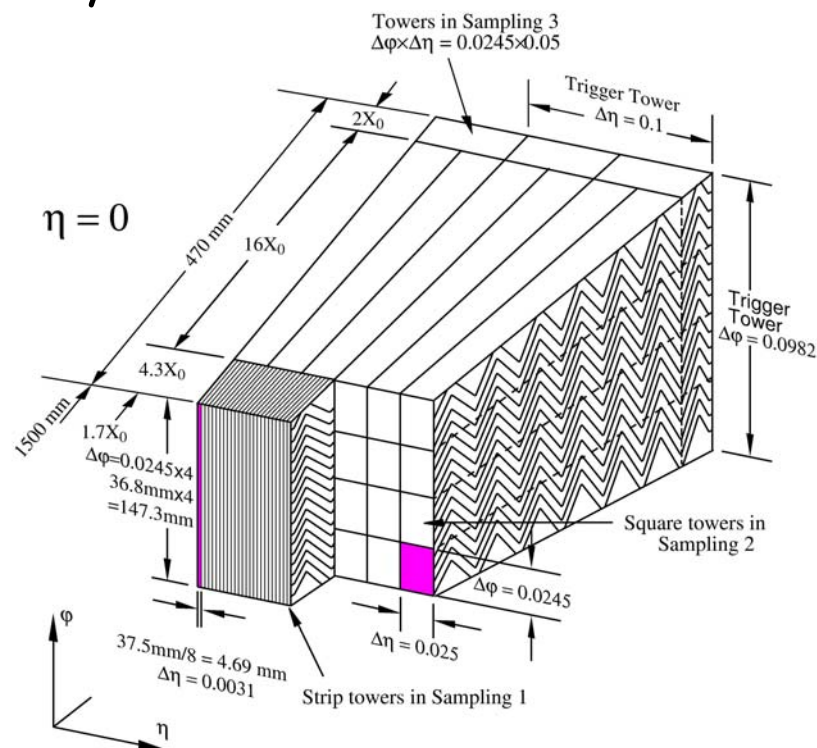
- present areas for initial upgrade studies
 - brainstorming meeting Jan. 2008 in Heidelberg
 - critical assessment of present system (lessons learnt)
 - to be continued during first data taking
 - granularity of input data
 - relation to upgrades of calorimeter f/e electronics
 - improvement of trigger algorithms
 - transfer part of Higher Level rejection to Level-1
 - architecture studies
 - possibilities to reduce/avoid data duplication (backplanes)
 - prototype/emulation board development
 - firmware development for algorithms
 - assessment of multi-Gbit link technologies
 - timing distribution
 - TTC inadequate for multi-Gbit links

Calorimeter trigger algorithm

- much finer granularity of cells in liquid argon calorimeter
 - additional rejection power (Higher Level trigger with calorimeter only)
 - investigate possibilities of using finer granularity for Level-1



- example: EM trigger
 - select e/γ at Level-1
 - narrow shower shape
 - no longitudinal leakage
 - transverse isolation
 - input: 'trigger towers'
 - summed energies of ≤ 60 cells



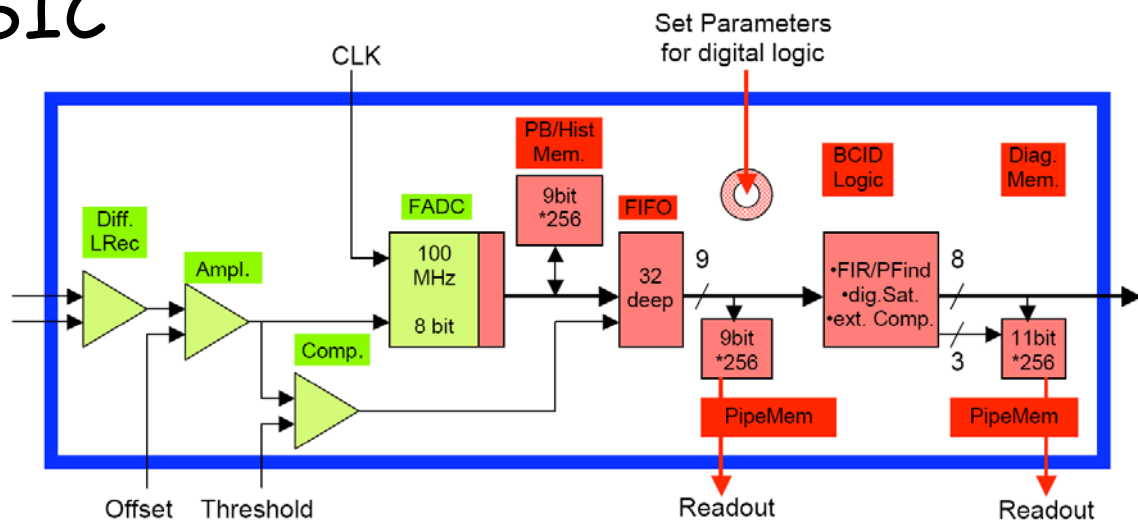
Calorimeter trigger upgrade: plans

• Heidelberg

→ integrate pre-processor functionality into higher density

→ mixed signal ASIC

- analog signal conditioning
- digitisation (FADC)
- bunch crossing identification



→ implement prototype channel in MPW-run

- 180 nm UMC process

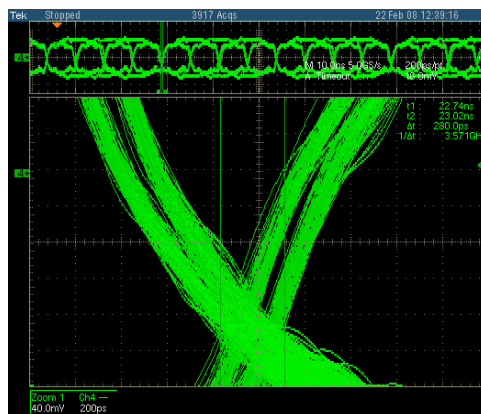
Calorimeter trigger upgrade: plans

• Mainz

→ investigate clock jitter / data integrity of high speed data links

→ using Xilinx demonstrator boards

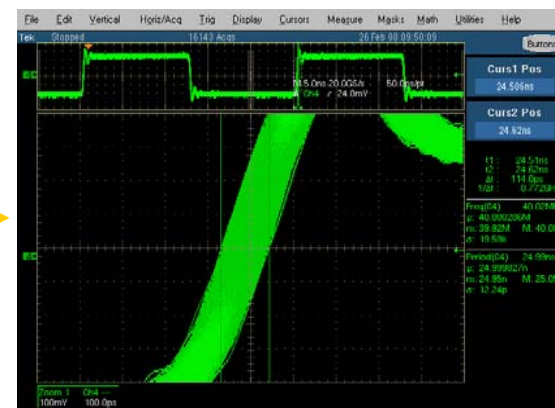
- develop jitter cleaner card
- synchronous vs. asynchronous transmission



$\Delta t \sim 300$ ps



Clock
recovery



$\Delta t \sim 120$ ps

→ develop demonstrator board for jet-energy sum-processor

- firmware developments for signal deserialisation and algorithmic processing in single FPGA
 - spread over several parts presently
- integrate into present system for detailed tests

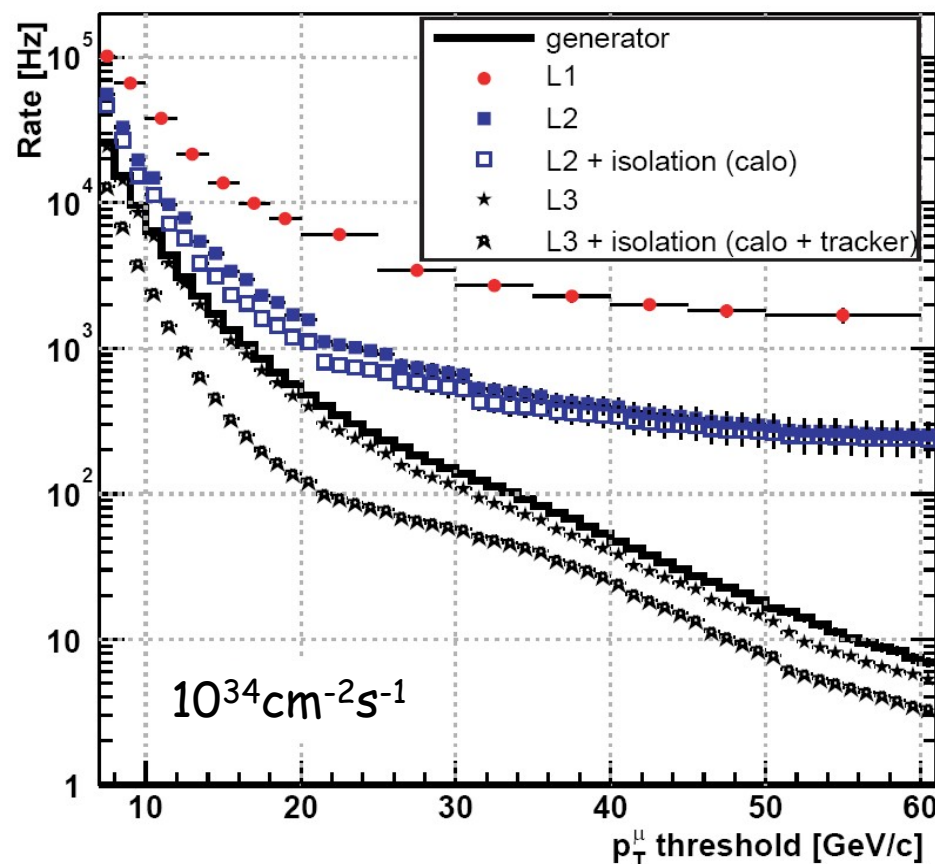
CMS: track trigger at Level-1

• motivation

- need to sufficiently reduce trigger rates at SLHC
- allow for increased algorithm complexity

• examples

- improve muon momentum measurement
- increase rejection of fake e/γ objects
- refine isolation criteria (track based)
- disentangle different primary vertex contributions

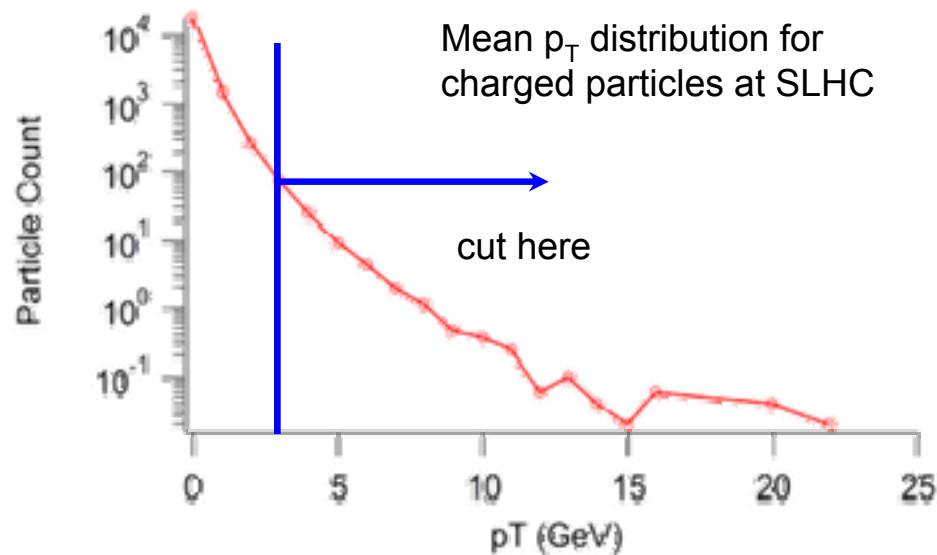


• muon trigger rate

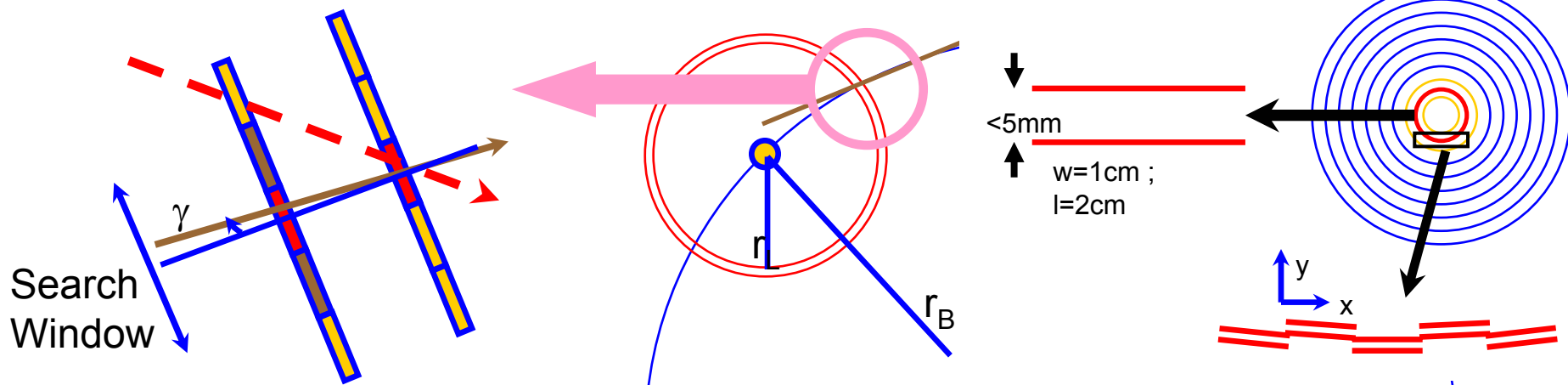
- limited rejection power at high p_T

CMS: trigger capable tracker modules

- Use close spaced stacked pixel layers
- Geometrical p_T cut on data (e.g. $\sim \text{GeV}$):
- Angle (γ) of track bisecting sensor layers defines p_T (\Rightarrow window)
- For a stacked system (sepn. $\sim 1\text{mm}$), this is ~ 1 pixel
- Use simple coincidence in stacked sensor pair to find tracklets

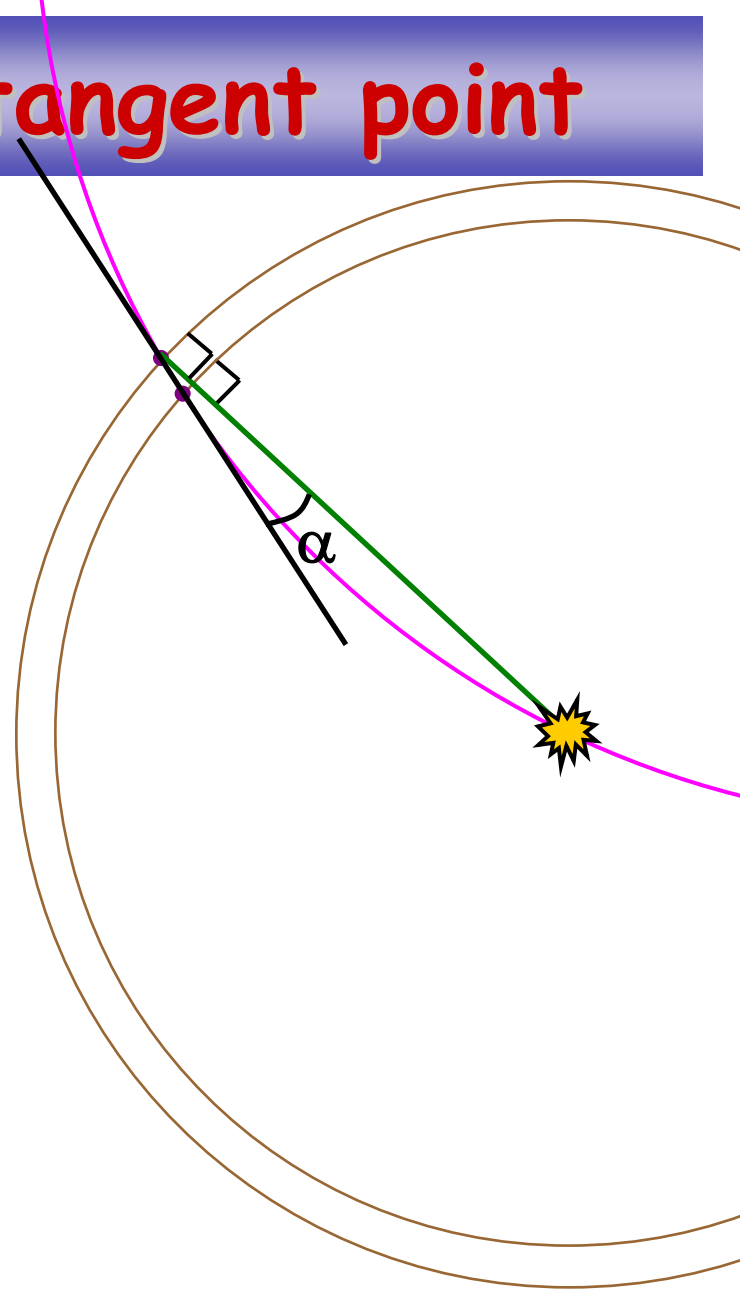


A track like this wouldn't trigger:

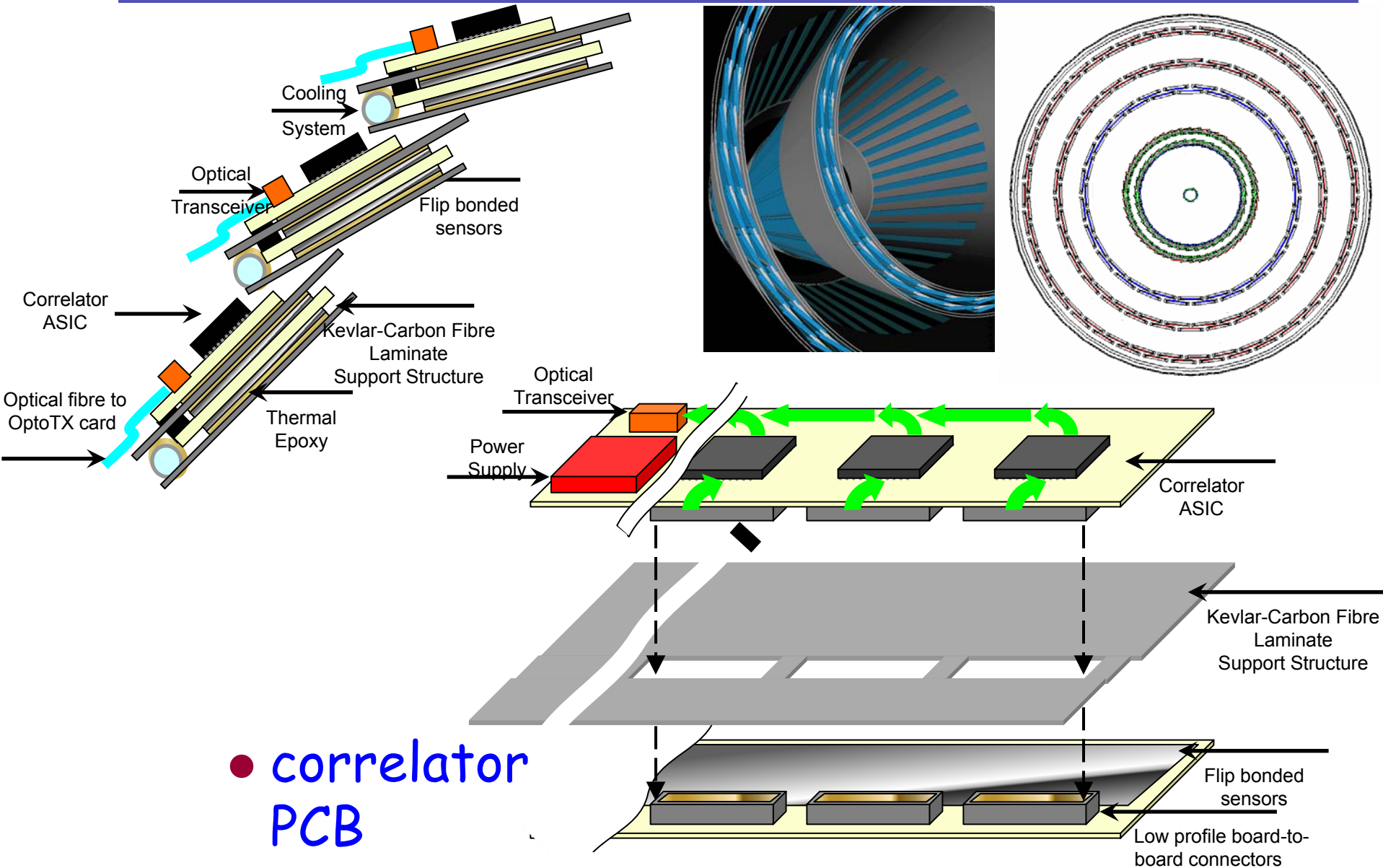


Reconstruction of tangent point

- assume IP $r=0$
- angle α determines p_T of track
- smaller α = greater p_T
 - can find high- p_T tracks by looking for small angular separation of hits in the two layers
 - correlation is fairly 'pure' provided separation is small and pixel pitch is small
- matching hits tend to be from the same track
 - if sensors are precisely aligned, column number for hit pixels in each layer can be compared
 - finding high- p_T tracks becomes a relatively simple difference analysis



CMS: conceptual design



Summary

- trigger upgrade for SLHC depends on
 - physics requirements (not yet really known)
 - machine parameters (might change again)
 - detector upgrades
- challenges at SLHC might/will be even larger than the ones for LHC
 - triggering will be a really tough job
- present activities with HGF alliance
 - Heidelberg and Mainz on Level-1 calo trigger