Pixel high rate test pulses

Daniel Pitzl, Simon Spannagel, DESY

Hamburg CMS Pixel Upgrade meeting, 22.2.2013

- update from 16.11.2012
- new test board firmware from Beat Meier PSI:
  - more efficient packing of digital ROC data:
    12 bits into one word (2 bytes)
  - extended 'event FIFO': 128 words

Data Rate Estimations

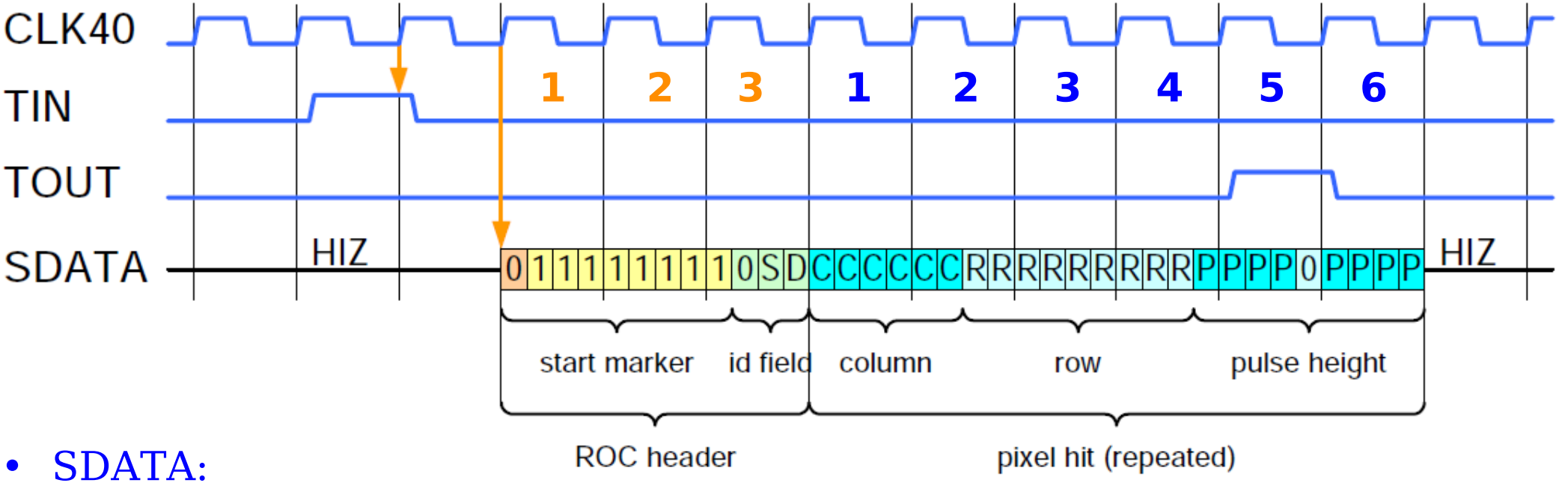
- Simulation with Pythia Z2 tune and GEANT4
- Assuming 24 bits per hit, 100 kHz level 1 trigger rate
- Peak luminosity = $2x10^{34}cm^{-2}s^{-1}$, σ_{tot}=80mb, σ_{signal}=1.5mb, 25 ns BC

Layer	1 @ 2.9cm		2	3	4
Pixel fluence [MHz/cm^2]	520		119	52	27
Hits / trigger / module	190		40	18	8.4
MBit/link/sec	435		118	66	45

1 ROC = 0.65 cm^2

Hans-Christian Kästli,
CMS Upgrade plenary,
20.7.2011

digital ROC data format



- SDATA:
  - 4 bits per 40 MHz clock cycle = 160 Mbit/s
  - ROC header: 12 bits
  - pixel hit: 24 bits

maximum: 6.6 Mpx/s readout from one ROC

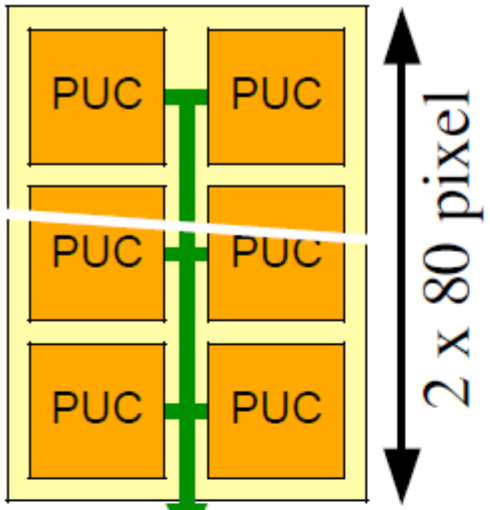
- FPGA version atb5:
  - 12 bits stored per data word (2 bytes)
  - deeper 'event FIFO'

- max read out: 6.6 Mpx/s/ROC

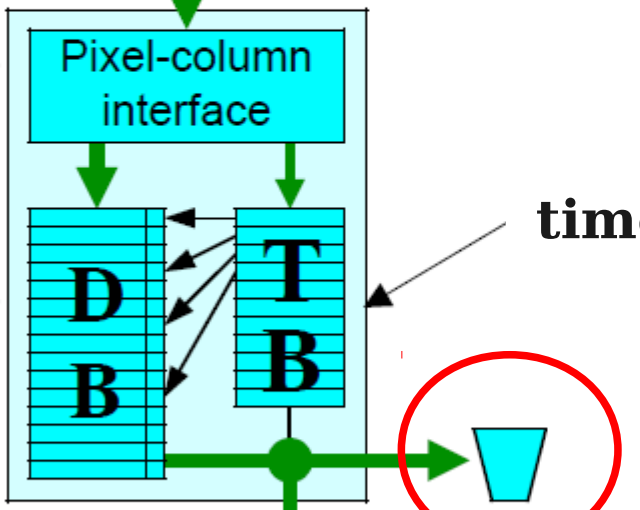
where does the rest go?

- to garbage!
- CMS trigger rate is 100 kHz max:
  - on average 10 µs between triggers
- ROC data buffer expires after ~135 bunch crossings (3.4 µs trigger latency = WBC)
  - 99.5% pixel hits are never readout

double column readout



X-rays produce mostly 1-pixel clusters: time buffer limit is reached first.

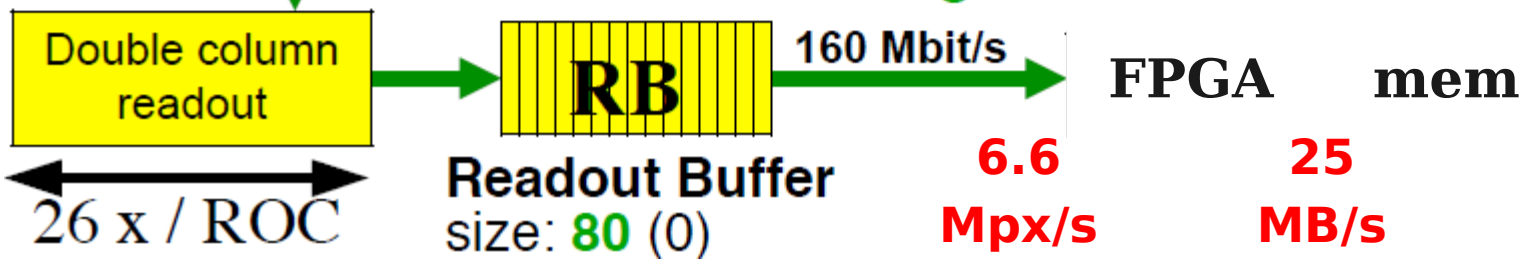


data buffer: 32 → 80

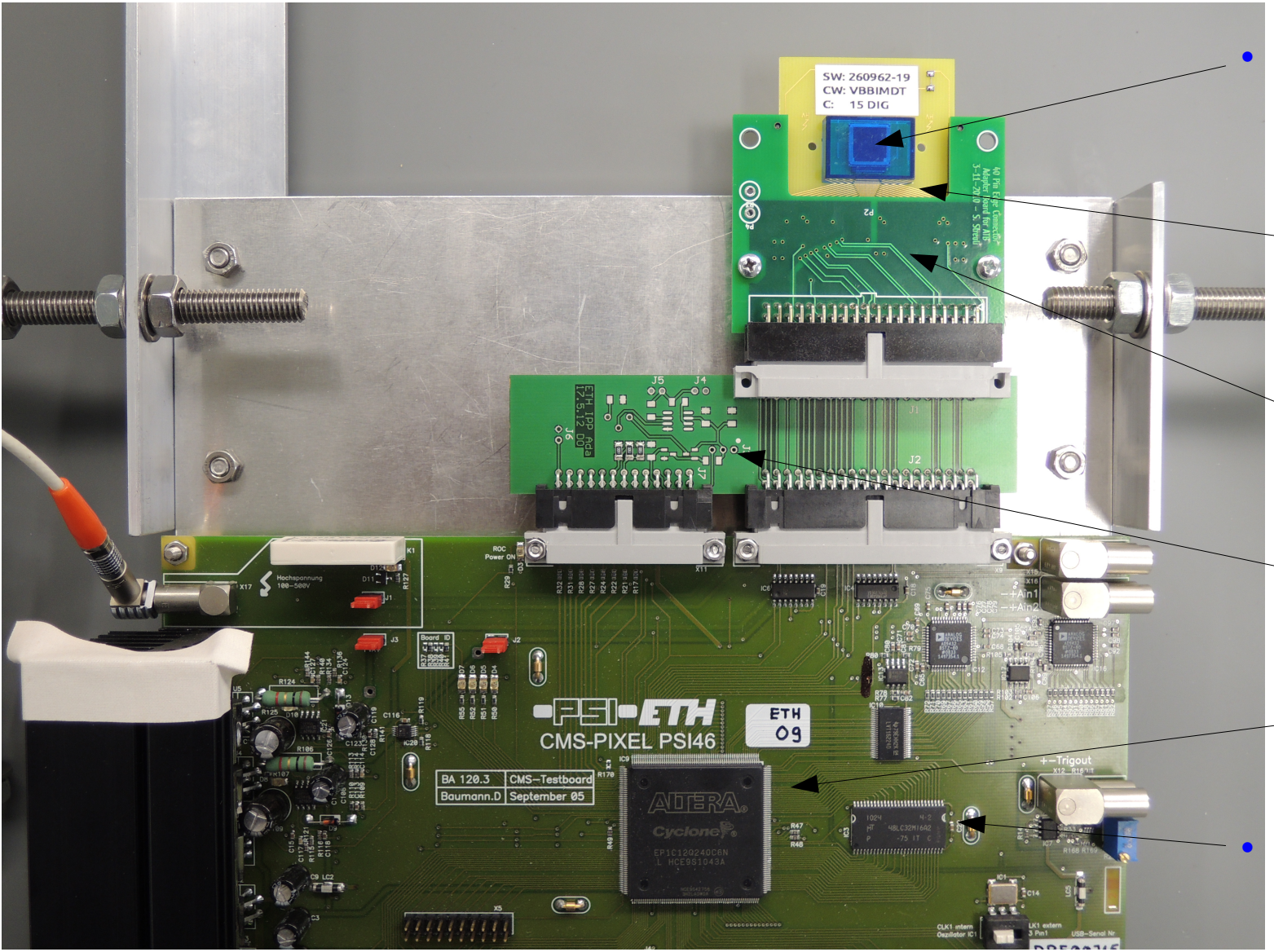
auto clear when full

time stamp buffer: 12 → 24

readout buffer: new



psi46 test board with digital ROC



- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
  - ETH adapter card for digital 160 MHz differential signal directly into FPGA (LCDS into LVDS)
- 64 MB memory

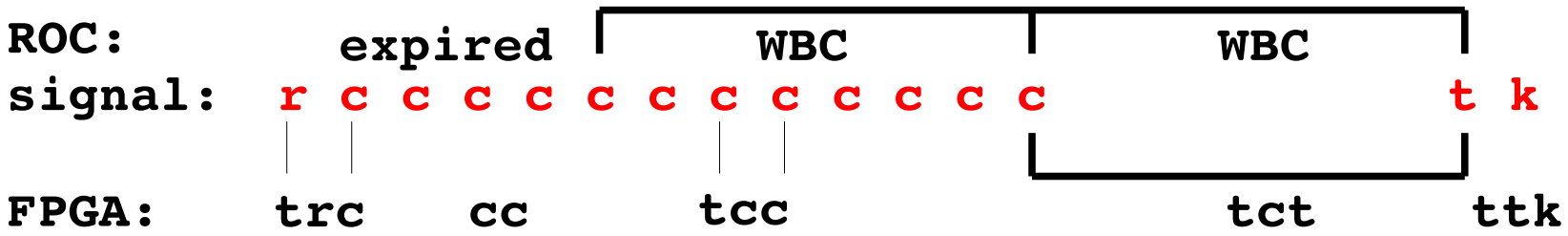
test board signals and steering

signal sequence from FPGA to ROC:

reset *n*×calibrate trigger token = r c(ccc) t k

tbParameters.dat:

trc	18	time between reset and cal [BC]
cc	20	calibrate counter *n*
tcc	38	time between calibrates [BC]
tct	167	time between calibrates and trigger
		WBC = tct – 5 = 162
ttk	18	time between trigger and readout token [BC]
trep	12	time between triggers [many BC]



High rate ROC test

pixels read out:

$$f_{read} = f_{trig}\ n_{pix/DC}\ n_{DC}$$

pixels active:

$$f_{act} = f_{trig}\ n_{cal}\ n_{pix/DC}\ n_{DC} = n_{cal}\ f_{read}$$

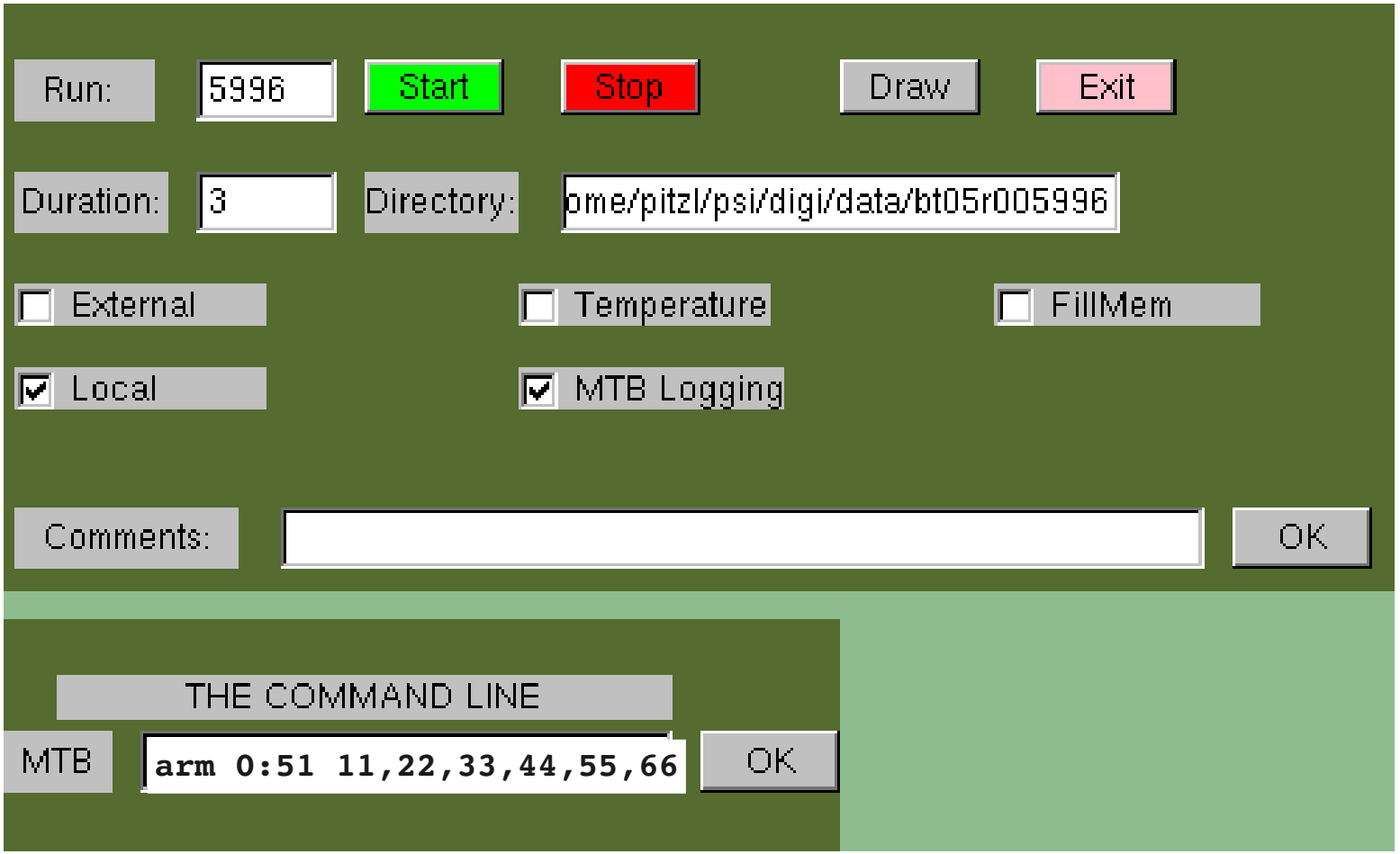
limit:

f_{read} **: write < 25 MB/s into memory, < 6.6 Mpx/s ROC rate**

reached:

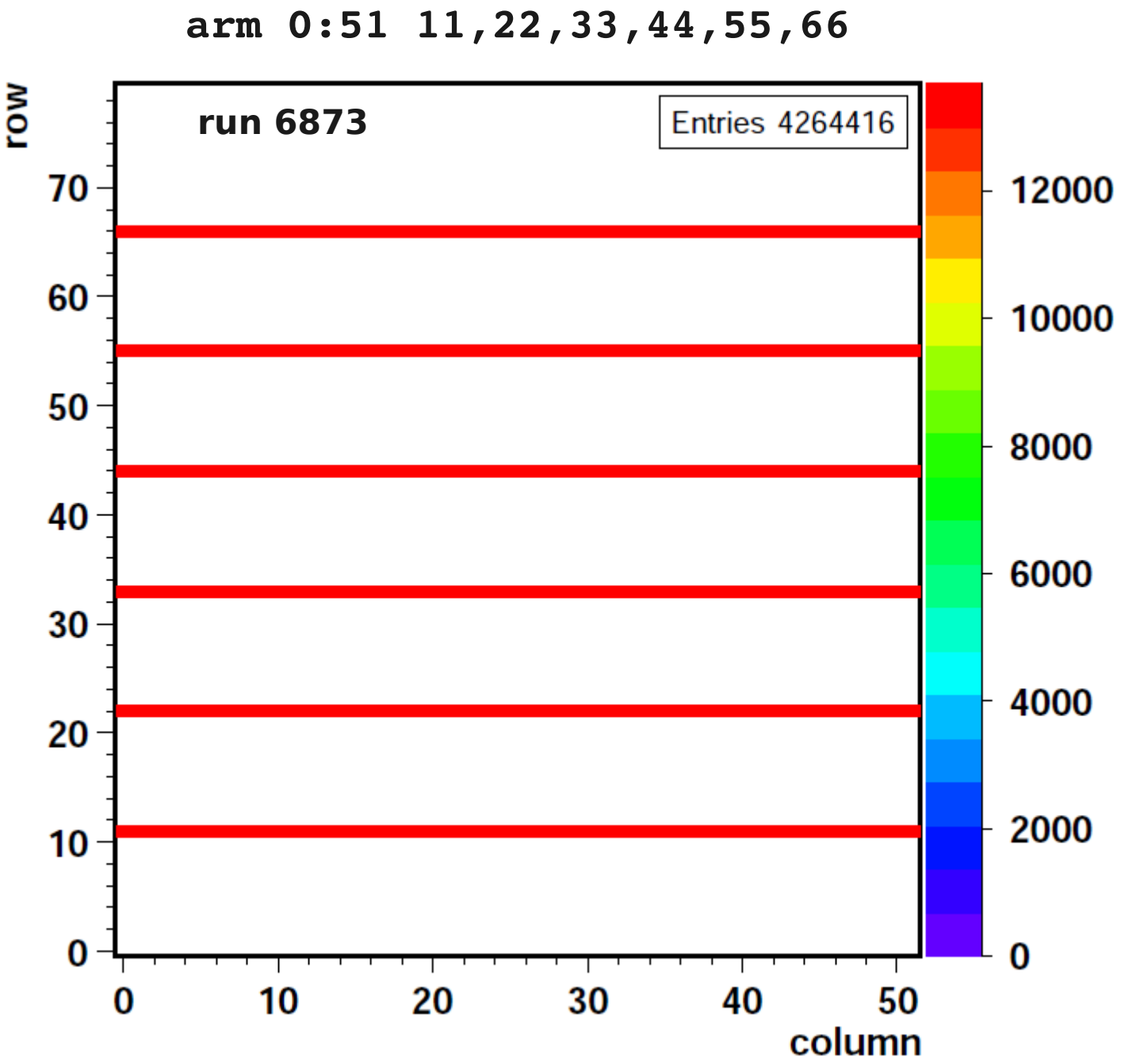
$n_{cal} = 20,\ f_{read} = 4$ Mpx/s => $f_{act} = 80$ Mpx/s/ROC

takeData with test pulses



activate test pulse for columns 0..51 in 6 rows

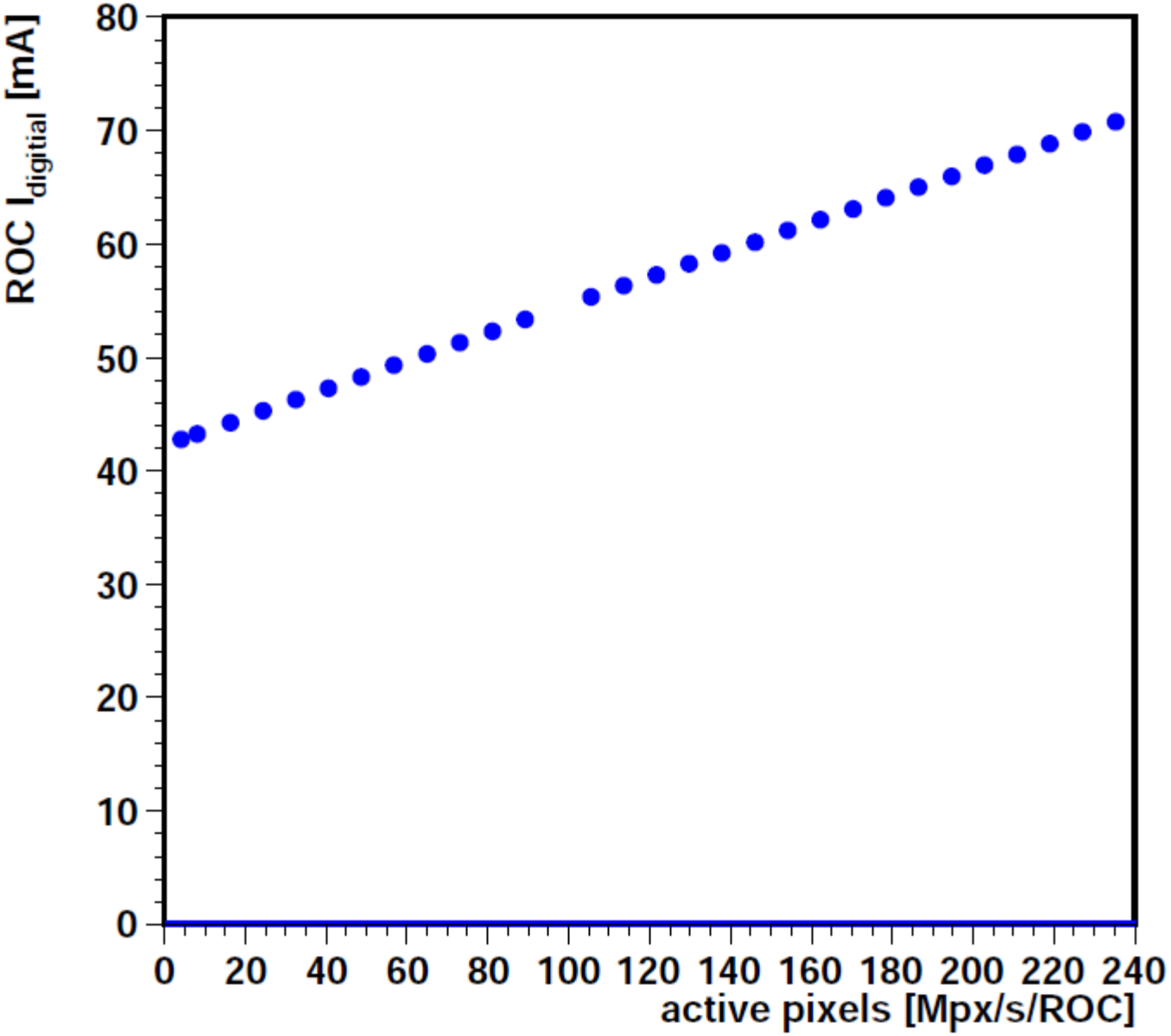
high rate test



- 312 pixels pulsed
- 13 kHz trigger rate (`trep 12`):
  - 4 Mpx/s read out
  - 19.6 MB/s
- 20 calibrate pulses:
  - **81 Mpx/s active.**
- 100% efficiency
- no data errors

ROC digital current vs activity

arm 0:51 11,22,33,44,55,66



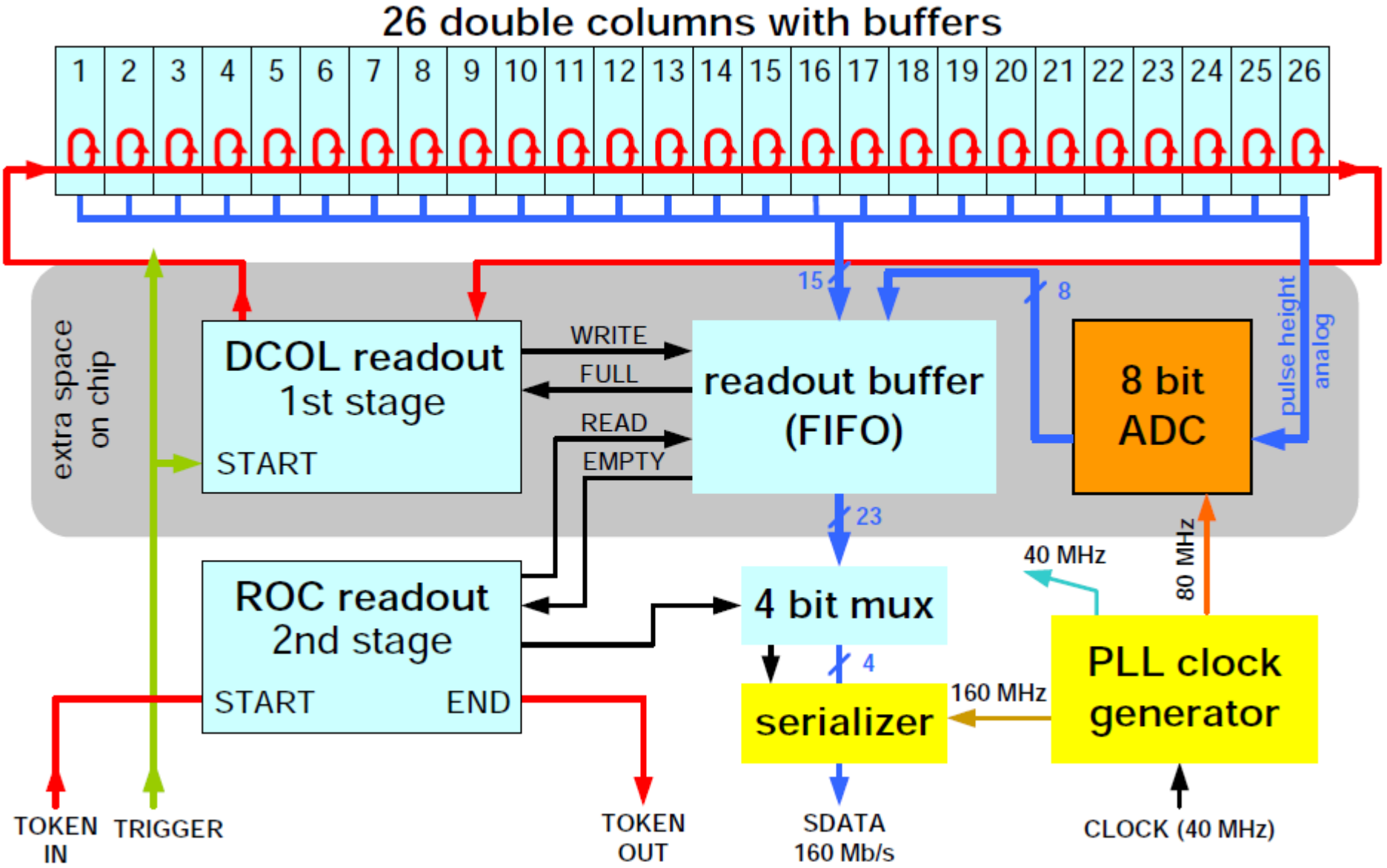
- 312 pixels pulsed
- 13 kHz readout
- vary number of calibrates: 1..60
- measure ROC digital current by DVM
- current increases linearly with ROC activity:
  - 1 mA / 8 Mpx/s

Summary and outlook

- New test board firmware allows to read out at higher rate:
  - ROC readout up to Mpx/s (24 bits/pixel at 160 MHz):
- Higher pixel activity generated by multiple calibrates:
  - reached 81 Mpx/s/ROC
  - corresponds to 125 Mpx/s/cm^2.
  - error-free readout
  - digital current increases linearly up to 250 Mpx/s/ROC
- Test board firm ware still has limitations:
  - higher trigger rate and/or more calibrates don't work
- next:
  - test irradiated ROCs

Back up

psi46dig periphery



digital ROC data format