

On-the-Fly Record of the Telescope “Gemba” Meeting

Takeo Higuchi
(Kavli IPMU, the University of Tokyo)

[01-a] C.Marinas

- **EUDET and MIMOSA will be covered in the meeting.**

[02-a] C.Niebuhr

- **Thermal mockup is assembled; waiting for MARCO.**
- **Magnetic field $B=1.2\text{T}$ at maximum.**
- **A MARCO pump (one of the CO₂ cooling system components) encountered some kind of faults.**
 - **MARCO should not to be used with the present pump.**
 - **Two new pumps are to be purchased.**

[02-b] C.Niebuhr

- The support structure *can* be designed to make the final fine tunings of sensor positions possible (if requested).
- Artificial misalignment within the structure is not a good idea, we can do equivalent thing in software.
- Can we rotate the support structure by 90° ?
→ Yes, in principle, but the event rate will get too low.
- Vibration of the structure from the cooling pump of PCMAG can be the issue.

[03-a] R.Itoh

- **Is it possible to have a dry run test bench of PXD in KEK?**
→ **A simulated ONSSEN output can be possible.**
- **Is it possible to have a dry run test bench of SVD in KEK?**
→ **FTB can generate simulated raw data.**
- **A dummy line FTSW→PXD-simulating-PC can be implemented on the TCP/IP network.**
- **Itoh-san likes dry run setup in KEK gets ready in September.**

[03-b] R.Itoh

- **We have one FTB in KEK, sufficient to dry run study.**
- **Wacek-san will be in charge of coding the FTB firmware to generate *the* dummy data.**

[04-a] S.Lange

- **Implementation of pedestal upload (green line) is needed; how to implement in EPICS PC?**
 - JTAG protocol will be used. Update should be made outside of the run (instead of online update).
- **Baseline assumptions: important summary**
 - L1 rate = 1kHz.
 - PXD throughput (normal operation) = 160kB/s.
 - PXD throughput (1Hz-full-frame operation) = 192kB/s.

[04-b] S.Lange

- DAQ group likes to use Belle-II DAQ for the telescope test.
- **HW:** For the telescope test, which protocol we use for connections of both $ATCA \leftrightarrow HLT$ and $ATCA \leftrightarrow EVB\#1$; TCP or UDP.
- A new TCP core developed by JAXA exists, which can handle multiple connections.

Digression [1-a]: MIMOSA

- **MIMOSA is controlled by TLU.**
- **MOMOSA will be read out by EUDAQ.**
- **Delicate question: do we really need MIMOSA?**
 - **For a low rate condition, it will be used to determine particles' momentum; while for a high rate condition, this may not be true.**

[05-a] D.Levit

- **DHH and DHHC are same hardware.**
- **EPICS is slow: 100kbps**
→ **Several tricks are employed to reduce the communication bandwidth between the DHHC and EPICS.**
- **DHH carrier module (ATCA) is under development and will (hopefully) be ready in Jan. 2014.**

[05-b] D.Levit

- **TODO list**
 - Integration into EUDET run control.
 - Integration of SWITCHER in slow control before system test in Bonn.
 - Test of the TLU interface.
 - Validation of the interface to DCDB.
 - Test of the DHH-ONSEN interface during system test in Bonn.

[06-a] D.Münchow

- **Newly implemented cluster-based pixel salvaging mechanism is confirmed working.**
- **TODO list**
 - For development: Local random data input needed
 - Generation of data and sending to BonnDAQ is possible.
 - Accepting of received data and writing to file not working yet.
 - Problems with recognizing of Trigger ID.
 - DHH data decoder has to be integrated.
 - Data visualisation has to be integrated.

[07-a] B.Spruck

- **Monitoring system monitors something related to PXD as a hit map, pedestal stability *etc.***
- **Several monitoring systems are considered.**
 - Basic ONSSEN:
 - IPMI. Monitoring of board health, power *etc.*
 - EPICS. For buffer usage, data rate, frame rate, Aurora errors, network *etc.*
 - Basic PXD on ONSSEN:
 - Anything beside “simple” counting is hard to do.
 - Example HitMap require random access to system memory in addition to all other components (additional RAM interface), because of RAM access time this cannot be directly added to the ROI core. Second data-unpacking path would be needed... and so on...

[07-b] B.Spruck

- **Several monitoring systems are considered.**
 - Request from DHH, have a raw data (memory dump) after pedestal update...
 - How are requirements for DESY 2014? Most likely not.
 - PXD monitoring should be done on PC.
 - In the telescope test, PXD monitoring is carried out mainly on mini ExpressReco and readout PC.
 - The preferred way to implement our monitoring is to run it on an intermediate PC that also does the UDP-to-TCP conversion. Implementing it within the basf2 framework right from the start would be interesting, but requires more manpower.

[07-c] B.Spruck

- **Monitoring system will demand NSM to halt the run when a faulty condition takes place.**
- **We will have a 24-hour beam time.**
 - **Shift-friendly monitoring system should be needed.**

[08-a] T.Geßler

- **The optical links of the xFP card were tested at 6.25Gbps using an Aurora connection**
- **BER was measured by connecting two xFP cards through the carrier board.**
 - 3.125Gbps: No problem.
 - 4.0Gbps: Tested by IHEP with no problem.
 - 5.0Gbps: Tested by IHEP with bit errors.
 - 6.25Gbps: Bit error rate of 10^{-12} in one and 10^{-7} in the opposite direction were observed.

[09-a] M.Schnell

- **The connection from FTB to DATCON will be made over the Belle2Link.**
- **Track finding algorithm = Hough transformation**
- **Track finding efficiency depends on the lower threshold of p_T .**
 - Tracks with multiple scattering tend to be undetected.
 - In MC events with 4 tracks generated, 1.5% of the generated tracks are undetected due mainly to the multiple scattering.
- **Track finding latency = 10-15 μ s per event.**

[09-b] M.Schnell

- **HW:** Rol generation within the HLT will be presented by Jakob-san in near future.
- **DATCON does not break the event ordering.**
- **Timeline**
 - April: Test of xFP cards, implementing the “DatCon” firmware.
 - Q2: Vienna data transmission and protocol decoding test with 4-SFP xFP; implementation of full FPGA tracking will start.
 - September-October: Rol send test with Gießen.
 - January: Test beam at DESY.

[10-a] M.Ritzert

- **Isn't it better to avoid duplicated efforts? How about recycling the existing monitoring system?**
→ **DAQ and PXD groups should work coherently on the monitoring issue.**
- **The monitoring system runs on the mini ExpressRECO PC.**
 - Pedestal update is also performed inside this PC. The updated pedestal information is transmitted to EPICS PC (not directly to the DHHC). Only the EPICS PC communicates with the DHHC.
 - Orange line from the mini ExpressRECO to the DHH in Lange-san's slide is a bug.

[11-a] M.Friedl

- **Some SVD-DAQ parts exist already, some are being designed.**
 - FTBs are in Cracow, the rests are in Vienna.
- **Data connectivity test with integrating most of the SVD-DAQ related parts will be carried out in the late of June in Vienna.**
 - Data connectivity = FADC → FTB → COPPER & FTB → DATCON.

[12-a] K.Hara

- **FTB prototype ver.2 production:**
 - PCB boards are ready.
 - Parts from one of the distributors are not delivered yet.
→ They will arrive by this Thursday.
 - The official order will be ready in this week.
 - Documents for parts and assembly work will be sent to the company by the end of this week.
 - The assembly work will take ~10 working days and finish by the end of Apr.
 - 1 month delay from the original plan (Mar.).

[13-a] P.Kvasnicka

- **Test beam package is in the basf2 SVN.**
 - First geometry is ready.
- **TODO list**
 - Event display → coherent work with M.Schnell-san.
 - Data simulators for the PXD and SVD part.
 - VXD alignment (offline alignment).
 - The VXD alignment software will be first used and tested for the test beam experiment.

[14-a] C.Irmeler

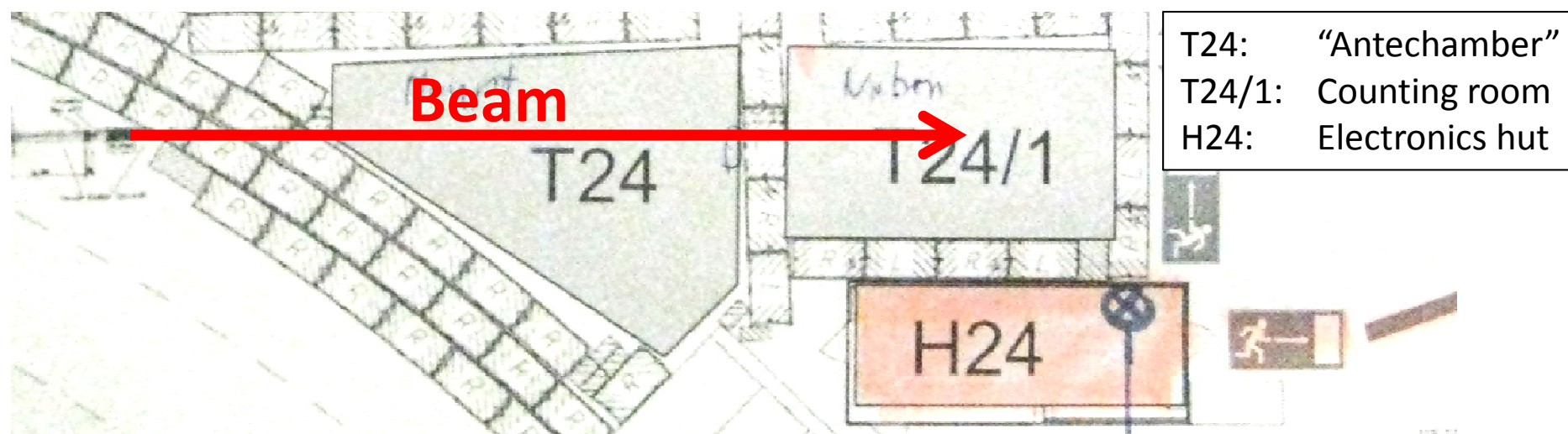
- **Important milestones in 2013**
 - FADC board: available by Jun.
 - FADC + FTB + DATCON connectivity test in Vienna: Jun.
 - Firmware development of NEKO board: Aug.-Nov.
 - Delivery of L3 sensors: Sep.
 - HW & FW test in Vienna with the full system: end of Oct.
 - Beam test preparation @ DESY: Oct.-Dec.
 - FADC firmware: until mid of Nov.
 - Shipment of SVD-readout modules to DESY: Nov.
- **Beam test = Jan. 2014**

[14-a] C.Irmmler

- **When does ONSSEN and POCKET DAQ meet with each other? → Oct. 2013?**

Visit to the Test-Beam Line [1]

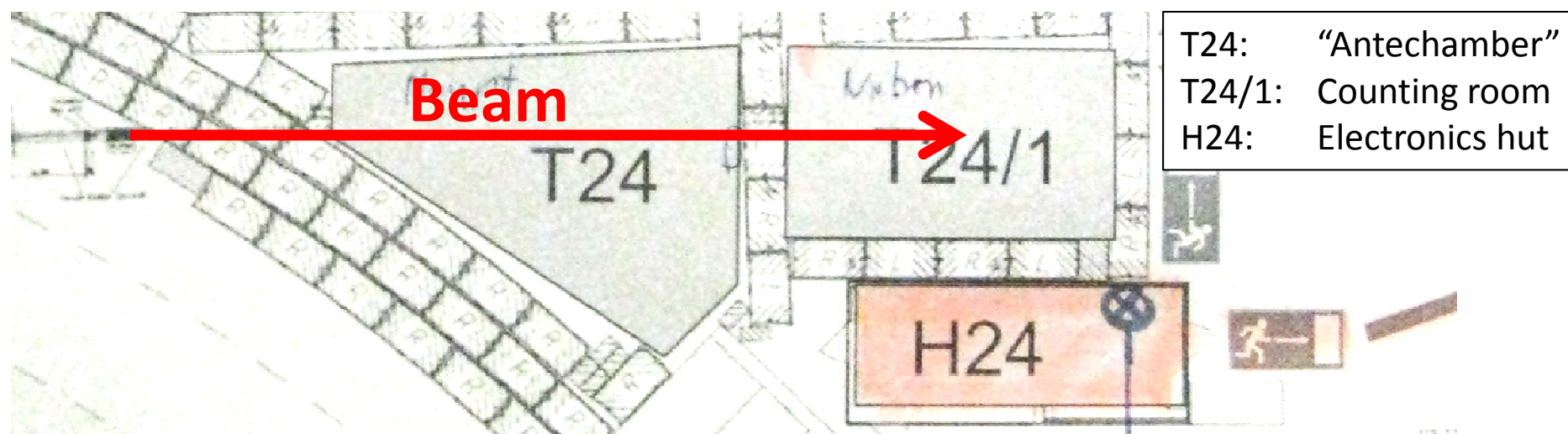
- Where to place the items?



- MARCO is located in T24.
- DHHs, ONSen, and DATCON are located in H24.
- FTBs are located in T24 (cable length from the DOCK in T24/1 to FTB over the wall is 12m, and that from the FTB to COPPER over the wall is 15m).

Visit to the Test-Beam Line [2]

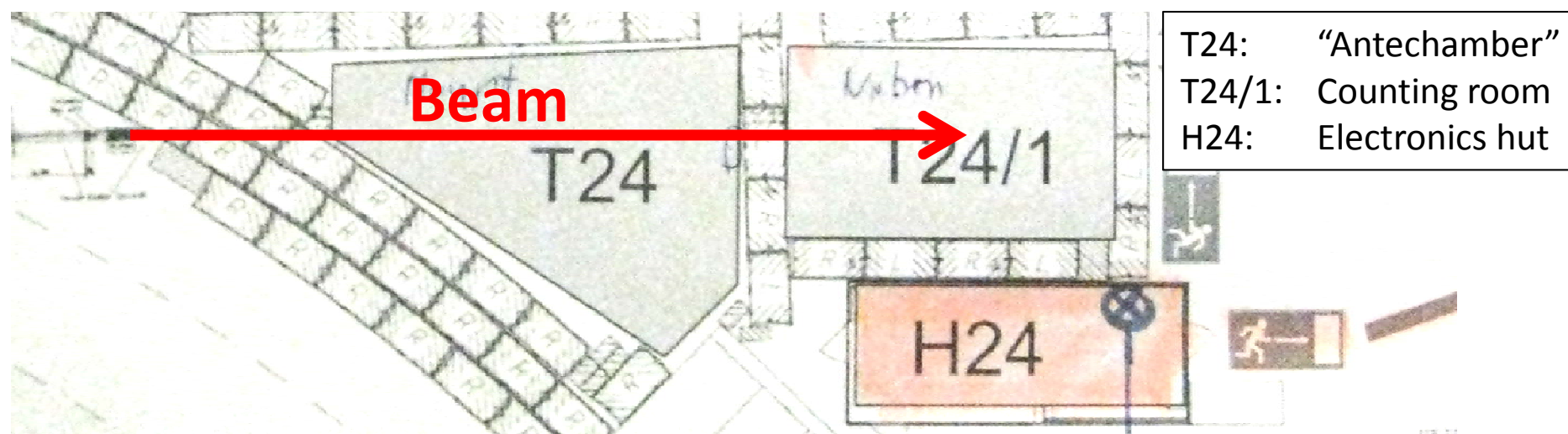
- Where to place the items?



- PXD+SVD power supplies are located in T24.
- COPPERs, FTSW, and PC servers are located in H24.
- Optional one FTSW + VME-6U crate may sit in T24.

Visit to the Test-Beam Line [3]

- Where to place the items?



- **HW**: Are TLU and two TLU-controlling PCs located in T24/1?
→ 20m cables to connect TLU and FTSW are needed; 15m ones are better. The first cable is for trigger, the second is for clock.

[15-a] M.Nakao

- **Who will be in charge of TLU operation? → DESY people.**
- **TLU uses 4-pair LVDS on Ethernet standard RJ-45 pin assignments, fully compatible with FTSW.**
- **Pin assignment of the CAT7 cable is slightly different in between TLU and FTSW → No problem.**
- **TLU has no clock input, and FTSW cannot use TLU's clock output (40MHz or 48MHz?) as the system clock.
→ TLU and FTSW work under different clock.**

[15-b] M.Nakao

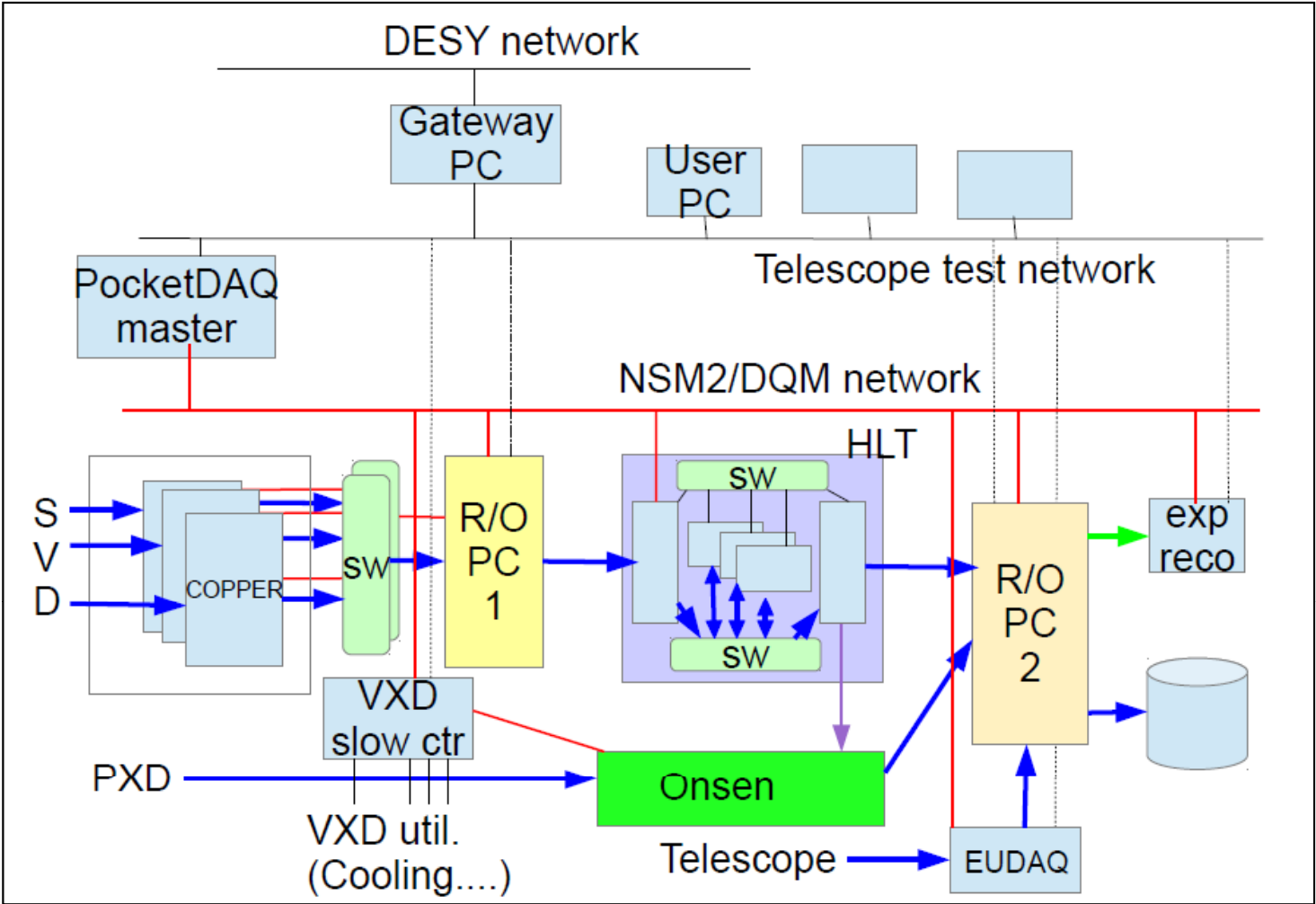
- **Trigger timing from TLU is asynchronous to any clock; it will have as 31ps RMS-jitter. FTSW will quantize it to 8ns LSB coarse trigger-timing (nobody complained about it).**

[15-c] M.Nakao

- **FTSW asserts a BUSY signal (dedicated LVDS pair) and receives 16-bit trigger counter to/from the TLU.**
- **Trigger latency by TLU is 27ns. Do we need to generate 5μs latency to imitate the real system?**
→ No. For SVD, even no latency is OK.
- **There exists no good way to synchronize TLU and FTSW timestamps and event number (for sanity check).**

[16-a] R.Itoh

- Itoh-san’s original idea about the network topology



[16-b] R.Itoh

- **Discussion**

- Telescope-test network and NSM2/DQM network can be merged.
- We add another network connections to the two EUDAQ PCs, which are linked to the Telescope-test/NSM2/DQM network.
- TLU should be connected to one of EUDAQ PCs.

[17-a] M.Nakao

- **NSM2 alpha release (2013.3)**
 - Low-level technology choices were made and implemented.
 - Very preliminary Belle II dedicated library is made.
- **NSM2 beta release plan**
 - Database interface for log messages and NSM shared memory data.
 - Belle II dedicated library for state handling with first targeting system being CDC/Belle2link/COPPER.

[17-b] M.Nakao

- **NSM2 to control EUDET**
 - CUI version of EUDET control is easy to understand and modify.
- **A quick hack: CONFIG/START/STOP from NSM2 to EUDET was coded in 1 hour.**
 - It is not yet working in a coordinated way, e.g., run numbers or error messages, but no technical problem foreseen.

[17-c] M.Nakao

- **NSM2 interface will be added to EUDET. The software is under design.**
 - Proper response and error forwarding back to NSM2.
 - Log message forwarding to NSM2.
 - Configuration parameters passed from NSM2.
- **Rest of the world is kept as it is from NSM2 point of view, but DataCollector will be modified to connect to EVB2.**

[18-a] R.Itoh

- **Procurement of PCs: DESY will afford the followings.**
 - x2 desktop PCs: POCKET DAQ control and DESY gateway (quad core @ >3GHz, x4 GbE NIC, 4GB memory).
 - x3 rack mount PCs (1U): Readout PC 1, HLT I/O (quad core @ >3GHz, x4 GbE NIC, 4GB memory).
 - x3 rack mount PC (1U): HLT worker nodes (≥ 8 cores @ >3GHz, x2 GbE NIC, >2GB/core).
 - x1 rack mount PC (2U): Readout PC 2 (quad core @ > 3GHz, x8 GbE NIC, 4GB memory, storage I/F).
 - x1 rack mount PC (1U): mini ExpressReco PC (quad core @ >3GHz, x2 GbE NIC, 8GB memory).

[18-b] R.Itoh

- **Procurement of peripherals: DESY affords as well.**
 - x1 storage disk (USB3 portable or rigid RAID?).
 - x1 file server PC with a few TB RAID.
 - x4 24-port GbE switch, wireless AP(?).
 - x1 rack.
 - NICs for EUDET PCs
 - Network cables (optical, metal).

[19-a] R.Itoh

- **DQM**
 - DQM framework is provided as a part of the POCKET DAQ.
 - Histogram accumulation should be done.
- **Where basf2 is supposed to run?**
 - ONSEN: on “UDP->TCP conversion PC” / Readout PC 2.
 - SVD: on COPPER (diagnostics) / Readout PC 1+2.
 - VXD (SVD+PXD): on mini ExpressReco.
- **The “DQM master” will be POCKET DAQ controlling PC.**
 - The POCKET DAQ controlling PC is in the procurement list.

[19-b] R.Itoh

- **Event display**
 - PXD+SVD displays are available on the mini ExpressReco, where the software is provided by Peter-san and Michael-san; detector hit signals together with reconstructed tracks will be displayed.
 - The image is dumped in an image file every 3 sec. (for example) so that it can be referred from web ← web server has to be implemented somewhere which shares the file system.
- **Raw data sampling**
 - Sampled events (at low rate) are kept in memory to be distributed to outside over network (event server), for the detailed monitoring by experts.

[20-a] R.Itoh

- **Remaining issues in the POKCET DAQ**
 - HLT, 2nd level event building at the readout PC 2, and migration of EUDAQ.

[21-a] T.Higuchi

- **Rol of the 64-bit version is preferred than the 48-bit version.**
- **TCP option should be considered.**
- **One packet per event may be inefficient
→ Combine multiple Rol-packets to one?**

Next Workshop

- **July 3rd, 2013 (a gap day between BGM and B2GM) in VPI + SeeVogh connections.**