DHH Development Status

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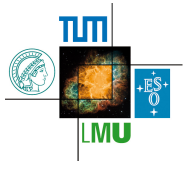

Bundesministerium
für Bildung
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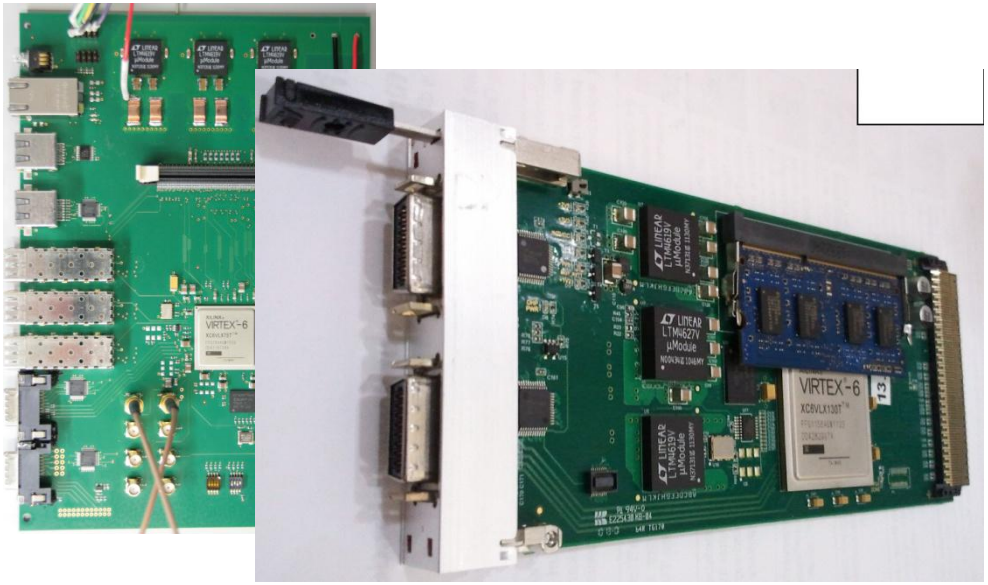
Outline

DHH/DHHC



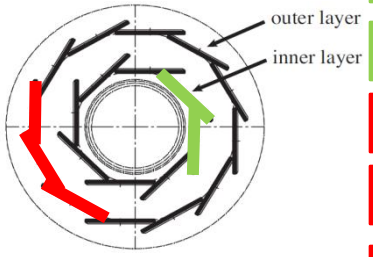
DHH prototype

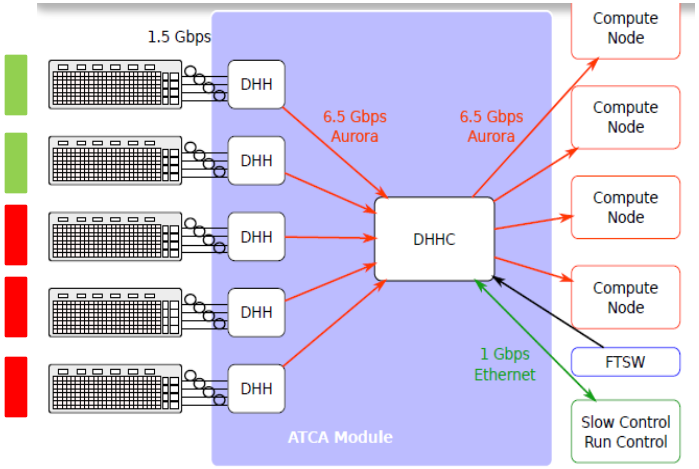
- tested with DHP Hybrid, FTSW and ONSEN modules
- integrated into EPICS slow control
- being prepared for May testbeam in DESY

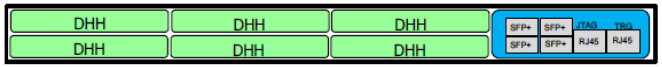
Final design

- AMC module, ATCA standard
- Module programmed as DHH or DHHC
- Load balancing
  30% peak data rate reduction
- Subevent building
- VIRTEX6 XC6VLX130T FPGA
- 2GB DDR3
- DHHC data throuput : 2.5 GB/s
- First DHH AMC module been delivered and being tested now
- Mass production by end of 2013

Readout scheme



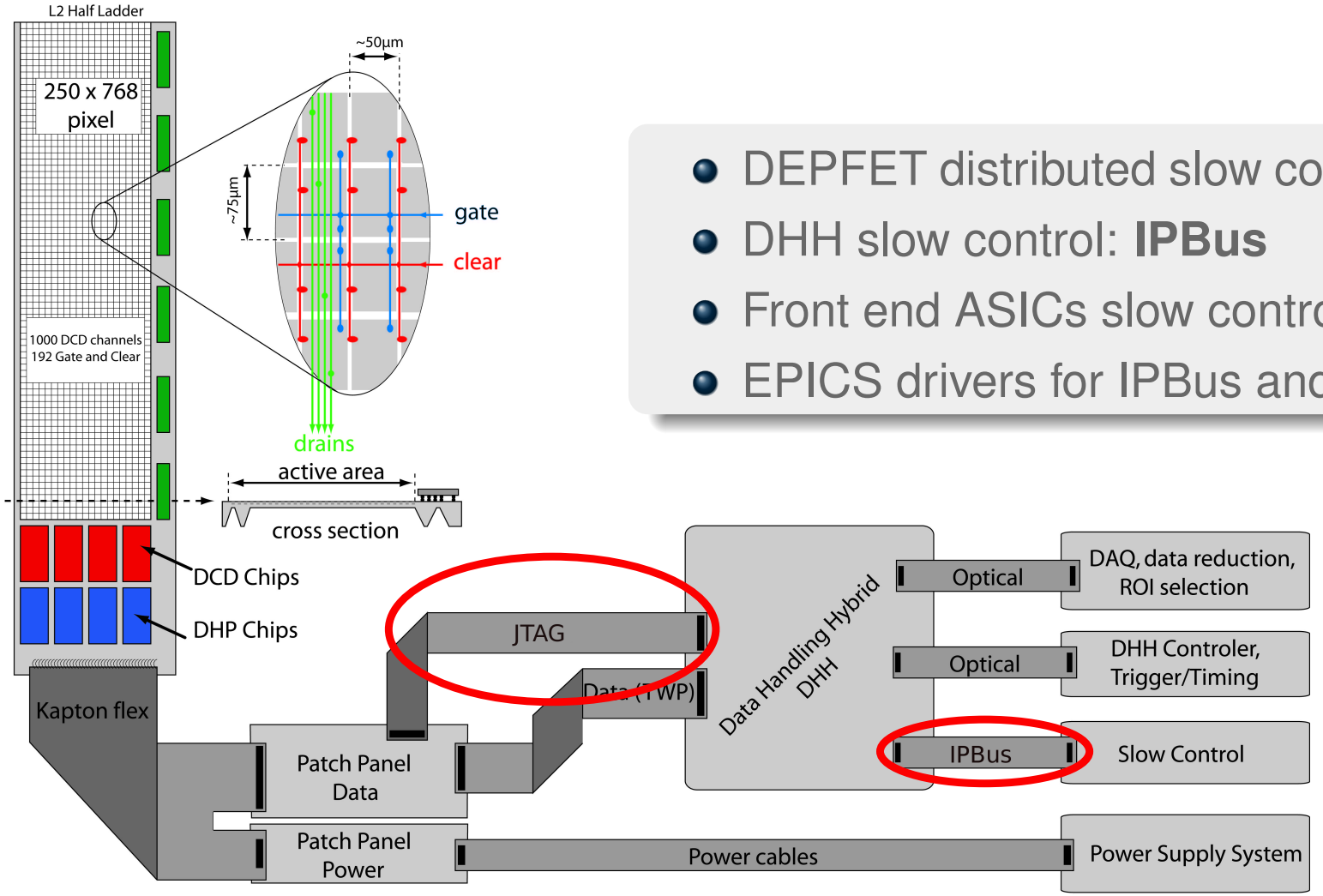




ATCA module

Outline

High Level Slow Control: EPICS



- DEPFET distributed slow control: **EPICS**
- DHH slow control: **IPBus**
- Front end ASICs slow control: **JTAG**
- EPICS drivers for IPBus and JTAG

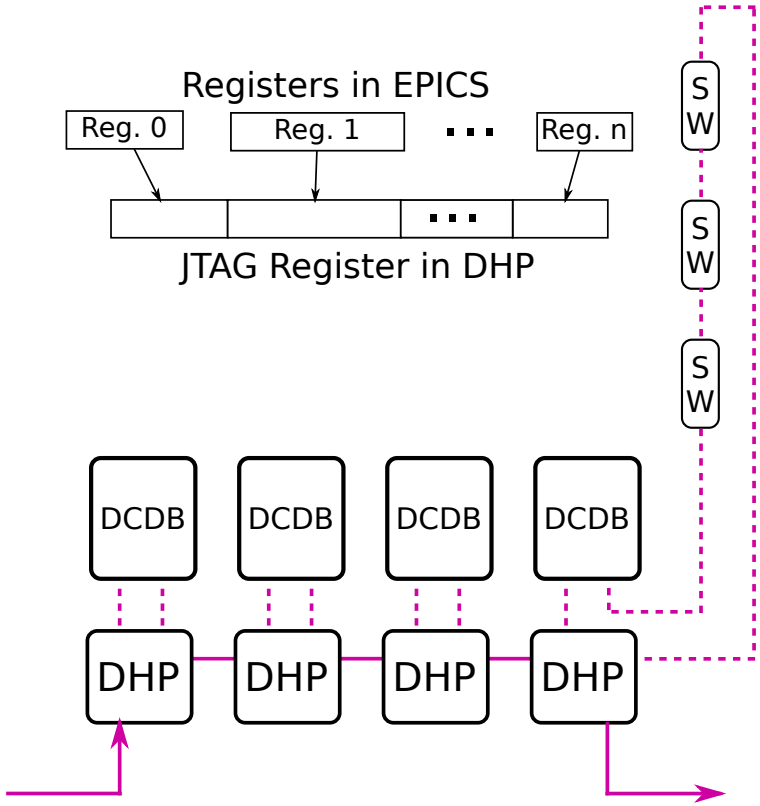
IPBus System

- UDP based protocol for slow control applications
- CPU-less implementation for FPGA
- Register based access
- C++ Hardware Access Library provided
- EPICS driver written by Alan Campbell

JTAG Chain Topology

Main challenges:

- not standardized register set
- dynamic chain configuration: DHP can exclude other ASICs from the JTAG chain



JTAG EPICS Driver

- not blocking driver: queries processed in background thread
  - IPBus library shared with IPBus driver: IPBus driver blocked during hardware access
- consists of **low level driver** and **device support**:
  - **low level driver**: bitstream generation, hardware access
  - **device support**: translation of the EPICS registers into JTAG and back, activating/deactivating DCDB and SWITCHER

JTAG Driver Operation

EPICS Registers

- two sets of registers for most registers:
  - read: suffix "_r"
  - write: suffix "_w"
  - type: epicsInt32
- dispatcher register for every JTAG register: hardware access only on write into dispatcher register
  - type: epicsInt8[]

- player calibration
- chain initialization: find what devices are in the JTAG chain
- register initialization
- device operation: issue read and write queries to the JTAG devices

JTAG Driver: Read and Write Operations

Write

- write register
- Only for composited registers: write dispatcher register for write
- if access successful: read register gets updated

Write

- write dispatcher register for read
- if access successful: read register gets updated

JTAG Driver: Pedestal Updates

EPICS is slow! Approx. 100 kbps

- UDP server for memory update in the driver
- port selected dynamically, published under dhh0:jtag_port_r
- special frame format required
- frame size limited by MTU
- replies with ”OK” or ”FAIL” after processing data

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JTAG Driver Test with DHP and DCDB Chain

Testing Hybrid 5 with DHP and DCDB

- DHP: read and write OK
  - errors during pedestal updates
  - estimated BER: $2 \cdot 10^{-7}$
- DCDB: configuration cannot be read back (bug in ASIC)
  - IDCODE reads correctly
  - current consumption drops, if analog part switched off over JTAG

Outline

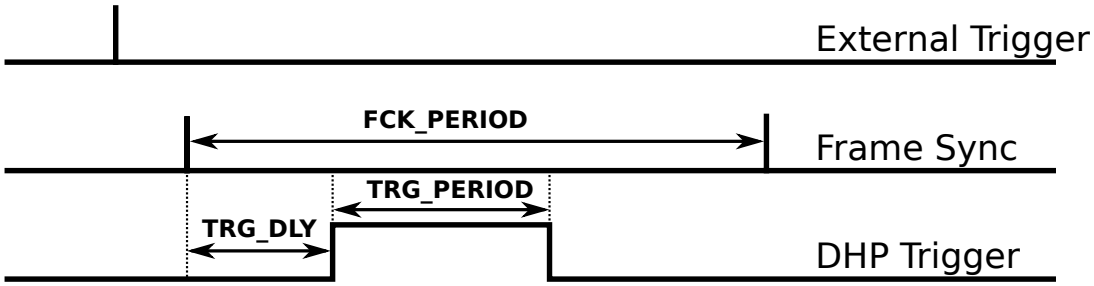
Trigger Module

Trigger Parameters

- TRG_EN
- TRG_PERIOD
- TRG_DLY
- FCK_PERIOD

TLU Integration

- using module from Uni Bonn
- DHP reset synchronous with TLU reset
- compatible with DHH hardware:
  - special cable prepared for TLU interface



Trigger timing

Trigger Module Testing

- Setup: DHP - DHH - PCIe evaluation Board (Virtex5), FTSW clock and trigger
- DHP mode: TEST, process data stored in memory
- Goal: validate DHP behavior with trigger module

Result:

- synchronization: OK
- trigger delay and trigger period handling: OK
- link stability issues: linked with firmware generation in ISE

Outline

ToDo List for Test Beam in May

TODO:

- integration into EUDET run control
- integration of SWITCHER in slow control
  - before system test in Bonn
- test of the TLU interface
- validation of the interface to DCDB
- test of the DHH-ONSEN interface
  - during system test in Bonn