Overview of data path

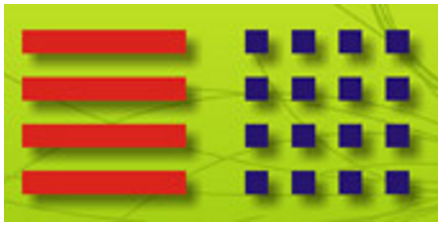
Corrected version 16.04.2013

S. Lange (Giessen)

Belle II VXD Workshop and GEMBA Meeting
04/9-10/2013 DESY, Hamburg

現場 (actual place; local; on-site)
„gemba meetings“ created by Ushiroda-san

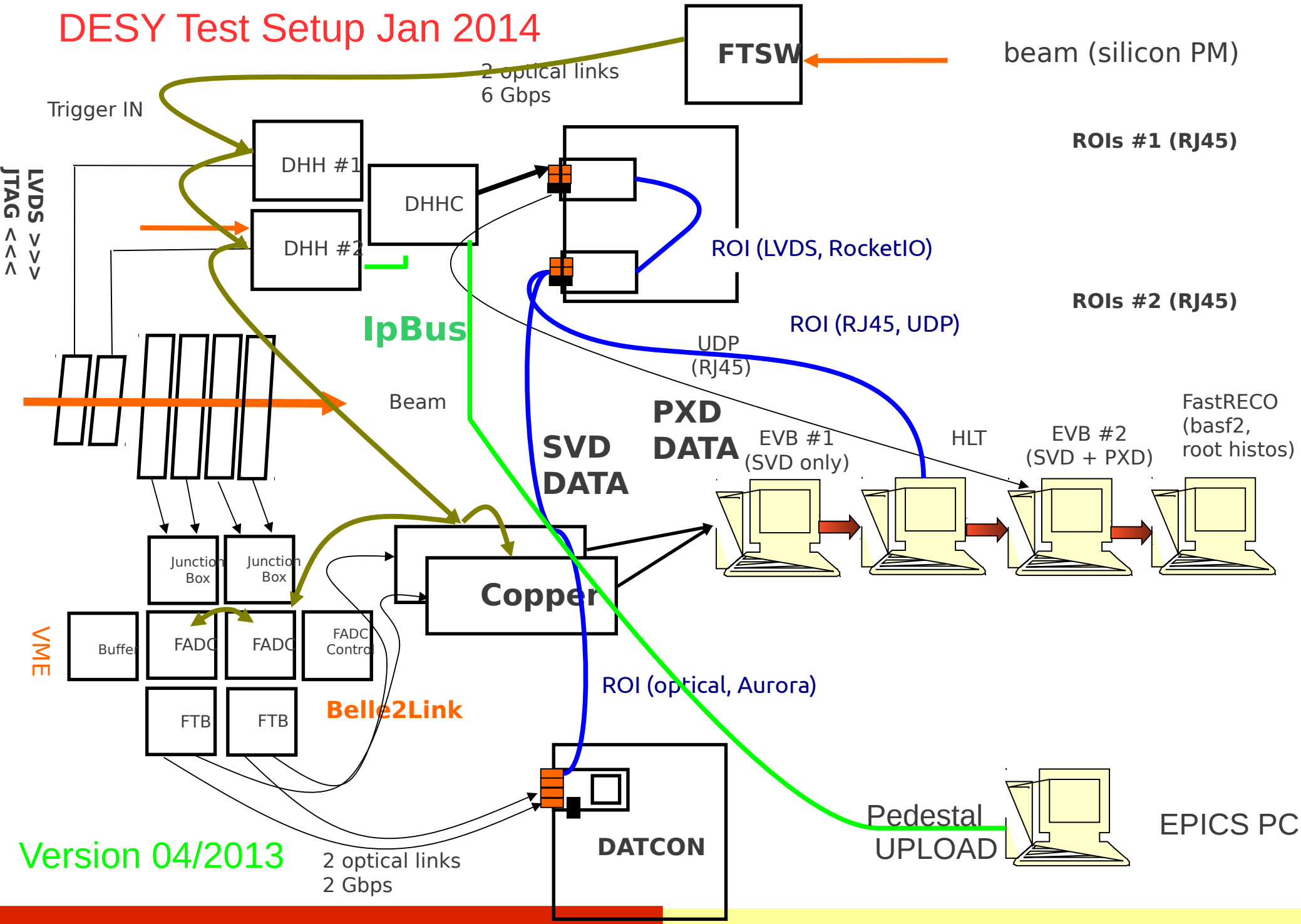
verb „gembarimasu“ (?) =
participating in a gemba meeting



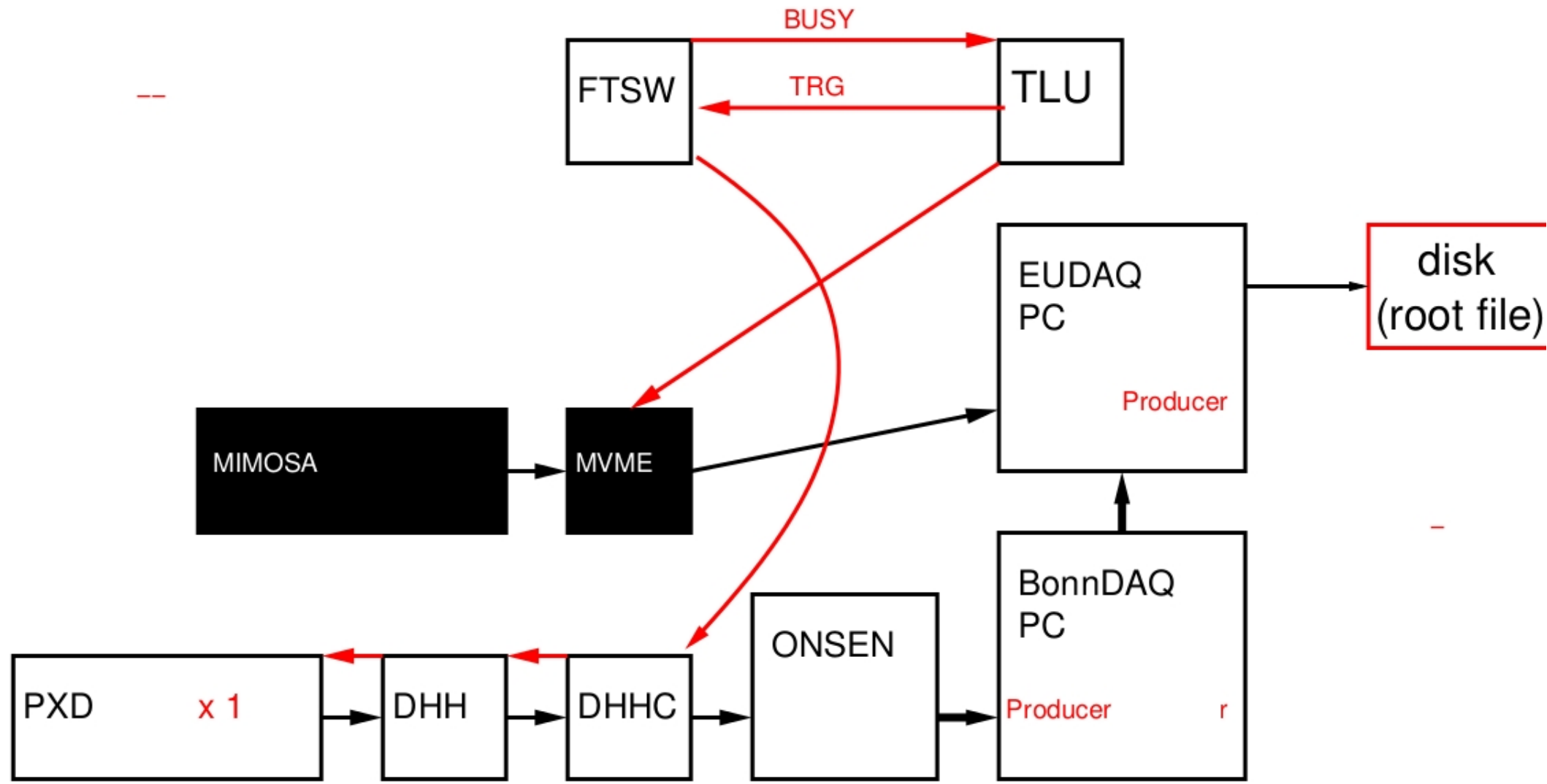
JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Bundesministerium
für Bildung
und Forschung

DESY Test Setup Jan 2014



Integration of MIMOSA Telescope – May 2013



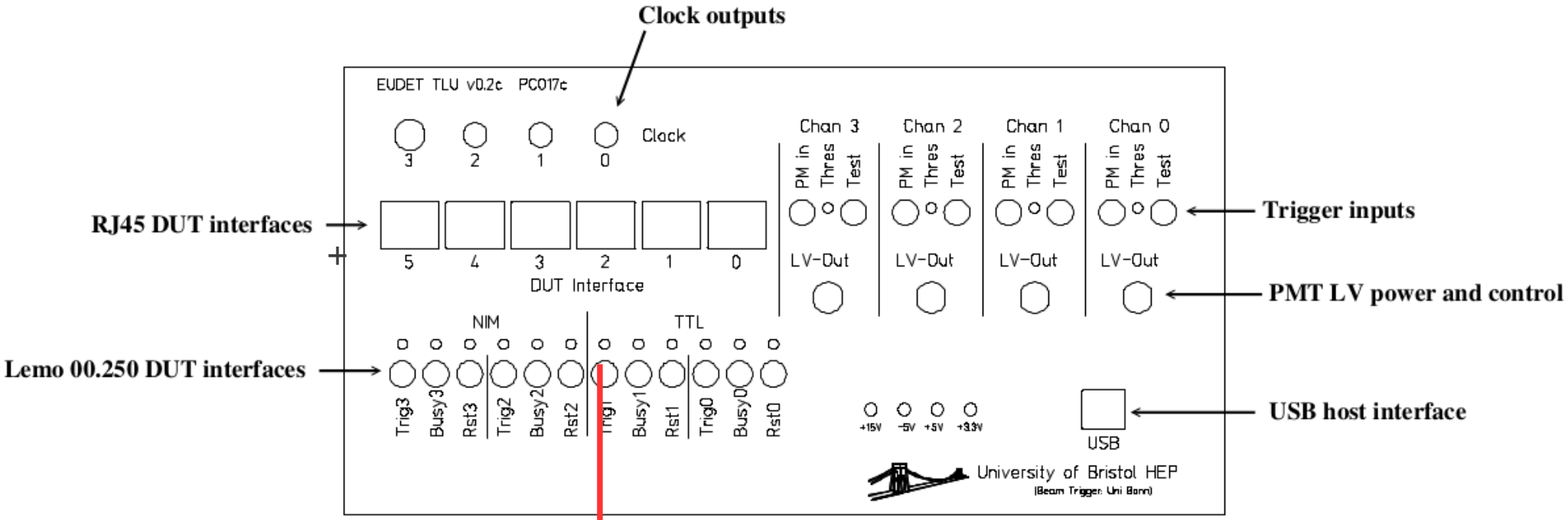


Figure 1: Front Panel of the TLU

To FTSW
and from FTSW to DHHC, Copper and FADC
and from DHHC to DHH
(return-busy probably not needed,
as 100 us MIMOSA > 20 us DEPFET)

May 2013 – Baseline Assumptions

- assume 1 kHz trigger rate
- magnet = target
  assume 5-10 secondary tracks
- „normal“ operation
  assume 10 tracks x 2 DHH x 2 hits/cluster x 4 bytes x 1000 Hz
  160 kByte/s
- full frames operation
  1 HalfLadder x 768 x 250 x 1 byte = 192 kB
  192 kByte/s (if 1 Hz full frames)

  (if „send pedestal and ADC“ mode, factor x 2)

Issues/TODO for May 2013 Test
(to be solved on this meeting)

ONSEN producer in Bonn DAQ (Florian + David)

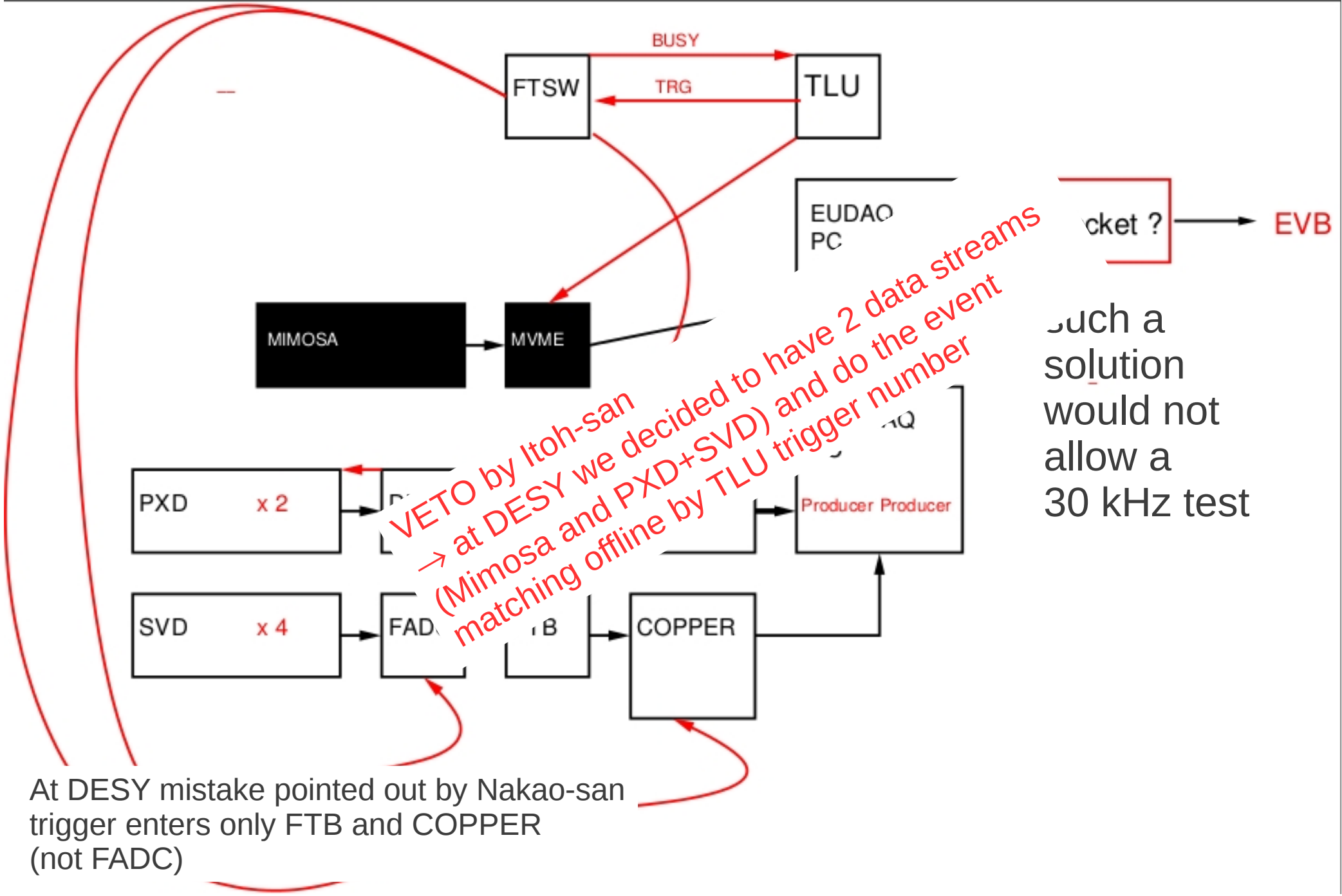
New Onsen AMC 3.2 card will be used (arrived with 3 months delay, report of test results by Thomas + Björn)

Pedestal upload (Dima, Benjamin)
- HOWTO integrate into EPICS ? (Michael, Alan)

TLU - FTSW interface (clocks ?)

full frame operation – mixed-in or separate runs ?
(mixed-in requires mode-flip on DHP „on-the-fly“)

data format DHH (not „pure“ DHP 0.2 format)
(6 bit common mode is stripped and put into extra event type)
o.k. for all decode/unpack ? (e.g. hit display or QA monitor)



such a solution would not allow a 30 kHz test

At DESY mistake pointed out by Nakao-san
trigger enters only FTB and COPPER
(not FADC)

Integration of MIMOSA Telescope – January 2014

Issues/TODO for January 2014 Test

New ROI distribution (not UDP broadcast, but ATCA onboard RocketIO with dedicated ROI receiver AMC)

Onsen – EVB interface

1. PAUSE frames for sending from ATCA to EVB

2. UDP handshaking
   (wait on Onsen for acknowledge from EVB)

3. SVD+PXD event building
   (also: EVB requires PXD data in basf2 root format)

basf2 3D event display ?

Random ROIs or „real“ ROIs ?
(will the track finders be operating with error handling ?)

ATCA/Onsen for DESY Test in May 2013

- 3.125 Gbps, Aurora 8B/10B

- no ROIs (i.e. no connection to HLT, no connection to DATCON)

ATCA/Onsen for DESY Test in January 2014

- 6.25 Gbps, Aurora 8B/10B

- send data to EVB by UDP on RJ45

- ROIs from HLT by UDP or TCP/IP on RJ45

- ROIs from DATCON by optical link (Aurora 6.25 Gbps 8B/10B)

THANK YOU.

DATA FORMATS

DHP 0.2

SOF (Frame Header) [32 bit]

SOR (Row Header) [16 bit]

DW (Data Word) [16 bit]

Data submitted:

- [3 bit] data type
- [13 bit] flags (not used yet)
- [16 bit] frame ID
- [1 bit] flag
- [9 bit] row address
- [7 bit] column address

- [6 bit] common mode
- [8 bit] ADC

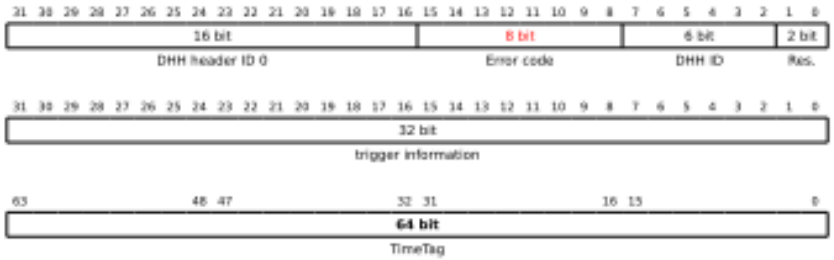
1 Event is 1 Aurora Frame
→ defines start/stop

16-bit alignment

1 bit of row addr
is encoded in column addr

DHH

DHH header 0 [2·32 bit, 1·64 bit → 128 bit]



DHH header 1 [32 bit]

DATA (same as DHP)
SOR (Row Header) [16 bit]

DW (Data Word) [16 bit]

Data submitted:

- [16 bit] DHH header ID 0
- [16 bit] DHH header ID 1
- [8/6 bit] Error code
- [6 bit] DHH ID
- [2 bit] Chip ID
- [2 bit] Reserved
- [2 bit] Data type
- [1 bit] flag
- [9 bit] row address
- [7 bit] column address

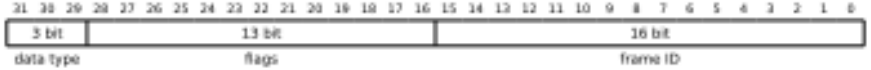
- [6 bit] common mode

- [8 bit] ADC

General questions:
How to seperate if header 0 or header 1

DCE3

SOF (Frame Header) [32 bit]



SOC (Start of Cluster) [16 bit]

CM (Cluster Member) [16 bit]

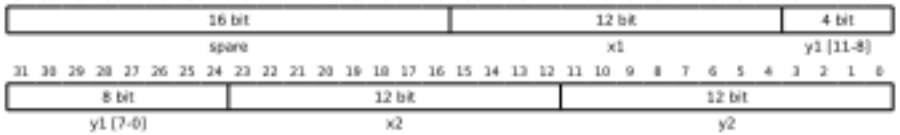
Data submitted:

- [3 bit] data type
- [13 bit] flags (not used yet)
- [16 bit] frame ID
- [1 bit] flag
- [10 bit] row address
- [8 bit] column address
- [1 bit] pop
- [2 bit] rel2prev
- [1 bit] push
- [1 bit] flag
- [2 bit] spare (not used yet)
- [1 bit] valid
- [8 bit] ADC

General questions:
Example cluster with picture and data stream and explanation could help a lot

ROI core Formats

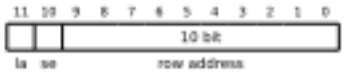
ROI input



Pixel input/output

Pixel definition

x



y

Data description:

- [16 bit] spare (not used yet)
- [8 bit] ADC
- [12 bit] x coordinate
  - [1 bit] DHH-layer (inner=0, outer=1)
  - [1 bit] DHH-sensor (0=backward-half, 1=forward-half)
  - [10 bit] row address
- [12 bit] x coordinate
  - [4 bit] DHH-ladder (inner layer 0-7, outer layer 0-11)
  - [2 bit] Chip ID
  - [6 bit] column address

DATA FORMATS

Schedule as submitted to BMBF (12/2011)