Data Concentrator

Plans for the testbeam at DESY

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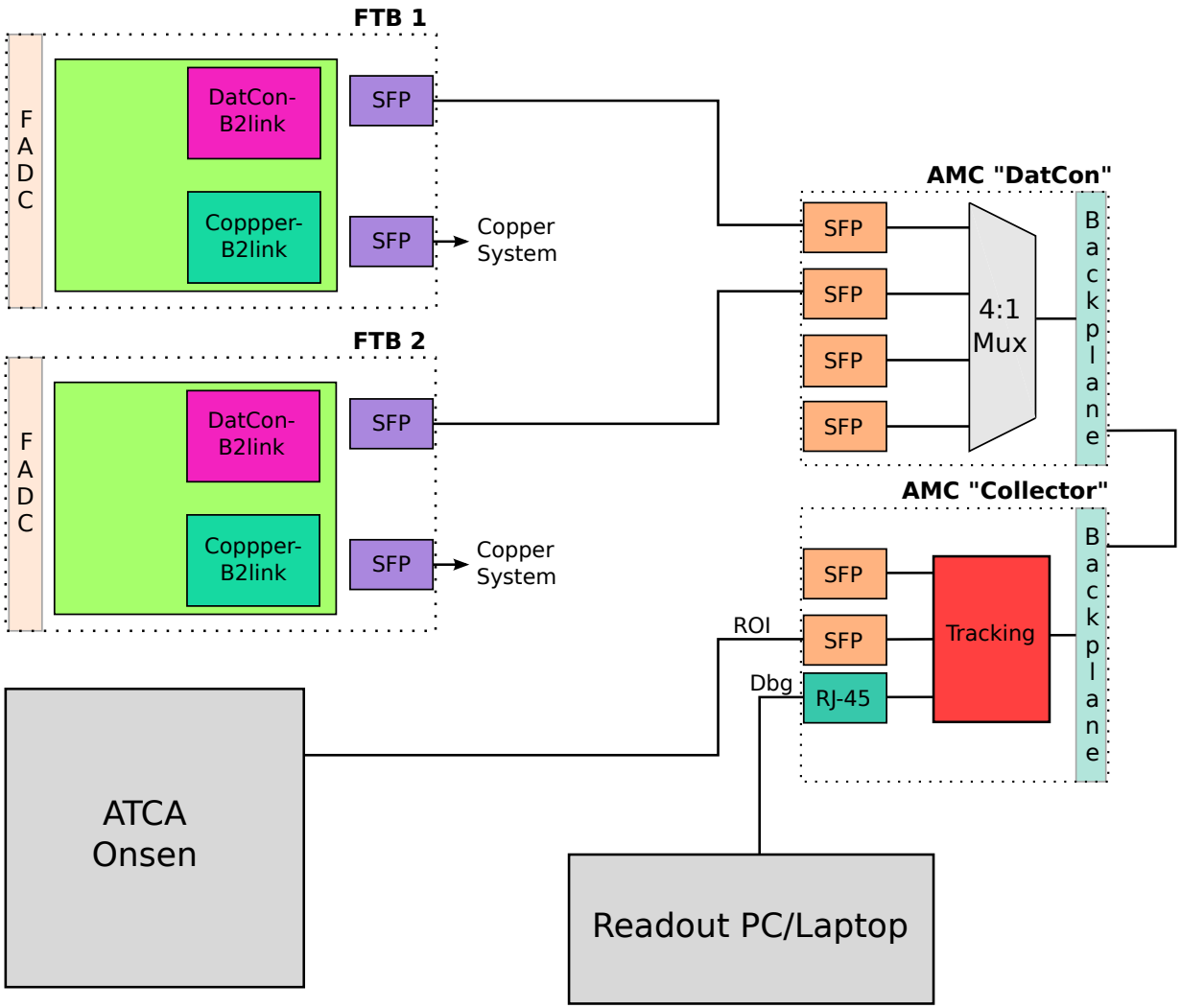
Content

1. Hardware
2. Data Aquisition

Setup: AMCs with mTCA Crate

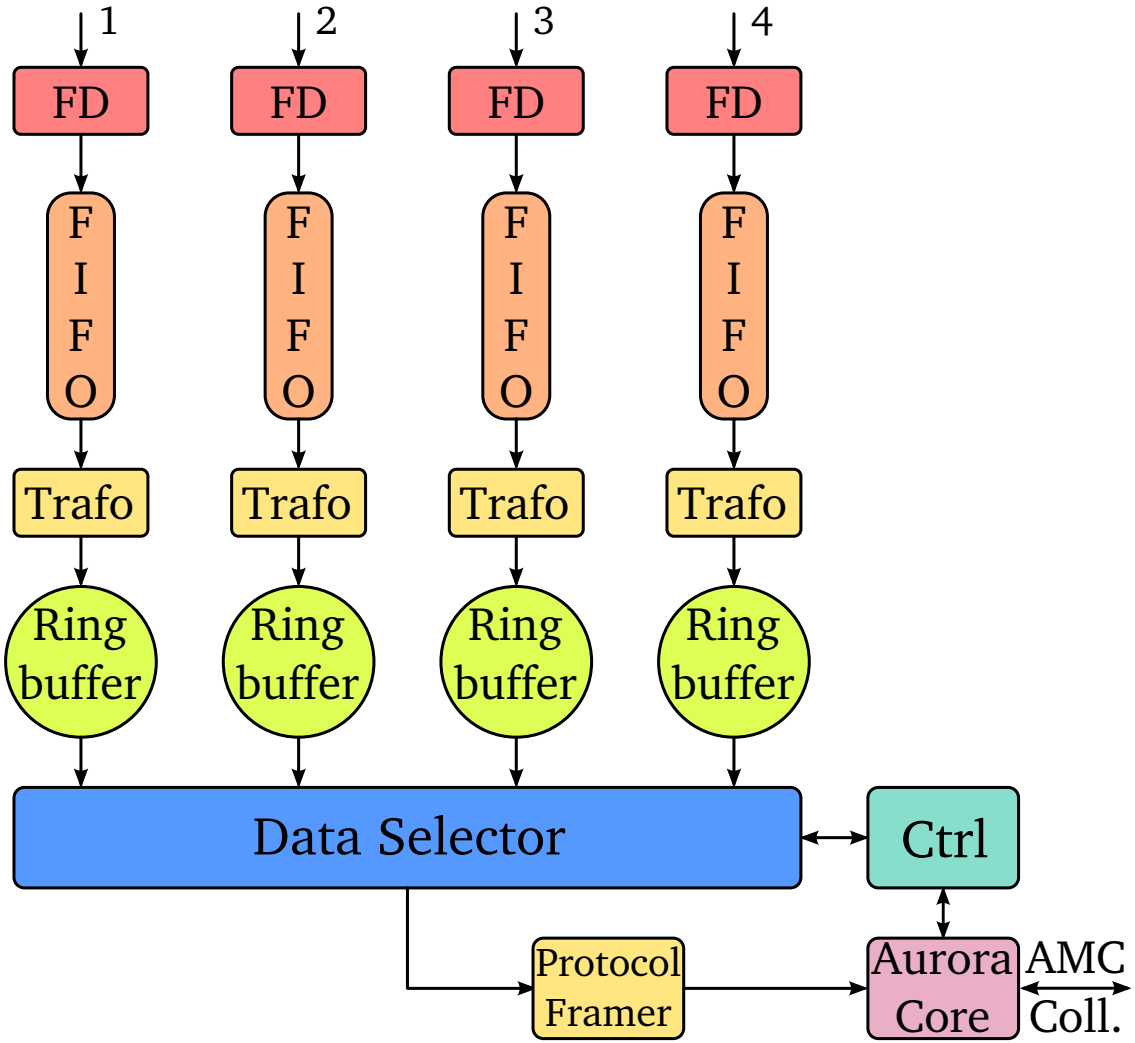


- 2x AMCs:
- 1x 4-SFP for acquisition
- 1x High Performance for tracking
- 9 Slot mTCA crate with D-Star backplane

Backup: Compute Node

- 2 FPGAs from 1x CN (already available)
- 2 Slot ATCA crate (available)
- Firmware must be ported (to Virtex 4)
- Not (close) to final design

AMC “DatCon” Layout

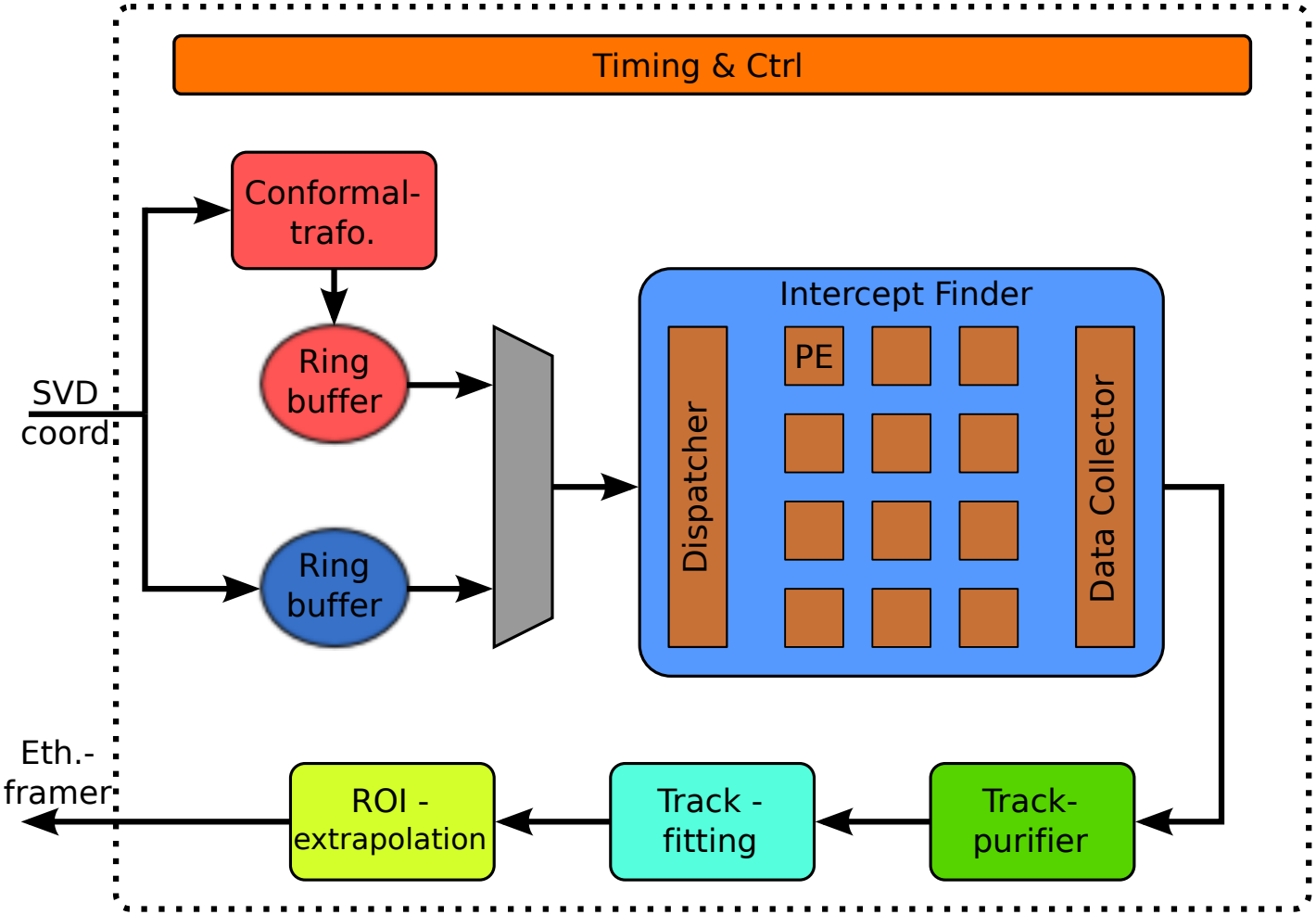


- FD: Frame Detection Unit
- Trafo: Transformation on incoming data, like coordinate translation...
- Ring buffer: Implemented in DDR2 memory.
- Ctrl: Control unit, sends data when next event is requested by collecting FPGA

Questions/Notes

- Data format of the FADC fixing in Q2
- Test in Q2 of FADC-FTB-DatCon (only readout)
- Slow control connection? (Ethernet debug connection is enough for us)
- FPGA firmware flashing PC?
- Connection to Onsen over RocketIO using Aurora?
- Monitoring over Ethernet connection

FPGA Track Reconstruction Prototype Architecture

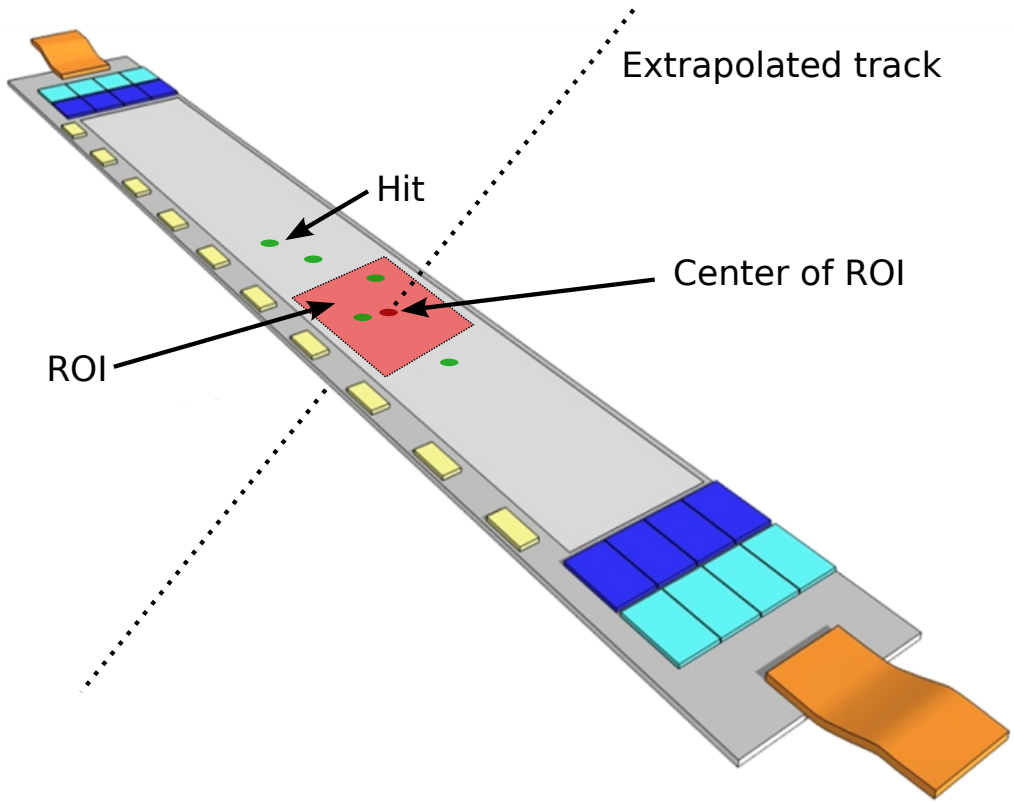


- PE: Processing Element, basic comparator to detect lines in cell
- Track Purifier: Remove duplicated found tracks and combine two 2D-sets

ROI Creation and Format

ROI creation:

1. Extrapolation of tracks to the coordinates of the different PXD layers
2. Use lookup table for "reverse" coordinate translation
3. Send center Pixel ID
4. And size of rectangular ROI in number of pixels, based on momentum lookup (lower momentum: larger ROI)



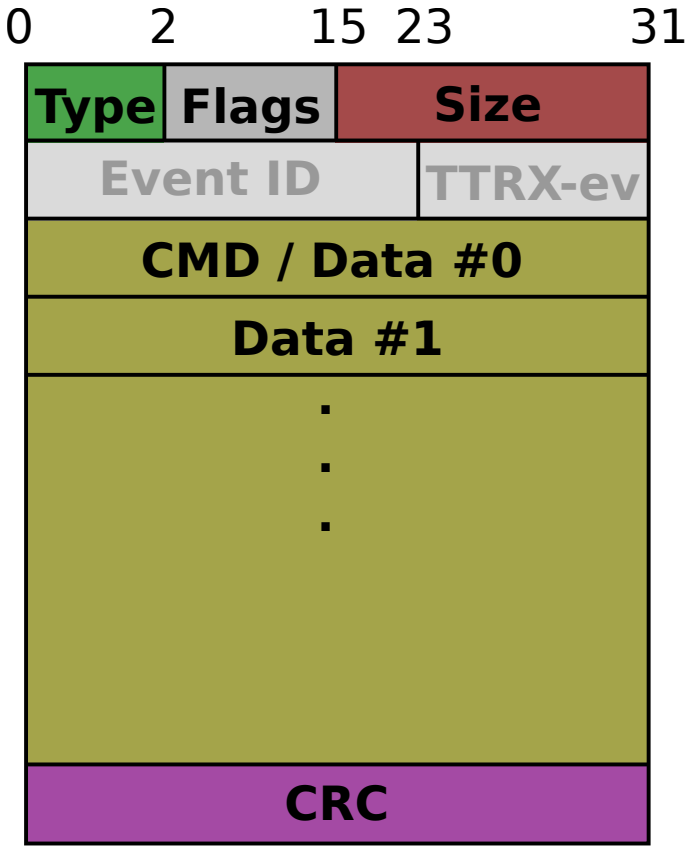
- Bachelor student working on the ROI size optimization

Timetable

- April: Test of AMC cards, implementing the 'DatCon' firmware
- Q2: Vienna data transmission and protocol decoding test with 4-SFP AMC
- Q2: Implementation full FPGA tracking
- September/October: ROI send test with Giessen
- January: Testbeam DESY

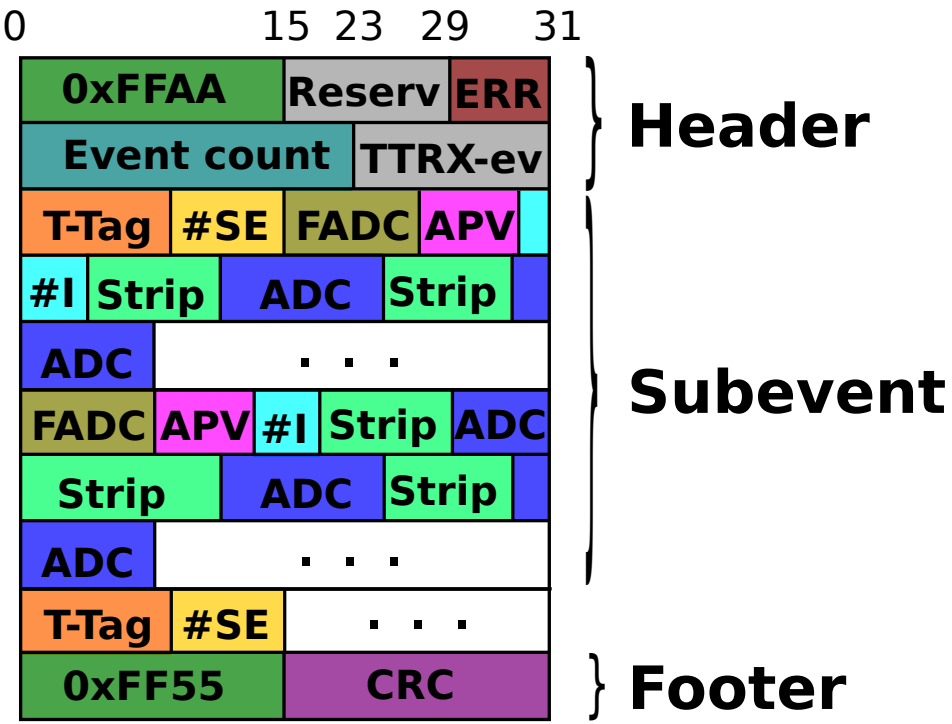
Thank you for your attention!

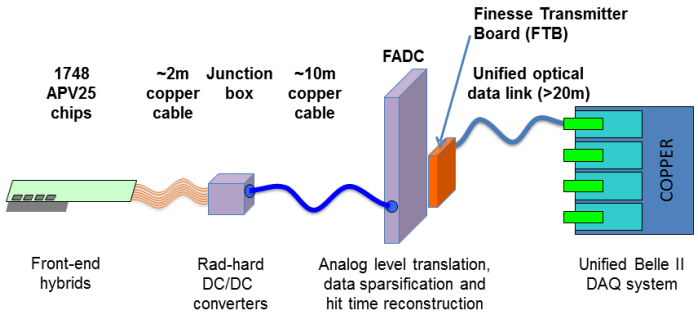
Internal Protocol



- Type: 2 Bit
  - 00: Command (CMD)
  - 01: User Data (DATA)
- Flags: 14 Bit
  - $(0000)_{16}$: Normal operation
  - $(0001)_{16}$: Test the connection, waiting for reply (only command)
  - $(0002)_{16}$: Test the connection, reply (only command)
  - $(1XXX)_{16}$: Error, kind of error indicated by XXX

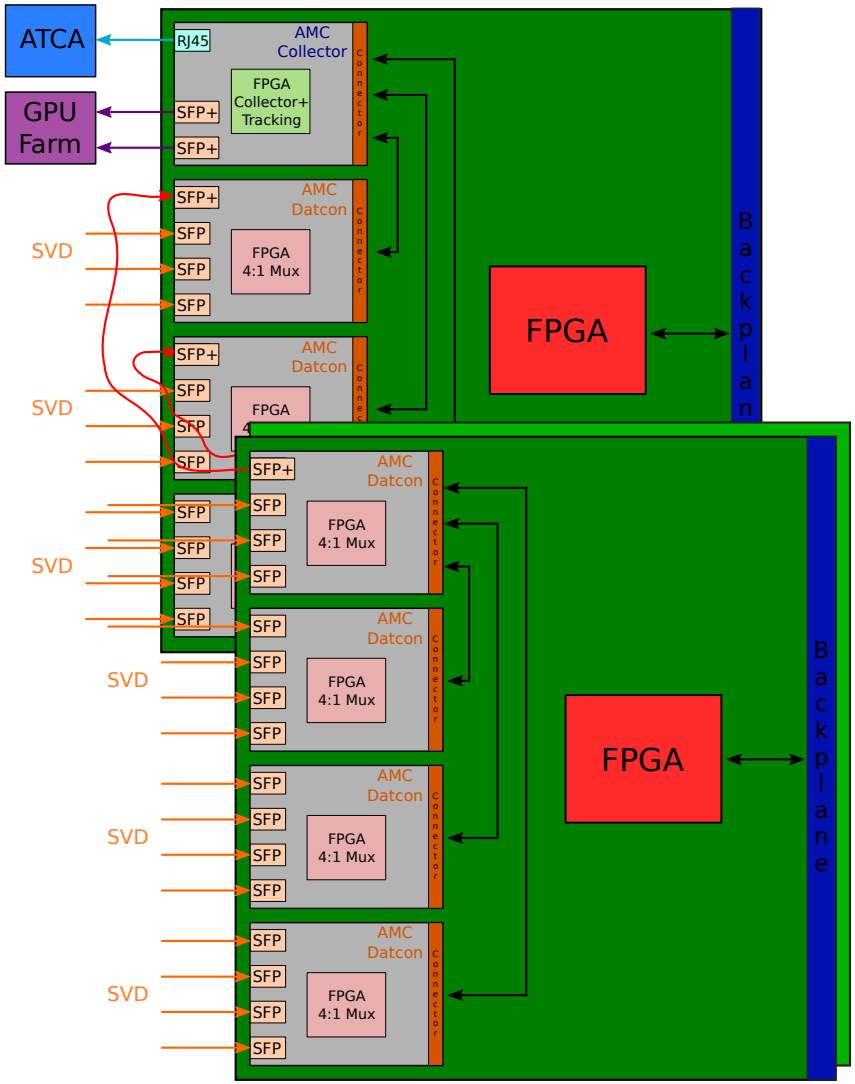
Proposal for the Belle II Link in SVD-DatCon Flavor





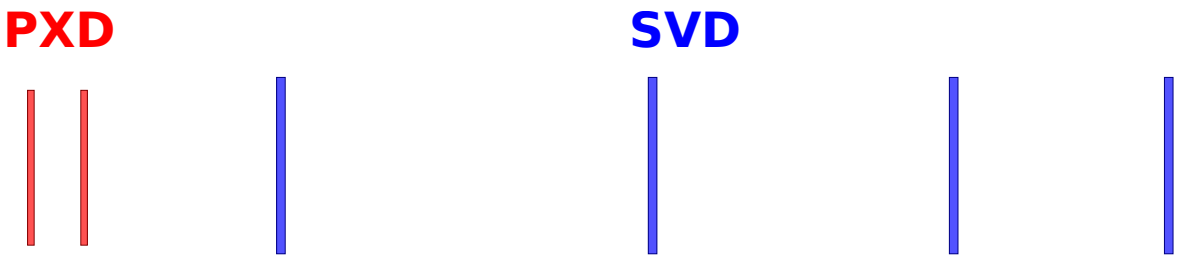
- Layout of header and footer as proposed in the TDR
  - 10 bit Time Tag (T-Tag): 1024 time slots within on event
  - 6 bit #SE: Number of the subevents
  - 6 bit APV: APV identification connected to the FADC
  - 6 bit #I: Number of Strip/ADC values for the FADC-APC
  - 7 bit Strip: Fired Strip ID for the FADC-APC
  - 10 bit ADC: Value of the ADC

Real Topology Layout



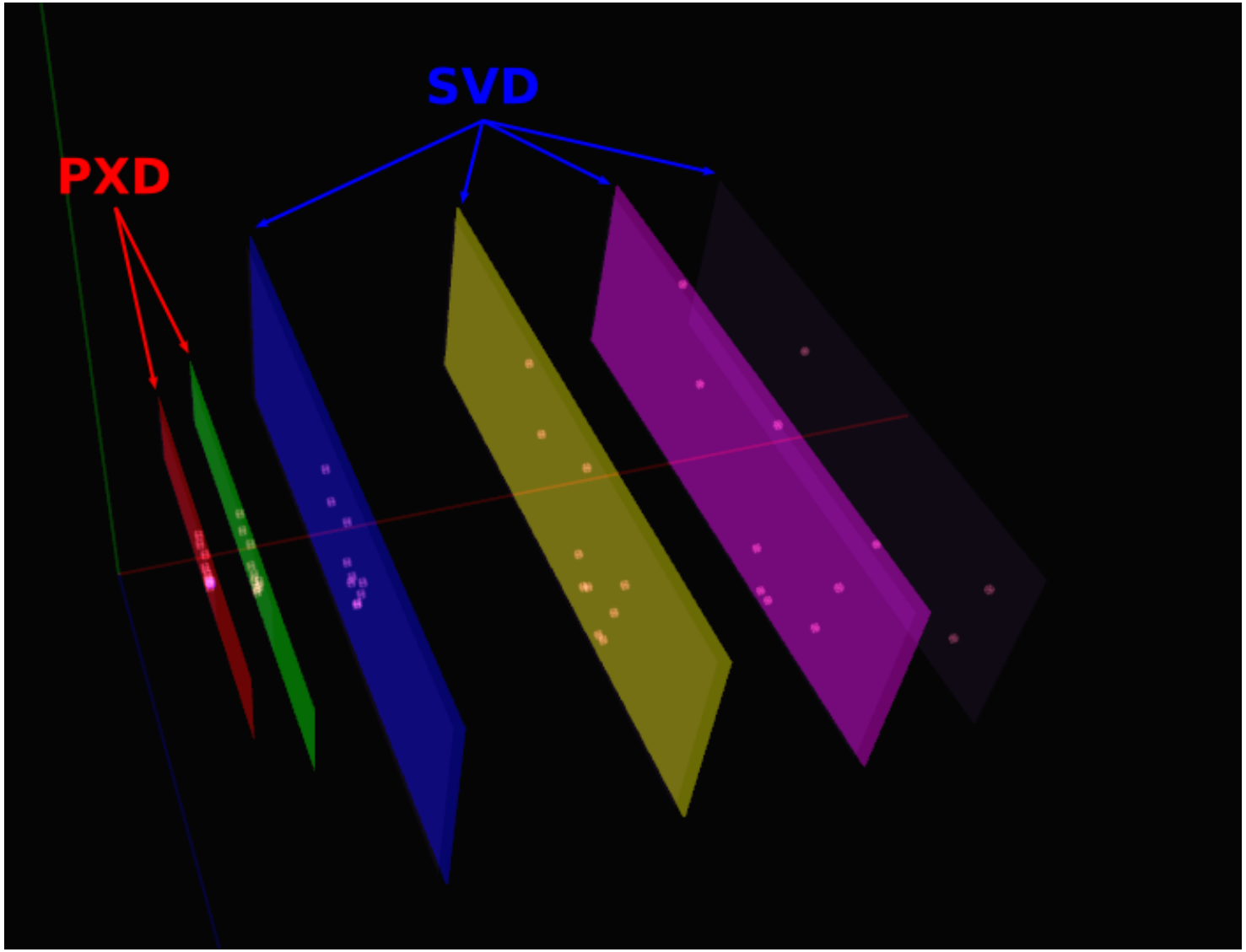
- 3 carrier boards with 4 AMCs
  - → 4:1 / 3:1 Multiplexer in each AMC card
  - → Use one SFP+ transceiver for inter-carrier board transmission
  - → AMC card interconnection over high-speed RocketIOs
- 1 AMC as data collector
  - → 3:1 Multiplexer with track reconstruction algorithm
  - → Ethernet connection for transmission of tracks to ATCA

Testbeam Simulation Setup

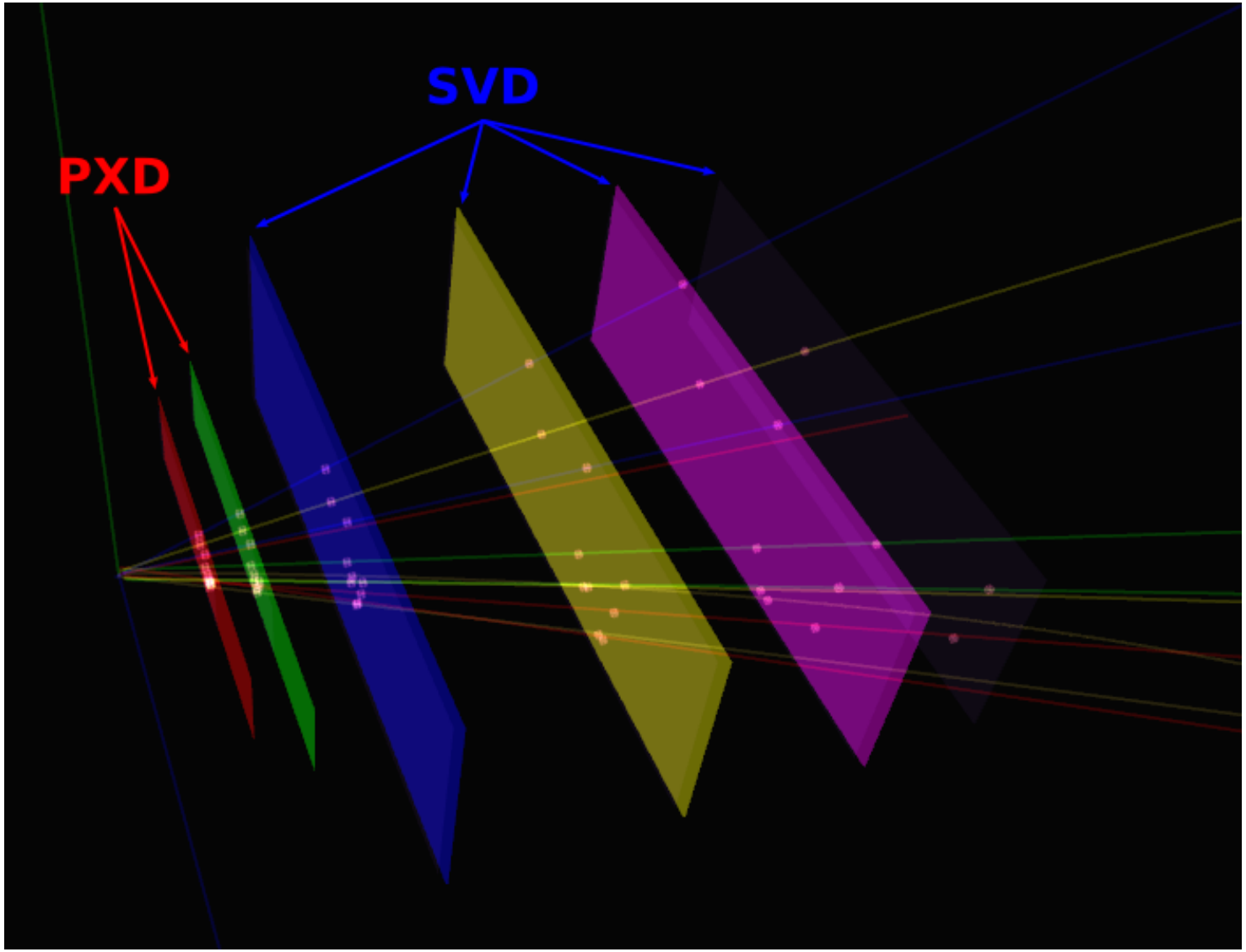


- Set up two layers with one PXD half ladder each.
- And four layers of the SVD in the suggested distance as in the final design
- Run simulation with electrons with energies between 0.5 and 2 *GeV*, 1 T magnet field

Testbeam Visualization



Testbeam Visualization



Testbeam Visualization